

Digilent Plug-in for Xilinx 11.x Tools User Manual

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1300 NE Henley Court Suite 3
Pullman, WA 99163
(509) 334 6306 Voice and Fax

Overview

The Digilent Plug-in for Xilinx tools allows Xilinx software tools to directly use the Digilent USB-JTAG FPGA configuration circuitry. Xilinx Chipscope Pro and Xilinx Microprocessor Debugger (XMD) command line mode are currently supported by the Plug-in. Refer to <http://www.xilinx.com/> for more information about these Xilinx design tools. Demonstration Designs for the Nexys2 and Basys2 boards are provided to verify correct operation of the plug-in.

Software Versions Tested:

Xilinx ISE Design Suite Version 11.x only (Refer to <http://www.digilentinc.com/> for versions of the plugin for later Xilinx ISE versions)

Digilent Adept System 2.4 (or Digilent Runtime 2.3 for Linux) or greater

Supported Operating Systems:

- Microsoft Windows 32-bit and 64-bit Operating Systems
- Linux: Red Hat, CentOS, and SUSE 32-bit and 64-bit Operating Systems

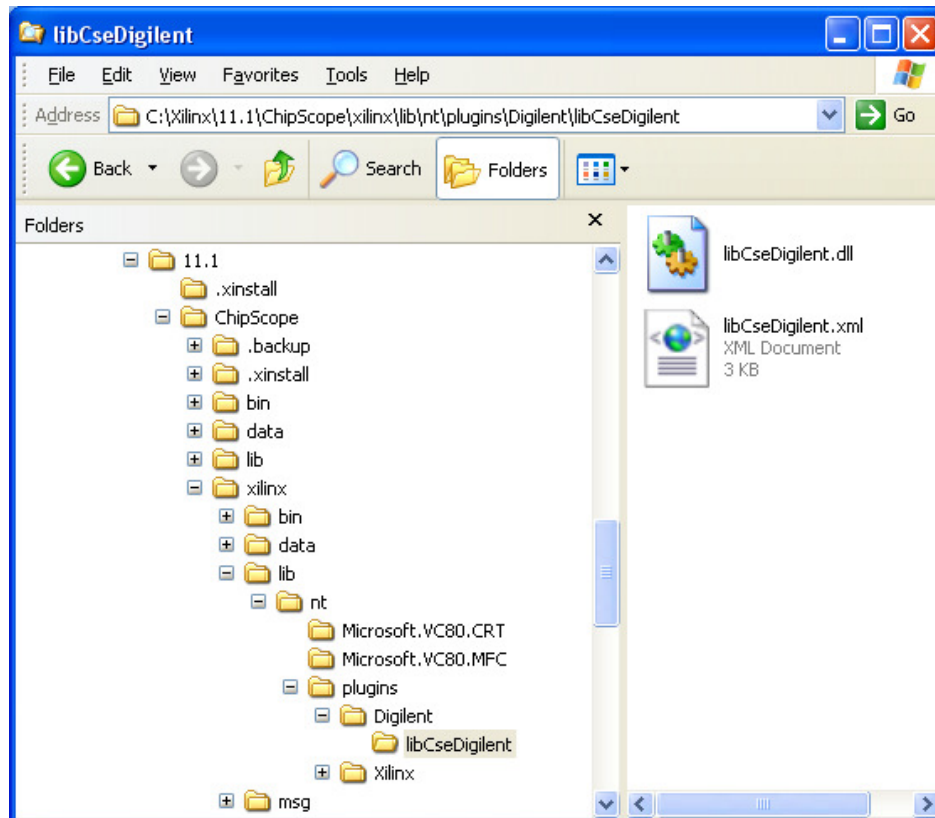
Windows Installation

To begin, ensure that the Xilinx ISE Suite (11.x only) and Digilent Adept System 2.4 (or greater) is installed on the host computer. The Plug-in files "libCseDigilent.dll" and "libCseDigilent.xml" must be copied into *both* the Chipscope and ISE Design Suite installations.

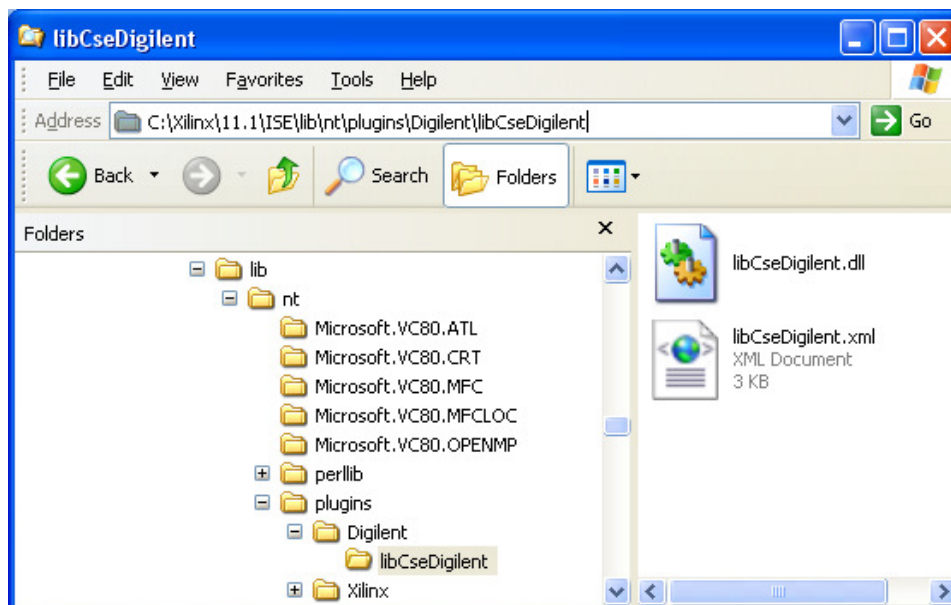
For Chipscope, the typical location is

C:\Xilinx\11.1\ChipScope\xilinx\lib\nt\plugins\Digilent\libCseDigilent

Note: For 64-bit Windows, use **nt64** in place of **nt**



For the ISE Design Suite, the typical location is
C:\Xilinx\11.1\ISE\lib\nt\plugins\Diligent\libCseDiligent
Note: For 64-bit Windows, use **nt64** in place of **nt**



Linux Installation

To begin, ensure that the Xilinx ISE Suite (11.x only) and Digilent Adept Runtime 2.3 (or greater) is installed on the host computer. The Plug-in files “libCseDigilent.so” and “libCseDigilent.xml” must be copied into *both* the Chipscope and ISE Design Suite installations.

For Chipscope, the typical location is **\$CHIPSCOPE/xilinx/lib/lin/plugins/Digilent/libCseDigilent**

Note: For 64-bit Windows, use **lin64** in place of **lin**

For the ISE Design Suite, the typical location is **\$XILINX/lib/lin/plugins/Digilent/libCseDigilent**

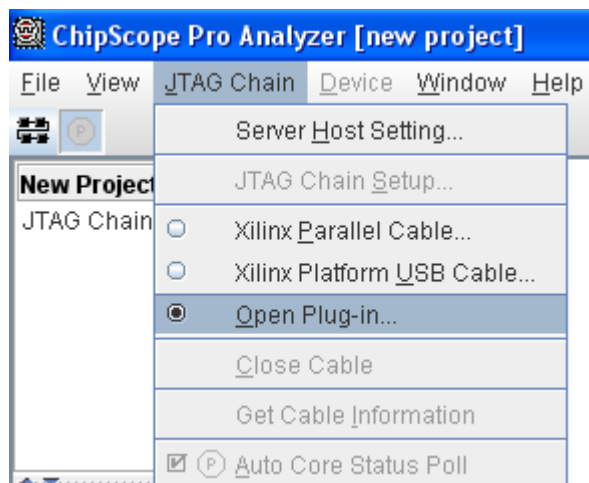
Note: For 64-bit Windows, use **lin64** in place of **lin**

Nexys2 Demonstration Project

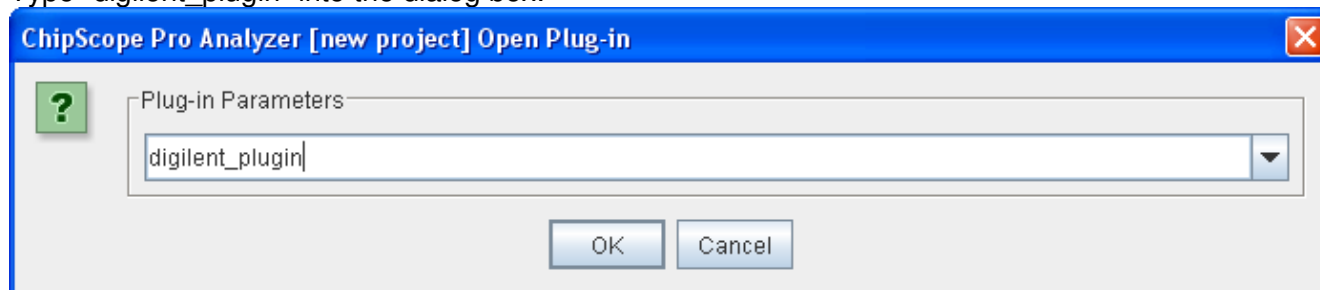
The Nexys2 Demonstration Project can be used to verify correct installation and operation of the Plug-in.

The Nexys2 Demonstration Project is a Xilinx EDK design with an embedded Chipscope Pro Virtual IO module. Refer to <http://www.xilinx.com/> for more information about these Xilinx design tools.

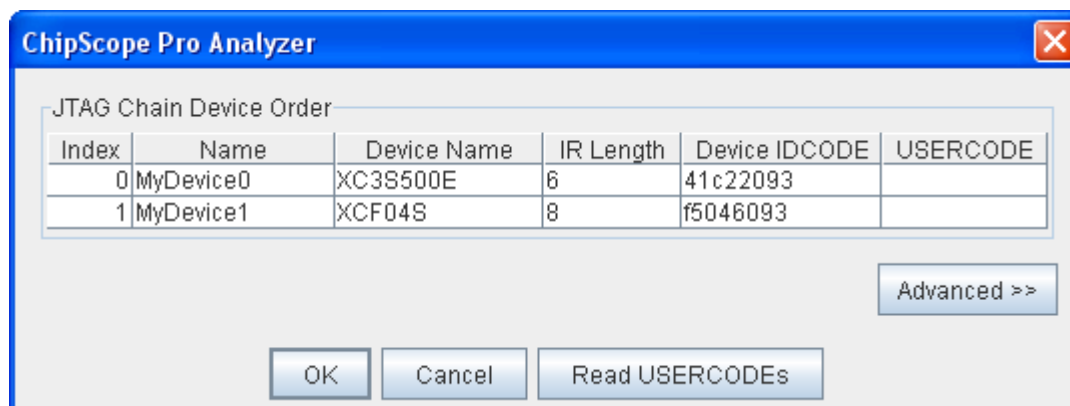
Launch Chipscope Pro Analyzer and Select the “JTAG Chain→Open Plug-in...” menu item.



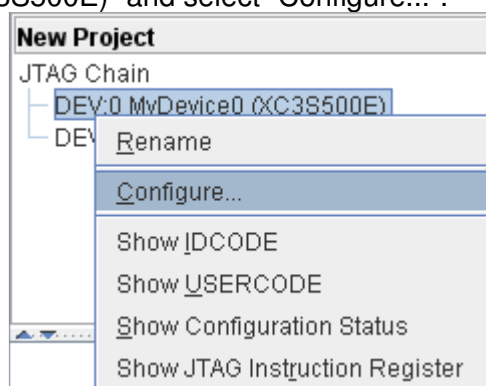
Type “digilent_plugin” into the dialog box:



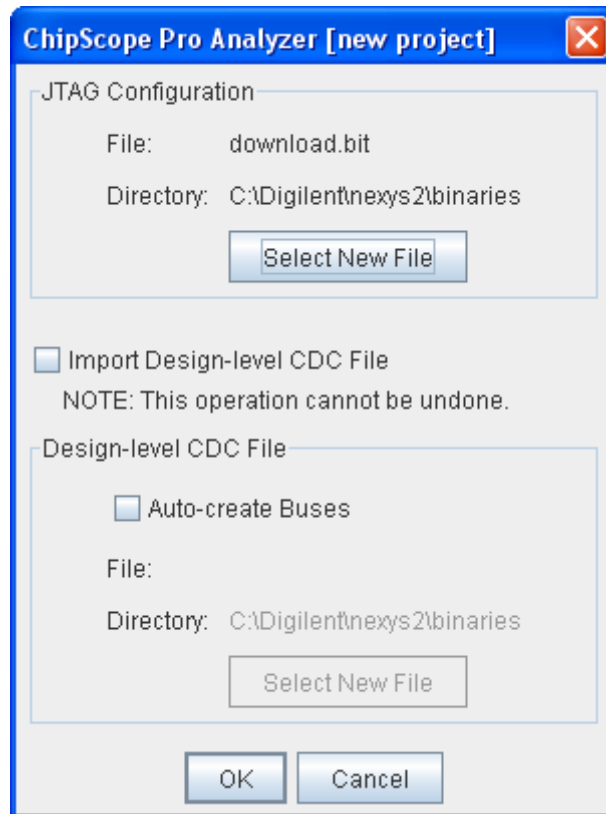
Chipscope Pro Analyzer will automatically detect the devices on the Nexys2 board:



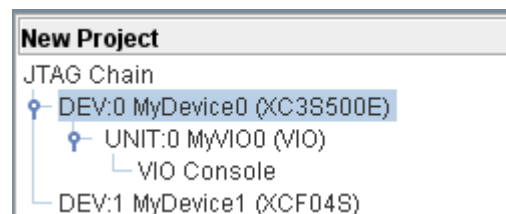
Right Click on "MyDevice0 (XC3S500E)" and select "Configure...":



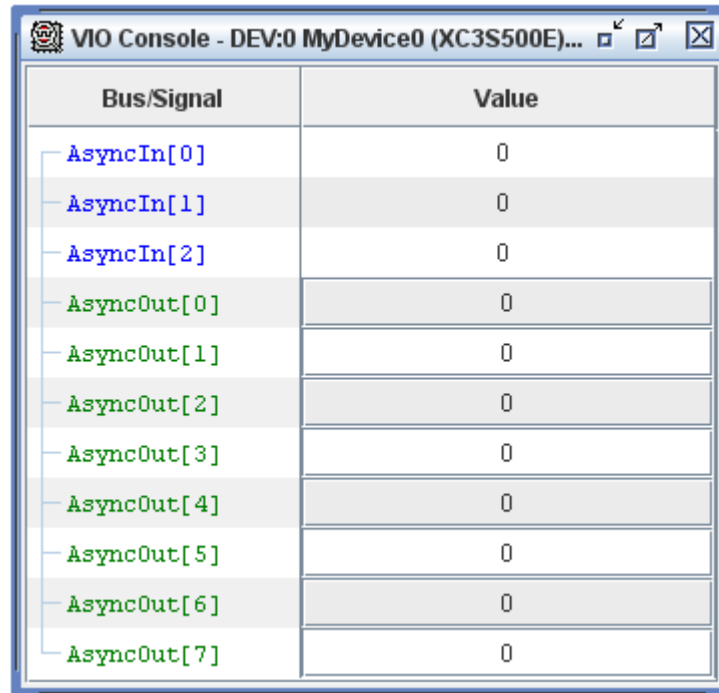
Select the "download.bit" file in the nexys2\binaries directory:



After selecting “OK”, Chipscope Pro Analyzer will configure the FPGA with the “download.bit” configuration file. After successful configuration, the Yellow “Done” LED should be light on the Nexys2 board. The GUI will show there is one VIO Console device attached:

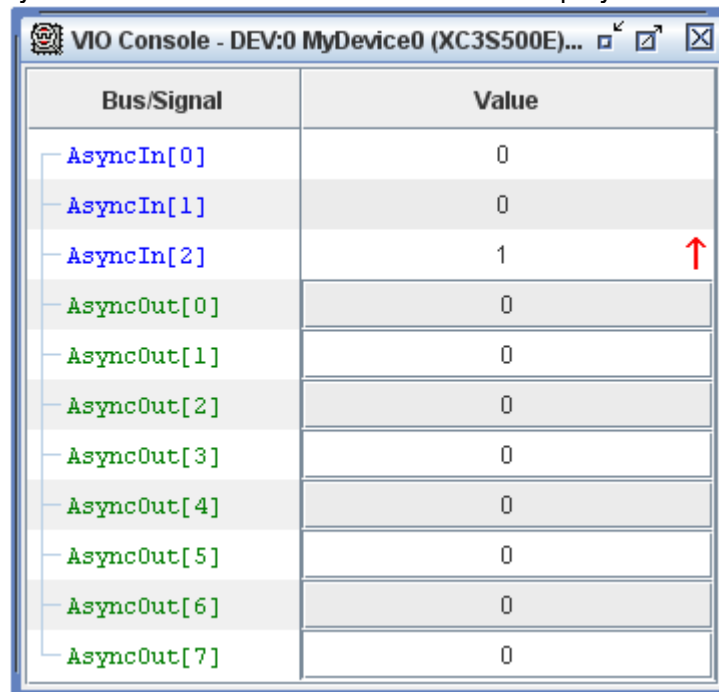


Double Click on the “VIO Console” item which brings up that window:



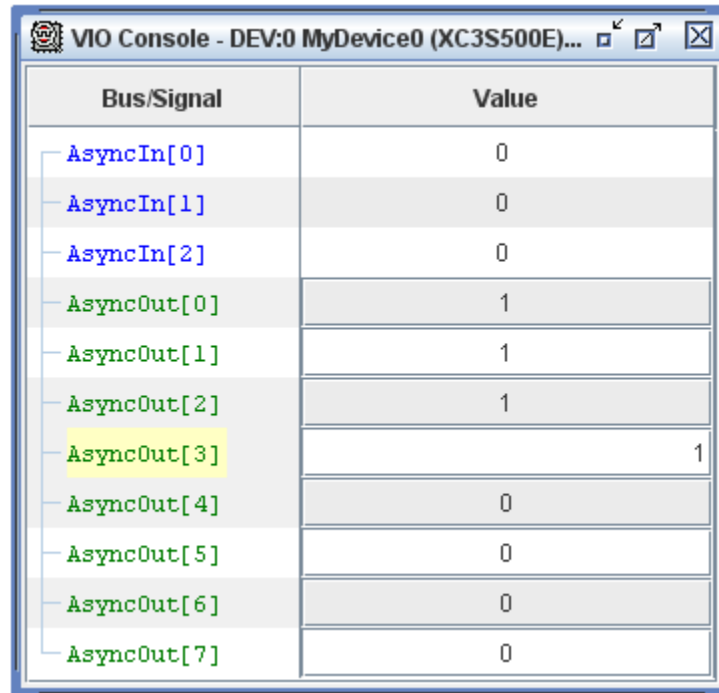
Bus/Signal	Value
AsyncIn[0]	0
AsyncIn[1]	0
AsyncIn[2]	0
AsyncOut[0]	0
AsyncOut[1]	0
AsyncOut[2]	0
AsyncOut[3]	0
AsyncOut[4]	0
AsyncOut[5]	0
AsyncOut[6]	0
AsyncOut[7]	0

Press BTN3 on the Nexys2 board and notice the VIO Console displays that action.



Bus/Signal	Value
AsyncIn[0]	0
AsyncIn[1]	0
AsyncIn[2]	1
AsyncOut[0]	0
AsyncOut[1]	0
AsyncOut[2]	0
AsyncOut[3]	0
AsyncOut[4]	0
AsyncOut[5]	0
AsyncOut[6]	0
AsyncOut[7]	0

The AsyncOut values are connected to the 8 LEDs on the Nexys2 board. Click on any of the Value cells to change their contents. The following configuration lights up 4 LEDs in a row:



Bus/Signal	Value
AsyncIn[0]	0
AsyncIn[1]	0
AsyncIn[2]	0
AsyncOut[0]	1
AsyncOut[1]	1
AsyncOut[2]	1
AsyncOut[3]	1
AsyncOut[4]	0
AsyncOut[5]	0
AsyncOut[6]	0
AsyncOut[7]	0

Close Chipscope Pro Analyzer. This concludes the Chipscope Pro part of the Demonstration Project. While only the Virtual IO Console was used in this design, any Chipscope Pro module can be utilized to assist in debugging the design.

The Plug-in can also be used with Xilinx Microprocessor Debugger (XMD) command line mode. By adding the option “**-cable type xilinx_plugin modulename digilent_plugin**” to commands which interface with the hardware, XMD will utilize the Plug-in.

Here is an annotated example iteration. Launch the EDK Bash Shell and type the following commands in **bold**.

```

Xilinx Bash Shell
Xilinx EDK 11.2 Build EDK_LS2.6
Copyright (c) 1995-2009 Xilinx, Inc. All rights reserved.

Analyzing Cygwin versions...
Xilinx tools detected Cygwin installation v1.5.17(0.129/4/2) on your machine.
This Cygwin will be used to run Xilinx tools.

~
$ cd /cygdrive/c/digilent/nexys2/binaries
~ /cygdrive/c/digilent/nexys2/binaries
$ xmd
Xilinx Microprocessor Debugger (XMD) Engine
Xilinx EDK 11.2 Build EDK_LS2.6
Copyright (c) 1995-2009 Xilinx, Inc. All rights reserved.

XMD%
XMD% fpga -f download.bit -cable type xilinx_plugin modulename digilent_plugin

JTAG chain configuration
-----

```

Launch xmd

Configure FPGA

Device	ID Code	IR Length	Part Name
1	41c22093	6	XC3S500E
2	f5046093	8	XCF04S

Connect to the
Microblaze Soft
Processor Debug port

Successfully downloaded bit file.

XMD% **connect mb mdm -cable type xilinx_plugin modulename digilent_plugin**

MicroBlaze Processor Configuration :

```

-----
Version.....7.20.a
Optimization.....Area
Interconnect.....PLBv46
MMU Type.....No_MMU
No of PC Breakpoints.....1
No of Read Addr/Data Watchpoints...0
No of Write Addr/Data Watchpoints..0
Instruction Cache Support.....off
Data Cache Support.....off
Exceptions Support.....off
FPU Support.....off
Hard Divider Support.....off
Hard Multiplier Support.....on - (Mul32)
Barrel Shifter Support.....off
MSR clr/set Instruction Support....on
Compare Instruction Support.....on
Data Cache Write-back Support.....off
  
```

Download Program
executable for
Microblaze to execute

Connected to "mb" target. id = 0

Starting GDB server for "mb" target. id = 0

XMD% **dow executable.elf**

System Reset DONE

Downloading Program -- executable.elf

```

section, .vectors.reset: 0x00000000-0x00000003
section, .vectors.sw_exception: 0x00000008-0x0000000b
section, .vectors.interrupt: 0x00000010-0x00000013
section, .vectors.hw_exception: 0x00000020-0x00000023
section, .text: 0x00000050-0x0000005eb
section, .init: 0x0000005ec-0x00000060f
section, .fini: 0x000000610-0x00000062b
section, .rodata: 0x00000062c-0x000000661
section, .sdata2: 0x000000662-0x000000667
section, .data: 0x000000668-0x000000777
section, .ctors: 0x000000778-0x00000077f
section, .dtors: 0x000000780-0x000000787
section, .eh_frame: 0x000000788-0x00000078b
section, .jcr: 0x00000078c-0x00000078f
section, .bss: 0x000000790-0x0000007b3
section, .heap: 0x0000007b4-0x0000009b7
section, .stack: 0x0000009b8-0x000000db7
  
```

Setting PC with Program Start Address 0x00000000

XMD% **read_uart**

Connected to MDM UART Target

XMD% **con**

Info:Digilent Plug-in: Found one device.

Info:Digilent Plug-in: Opening device : "Nexys2", SN:10054D197402.

Info:Digilent Plug-in: JTAG frequency: 1714286 Hz.

Info:Processor started. Type "stop" to stop processor

RUNNING> XMD% -- Entering main() --

-- Exiting main() --

XMD% **stop**

XMD% Info:User Interrupt, Processor Stopped at 0x0000006c

Start Microblaze Executing

Display Microblaze registers

```
XMD% rrd
r0: 00000000    r8: 00000000    r16: 00000000    r24: 00000000
r1: 00000d88    r9: 00000000    r17: 00000000    r25: 00000000
r2: 00000668    r10: 00000000   r18: 00000000    r26: 00000000
r3: 00000000    r11: 00000000   r19: 00000000    r27: 00000000
r4: 00000000    r12: 00000000   r20: 00000000    r28: 00000000
r5: 00000000    r13: 00000790   r21: 00000000    r29: 00000000
r6: 00000000    r14: 00000000   r22: 00000000    r30: 00000000
r7: 00000000    r15: 000003a8   r23: 00000000    r31: 00000000
pc: 0000006c    msr: 00000000
```

Read the values of the 8 Slide Switches via GPIO

```
XMD% mrd 0x81400000
81400000: 00000069
```

Manually Change the Slide Switch positions and re-read the values

```
XMD% mrd 0x81400000
81400000: 000000A5
```

```
XMD% exit
```

```
~ /cygdrive/c/digilent/nexys2/binaries
```

This concludes the Xilinx Microprocessor Debugger (XMD) part of the Demonstration Project.

Basys2 Demonstration Project

The Basys2 Demonstration Project can be used to verify correct installation and operation of the Plug-in. It is functionally equivalent to the Nexys2 design. Please follow the procedure documented in the Nexys2 Demonstration Project section above.