

Introduction

The ChipScope™ Pro Integrated CONTroller core (ICON) provides an interface between the JTAG Boundary Scan (BSCAN) interface of the FPGA device and the ChipScope Pro cores, including the following types of cores:

- Integrated Logic Analyzer (ILA)
- Virtual Input/Output (VIO)
- Agilent Trace Core 2 (ATC2)
- Integrated Bus Analyzer (IBA)

This interface allows the ChipScope Pro Analyzer software to communicate with these cores through the JTAG port of the device. The ICON core is designed to be easily instantiated and connected to these cores directly in a Verilog or VHDL design. The ICON core can also be added to an embedded processor system design using the Xilinx® Embedded Development Kit (EDK) tools.

Features

- Provides a communication path, using the JTAG port, between the ChipScope Pro Analyzer software and the ILA, VIO, ATC2, and IBA cores
- Connects to the JTAG chain through the USER scan chain feature of the BSCAN component
- Supports up to 15 connections to ILA, VIO, ATC2, and IBA cores
- Optionally attaches to either internally- or externally-instantiated BSCAN primitives, such as the one provided by the opb_mdm EDK core

For more information about the ICON core, refer to the *ChipScope Pro Software and Cores User Guide*.

LogiCORE IP Facts				
Core Specifics				
Supported Device Family ⁽¹⁾	Spartan®-3, Spartan-3E, Spartan-3A, Spartan-3A DSP, Spartan-6, Virtex®-4, Virtex-5, Virtex-6			
Resources Used ⁽²⁾	I/O	LUTs	FFs	Block RAMs
	0	193	28	0
Special Features	Includes BSCAN primitive by default			
Provided with Core				
Documentation	Product Specification			
Design File Formats	N/A			
Constraints File	N/A			
Verification	N/A			
Instantiation Template	Verilog and VHDL Wrapper			
Reference Designs /Application Notes	None			
Additional Items	N/A			
Design Tool Requirements				
Xilinx Implementation Tools	ISE® 11.2			
Verification	ChipScope Pro 11.2			
Simulation	Not supported in simulation			
Synthesis	Netlist is pre-synthesized by XST			
Support				
Provided by Xilinx, Inc.				

1. Including the variants of these FPGA device families.
2. These estimates are based on a Virtex-4 device family with four control ports. Results may vary depending on device family and parameters used.

Applications

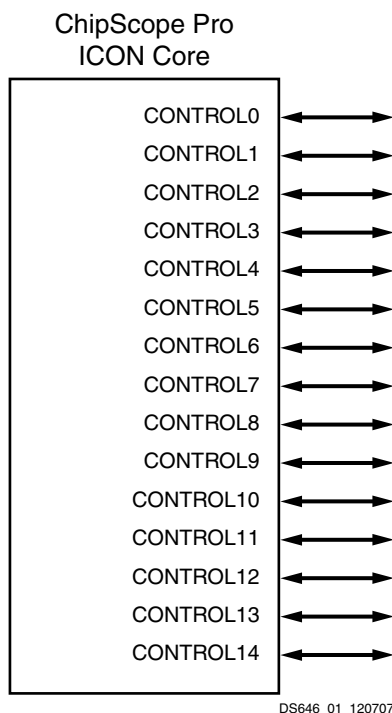
The ICON core is designed to be used in any application that requires verification or debugging using the ChipScope Pro software and cores.

Functional Description

The ICON core provides an interface between the ChipScope Pro Analyzer tool and up to 15 ChipScope Pro target cores (such as ILA, IBA, VIO, and ATC2) via the JTAG Boundary Scan port of the target FPGA. The ICON core bridges the gap between the JTAG Boundary Scan TAP controller of the FPGA and the target cores using the USER scan chains provided by the BSCAN primitive component of the FPGA. The ICON core is responsible for routing various commands sent from the Analyzer tool to the intended target cores.

The ICON core can be configured to automatically include the BSCAN primitive component (see [Figure 1](#)) or to use a BSCAN elsewhere in the design (see [Figure 2, page 3](#)). The ICON core can also route unused BSCAN USER scan chains to port signals if the BSCAN is included in the ICON core and the FPGA device family supports multiple USER scan chains per BSCAN component (see [Figure 3, page 3](#)).

The ICON core connection to the target cores is implemented as a dedicated bi-directional control port. This control port includes JTAG clock, input and output data, and control signals necessary to configure and communicate with the target core.



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Figure 1: ICON Core with Internal BSCAN Component

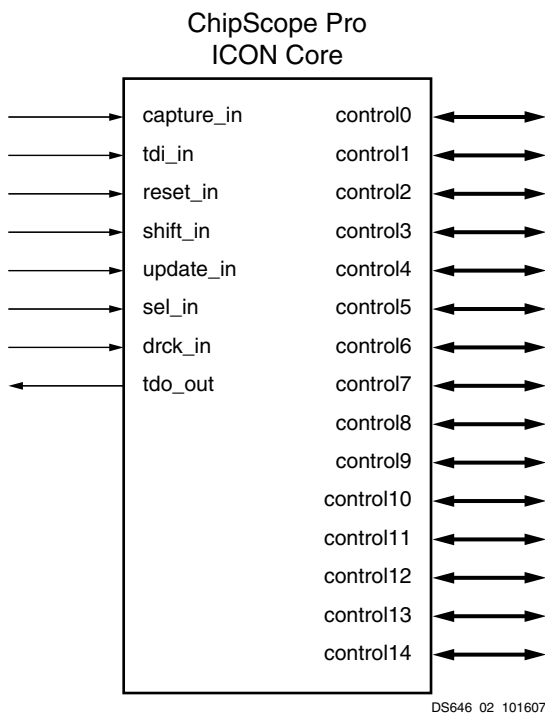


Figure 2: ICON Core with External BSCAN Component

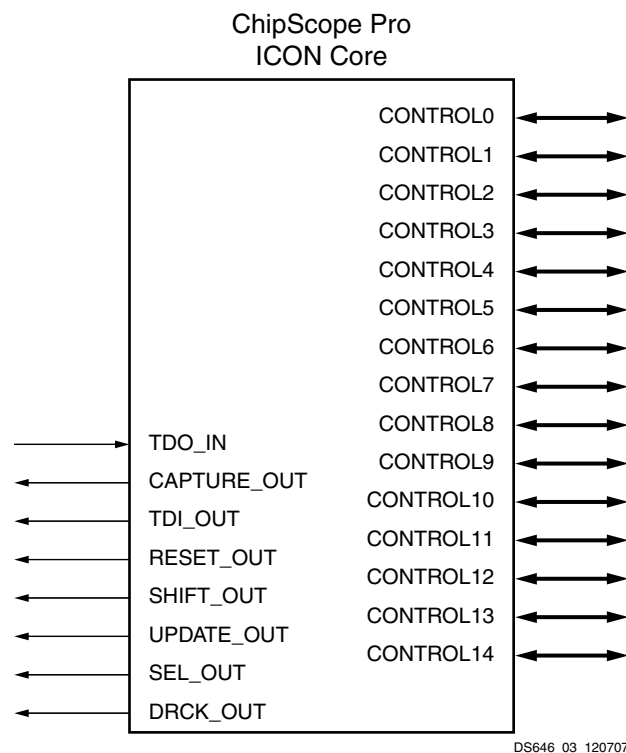


Figure 3: ICON Core with Internal BSCAN Component and Exported Unused BSCAN Signals

ICON Interface Ports

The I/O signals of the ICON core consist of control buses necessary to connect the ICON core to the target core(s) as well as optional BSCAN-related signals.

Table 1: ICON Interface Ports

Port Name	Direction	Description
CAPTURE_IN	IN	CAPTURE signal from the external BSCAN component. Optional (depends on <i>use_ext_bscan</i> parameter).
CAPTURE_OUT	OUT	CAPTURE signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on <i>use_unused_bscan</i> parameter).
CONTROL0[35:0]	INOUT	Provides control and status connection to the first ChipScope Pro target core. Mandatory.
CONTROL1[35:0]	INOUT	Provides control and status connection to the second ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL2[35:0]	INOUT	Provides control and status connection to the third ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL3[35:0]	INOUT	Provides control and status connection to the fourth ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL4[35:0]	INOUT	Provides control and status connection to the fifth ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL5[35:0]	INOUT	Provides control and status connection to the sixth ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL6[35:0]	INOUT	Provides control and status connection to the seventh ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL7[35:0]	INOUT	Provides control and status connection to the eighth ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL8[35:0]	INOUT	Provides control and status connection to the ninth ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL9[35:0]	INOUT	Provides control and status connection to the tenth ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL10[35:0]	INOUT	Provides control and status connection to the eleventh ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL11[35:0]	INOUT	Provides control and status connection to the twelfth ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL12[35:0]	INOUT	Provides control and status connection to the thirteenth ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL13[35:0]	INOUT	Provides control and status connection to the fourteenth ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
CONTROL14[35:0]	INOUT	Provides control and status connection to the fifteenth ChipScope Pro target core. Optional (depends on <i>number_control_ports</i> parameter).
DRCK_IN	IN	DRCK signal from the external BSCAN component. Optional (depends on <i>use_ext_bscan</i> parameter).
DRCK_OUT	OUT	DRCK signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on <i>use_unused_bscan</i> parameter).
RESET_IN	IN	RESET signal from the external BSCAN component. Optional (depends on <i>use_ext_bscan</i> parameter).
RESET_OUT	OUT	RESET signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on <i>use_unused_bscan</i> parameter).

Table 1: ICON Interface Ports (Cont'd)

Port Name	Direction	Description
SEL_IN	IN	SEL signal from the external BSCAN component. Optional (depends on <i>use_ext_bscan</i> parameter).
SEL_OUT	OUT	SEL signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on <i>use_unused_bscan</i> parameter).
SHIFT_IN	IN	SHIFT signal from the external BSCAN component. Optional (depends on <i>use_ext_bscan</i> parameter).
SHIFT_OUT	OUT	SHIFT signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on <i>use_unused_bscan</i> parameter).
TDI_IN	IN	TDI signal from the external BSCAN component. Optional (depends on <i>use_ext_bscan</i> parameter).
TDI_OUT	OUT	TDI signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on <i>use_unused_bscan</i> parameter).
TDO_IN	IN	TDO signal to the unused USER scan chain of the internal BSCAN component. Optional (depends on <i>use_unused_bscan</i> parameter).
TDO_OUT	OUT	TDO signal to the external BSCAN component. Optional (depends on <i>use_ext_bscan</i> parameter).
UPDATE_IN	IN	UPDATE signal from the external BSCAN component. Optional (depends on <i>use_ext_bscan</i> parameter).
UPDATE_OUT	OUT	UPDATE signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on <i>use_unused_bscan</i> parameter).

ICON XCO Parameters

The XCO parameters of the ICON core are shown in [Table 2](#).

Table 2: ICON XCO Parameters

Parameter Name	Allowable Values	Default Value	Description
component_name	String with A-z, 0-9, and _ (underscore)	icon	Name of instantiated component
number_control_ports	1 to 15	1	Number of ChipScope Pro target cores to be connected to this ICON core.
use_ext_bscan	False = Use internal True = Use external	False	Use an external or internal instance of the BSCAN primitive component
use_jtag_bufg	False = Enable BUFG True = Disable BUFG	False	Specifies whether or not a BUFG is added to the JTAG (or DRCK) clock signal
use_unused_bscan	False = Don't bond out True = Bond out	0	Indicates whether or not unused internal BSCAN component signals are bonded out to ports.
user_scan_chain	USER1, USER2, USER3, USER4	USER1	BSCAN USER scan chain number to be used by the ICON core ⁽¹⁾

1. USER1, USER2, USER3, and USER4 are supported only by the Virtex-4 and Virtex-5 device families. All other device families support USER1 and USER2 only.

Restrictions

Currently, the ChipScope Pro tools support only one ICON core per design.

Using ICON Core in EDK

The ICON core can be inserted into an embedded processor design using the Xilinx Embedded Development Kit (EDK). In this case, the ICON core depends on a BSCAN component instance whose interface is exported by the OPB_MDM peripheral component (see [Figure 4](#)).

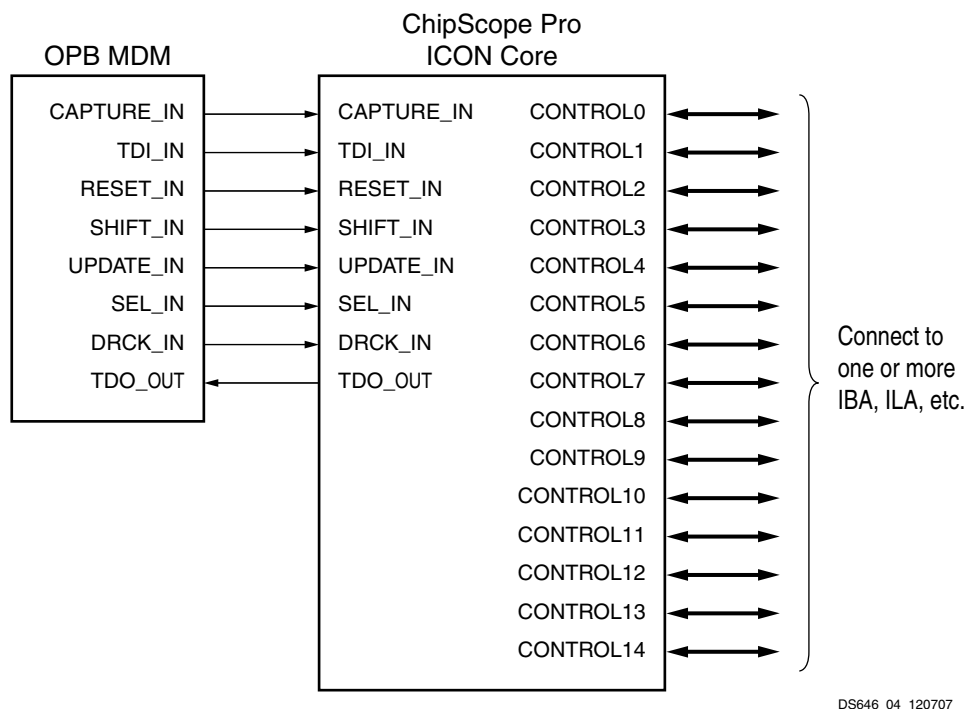


Figure 4: ICON Core Component in EDK XPS Design

In EDK, the ICON core is integrated into the tool using a Tcl script. When the EDK Platgen tool runs, the Tcl script is called and the script internally calls CORE Generator in command line mode. The Tcl script provides CORE Generator a parameters file (.xco) to generate the ICON core netlist. The Tcl script also generates an HDL wrapper to match the ICON ports based on the core parameters found in [Table 3](#). The XST synthesis tool is used for synthesizing the wrapper HDL generated for the ICON core. The NGC netlist outputs from XST and ChipScope Pro Core Generator are subsequently incorporated into the Xilinx ISE tool suite for actual device implementation.

Table 3: ICON EDK-Specific Parameters

Parameter Name	Allowable Values	Default Value	Description
c_disable_jtag_bufg_insertion	Integer: 1 = Disable BUFG 0 = Enable BUFG	0	Specifies whether or not a BUFG is added to the JTAG (or DRCK) clock signal.
c_family	virtex4, virtex5, virtex6, virtex6l, spartan3, spartan3E, spartan3A, spartan3Adsp, spartan6	N/A	Target FPGA device family.
c_force_bscan_user_port	Integer: 1, 3, or 4 (port 2 is used by OPB_MDM)	1	BSCAN USER scan chain number to be used by the ICON core.
c_num_control_ports	Integer: 1-15	1	Number of ChipScope Pro target cores to be connected to this ICON core.
c_system_contains_mdm	Integer: 1 = system contains MDM 0 = system does not contain MDM	0 (automatically calculated by tools)	Indicates whether or not the system containing the ICON core also contains the OPB_MDM peripheral. This parameter dictates whether a BSCAN component should be instantiated.

Verification

Xilinx has verified the ICON core in a proprietary test environment using an internally developed bus functional model.

References

- [1] More information on the ChipScope Pro software and cores is available in the *Software and Cores User Guide*, located at http://www.xilinx.com/support/documentation/sw_manuals/chipscope_pro_sw_cores_10_1_ug029.pdf
- [2] Information about hardware debugging using ChipScope Pro in EDK is available in the Platform Studio 11.2 online help, located at http://www.xilinx.com/itp/xilinx11/help/platform_studio/platform_studio_start.htm.
- [3] Information about hardware debugging using ChipScope Pro in System Generator for DSP is available in the *Xilinx System Generator for DSP User Guide*, located at http://www.xilinx.com/support/sw_manuals/sysgen_ug.pdf.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The ICON core is provided under the [SignOnce IP Site License](#) and can be generated using the Xilinx CORE Generator system v11.2 or higher. The CORE Generator system is shipped with Xilinx ISE Foundation Series Development software.

Please contact your local Xilinx [sales representative](#) for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx [IP Center](#).

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/24/2008	1.0	Release 10.1 (Initial Xilinx release).
09/19/2008	1.1	Release 10.1, Service Pack 3 changes.
04/07/2009	2.0	Release 11.1.
06/24/2009	2.1	Release 11.2.

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