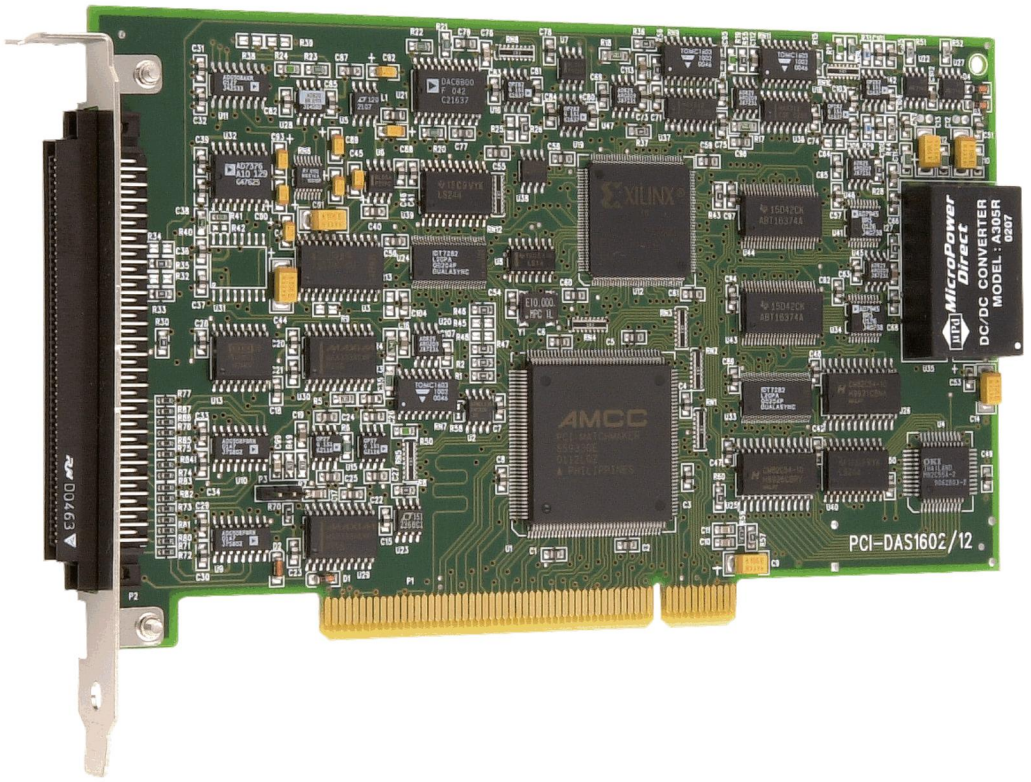
# PCI-DAS1602/12

Analog and Digital I/O Board

# User's Guide




MEASUREMENT COMPUTING™

# PCI-DAS1602/12

## Analog and Digital I/O Board

## User's Guide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# Table of Contents

# About This User's Guide

## What you will learn from this user's guide

This user's guide explains how to install, configure, and use the PCI-DAS1602/12 so that you get the most out of its get the most out of its analog, digital, and timing I/O features.

This user's guide also refers you to related documents available on our web site, and to technical support resources.

## Conventions in this user's guide

**For more information on …**

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

**Caution!** Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

<#:#> Angle brackets that enclose numbers separated by a colon signify a range of numbers, such as those assigned to registers, bit settings, etc.

**bold** text **Bold** text is used for the names of objects on the screen, such as buttons, text boxes, and check boxes. For example:
**1.** Insert the disk or CD and click the **OK** button.

*italic* text *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase. For example:
The *Insta*Cal installation procedure is explained in the *Quick Start Guide*.
*Never* touch the exposed pins or circuit connections on the board.

## Where to find more information

The following electronic documents provide helpful information relevant to the operation of the PCI-DAS1602/12.

- MCC's *Specifications: PCI-DAS1602/12* (the PDF version of the *Specifications* chapter in this guide) is available on our web site at www.mccdaq.com/pdfs/Specs/PCI-DAS1602-12-spec.pdf.
- MCC's *Quick Start Guide* is available on our web site at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.
- MCC's *Guide to Signal Connections* is available on our web site at www.mccdaq.com/signals/signals.pdf.
- MCC's *Universal Library User's Guide* is available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-user-guide.pdf.
- MCC's *Universal Library Function Reference* is available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-functions.pdf.
- MCC's *Universal Library for LabVIEW™ User's Guide* is available on our web site at www.mccdaq.com/PDFmanuals/SM-UL-LabVIEW.pdf.

*PCI-DAS1602/12 User's Guide* (this document) is also available on our web site at www.mccdaq.com/PDFmanuals/PCI-DAS1602-12.pdf.

## Register-level programming

You should use the Universal Library to control your board. Only experienced programmers should try register-level programming.

If you need to program at the register level in your application, you can find more information in the *Register Map for the* PCI-DAS1602/12 (available at www.mccdaq.com/registermaps/RegMapPCI-DAS1602-12.pdf).

# Introducing the PCI-DAS1602/12

## Overview: PCI-DAS1602/12 board features

The PCI-DAS1602/12 multifunction analog and digital I/O board sets a new standard for high performance data acquisition on the PCI bus. This manual explains how to install and use your PCI-DAS1602/12 data acquisition board.

The PCI-DAS1602/12 is a multifunction measurement and control board designed for the PCI bus. This board can be used for applications such as data acquisition, system timing, and industrial process control.

The PCI-DAS1602/12 board is completely plug and play, with no switches, jumpers or potentiometers to set. All board addresses and interrupt sources are set with software. You calibrate the board with software that uses programmable on-board digital potentiometers and trim D/A converters.

The PCI-DAS1602/12 provides the following features:

- Eight differential inputs or 16 single-ended 12-bit analog inputs
- Sample rates of up to 330 kHz
- 24 bits of digital I/O
- Three 16-bit down-counters
- 100-pin high density I/O connector
- Two FIFO-buffered 12-bit analog outputs with update rates of up to 250 kHz

Analog input ranges are selectable via software as bipolar or unipolar. Bipolar input ranges are ±10 V, ±5 V, ±2.5 V, and ±1.25 V. Unipolar input ranges are 0 to 10 V, 0 to 5 V, 0 to 2.5 V, and 0 to 1.25 V. The PCI-DAS1602/12 board has an analog trigger input. The trigger level and direction are software configurable.

The PCI-DAS1602/12 board has two 82C54 counter chips. Each chip contains three 16-bit down counters that provide clock, gate, and output connections.

## Software features

For information on the features of *Insta*Cal and the other software included with your PCI-DAS1602/12, refer to the *Quick Start Guide* that shipped with your device. The *Quick Start Guide* is also available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Check www.mccdaq.com/download.htm for the latest software version or versions of the software supported under less commonly used operating systems.

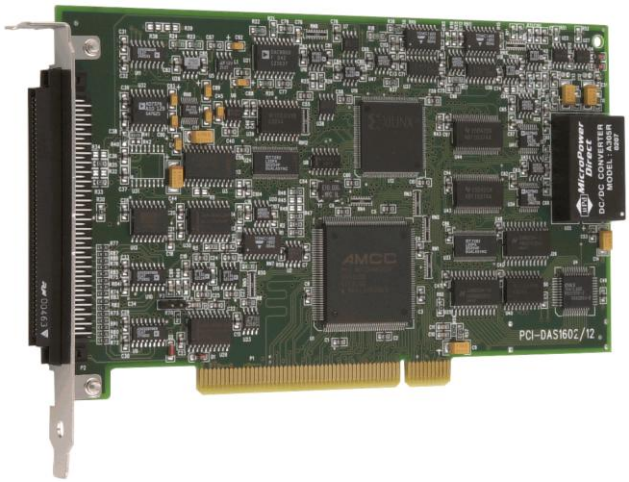
# Installing the PCI-DAS1602/12

## What comes with your PCI-DAS1602/12 shipment?

The following items are shipped with the PCI-DAS1602/12.

### Hardware

- PCI-DAS1602/12



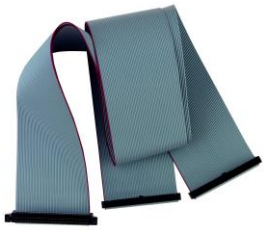
### Additional documentation

In addition to this hardware user's guide, you should also receive the *Quick Start Guide* (available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf). This booklet supplies a brief description of the software you received with your PCI-DAS1602/12 and information regarding installation of that software. Please read this booklet completely before installing any software or hardware..

## Optional components

If you ordered any of the following products with your board, they should be included with your shipment..

- Cables



C100FF-x

### Signal termination and conditioning accessories

MCC provides signal conditioning and termination products for use with the PCI-DAS1602/12. Refer to Field wiring and signal termination on page 15 for a complete list of compatible accessory products.

## Unpacking the PCI-DAS1602/12

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the PCI-DAS1602/12 from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

If any components are missing or damaged, notify Measurement Computing Corporation immediately by phone, fax, or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

## Installing the software

Refer to the *Quick Start Guide* for instructions on installing the software on the *Measurement Computing Data Acquisition Software CD*. This booklet is available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

## Installing the PCI-DAS1602/12

The PCI-DAS1602/12 board is completely plug-and-play, with no switches or jumpers to set. Configuration is controlled by your system's BIOS. To install your board, follow the steps below.

**Install the MCC DAQ software before you install your board**

The driver needed to run your board is installed with the MCC DAQ software. Therefore, you need to install the MCC DAQ software before you install your board. Refer to the *Quick Start Guide* for instructions on installing the software.

1. Turn your computer off, open it up, and insert your board into an available PCI slot.
2. Close your computer and turn it on.

   If you are using an operating system with support for plug-and-play (such as Windows 2000 or Windows XP), a dialog box opens as the system loads, indicating that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you are prompted for the disk containing this file. The *Measurement Computing Data Acquisition Software* CD supplied with your board contains this file. If required, insert the disk or CD and click **OK**.
3. To test your installation and configure your board, run the *Insta*Cal utility installed in the previous section. Refer to the *Quick Start Guide* that came with your board for information on how to initially set up and load *Insta*Cal.

If your board has been powered-off for more than 10 minutes, allow your computer to warm up for at least 15 minutes before acquiring data with this board. This warm-up period is required in order for the board to achieve its rated accuracy. The high speed components used on the board generate heat, and it takes this amount of time for a board to reach steady state if it has been powered off for a significant amount of time

# Configuring the PCI-DAS1602/12

All hardware configuration options on the PCI-DAS1602/12 are software controlled. You can select some of the configuration options using *Insta*Cal, such as the analog input configuration (16 single-ended or eight differential channels), the edge used for triggering when using an external pacer, and the counter source. Once selected, any program that uses the Universal Library initializes the hardware according to these selections.

# Connecting the board for I/O operations

## Connectors, cables – main I/O connector

The table below lists the board connectors, applicable cables, and compatible accessory products for the PCI-DAS1602/12.

Board connector, cables, and accessory equipment

| | |
|---|---|
| Connector type | 100-pin high-density Robinson-Nugent |
| Compatible cables | C100FF-x |
| Compatible accessory products with the C100FF-x cable | ▪ ISO-RACK16/P<br>▪ ISO-DA02/P<br>▪ BNC-16SE<br>▪ BNC-16DI<br>▪ CIO-MINI50<br>▪ CIO-TERM100<br>▪ SCB-50<br>▪ SSR-RACK24 (DADP-5037 adaptor required)<br>▪ SSR-RACK08 (DADP-5037 with TN-MC78M05CT adaptor required)<br>▪ CIO-ERB24 (DADP-5037 adaptor required)<br>▪ CIO-ERB08 (DADP-5037 adaptor required)<br>▪ CIO-SERB08 (DADP-5037 adaptor required) |

The PCI-DAS1602/12 board's main I/O connector is a 100-pin high density connector labeled **J1**. All signals pass through this connector. The pinout for eight-channel differential mode is listed on page 12. The pinout for 16-channel single ended mode is listed on page 13.

**Information on signal connections**

General information regarding signal connection and configuration is available in the *Guide to Signal Connections* (available at www.mccdaq.com/signals/signals.pdf).

**Caution!** When connecting a cable to the board's I/O connector, make sure that the arrow indicating pin 1 on the board connector lines up with the arrow indicating pin 1 on the cable connector. Connecting cables can damage the board and the I/O controller.

## Pinout – main I/O connector

8-channel differential mode pin out

| Signal Name | Pin | | | Pin | Signal Name |
|---|---|---|---|---|---|
| GND | 100 | ■ | ■ | 50 | GND |
| EXTERNAL INTERRUPT | 99 | ■ | ■ | 49 | SSH OUT |
| n/c | 98 | ■ | ■ | 48 | PC +5 V |
| EXTERNAL D/A PACER GATE | 97 | ■ | ■ | 47 | n/c |
| D/A INTERNAL PACER OUTPUT | 96 | ■ | ■ | 46 | n/c |
| A/D INTERNAL PACER OUTPUT | 95 | ■ | ■ | 45 | A/D EXTERNAL TRIGGER IN |
| n/c | 94 | ■ | ■ | 44 | D/A EXTERNAL PACER IN |
| n/c | 93 | ■ | ■ | 43 | ANALOG TRIGGER IN |
| -12 V | 92 | ■ | ■ | 42 | A/D EXTERNAL PACER |
| GND | 91 | ■ | ■ | 41 | CTR 4 OUT |
| +12 V | 90 | ■ | ■ | 40 | CTR 4 GATE |
| GND | 89 | ■ | ■ | 39 | CTR 4 CLK |
| n/c | 88 | ■ | ■ | 38 | D/A OUT 1 |
| n/c | 87 | ■ | ■ | 37 | D/A GND 1 |
| n/c | 86 | ■ | ■ | 36 | D/A OUT 0 |
| n/c | 85 | ■ | ■ | 35 | D/A GND 0 |
| n/c | 84 | ■ | ■ | 34 | n/c |
| n/c | 83 | ■ | ■ | 33 | n/c |
| n/c | 82 | ■ | ■ | 32 | n/c |
| n/c | 81 | ■ | ■ | 31 | n/c |
| n/c | 80 | ■ | ■ | 30 | n/c |
| n/c | 79 | ■ | ■ | 29 | n/c |
| n/c | 78 | ■ | ■ | 28 | n/c |
| n/c | 77 | ■ | ■ | 27 | n/c |
| n/c | 76 | ■ | ■ | 26 | n/c |
| n/c | 75 | ■ | ■ | 25 | n/c |
| FIRSTPORTC Bit 7 | 74 | ■ | ■ | 24 | n/c |
| FIRSTPORTC Bit 6 | 73 | ■ | ■ | 23 | n/c |
| FIRSTPORTC Bit 5 | 72 | ■ | ■ | 22 | n/c |
| FIRSTPORTC Bit 4 | 71 | ■ | ■ | 21 | n/c |
| FIRSTPORTC Bit 3 | 70 | ■ | ■ | 20 | n/c |
| FIRSTPORTC Bit 2 | 69 | ■ | ■ | 19 | n/c |
| FIRSTPORTC Bit 1 | 68 | ■ | ■ | 18 | LLGND |
| FIRSTPORTC Bit 0 | 67 | ■ | ■ | 17 | CH7 LO |
| FIRSTPORTB Bit 7 | 66 | ■ | ■ | 16 | CH7 HI |
| FIRSTPORTB Bit 6 | 65 | ■ | ■ | 15 | CH6 LO |
| FIRSTPORTB Bit 5 | 64 | ■ | ■ | 14 | CH6 HI |
| FIRSTPORTB Bit 4 | 63 | ■ | ■ | 13 | CH5 LO |
| FIRSTPORTB Bit 3 | 62 | ■ | ■ | 12 | CH5 HI |
| FIRSTPORTB Bit 2 | 61 | ■ | ■ | 11 | CH4 LO |
| FIRSTPORTB Bit 1 | 60 | ■ | ■ | 10 | CH4 HI |
| FIRSTPORTB Bit 0 | 59 | ■ | ■ | 9 | CH3 LO |
| FIRSTPORTA Bit 7 | 58 | ■ | ■ | 8 | CH3 HI |
| FIRSTPORTA Bit 6 | 57 | ■ | ■ | 7 | CH2 LO |
| FIRSTPORTA Bit 5 | 56 | ■ | ■ | 6 | CH2 HI |
| FIRSTPORTA Bit 4 | 55 | ■ | ■ | 5 | CH1 LO |
| FIRSTPORTA Bit 3 | 54 | ■ | ■ | 4 | CH1 HI |
| FIRSTPORTA Bit 2 | 53 | ■ | ■ | 3 | CH0 LO |
| FIRSTPORTA Bit 1 | 52 | ■ | ■ | 2 | CH0 HI |
| FIRSTPORTA Bit 0 | 51 | ■ | ■ | 1 | LLGND |
| PCI slot ↓ | | | | | |

16-channel single-ended mode pin out

| Signal Name | Pin | | | Pin | Signal Name |
|---|---|---|---|---|---|
| GND | 100 | ■ | ■ | 50 | GND |
| EXTERNAL INTERRUPT | 99 | ■ | ■ | 49 | SSH OUT |
| n/c | 98 | ■ | ■ | 48 | PC +5 V |
| EXTERNAL D/A PACER GATE | 97 | ■ | ■ | 47 | n/c |
| D/A INTERNAL PACER OUTPUT | 96 | ■ | ■ | 46 | n/c |
| A/D INTERNAL PACER OUTPUT | 95 | ■ | ■ | 45 | A/D EXTERNAL TRIGGER IN |
| n/c | 94 | ■ | ■ | 44 | D/A EXTERNAL PACER IN |
| n/c | 93 | ■ | ■ | 43 | ANALOG TRIGGER IN |
| -12 V | 92 | ■ | ■ | 42 | A/D EXTERNAL PACER |
| GND | 91 | ■ | ■ | 41 | CTR 4 OUT |
| +12 V | 90 | ■ | ■ | 40 | CTR 4 GATE |
| GND | 89 | ■ | ■ | 39 | CTR 4 CLK |
| n/c | 88 | ■ | ■ | 38 | D/A OUT 1 |
| n/c | 87 | ■ | ■ | 37 | D/A GND 1 |
| n/c | 86 | ■ | ■ | 36 | D/A OUT 0 |
| n/c | 85 | ■ | ■ | 35 | D/A GND 0 |
| n/c | 84 | ■ | ■ | 34 | n/c |
| n/c | 83 | ■ | ■ | 33 | n/c |
| n/c | 82 | ■ | ■ | 32 | n/c |
| n/c | 81 | ■ | ■ | 31 | n/c |
| n/c | 80 | ■ | ■ | 30 | n/c |
| n/c | 79 | ■ | ■ | 29 | n/c |
| n/c | 78 | ■ | ■ | 28 | n/c |
| n/c | 77 | ■ | ■ | 27 | n/c |
| n/c | 76 | ■ | ■ | 26 | n/c |
| n/c | 75 | ■ | ■ | 25 | n/c |
| FIRSTPORTC Bit 7 | 74 | ■ | ■ | 24 | n/c |
| FIRSTPORTC Bit 6 | 73 | ■ | ■ | 23 | n/c |
| FIRSTPORTC Bit 5 | 72 | ■ | ■ | 22 | n/c |
| FIRSTPORTC Bit 4 | 71 | ■ | ■ | 21 | n/c |
| FIRSTPORTC Bit 3 | 70 | ■ | ■ | 20 | n/c |
| FIRSTPORTC Bit 2 | 69 | ■ | ■ | 19 | n/c |
| FIRSTPORTC Bit 1 | 68 | ■ | ■ | 18 | LLGND |
| FIRSTPORTC Bit 0 | 67 | ■ | ■ | 17 | CH15 HI |
| FIRSTPORTB Bit 7 | 66 | ■ | ■ | 16 | CH7 HI |
| FIRSTPORTB Bit 6 | 65 | ■ | ■ | 15 | CH14 HI |
| FIRSTPORTB Bit 5 | 64 | ■ | ■ | 14 | CH6 HI |
| FIRSTPORTB Bit 4 | 63 | ■ | ■ | 13 | CH13 HI |
| FIRSTPORTB Bit 3 | 62 | ■ | ■ | 12 | CH5 HI |
| FIRSTPORTB Bit 2 | 61 | ■ | ■ | 11 | CH12 HI |
| FIRSTPORTB Bit 1 | 60 | ■ | ■ | 10 | CH4 HI |
| FIRSTPORTB Bit 0 | 59 | ■ | ■ | 9 | CH11 HI |
| FIRSTPORTA Bit 7 | 58 | ■ | ■ | 8 | CH3 HI |
| FIRSTPORTA Bit 6 | 57 | ■ | ■ | 7 | CH10 HI |
| FIRSTPORTA Bit 5 | 56 | ■ | ■ | 6 | CH2 HI |
| FIRSTPORTA Bit 4 | 55 | ■ | ■ | 5 | CH9 HI |
| FIRSTPORTA Bit 3 | 54 | ■ | ■ | 4 | CH1 HI |
| FIRSTPORTA Bit 2 | 53 | ■ | ■ | 3 | CH8 HI |
| FIRSTPORTA Bit 1 | 52 | ■ | ■ | 2 | CH0 HI |
| FIRSTPORTA Bit 0 | 51 | ■ | ■ | 1 | LLGND |
| PCI slot ↓ | | | | | |

The signal names for pins 2 to 17 define the functions for both single-ended modes and also for differential input modes. For example, if you are using eight differential inputs, pin 2 is the high side of channel 0 (CH0 HI) and pin 3 is the low side (CH0 LO) of channel 0. If you are using single-ended inputs, pin 2 is channel 0 (CH0 HI), but pin 3 is now channel 8 (CH8 HI). When you use single-ended inputs, use LLGND (and not GND) for analog signal returns.

## Cabling

You can use a C100FF-*x* cable to connect signals to the PCI-DAS1602/12 board. The C100FF-*x* cable is made up of two 50-pin ribbon cables that are joined at one end with a 100-pin connector. The two 50-pin cables diverge and are terminated at the other end with standard 50-pin header connectors.

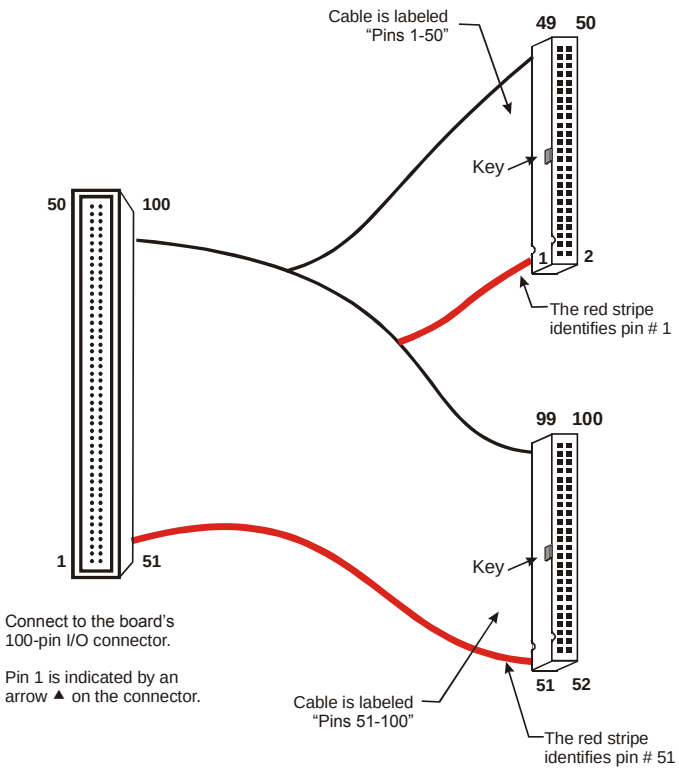



Figure 1. C100FF-x cable

The first 50-pin connector is used primarily for analog signals (pins 1-50 of the 100-pin connector). The second 50-pin connector is used primarily for digital I/O signals (pins 51-100 of the 100-pin connector). This configuration minimizes noise in the analog signal lines, and greatly simplifies field wiring and connections to external devices. You can purchase C100FF-x series cables from our web site at www.mccdaq.com/products/accessories.aspx.

## Field wiring and signal termination

You can use the following MCC screw terminal boards to terminate field signals and route them into the PCI-DAS1602/12 board using the C100FF-*x* cable:

### Screw terminal boards

- **CIO-TERM100** – 100 pin, 16 x 4 screw terminal board.
- **CIO-MINI50** – 50-pin universal screw terminal accessory. Two boards are required.
- **SCB-50** – 50-conductor, shielded signal connection/screw terminal box providing two independent 50-pin connections. One box is required.

Details on these products are available at www.mccdaq.com/products/screw_terminal_bnc.aspx.

### BNC connector interface boxes

- **BNC-16SE** – 16-channel single-ended BNC connector box.
- **BNC-16DI** – Eight-channel differential BNC connector box.

Details on these products are available at www.mccdaq.com/products/screw_terminal_bnc.aspx.

### Analog signal conditioning and expansion

- **ISO-RACK16/P** – 16-channel isolation module mounting rack.
- **ISO-DA02/P** – Two-channel, 5B module rack.

Details on these products are available at www.mccdaq.com/products/signal_conditioning.aspx.

### Digital signal conditioning

The following digital signal conditioning products have 37-pin connectors. Use the DADP-5037 adaptor board for connections to the C100FF-x cable's 50-pin connectors.

- **SSR-RACK24** – 24-position solid state relay rack. The DADP-5037 adaptor board is required.
- **SSR-RACK08** – Eight-channel solid state relay rack. The DADP-5037 with TN-MC78M05CT adaptor board is required.
- **CIO-ERB24** – 24-channel electromechanical relay accessory for digital I/O boards. The DADP-5037 adaptor board is required.
- **CIO-ERB08** – Eight-channel electromechanical relay accessory for digital I/O boards. The DADP-5037 adaptor board is required.

Details on digital signal conditioning products are available at www.mccdaq.com/products/signal_conditioning.aspx. Details on the DADP-5037 adapter board are available at www.mccdaq.com/products/accessories.aspx.

**Caution!** Before connecting signals to the PCI-DAS1602/12, measure the voltage between ground at the signal source and ground at the PC. If you measure >10 volts, do not connect the board to this signal source, as you are beyond the usable input range of the board. Either adjust your grounding system or add isolation signal conditioning to take useful measurements. A ground offset voltage of more than 30 volts may damage the board and possibly your computer. An offset voltage much greater than 30 volts will damage your electronics, and may be hazardous to your health.

To terminate signals and route them into the PCI-DAS1602/12, use the SCB-50 signal connection box, CIO-TERM100 screw terminal board, or two CIO-MINI50 screw terminal boards.

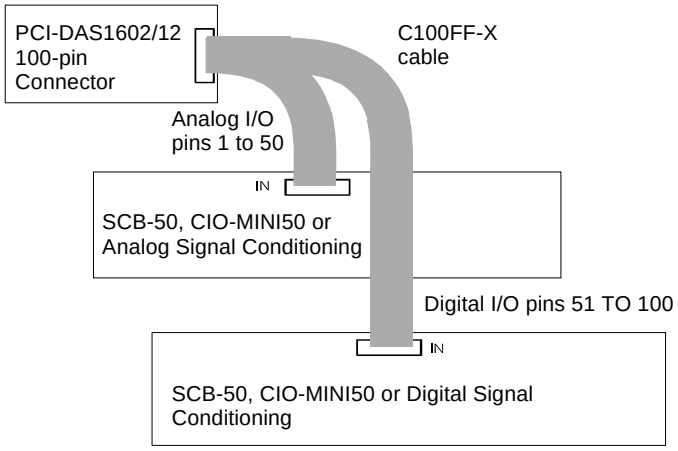



Figure 2. Sample wiring configuration using the C100FF-x cable

# Functional Details

## PCI-DAS1602/12 block diagram

The PCI-DAS1602/12 provides the following features:

- 16 single-ended or eight fully differential 16-bit analog inputs
- Two 12-bit analog outputs
- 24-bits, high current digital I/O
- Three 16-bit down counters

PCI-DAS1602/12 functions are illustrated in the block diagram shown here.

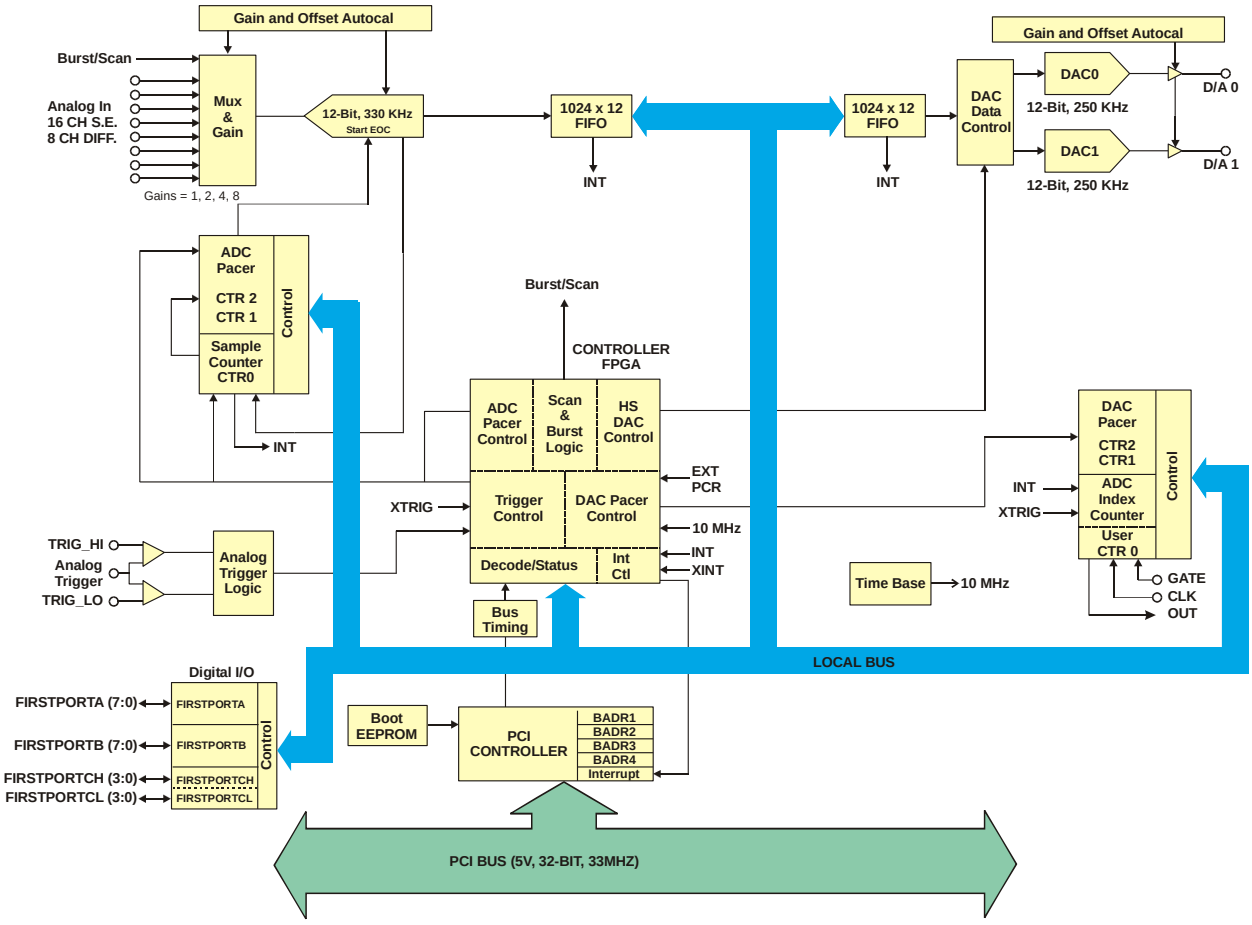



Figure 3. PCI-DAS1602/12 functional block diagram

# Analog inputs

The PCI-DAS1602/12 provides eight differential inputs, or 16 single-ended analog inputs. The input mode is software selectable, with no switches or jumpers to set. The board offers a 330 kHz maximum sample rate in single and multi-channel scans at any gain setting. A 1024 sample FIFO assures data taken from the board is transferred into computer memory without the possibility of missed samples.

Software also selects the bipolar/unipolar input configuration as well as selecting among the input ranges. The table below lists the input ranges and resolutions for the available input configurations and gains.

Input range and resolution

| Bipolar Range | Resolution | Unipolar Range | Resolution |
|---|---|---|---|
| ±10 V | 4.88 mV | 0 to 10 V | 2.44 mV |
| ±5 V | 2.44 mV | 0 to 5 V | 1.22 mV |
| ±2.5 V | 1.22 mV | 0 to 2.5 V | 0.61 mV |
| ±1.25 V | 0.61 mV | 0 to 1.25 V | 305 µV |

## Burst mode

Channel-to-channel skew results from multiplexing the A/D inputs. Channel-to-channel skew is defined as the time between consecutive samples. For example, if four channels are sampled at a rate of 1 kHz per channel, the channel skew is 250 µs (1 ms/4).

Burst mode minimizes channel-to-channel skew by clocking the A/D at the maximum rate between successive channels. Burst mode timing is illustrated in Figure 4. At the 1-ms pulse, channel 0 is sampled. After 3 µs, channel 2 is sampled. Channel 3 is sampled 3 µs after channel 2 is sampled. No samples are then taken until the next 1-ms pulse, when channel 0 is sampled again. In this mode, the rate for all channels is 1 kHz, but the channel-to-channel skew (delay) is now 3 µs, or 9 µs total. The minimum burst mode skew/delay on the PCI-DAS1602/12 is 3 µs.

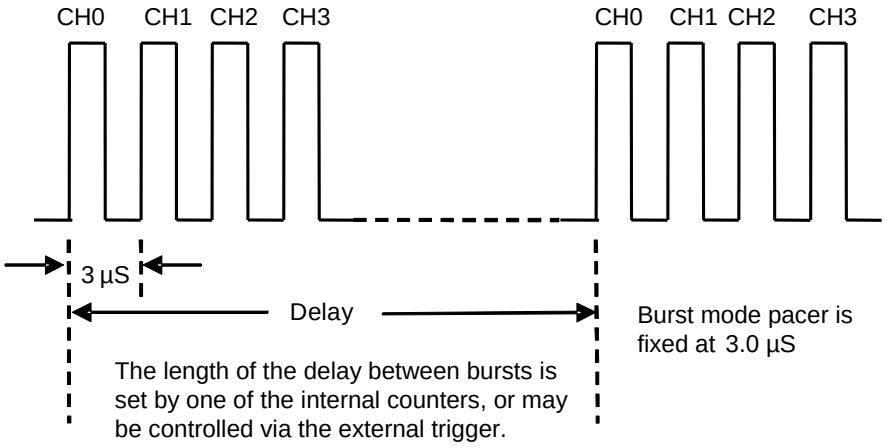



Figure 4. Burst mode timing

## Analog outputs

The PCI-DAS1602/12 provides two channels of high-speed 12-bit analog output. The analog outputs are updated via an on-board FIFO and REP OUTSW commands and provide a 250 kHz maximum update rate. Software selectable output ranges are 0 to 10 V, 0 to 5 V, ±10 V, and ±5 V. Channels may be set at different ranges. The D/A outputs provide rated accuracy to ±5 mA, are short circuit protected (25 mA limit) and are cleared to 0 volts on power up or reset.

## Parallel digital I/O

The PCI-DAS1602/12 provides 24 bits of parallel, digital I/O in the form of two eight-bit ports, and two four-bit ports. This digital capability is based on an on-board 82C55 PIA chip, which allows each of the ports to be set independently as input or output. The ports default to the input state (high impedance) on power up or reset.

## Counter/timer I/O

The PCI-DAS1602/12 provides three 16-bit down counters (one third of an 82C54 chip). The counters provide clock, gate and output connections. The counter clock may also be connected to the on-board 10 MHz crystal oscillator or may be left uncommitted for user input.

# Calibrating the PCI-DAS1602/12

The PCI-DAS1602/12 is equipped with software auto calibration. The *Insta*Cal software makes gain and offset corrections to the board using on-board digital potentiometers and trim D/A converters. No user intervention or external equipment is required. The PCI-DAS1602/16 is shipped fully-calibrated from the factory.

All adjustments are made via 8-bit calibration DACs or 7-bit digital potentiometers that are referenced to an on-board factory calibrated standard. Calibration factors are stored on the serial nvRAM. At run time, these calibration factors can be loaded into system memory and can be automatically retrieved when a different DAC/ADC range is specified

You can recalibrate with respect to the factory-measured voltage standards at any time by selecting the **Calibrate** menu in *Insta*Cal. Full calibration requires less than two minutes and requires no external equipment or user adjustments.

The standard calibration involves calibrating one channel with 0 volts input (offset), and then with a known input voltage (gain). The PCI-DAS1602/12's on board circuitry first shorts the inputs for offset calibration, then connects the inputs to the ultra-stable precision voltage reference for the gain calibration.

## Analog input calibration

Analog inputs are calibrated for offset and gain. Offset calibration is performed in the instrumentation amplifier gain stage. Front-end gain adjustment is performed via a variable attenuator/gain stage.

The analog input calibration system is shown in Figure 5.

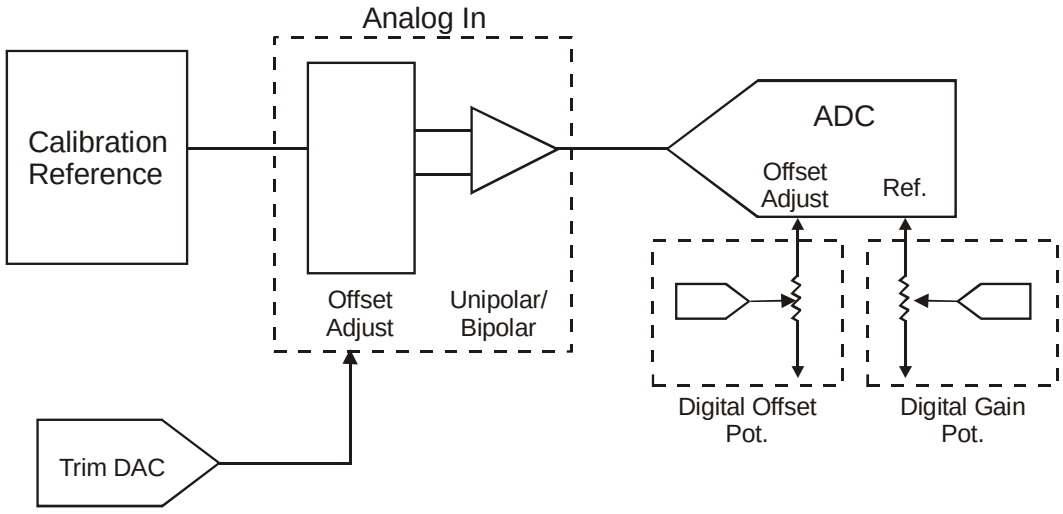



Figure 5. Analog input calibration

## Analog output calibration

Analog output circuits are calibrated for offset and gain. Coarse and fine offset adjustments are made in the output buffer section. The tuning range of these adjustments allows for maximum DAC and output buffer offsets. Coarse and fine gain calibration is performed via adjustments to the DAC reference.

The analog output calibration system is shown in Figure 6. This circuit is duplicated for both DAC0 and DAC1.

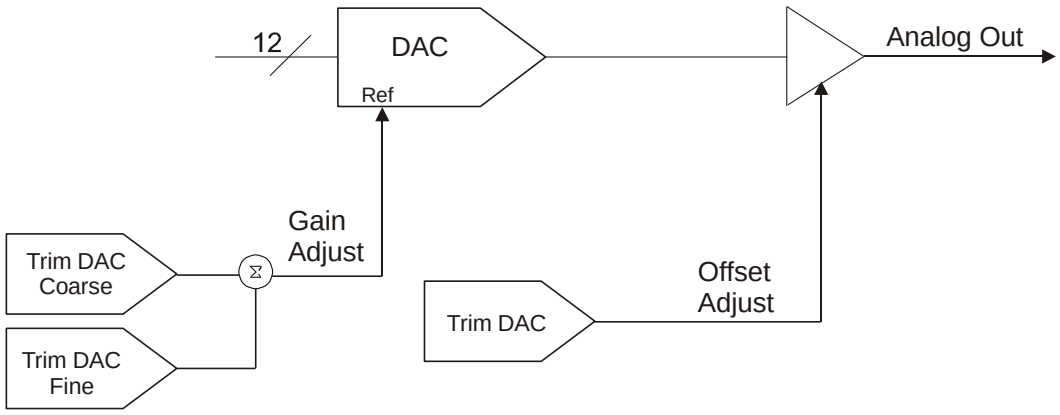



Figure 6. Analog output calibration

# Specifications

**Typical for 25 °C unless otherwise specified.**

**Specifications in *italic text* are guaranteed by design.**

## Analog input

Table 1. Analog input specifications

| | |
|---|---|
| A/D converter type | ADS7800 |
| Resolution | 12 bits |
| Number of channels | 16 single ended / 8 differential, software selectable |
| Input ranges<br>(SW programmable) | Bipolar: ±10 V, ±5 V, ±2.5 V, ±1.25 V<br>Unipolar: 0 to 10 V, 0 to 5 V, 0 to 2.5 V, 0 to 1.25 V |
| Polarity | Unipolar/Bipolar, software selectable |
| A/D pacing<br>(SW programmable) | Internal counter |
| | External source (A/D External Pacer) |
| | Software polled |
| Burst mode | Software selectable option, burst rate = 3 µS. |
| A/D trigger sources | External digital (A/D External Trigger) |
| | External analog (Analog Trigger In) |
| A/D triggering modes | External digital: Software configurable for:<br>▪ edge (triggered)<br>▪ level-activated (gated).<br>Programmable polarity (rising/falling edge trigger, high/low gate). |
| | External analog: Software-configurable for:<br>▪ Positive or negative slope.<br>▪ Above or below reference<br>▪ Positive or negative hysteresis<br>▪ In or out of window<br>Trigger levels set by DAC0 and/or DAC1, 4.88 mV resolution. |
| | Unlimited pre- and post-trigger samples. Total # of samples must be > 512. Compatible with both digital and analog trigger options. |
| Data transfer | From 1024 sample FIFO via REPINSW |
| | Programmed I/O |
| *A/D conversion time* | *3.0 µS max* |
| Throughput | 330 kS/s min |
| Calibration | Auto-calibration, calibration factors for each range stored on board in non-volatile RAM. |

## Accuracy

330 kHz sampling rate, single channel operation and a 60-minute warm-up. Accuracies are listed for operational temperatures within ±2 ºC of internal calibration temperature. Calibrator test source high side tied to Channel 0 High, and low side tied to Channel 0 Low. Low-level ground is tied to Channel 0 Low at the user connector.

Table 2. Absolute accuracy specifications

| Range | Absolute Accuracy (LSB) | Absolute Accuracy (mV) |
|---|---|---|
| ±10 V | ±2.5 LSB | ±12.2 |
| ±5 V | ±2.5 LSB | ±6.10 |
| ±2.5 V | ±2.5 LSB | ±3.05 |
| ±1.25 V | ±2.5 LSB | ±1.53 |
| 0 V to +10 V | ±2.5 LSB | ±6.10 |
| 0 V to +5 V | ±2.5 LSB | ±3.05 |
| 0 V to +2.5 V | ±2.5 LSB | ±1.53 |
| 0 V to +1.25 V | ±2.5 LSB | ±0.76 |

Table 3. Accuracy components (errors in LSBs)

| Range | Gain Error | Offset Error | DLE | ILE |
|---|---|---|---|---|
| ±10 V | ±1.0 max | ±1.0 max | ±0.75 max | ±1.5 max |
| ±5 V | ±1.0 max | ±1.0 max | ±0.75 max | ±1.5 max |
| ±2.5 V | ±1.0 max | ±1.0 max | ±0.75 max | ±1.5 max |
| ±1.25 V | ±1.0 max | ±1.0 max | ±0.75 max | ±1.5 max |
| 0 to +10 V | ±1.0 max | ±1.0 max | ±0.75 max | ±1.5 max |
| 0 to +5 V | ±1.0 max | ±1.0 max | ±0.75 max | ±1.5 max |
| 0 to +2.5 V | ±1.0 max | ±1.0 max | ±0.75 max | ±1.5 max |
| 0 to +1.25 V | ±1.0 max | ±1.0 max | ±0.75 max | ±1.5 max |

Each PCI-DAS1602/12 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in Table 2.

As shown in Table 3, total board error is a combination of gain, offset, differential linearity error (DLE) and integral linearity error (ILE). The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case errors are realized only in the unlikely event that each of the component errors is at their maximum level, and causing error in the same direction.

Table 4. Analog input drift specifications

| | |
|---|---|
| ADC full-scale gain drift | ±6 ppm/°C |
| ADC zero drift | ±6 ppm/°C |
| No missing codes guaranteed | 12 bits |
| Common mode range | ±10 V |
| CMRR @ 60 Hz | -70 dB typ |
| *Input impedance* | *10 MOhm min* |
| *Input leakage current* | *200 nA max* |
| *Absolute maximum input voltage* | *±35 V power on or off* |
| Warm-up time | 60 minutes |

### Noise performance

Table 5 summarizes the noise performance for the PCI-DAS1602/12. Noise distribution is determined by gathering 50 K samples @ 330 kHz with inputs tied to ground at the user connector.

Table 5. Noise performance specifications

| Range | % within ±2 counts | % within ±1 count | MaxCounts | LSBrms* |
|---|---|---|---|---|
| ±10 V | 100% | 100% | 3 | 0.45 |
| ±5 V | 100% | 100% | 3 | 0.45 |
| ±2.5 V | 100% | 100% | 3 | 0.45 |
| ±1.25 V | 100% | 100% | 5 | 0.76 |
| 0 to +10 V | 100% | 100% | 3 | 0.45 |
| 0 to +5 V | 100% | 100% | 3 | 0.45 |
| 0 to +2.5 V | 100% | 100% | 3 | 0.45 |
| 0 to +1.25 V | 100% | 100% | 5 | 0.76 |

* RMS noise is defined as the peak-to-peak bin spread divided by 6.6.

## Analog output

Table 6. Analog output specifications

| | |
|---|---|
| *A/D converter type* | *AD7945BR multiplying type* |
| *Resolution* | *12-bits* |
| *Number of channels* | *2* |
| Voltage ranges | ±10 V, ±5 V, 0 to 5 V, 0 to 10 V. Each independently programmable |
| *Monotonicity* | *Guaranteed monotonic over temperature* |
| Overall analog output drift | ▪ ±0.02 LSB/°C |
| Slew rate | ▪ ±10 V Range: 15 V/µs<br>▪ ±5 V Range: 10 V/µs<br>▪ 0 to 10 V Range: 7.5V/µs<br>▪ 0 to 5 V Range: 5 V/µs |
| Settling time | 20 V step to 0.012%: 4 µs max |
| Current drive | ±5 mA |
| *Output short-circuit duration* | *Indefinite @ 25 mA* |
| *Output coupling* | *DC* |
| Output impedance | 0.1 ohms |
| Power up and reset | DACs cleared to 0 volts ±200 mV max |

### Accuracy

Table 7. Absolute accuracy specifications

| Range | Absolute Accuracy |
|---|---|
| ±10 V | ±3.0 LSB |
| ±5 V | ±3.0 LSB |
| 0 V to +10 V | ±3.0 LSB |
| 0 V to +5 V | ±3.0 LSB |

Table 8. Accuracy components (errors in LSBs)

| Range | Gain Error (LSB) | Offset Error (LSB) | DLE (LSB) | ILE (LSB) |
|---|---|---|---|---|
| ±10 V | ±2.0 max | ±0.1 max | ±1.0 max | ±1.0 max |
| ±5 V | ±2.0 max | ±0.2 max | ±1.0 max | ±1.0 max |
| 0 to +10 V | ±2.0 max | ±0.2 max | ±1.0 max | ±1.0 max |
| 0 to +5 V | ±2.0 max | ±0.4 max | ±1.0 max | ±1.0 max |

Each PCI-DAS1602/12 is tested at the factory to assure the board's overall error does not exceed ±3.0 LSB.

Total board error is a combination of gain, offset, integral linearity and differential linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction. Although an examination of the chart and a summation of the maximum theoretical errors shows that the board could theoretically exhibit a ±4.4 LSB error, our testing assures this error is never realized in a board that we ship.

### Analog output pacing and triggering

Table 9. Analog output pacing and triggering specifications

| | |
|---|---|
| D/A pacing (SW programmable) | Internal counter |
| | External source (D/A EXTERNAL PACER) |
| | Software paced |
| D/A trigger Modes | External digital (EXTERNAL D/A PACER GATE) |
| | Software triggered |
| Data transfer | From 1024 sample FIFO via REPOUTSW mode. Data interleaved for dual analog output mode. |
| | Programmed I/O |
| | Update DACs individually or simultaneously (SW selectable) |
| Throughput | 250 KHz max per channel, 2 channels simultaneous |

## Digital input/output

Table 10. Digital input/output specifications

| | |
|---|---|
| Digital type | 82C55 |
| Number of I/O | 24 (FIRSTPORTA Bit 0 through FIRSTPORTC Bit 7) |
| Configuration | 2 banks of 8 and 2 banks of 4 or |
| | 3 banks of 8 or |
| | *2 banks of 8 with handshake* |
| *Input high voltage* | *2.0 V min, 5.5 V absolute max* |
| *Input low voltage* | *0.8 V max, –0.5 V absolute min* |
| *Output high voltage (IOH = -2.5 mA)* | *3.0 V min* |
| *Output low voltage (IOL = 2.5 mA)* | *0.4 V max* |
| Power-up / reset state | Input mode (high impedance) |

# Interrupts

Table 11. Interrupt specifications

| | |
|---|---|
| Interrupt | INTA# - mapped to IRQ*n* via PCI BIOS at boot-time |
| PCI Interrupt enable | Programmable |
| Interrupt sources | ▪ External (rising TTL edge event)<br>▪ Residual sample counter<br>▪ A/D end of conversion<br>▪ A/D end of channel scan<br>▪ A/D FIFO-not-empty<br>▪ A/D FIFO-half-full<br>▪ D/A FIFO-not-empty<br>▪ D/A FIFO-half-full |

# Counters

Table 12. Counter specifications

| | | |
|---|---|---|
| Counter type | 82C54 | |
| Configuration | Two 82C54 devices. 3 down counters per 82C54, 16 bits each | |
| Counter 1 — ADC residual sample counter | Source: | ADC Clock |
| | Gate: | Programmable source |
| | Output: | End-of-Acquisition interrupt source |
| Counter 2 — ADC pacer lower divider | Source: | Internal 10 MHz |
| | Gate: | Tied to counter 3 gate, programmable source. |
| | Output: | Chained to counter 3 clock |
| Counter 3 — ADC pacer upper divider | Source: | Counter 2 output |
| | Gate: | Tied to counter 2 gate, programmable source |
| | Output: | ADC Pacer clock (if software selected), available at user connector |
| Counter 4 — Pre-trigger mode | Source: | ADC Clock |
| | Gate: | A/D External Trigger |
| | Output: | End-of-Acquisition interrupt source |
| Counter 4 — Non pre-trigger mode | Source: | User input at 100-pin connector (CLK 4) or internal 10 MHz (software selectable) |
| | Gate: | User input at 100-pin connector (GATE 4) |
| | Output: | Available at 100-pin connector (OUT 4) |
| Counter 5 — DAC pacer lower divider | Source: | Internal 10 MHz |
| | Gate: | Tied to counter 6 gate, programmable source. |
| | Output: | Chained to counter 6 clock |
| Counter 6 — DAC pacer upper divider | Source: | Counter 5 output |
| | Gate: | Tied to Counter 5 gate, programmable source. |
| | Output: | DAC Pacer clock, available at user connector (D/A INTERNAL PACER OUTPUT) |
| *Gate width high* | *50 ns min* | |
| *Gate width low* | *50 ns min* | |
| *Input high* | *2.0 volts min, 5.5 volts absolute max* | |
| *Input low* | *0.8 volts max, -0.5 volts absolute min* | |
| *Output high* | *3.0 volts min @ -2.5 mA* | |
| *Output low* | *0.4 volts max @ 2.5 mA* | |
| Crystal oscillator frequency | 10 MHz | |

## Power consumption

Table 13. Power consumption specifications

| | |
|---|---|
| +5 V | 1.2 A typical, 1.5 A max |
| +12 V | 30 mA max |

## Environmental

Table 14. Environmental specifications

| | |
|---|---|
| Operating temperature range | 0 to 70°C |
| Storage temperature range | -40 to 100°C |
| Humidity | 0 to 95% non-condensing |

## Mechanical

Table 15. Mechanical specifications

| | |
|---|---|
| Card dimensions | PCI half card: 174.4 mm (L) x 100.6 mm (W) x 11.65 mm (H) |

## Main connector and pin out

Table 16. Main connector specifications

| | |
|---|---|
| Connector type | 100-pin high-density Robinson-Nugent. |
| Compatible cables | C100FF-x |
| Compatible accessory products | ISO-RACK16/P<br>ISO-DA02/P<br>BNC-16SE<br>BNC-16DI<br>CIO-MINI50<br>CIO-TERM100<br>SCB-50<br>SSR-RACK24 (DADP-5037 adaptor required)<br>SSR-RACK08 (DADP-5037 with TN-MC78M05CT adaptor required)<br>CIO-ERB24 (DADP-5037 adaptor required)<br>CIO-ERB08 (DADP-5037 adaptor required)<br>CIO-SERB08 (DADP-5037 adaptor required) |

Table 17. 8-channel differential mode

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | LLGND | 51 | FIRSTPORTA Bit 0 |
| 2 | CH0 HI | 52 | FIRSTPORTA Bit 1 |
| 3 | CH0 LO | 53 | FIRSTPORTA Bit 2 |
| 4 | CH1 HI | 54 | FIRSTPORTA Bit 3 |
| 5 | CH1 LO | 55 | FIRSTPORTA Bit 4 |
| 6 | CH2 HI | 56 | FIRSTPORTA Bit 5 |
| 7 | CH2 LO | 57 | FIRSTPORTA Bit 6 |
| 8 | CH3 HI | 58 | FIRSTPORTA Bit 7 |
| 9 | CH3 LO | 59 | FIRSTPORTB Bit 0 |
| 10 | CH4 HI | 60 | FIRSTPORTB Bit 1 |
| 11 | CH4 LO | 61 | FIRSTPORTB Bit 2 |
| 12 | CH5 HI | 62 | FIRSTPORTB Bit 3 |
| 13 | CH5 LO | 63 | FIRSTPORTB Bit 4 |
| 14 | CH6 HI | 64 | FIRSTPORTB Bit 5 |
| 15 | CH6 LO | 65 | FIRSTPORTB Bit 6 |
| 16 | CH7 HI | 66 | FIRSTPORTB Bit 7 |
| 17 | CH7 LO | 67 | FIRSTPORTC Bit 0 |
| 18 | LLGND | 68 | FIRSTPORTC Bit 1 |
| 19 | N/C | 69 | FIRSTPORTC Bit 2 |
| 20 | N/C | 70 | FIRSTPORTC Bit 3 |
| 21 | N/C | 71 | FIRSTPORTC Bit 4 |
| 22 | N/C | 72 | FIRSTPORTC Bit 5 |
| 23 | N/C | 73 | FIRSTPORTC Bit 6 |
| 24 | N/C | 74 | FIRSTPORTC Bit 7 |
| 25 | N/C | 75 | N/C |
| 26 | N/C | 76 | N/C |
| 27 | N/C | 77 | N/C |
| 28 | N/C | 78 | N/C |
| 29 | N/C | 79 | N/C |
| 30 | N/C | 80 | N/C |
| 31 | N/C | 81 | N/C |
| 32 | N/C | 82 | N/C |
| 33 | N/C | 83 | N/C |
| 34 | N/C | 84 | N/C |
| 35 | D/A GND 0 | 85 | N/C |
| 36 | D/A OUT 0 | 86 | N/C |
| 37 | D/A GND 1 | 87 | N/C |
| 38 | D/A OUT 1 | 88 | N/C |
| 39 | CTR4 CLK | 89 | GND |
| 40 | CTR4 GATE | 90 | +12 V |
| 41 | CTR4 OUT | 91 | GND |
| 42 | A/D EXTERNAL PACER | 92 | -12 V |
| 43 | ANALOG TRIGGER IN | 93 | N/C |
| 44 | D/A EXTERNAL PACER IN | 94 | N/C |
| 45 | A/D EXTERNAL TRIGGER IN | 95 | A/D INTERNAL PACER OUTPUT |
| 46 | N/C | 96 | D/A INTERNAL PACER OUTPUT |
| 47 | N/C | 97 | EXTERNAL D/A PACER GATE |
| 48 | PC +5 V | 98 | N/C |
| 49 | SSH OUT | 99 | EXTERNAL INTERRUPT |
| 50 | GND | 100 | GND |

Table 18. 16-channel single-ended mode

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | LLGND | 51 | FIRSTPORTA Bit 0 |
| 2 | CH0 HI | 52 | FIRSTPORTA Bit 1 |
| 3 | CH8 HI | 53 | FIRSTPORTA Bit 2 |
| 4 | CH1 HI | 54 | FIRSTPORTA Bit 3 |
| 5 | CH9 HI | 55 | FIRSTPORTA Bit 4 |
| 6 | CH2 HI | 56 | FIRSTPORTA Bit 5 |
| 7 | CH10 HI | 57 | FIRSTPORTA Bit 6 |
| 8 | CH3 HI | 58 | FIRSTPORTA Bit 7 |
| 9 | CH11 HI | 59 | FIRSTPORTB Bit 0 |
| 10 | CH4 HI | 60 | FIRSTPORTB Bit 1 |
| 11 | CH12 HI | 61 | FIRSTPORTB Bit 2 |
| 12 | CH5 HI | 62 | FIRSTPORTB Bit 3 |
| 13 | CH13 HI | 63 | FIRSTPORTB Bit 4 |
| 14 | CH6 HI | 64 | FIRSTPORTB Bit 5 |
| 15 | CH14 HI | 65 | FIRSTPORTB Bit 6 |
| 16 | CH7 HI | 66 | FIRSTPORTB Bit 7 |
| 17 | CH15 HI | 67 | FIRSTPORTC Bit 0 |
| 18 | LLGND | 68 | FIRSTPORTC Bit 1 |
| 19 | N/C | 69 | FIRSTPORTC Bit 2 |
| 20 | N/C | 70 | FIRSTPORTC Bit 3 |
| 21 | N/C | 71 | FIRSTPORTC Bit 4 |
| 22 | N/C | 72 | FIRSTPORTC Bit 5 |
| 23 | N/C | 73 | FIRSTPORTC Bit 6 |
| 24 | N/C | 74 | FIRSTPORTC Bit 7 |
| 25 | N/C | 75 | N/C |
| 26 | N/C | 76 | N/C |
| 27 | N/C | 77 | N/C |
| 28 | N/C | 78 | N/C |
| 29 | N/C | 79 | N/C |
| 30 | N/C | 80 | N/C |
| 31 | N/C | 81 | N/C |
| 32 | N/C | 82 | N/C |
| 33 | N/C | 83 | N/C |
| 34 | N/C | 84 | N/C |
| 35 | D/A GND 0 | 85 | N/C |
| 36 | D/A OUT 0 | 86 | N/C |
| 37 | D/A GND 1 | 87 | N/C |
| 38 | D/A OUT 1 | 88 | N/C |
| 39 | CTR4 CLK | 89 | GND |
| 40 | CTR4 GATE | 90 | +12 V |
| 41 | CTR4 OUT | 91 | GND |
| 42 | A/D EXTERNAL PACER | 92 | -12 V |
| 43 | ANALOG TRIGGER IN | 93 | N/C |
| 44 | D/A EXTERNAL PACER IN | 94 | N/C |
| 45 | A/D EXTERNAL TRIGGER IN | 95 | A/D INTERNAL PACER OUTPUT |
| 46 | N/C | 96 | D/A INTERNAL PACER OUTPUT |
| 47 | N/C | 97 | EXTERNAL D/A PACER GATE |
| 48 | PC +5 V | 98 | N/C |
| 49 | SSH OUT | 99 | EXTERNAL INTERRUPT |
| 50 | GND | 100 | GND |

# CE Declaration of Conformity

Manufacturer: Measurement Computing Corporation
Address: 10 Commerce Way
Suite 1008
Norton, MA 02766
USA

Category: Information technology equipment.

Measurement Computing Corporation declares under sole responsibility that the product

**PCI-DAS1602/12**

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EC EMC Directive 2004/108/EC: Electromagnetic Compatibility, EN 61326-1:2006 (IEC 61326-1:2005)

Emissions: Group 1, Class B

- EN55022 (1995)/CISPR 22: Radiated and Conducted emissions.

Immunity: EN61326-1:2006, (IEC 61326-1:2005)

- EN61000-4-2 (2001): Electrostatic Discharge immunity.
- EN61000-4-3 (2002): Radiated Electromagnetic Field immunity.
- EN61000-4-4 (2004): Electric Fast Transient Burst immunity.
- EN61000-4-5 (2001): Surge immunity.
- EN61000-4-6 (2003): Radio Frequency Common Mode immunity.
- EN61000-4-11 (2004): Voltage Dip and Interrupt immunity.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in September, 2001. Test records are outlined in Chomerics Test Report #EMI3053.01. Further testing was conducted by Chomerics Test Services, Woburn, MA. 01801, USA in December, 2008. Test records are outlined in Chomerics Test report #EMI5241.08.

We hereby declare that the equipment specified conforms to the above Directives and Standards.

Carl Haapaoja, Director of Quality Assurance

**Measurement Computing Corporation**
**10 Commerce Way**
**Suite 1008**
**Norton, Massachusetts 02766**
**(508) 946-5100**
**Fax: (508) 946-9500**
**E-mail: info@mccdaq.com**
**www.mccdaq.com**