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MIPI CSI-2 Receiver 1.1 IP Core User Guide

Revised September 12, 2018; Author Elod Gyorgy

1 Introduction

This user guide describes the Digilent MIPI CSI-2 Receiver Intellectual Property. This IP is compatible with CSI-2 1.0 specifications and supports decoding selected pixel formats and packing data into an AXI-Stream. It pairs up with a MIPI D-PHY Receiver IP over the standard PHY Protocol Interface (PPI) to source a video subsystem.

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Xilinx®: AXI4-Lite, AXI-Stream, rx_mipi_ppi
Provided with core	
Design files	VHDL
Simulation model	VHDL Behavioral
Constraints file	XDC
Software driver	standalone
Tested design flows	
Design entry	Vivado™ Design Suite 2017.4
Synthesis	Vivado Synthesis 2017.4

2 Features

- Single or dual lane support
- RAW10 support
- Four pixels per beat AXI-Stream output for high bandwidth applications
- Xilinx interfaces used: AXI4-Lite, AXI-Stream, rx_mipi_ppi_if_rtl:1.0

3 Performance

The IP has been tested in dual-lane configuration with an 84 MHz PPI high-speed byte clock (RxByteClkHS) and 150 MHz AXI-Stream clock (video_aclk).

4 Resource Utilization

Device	Configuration	Resource				
		LUT	FF	BRAM	URAM	DSP
xc7z020clg400-1	AXI-Lite Interface	430	693	2.5	0	0

5 Overview

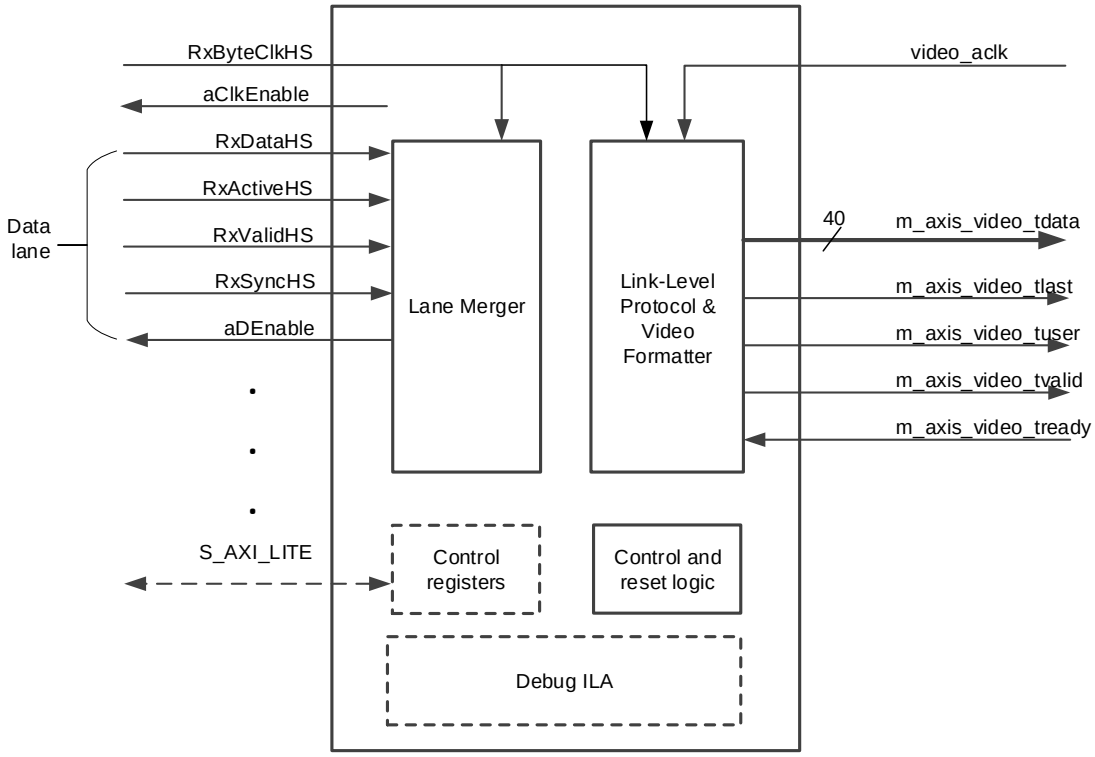

Figure 1. DVI to VGA converter block diagram.

The IP is built from multiple blocks: lane merger, link-level protocol/video formatter, control logic and optional debug modules.

6 Port Descriptions

7 Designing with the core

7.1 Constraints

7.2 Customization

8 Debugging

9 References