

Video Scaler 1.0 IP Core User Guide

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1 Introduction

This user guide describes the Digilent Video Scaler Intellectual Property. It takes video frames of arbitrary resolution over a slave AXI-Stream interface, resizes them to an arbitrary output resolution and outputs on a master AXI-Stream interface. It has an AXI4-Lite interface for control.

2 Features

- One pixel per beat
- 24-bit color depth
- RGB format
- Xilinx interfaces used: AXI4-Lite, AXI-Stream
 Port Descriptions

3 Designing with the core

3.1 Constraints

3.2 Customization

4 Register map

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Xilinx®: AXI4-Lite, AXI-Stream
Provided with core	
Design files	VHDL
Simulation model	VHDL Behavioral
Constraints file	XDC
Software driver	standalone
Tested design flows	
Design entry	Vivado™ HLS 2018.2
Synthesis	Vivado Synthesis 2018.2

Offset	Register Name	Description
0x00	Control signals	bit 0 - ap_start (Read/Write/COH) bit 1 - ap_done (Read/COR) bit 2 - ap_idle (Read) bit 3 - ap_ready (Read) bit 7 - auto_restart (Read/Write) others - reserved
0x04	Global Interrupt Enable Register	bit 0 - Global Interrupt Enable (Read/Write)
0x08	IP Interrupt Enable Register (Read/Write)	bit 0 - Channel 0 (ap_done) bit 1 - Channel 1 (ap_ready)

Offset	Register Name	Description
0x0C	IP Interrupt Status Register (Read/TOW)	bit 0 - Channel 0 (ap_done) bit 1 - Channel 1 (ap_ready)
0x10	Data signal of in_width	bit 31~0 - in_width[31:0] (Read/Write)
0x18	Data signal of in_height	bit 31~0 - in_height[31:0] (Read/Write)
0x20	Data signal of out_width	bit 31~0 - out_width[31:0] (Read/Write)
0x28	Data signal of out_height	bit 31~0 - out_height[31:0] (Read/Write)

// (SC = Self Clear, COR = Clear on Read, TOW = Toggle on Write, COH = Clear on Handshake)

5 Debugging

Opening the IP in HLS is possible by executing the following command in the Vivado HLS Command Prompt:

```
cd <path_to_IP>/hls_src  
vivado_hls -f script.tcl
```

6 References