1300 Henley Court
Pullman, WA 99163
509.334.6306
www.digilentinc.com

HLS Gamma Correction 1.0 IP Core User Guide

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1 Introduction

This user guide describes the Digilent Gamma Correction Intellectual Property. This IP interfaces to both the Axi-Lite and Axi-Stream in order to process a video stream and control the resolution and the gamma factor.

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Axi-Lite Axi-Stream
Provided with core	
Design files	C++
Simulation model	HLS Simulation
Constraints file	XDC
Software driver	Automatically generated
Tested design flows	
Design entry	Vivado™ Design Suite 2017.4
Synthesis	Vivado Synthesis 2017.4

2 Features

- Axi- Stream 24-bit video input and output
- Axi-Lite interface for gamma and resolution control
- Resolution supported: up to 1920x1080/60Hz (clock: 148.5 MHz)
- Gamma adjustment: 0.4, 0.2, 1, 1.2, 1.4, 1.6, 1.8, 2.0, 2.2

3 Performance

The IP has been written in HLS with a target clock frequency of 150 MHz (6.67 ns) for a maximum resolution of 1920x1080. The maximum latency is at 2081164 ns with an initiation interval of 2081164 ns which is approximately one frame. The latency and initiation interval are scaled with the input resolution, meaning that a lower resolution the latency will also be lower.

4 Usage

The IP has been initially designed for a xc7z020clg400-1 target device, the resource usage for this FPGA are illustrated in

Name	BRAM-18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	8
FIFO	0	-	65	300
Instance	16	-	1030	1984
Memory	-	-	-	-
Multiplexer	-	-	-	18
Register	-	-	2	-
Total	16	0	1097	2358
Utilization(%)	5	0	1	4

Table 1 FPGA usage

5 Overview

The IP core has been written entirely in Vivado HLS by using the HLS Video Library provided by Xilinx and a custom gamma correction function written by the author. In order to minimize the resource cost of the IP core, the values of the gamma have been precompiled and stored in to lookup tables. The selection of the desired gamma is done using a simple case structure which multiplexes the LUTs which will be implemented.

5.1 Processing

The input format for the image/video stream is the Axi-stream interface which can accept 24 bits of RGB data (8 bit/color) respecting the Xilinx video format. Before the actual gamma enhancement, the input stream is converted in to a matrix format with de height and width corresponding to the resolution of the input image, this is done using the HLS Video Library function *AXIvideo2cvMat.*

Once the gamma processing has been finished the image is outputted to the Axi-Stream interface. The output Axi-Stream interface has the same format as the input Axi-Stream interface.

5.2 Gamma Correction

Gamma correction changes the lighting value of an image in a non-linear way which is closer to how the human eye perceives the it. This correction dose not effect the other elements of an image besides the light thus it can be applied directly to the RGB comments individually. As a rule gamma correction must be applied after all the previous image processing functions have been applied.

The mathematical function which is used to create the LUTs is given by the following equation

$$dst = \left(\frac{src}{255}\right)^{\frac{1}{gamma}} * 255$$

Equation 1.Gamma correction algorithm

Like previously mentioned the IP contain predefined LUT's for some *gamma* variable which have been calculated using this function which has been implemented in to the Test Bench of the HLS project. For a visual representation of the function with the chosen fact values of the LUTs please refer to the following chart

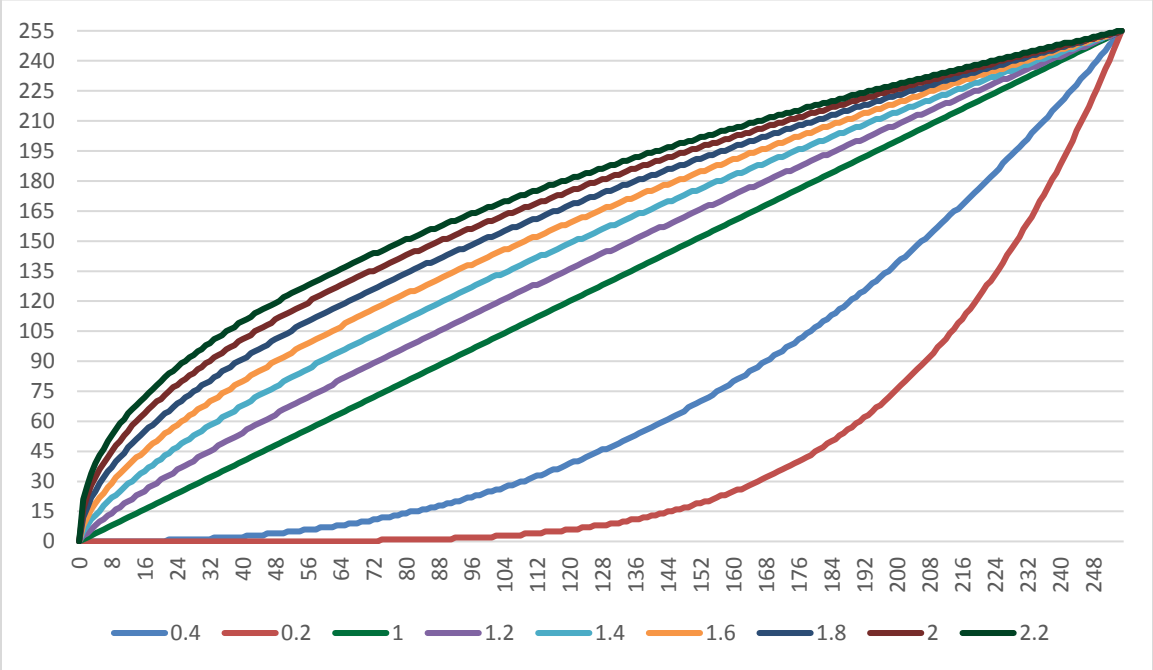

Figure 1 In/Out characteristic of gamma correction

5.3 HLS directives

The used directives for this IP core have been added to the source files, for further information on how they work and how to use them please refer to UG902: High-Level Synthesis by Xilinx.

5.4 Axi-Lite

The Axi-Lite interface is defined using HLS and controls three input variables of the main Gamma correction function. Using this interface, the user can change the resolution of both the input and the output image to a maximum of 1920x1080 and the desired gamma factor. Access to these parameters is provided via the automatically generated software driver, which respects the format of software drivers provided by Xilinx.

To change the gamma factor, the function *XHls_gamma_correction_Set_gamma* must be called. Gamma will change respecting the following rule:

Gamma	Factor
0	1
1	0.4
2	0.2
3	1.2
4	1.4
5	1.6
6	1.8
7	2.0
8	2.2

Table 2 Gamma selection

6 Port Descriptions

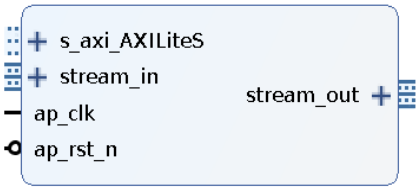

Figure 2 HLS Gamma Correction IP core

Signal Name	Interface	Signal Type	Init State	Description
Ap_rst_n	-	I	N/A	Asynchronous reset for the core
ap_clk	-	I	N/A	Clock for the IP core, used for Stream in/output and Axi-Lite
s_axi_AXILiteS*	Axi-Lite	I	N/A	Axi-Lite interface used to configure height, width and gamma
stream_in	Axi-Stream	I	N/A	Input video stream on 24 bits, using Xilinx video format
stream_out	Axi-Stream	O	N/A	Output video stream on 24 bits, using Xilinx video format

Table 3. Port descriptions.

7 Designing with the core

7.1 Customization

The currently IP core has been packaged for a maximum frequency of 150 MHz and a maximum resolution of 1920x1080 designed for a Zynq xc7z020clg400-1 device. Fur customization and further changes please create a HLS project and import all the files provided in the hls_src folder of the IP.

8 References

The following document provides additional information on the subjects discussed:

1. Xilinx Inc., UG902: High-Level Synthesis, v2017.4, February 2, 2018.