CIO-DI48,
CIO-DI96,
CIO-DI192

User's Manual

Revision 3A
October, 2000

Trademark and Copyright Information

Measurement Computing Corporation, InstaCal, Universal Library, and the Measurement Computing logo are either trademarks or registered trademarks of Measurement Computing Corporation. Refer to the Copyrights & Trademarks section on mccdaq.com/legal for more information about Measurement Computing trademarks. Other product and company names mentioned herein are trademarks or trade names of their respective companies.

© 2000 Measurement Computing Corporation. All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted, in any form by any means, electronic, mechanical, by photocopying, recording, or otherwise without the prior written permission of Measurement Computing Corporation.

Notice

Measurement Computing Corporation does not authorize any Measurement Computing Corporation product for use in life support systems and/or devices without prior written consent from Measurement Computing Corporation. Life support devices/systems are devices or systems that, a) are intended for surgical implantation into the body, or b) support or sustain life and whose failure to perform can be reasonably expected to result in injury. Measurement Computing Corporation products are not designed with the components required, and are not subject to the testing required to ensure a level of reliability suitable for the treatment and diagnosis of people.

Table of Contents

This page is intentionally blank.

1.0 INTRODUCTION

The CIO-DI48, 96 and 192 are designed to have the best quality and lowest cost of any digital input board.

Throughout this manual the model number CIO-DI## is used when the information applies to the CIO-DI48, CIO-DI96 and CIO-DI192 inclusive. Exclusive information for a particular version will be identified.

CIO-DI48 is a dedicated 48-line digital input board built up of six, eight-input logic chips. There are no control registers. The input pins present a single LSTTL load. Similarly, the 96-line and 192-line versions use 12 or 24 eight-input logic chips respectively.

The CIO-DI## also conforms to the connector pin specification of all the CIO-DIO family of digital boards, so may be used in place of one another without changing cabling or connectors.

All these products are supported by Universal Library programming library.

A group of application notes at the end of this manual describes electrical interfacing subjects that may be useful for digital I/O applications.

2.0 SOFTWARE INSTALLATION

In order to easily test your installation, it is recommended that you install *Insta*Cal, the installation, calibration and test utility that was supplied with your board. Refer to the *Extended Software Installation Manual* for information on the initial setup, loading, and installation of *Insta*Cal and optional Universal Library software.

InstaCal will guide you through hardware settings and allow you to easily test for conflicts. If you decide not to use Instacal to assist board configuration, details are provided in the following section.

3.0 HARDWARE SETUP

3.1 BASE ADDRESS SELECTION

The CIO-DI## employs the PC bus for power, communications and data transfer. As such it draws power from the PC, monitors the address lines and control signals and responds to it's I/O address, and it receives and places data on the 8 data lines.

The BASE address is the most important user-selectable feature of the CIO-DI##. The base address, and offsets from it, are the locations that PC software reads input data from.

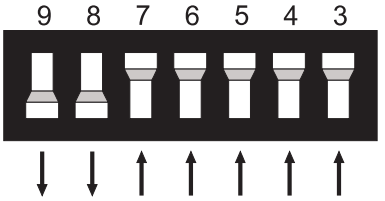
Base address dip switches are used for setting the base address. Each switch position corresponds to one of the PC bus address lines. Placing a switch down puts it in the active position.
A complete address is constructed by adding the HEX or decimal number which corresponds to all the address bits the CIO-DI## has been instructed to respond to. For example shown in Figure 3-1, switches 9 and 8 are DOWN, all others UP. Address 9 = 200h (512D) and address 8 = 100h
(256D), When added together they equal 300h (768D).

NOTE

Disregard the numbers printed on the switch; refer only to the numbers printed in white on the board!

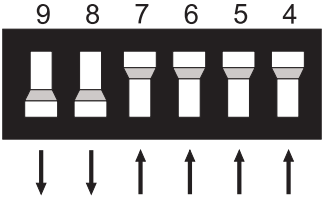
In Figure 3-1, note that the number of switches varies with the board version.

Certain addresses are used by the PC, others are free and may be used by the CIO-DI## and other expansion boards. We recommend trying the factory default address 300h (768D) first.



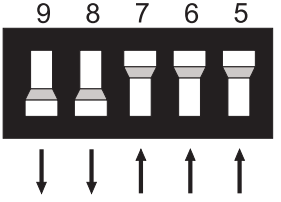
SW	HEX
A9	200
A8	100
A7	80
A6	40
A5	20
A4	10
A3	08

CIO-DI48
BASE ADDRESS SWITCH - Address 300h shown



SW	HEX
A9	200
A8	100
A7	80
A6	40
A5	20
A4	10

CIO-DI96
BASE ADDRESS SWITCH - Address 300h shown



SW	HEX
A9	200
A8	100
A7	80
A6	40
A5	20

CIO-DI192
BASE ADDRESS SWITCH - Address 300h shown

Figure 3-1. Base Address Switches

Table 2-1. PC I/O Addresses

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

The BASE switch can be set for address in the range of 000-3F8 so it should not be hard to find a free address area for you CIO-DI##. Once again, if you are not using IBM prototyping cards or some other board which occupies these addresses, then 300-31F HEX are free to use.

Addresses not specifically listed, such as 390-39F, are not reserved and may be available. Check your computer for other boards which may use I/O addresses.

4.0 HARDWARE INSTALLATION

4.1 INSTALLING THE BOARD

1. Turn the power off.
2. Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.
3. Locate an empty expansion slot in your computer.
4. Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DI##.

4.2 CABLING TO THE CONNECTOR(S)

The input connector(s) are accessible through the PC/AT expansion bracket. The connector is a standard 50-pin header connector. Cables with mating connectors (C50FF-#) can be purchased from Measurement Computing Corporation.

Those familiar with the CIO-DIO series boards will find the signal levels and pin assignments are identical with those on the CIO-DI##.

4.3 DIGITAL SIGNAL CHARACTERISTICS

Inputs are LSTTL (Low power Schotky TTL), a standard for digital signals which are either at 0V or 5V (nominal).

Low state	Near 0V
High state	Near 5V

See the electrical specification in this manual for details regarding logic levels and maximum voltages allowed at the inputs.

In addition to voltage and load matching, digital signals often need to be filtered ("de-bounced") to remove spurious false signals from relay or switch contacts. A description of this filtering method and other subjects on digital interfacing techniques is in the section on Interface Electronics in this manual.

4.4 CONNECTOR PIN-OUT DIAGRAMS

The CIO-DI## series boards use 50-pin header-type connector(s) mounted on the board that are accessible from the rear of the PC through the expansion backplate.

- The CIO-DI48 has one connector (Figure 4-2).
- The CIO-DI96 has two connectors (Figure 4-3).
- The CIO-DI192 has four connectors Figure 4-4).

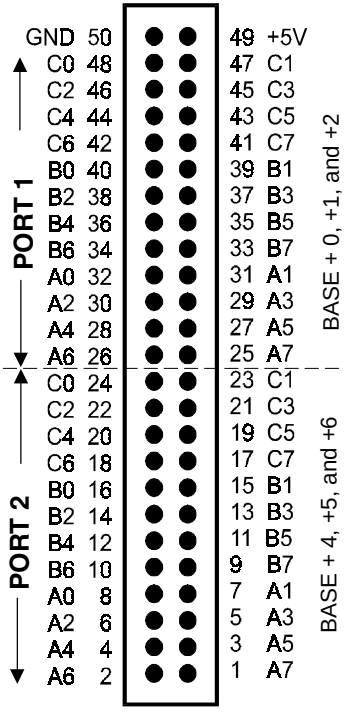


Figure 4-2. CIO-DI48 Connector Pin-Out & Register Assignments

NOTE: The input signals are direct connections to a digital buffer chip.

The connector accepts female 50-pin header type connectors, such as those on the C50FF-2, 2 foot cable with connectors.

If frequent changes to signal connections or signal conditioning is required, please refer to the information on the CIO-TERM100, CIO-SPADE50 and CIO-MINI50 screw terminal boards.

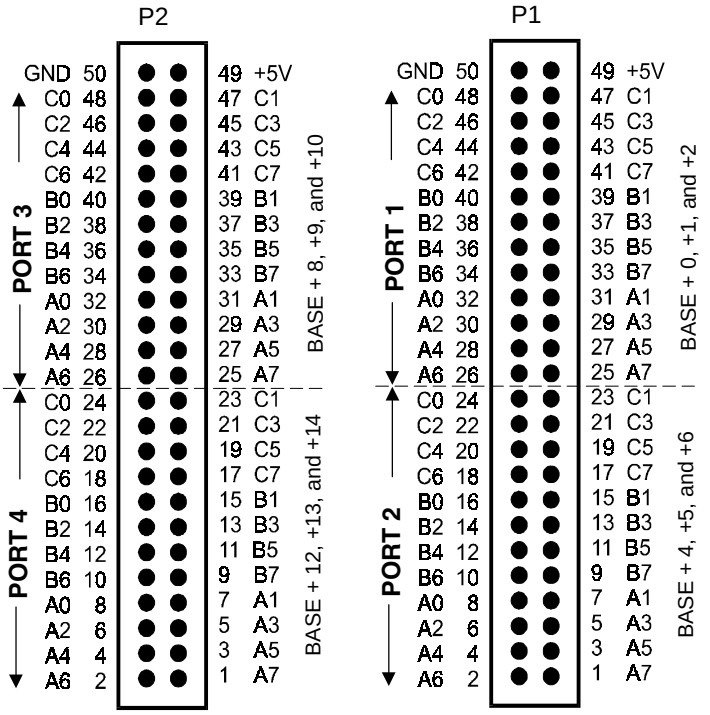


Figure 4-3. CIO-DI96 Pin-outs & Register Assignments

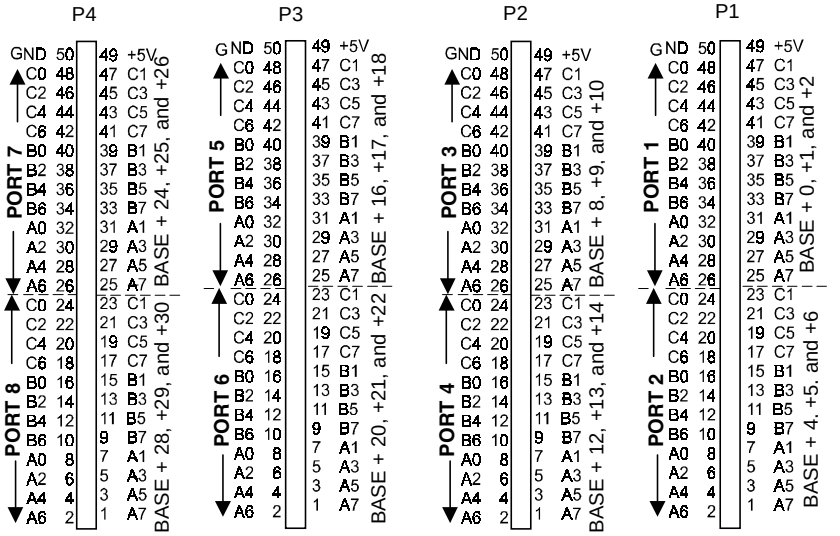


Figure 4-4. CIO-DI192 Connector Pin-outs & Register Assignments

5.0 DATA REGISTERS

5.1 INTRODUCTION

Each CIO-DI## is composed of parallel input chips. Each input buffer senses eight input pins. The ports are arranged in sets of three, with an intervening register that is not used. This scheme allows compatibility with software written to control 82C55 based boards when the 82C55 is used as all inputs. (On those boards, every fourth register is a control register.)

The first address, or BASE ADDRESS +0, is determined by setting a bank of switches on the board.

To read data from an input register, a byte is read representing the status of up to eight digital input lines.

5.2 CIO-DI48 REGISTERS

The CIO-DI48 uses eight registers. Their function is listed on Table 5-1.

Table 5-1. CIO-DI48 Registers

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE + 0	Read Port 1A Data	None
BASE + 1	Read Port 1B Data	None
BASE + 2	Read Port 1C Data	None
BASE + 3	None	None
BASE + 4	Read Port 2A Data	None
BASE + 5	Read Port 2B Data	None
BASE + 6	Read Port 2C Data	None
BASE + 7	None	None

PORTS 1A and 2A DATA
BASE ADDRESS + 0 and +4

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

PORTS 1B and 2B DATA
BASE ADDRESS + 1 and +5

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

PORTS 1C and 2C DATA
BASE ADDRESS + 2 and +6

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0

5.3 CIO-DI96 REGISTERS

The CIO-DI96 has 16 registers. Their function is listed on Table 5-2.

Table 5-2. CIO-DI96 Registers

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE + 0	Read Port 1A Data	None
BASE + 1	Read Port 1B Data	None
BASE + 2	Read Port 1C Data	None
BASE + 3	None	None
BASE + 4	Read Port 2A Data	None
BASE + 5	Read Port 2B Data	None
BASE + 6	Read Port 2C Data	None
BASE + 7	None	None
BASE + 8	Read Port 3A Data	None
BASE + 9	Read Port 3B Data	None
BASE + 10	Read Port 3C Data	None
BASE + 11	None	None
BASE + 12	Read Port 4A Data	None
BASE + 13	Read Port 4B Data	None
BASE + 14	Read Port 4C Data	None
BASE + 15	None	None

PORTS 1A, 2A, 3A, and 4A DATA
BASE ADDRESS + 0, +4, +8, and +12

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

PORTS 1B, 2B, 3B, and 4B DATA
BASE ADDRESS + 1, +5, +9, and +13

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

PORTS 1C, 2C, 3C, and 4C DATA
BASE ADDRESS + 2, +6, +10, and +14

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0

5.4 CIO-DI192 REGISTERS

The CIO-DI192 has 32 registers. Their function is listed on Table 5-3.

Table 5-3. CIO-DI192 Registers

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE + 0	Read Port 1A Data	None
BASE + 1	Read Port 1B Data	None
BASE + 2	Read Port 1C Data	None
BASE + 3	None	None
BASE + 4	Read Port 2A Data	None
BASE + 5	Read Port 2B Data	None
BASE + 6	Read Port 2C Data	None
BASE + 7	None	None
BASE + 8	Read Port 3A Data	None
BASE + 9	Read Port 3B Data	None
BASE + 10	Read Port 3C Data	None
BASE + 11	None	None
BASE + 12	Read Port 4A Data	None
BASE + 13	Read Port 4B Data	None
BASE + 14	Read Port 4C Data	None
BASE + 15	None	None
BASE + 16	Read Port 5A Data	None
BASE + 17	Read Port 5B Data	None
BASE + 18	Read Port 5C Data	None
BASE + 19	None	None
BASE + 20	Read Port 6A Data	None
BASE + 21	Read Port 6B Data	None
BASE + 22	Read Port 6C Data	None
BASE + 23	None	None
BASE + 24	Read Port 7A Data	None
BASE + 25	Read Port 7B Data	None
BASE + 26	Read Port 7C Data	None
BASE + 27	None	None
BASE + 28	Read Port 8A Data	None
BASE + 29	Read Port 8B Data	None
BASE + 30	Read Port 8C Data	None
BASE + 31	None	None

PORTS 1A through 8A DATA
BASE ADDRESS + 0, +4, +8, +12, +16, +20, +24, +28

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

PORTS 1B through 8B DATA
BASE ADDRESS + 1, +5, +9, +13, +17, +21, +25, and +29

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

PORTS 1C through 8C DATA
BASE ADDRESS + 2, +6, +10, +14, +18, +22, +26, and +30

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0

6.0 SPECIFICATIONS

Typical for 25°C unless otherwise specified.

POWER CONSUMPTION

+5V quiescent	
CIO-DI48	300 mA typical, 390 mA max
CIO-DI96	475 mA typical, 620 mA max
CIO-DI192	630 mA typical, 820 mA max

DIGITAL INPUT / OUTPUT

Digital Type	74LS373
Configuration	Input only
CIO-DI48	6 banks of 8 bits
CIO-DI96	12 banks of 8 bits
CIO-DI192	24 banks of 8 bits
Number of channels	
CIO-DI48	48 inputs
CIO-DI96	96 inputs
CIO-DI192	192 inputs
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, –0.5 volts absolute min
Miscellaneous	Locations provided for installation of pull-up or pull-down resistors.

ENVIRONMENTAL

Operating temperature range	0 to 70°C
Storage temperature range	–40 to 100°C
Humidity	0 to 90% non-condensing

7.0 INTERFACING TECHNIQUES

This brief introduction to the electronics most often needed by digital I/O board users covers a few basic concepts.

7.1 UNCONNECTED INPUTS FLOAT

Keep in mind that unconnected inputs float. If you are using the CIO-DI## board with unconnected inputs, ignore the data from those lines.

In other words, if you connect bit A0 and not bit A1, do not be surprised if A1 stays low, stays high or tracks A0. It is unconnected and so unspecified. The input buffer is not malfunctioning. In the absence of a pull-up or pull-down resistor, any input to a CIO-DI## which is unconnected, is unspecified!

You do not have to tie input lines, and unconnected lines will not affect the performance of connected lines. Just make sure that you mask out any unconnected bits in software!

An alternative to masking inputs is to define the state of unused inputs by using pull-up or pull-down resistors. There are locations on the board for installation of these resistors marked RN1 through RN6 on the DI48, through RN12 on the DI96 and through RN24 of the DI192. The location associated with FIRST PORT A (the port at Base +0) is RN1. The location for FIRST PORT B (the port at Base +1) is RN2. FIRST PORT C (Base +2) is RN3; SECOND PORT A (Base +4) is RN4; SECOND PORT B (Base +5) is RN5; SECOND PORT C (Base +6) is RN6 and so on.

A 10Kohm, eight-resistor SIP has all its resistors connected on one end to a single common pin. The common pin is marked with a dot and is at one end of the SIP. The other ends connect to eight in-line pins.

The SIP can be installed to pull-up or pull-down. At each location there are 10 holes in a line. One end of the line is marked HI; the other end LO. The eight holes in the middle are connected to the eight lines of a port, A, B, or C.

To pull-up lines, orient the SIP with the common pin (dot) in toward the HI end; to pull-down, install the resistor with the common pin in the LO hole.

Carefully solder the SIP in place.

A resistor value of 10K is recommended. Use other values only if you have determined the necessity for doing so.

7.2 TTL TO SOLID STATE RELAYS

Many applications require digital monitoring of fairly high AC and DC input voltages. These AC and high DC voltages cannot be read directly by the CIO-DI##.

Solid State Relays, such as those available from Measurement Computing Corporation allow control and monitoring of AC and high DC voltages and provide 400V isolation. Solid State Relays (SSRs) are the recommended method of interfacing to AC and high DC signals.

The most convenient way to use solid state relays and a CIO-DI## board is to purchase a Solid State Relay Rack. SSR Racks are available from Measurement Computing Corporation.

7.3 VOLTAGE DIVIDERS

If you wish to measure a signal which varies over a range greater than the input range of a digital input, a voltage divider can drop the voltage of the input signal to the level the digital input can measure.

A voltage divider takes advantage of Ohm's law, which states,

> Voltage = Current * Resistance

and Kirkoff's voltage law which states,

> The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.

Implied in the above is that any variation in the voltage drop for the circuit as a whole will have a proportional variation in all the voltage drops in the circuit.

A voltage divider takes advantage of the fact that the voltage across one of the resistors in a circuit is proportional to the voltage across the total resistance in the circuit.

The trick to using a voltage divider is to choose two resistors with the proper proportions relative to the full scale of the digital input and the maximum signal voltage.

The process of dropping the voltage proportionally is often called attenuation. The formula for attenuation is:

$$\text{Attenuation} = \frac{R1 + R2}{R2}$$

The variable attenuation is the proportional difference between the signal voltage max and the full scale of the analog input.

$$2 = \frac{10K + 10K}{10K}$$

For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the attenuation is 2:1 or just 2.

$$R1 = (A-1) * R2$$

For a given attenuation, pick a handy resistor and call it R2, the use this formula to calculate R1.

For example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to the CIO-DI## digital inputs. The voltage must be dropped to 5 volts maximum when on. The Attenuation is 24:5 or 4.8. Use the equation above to find an appropriate R1 if R2 is 10K. Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

> **IMPORTANT NOTE**: The resistors, R1 and R2, are going to dissipate all the power in the divider circuit according to the equation Current = Voltage/Resistance and power is current-squared times resistance ($P_{watts} = I^2 \times R$). The higher the value of the resistance (R1 + R2) the less power dissipated by the divider circuit. Here is a simple rule:
>
> For Attenuation of 5:1 or less, no resistor should be less than 10K.
>
> For Attenuation of greater than 5:1, no resistor should be less than 1K.

7.4 LOW-PASS FILTERS DE-BOUNCE INPUTS

A low-pass filter can be placed on the signal wires between a signal and an A/D board. It attenuates frequencies higher than the cut-off frequency, preventing them from entering the A/D board's digital inputs.

The key parameter in a low-pass filter circuit is the cut-off frequency. The cut-off frequency is that frequency above which no variation of voltage can enter the circuit. For example, if a low pass filter had a cut off frequency of 30 Hz, the kind of

interference associated with line voltage (60 Hz) would be filtered out but a signal of 25 Hz would be allowed to pass.

In digital input circuits, low-pass filters are sometimes used to “de-bounce” inputs from relay or switch contacts.

A simple low-pass filter may be constructed from one resistor (R) and one capacitor (C). The cut-off frequency is determined by the formula:

$$Fc = \frac{1}{2 * \pi * R * C}$$

$$R = \frac{1}{2 * \pi * C * Fc}$$

Where $\pi = 3.14...$
Fc = frequency in cycles per second
R = resistance in Ohms
C = capacitance in Farads

EC Declaration of Conformity

We, Measurement Computing Corporation, declare under sole responsibility that the product:

Part Number	Description
CIO-DI48	48 channel digital input board
CIO-DI96	96 channel digital input board
CIO-D1192	192 channel digital input board

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

Measurement Computing Corporation
10 Commerce Way
Suite 1008
Norton, Massachusetts 02766
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@mccdaq.com
www.mccdaq.com