CIO-DAS6402/12
&
CIO-DAS6402/16

Analog and Digital I/O Boards

MEASUREMENT COMPUTING™

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1 INTRODUCTION

The CIO-DAS6402/16 and CIO-DAS6402/12 provide 32 differential or 64 single-ended inputs. They have sample rates as high as 330 kHz (100 kHz for the 16-bit version). Using a 100-pin connector, the CIO-DAS6402 board provides large channel counts without the need for external expansion boards.

The installation and operation of all CIO-DAS6402 series boards is very similar. Throughout this manual we use CIO-DAS6402 as a generic designation for the CIO-DAS6402/12 and CIO-DAS6402/16. When required, due to the differences in the boards, the specific board name is used.

The board's analog input ranges are entirely software-selectable in bipolar ranges from ±10 to ±1.25 Volts and unipolar ranges from 0 to 10V to 0 to 1.25V. The A/D converter can be triggered externally, or internally based on edge or level trigger sources. The board supports standard (post) and pre-trigger operation and so is capable of continuous, scheduled or event-triggered data acquisition.

High speed data acquisition without the chance of a lost sample is assured by the boards' use of the REP INSW data transfers and the on-board 1-Kilosample FIFO memory. In addition to the analog input section, each board also provides two channels of analog output, eight bits of digital input, eight bits of digital output, and a number of counter/timer functions.

All CIO-DAS6402 functions are fully supported by the Universal Library™ software package. This software provides upper level programming support for all DOS and Windows based operating systems. The CIO-DAS6402 is also shipped with InstaCal™, a powerful and easy-to-use installation, test, and calibration software package.

We recommend that you install InstaCal™ before installing the board in your computer. The InstaCal™ operations will show you how to set the switches and jumpers on the board.

2 SOFTWARE INSTALLATION

The CIO-DAS6402 has a variety of switches and jumpers to set before installing the board in your computer. By far the simplest way to configure your board is to use the *Insta*Cal™ program provided as part of your CIO-DAS6402 software package. *Insta*Cal™ will show you all available options, how to configure the various switches and jumpers to match your application requirements, and will create a configuration file that your application software (and the Universal Library) will refer to so the software you use will automatically know the exact configuration of the board.

Please refer to the *Software Installation Manual* regarding the installation and operation of *Insta*Cal™. The following hard copy information is provided as a matter of completeness, and will allow you to set the hardware configuration of the CIO-DAS6402 board if you do not have immediate access to *Insta*Cal™ and/or your computer. The locations of each of the switches and jumpers are shown in the figures below.

3.1   BASE ADDRESS

Unless there is already a board in your system using address 300h (768 Decimal), leave the switches as they are set at the factory. In Figure 3-1, the CIO-DAS6402 is set at base address 300h. See Figures 3-6 and 3-7 for the locations of the switches
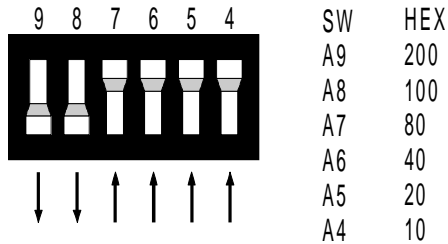
BASE ADDRESS SWITCH - Address 300H shown here.

Figure 3-1. Base Address Switches

3.2   D/A OUTPUT RANGE SWITCH (CIO-DAS6402/16 ONLY)

The analog output ranges of the CIO-DAS6402/12 are set via software. The analog output ranges of the CIO-DAS6402/16 are set by dip switches on the board (Figure 3-7). Figure 3-2 shows the the allowable switch settings and Table 3-1 gives the range/switch settings.
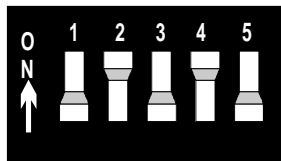
**CIO-DAS6402/16 Analog Output
Configuration Switch
(shown as +/- 10 Volt full-scale)**

Figure 3-4. D/A Output Range Switches

Table 3-1. D/A Analog Range Switch Settings

Range	*SW 1*	*SW 2*	*SW 3*	*SW 4*	*SW 5*
±10.0 V	DN	UP	DN	UP	DN
±5.0 V	DN	UP	DN	DN	UP
±2.5 V	DN	UP	DN	DN	DN
0 to 10 V	UP	DN	UP	UP	DN
0 to 5.0 V	UP	DN	UP	DN	UP
0 to 2.5 V	UP	DN	UP	DN	DN

3.3   D/A UPDATE MODE (CIO-DAS6402/16 ONLY)

The analog outputs can be configured to update independently or simultaneously. The update mode is set by a jumper on the CIO-DAS6402/16. This jumper is shown in Figure 3-5.

Place the jumper on the XFER side for simultaneous update. Place the jumper on the UPDATE side for independent operation.

UPDATE   XFER

CIO-DAS6402/16 D/A
UPDATE MODE SELECT
(SHOWN IN SIMULTANEOUS UPDATE MODE)
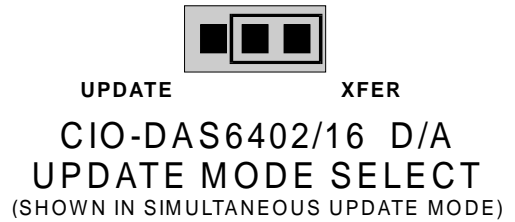
Figure 3-5. D/A Update Mode Select Jumper

Base Address Switch
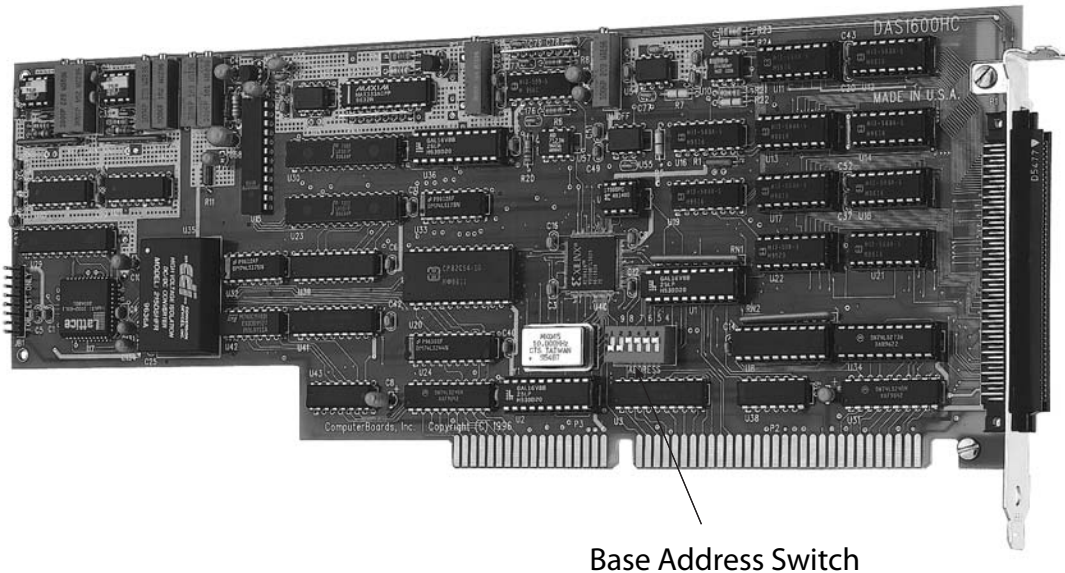
Figure 3-6. CIO-DAS6402/12 Base Address Switches Location

3

D/A Range and Mode Selection Switches

Update Mode Select Jumper

Base Address Switch
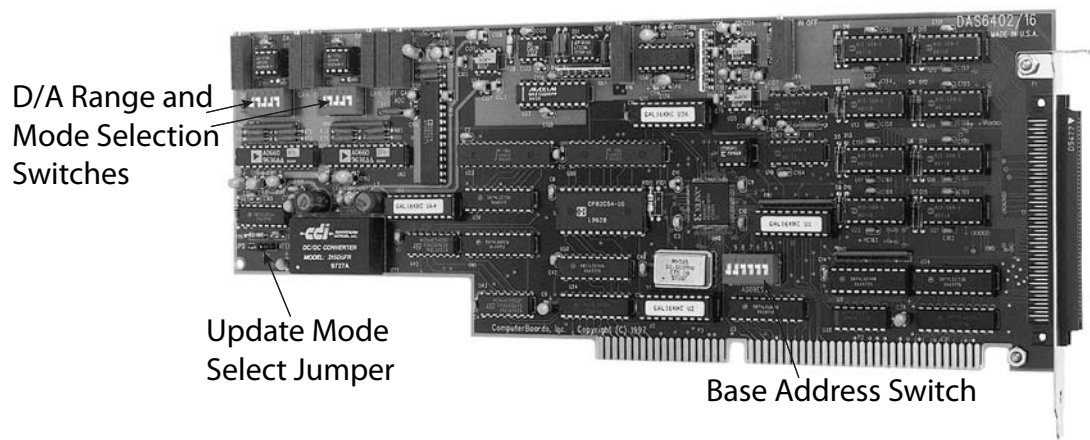
Figure 3-7. CIO-DAS6402/16 Base Address, D/A Range & Mode Switches Location

3.4   CONNECTOR PIN-OUT

The CIO-DAS6402 analog connector (Figure 3-8) is a 100 pin high-density connector accessible from the rear of the PC through the expansion back plate.

The connector interfaces with the C100FF-2, a two-foot cable. This cable connects directly to the CIO-TERM100 screw terminal board.

```
        LLGND    1   ● ●    51  LLGND
          IN0+   2   ● ●    52  IN16+
     IN0-/IN32+  3   ● ●    53  IN16-/IN48+
          IN1+   4   ● ●    54  IN17+
     IN1-/IN33+  5   ● ●    55  IN17-/IN49+
          IN2+   6   ● ●    56  IN18+
     IN2-/IN34+  7   ● ●    57  IN18-/IN50+
          IN3+   8   ● ●    58  IN19+
     IN3-/IN35+  9   ● ●    59  IN19-/IN51+
          IN4+  10   ● ●    60  IN20+
     IN4-/IN36+ 11   ● ●    61  IN20-/IN52+
          IN5+  12   ● ●    62  IN21+
     IN5-/IN37+ 13   ● ●    63  IN21-/IN53+
          IN6+  14   ● ●    64  IN22+
     IN6-/IN38+ 15   ● ●    65  IN22-/IN54+
          IN7+  16   ● ●    66  IN23+
     IN7-/IN39+ 17   ● ●    67  IN23-/IN55+
        LLGND   18   ● ●    68  LLGND
          IN8+  19   ● ●    69  IN24+
     IN8-/IN40+ 20   ● ●    70  IN24-/IN56+
          IN9+  21   ● ●    71  IN25+
     IN9-/IN41+ 22   ● ●    72  IN25-/IN57+
         IN10+  23   ● ●    73  IN26+
    IN10-/IN42+ 24   ● ●    74  IN26-/IN58+
         IN11+  25   ● ●    75  IN27+
    IN11-/IN43+ 26   ● ●    76  IN27-/IN59+
         IN12+  27   ● ●    77  IN28+
    IN12-/IN44+ 28   ● ●    78  IN28-/IN60+
         IN13+  29   ● ●    79  IN29+
    IN13-/IN45+ 30   ● ●    80  IN29-/IN61+
         IN14+  31   ● ●    81  IN30+
    IN14-/IN46+ 32   ● ●    82  IN30-/IN62+
         IN15+  33   ● ●    83  IN31+
    IN15-/IN47+ 34   ● ●    84  IN31-/IN63+
GROUND FOR DAC0 35   ● ●    85  DOUT0
    DAC0 OUTPUT 36   ● ●    86  DOUT1
GROUND FOR DAC1 37   ● ●    87  DOUT2
    DAC1 OUTPUT 38   ● ●    88  DOUT3
     CTR0 CLK IN 39  ● ●    89  CHASSIS GND
  DIN2/CTR0 GATE 40  ● ●    90  +12V SUPPLY OUT
 COUNTER 0 OUTPUT 41 ● ●    91  CHASSIS GND
  DIN0/AD PACER IN 42 ● ●   92  -12V SUPPLY OUT
DIN1/AD GATE/AD TRIG 43 ● ● 93  DIN6
          DIN 3  44  ● ●    94  DIN7
          DIN 4  45  ● ●    95  DOUT4
          DIN 5  46  ● ●    96  DOUT5
      -5V REF OUT 47  ● ●   97  DOUT6
   +5V SUPPLY OUT 48  ● ●   98  DOUT7
         SSH OUT  49  ● ●   99  EXTERNAL INTERRUPT IN
      CHASSIS GND 50  ● ●  100  CHASSIS GND
```

CIO-DAS6402 ANALOG SIGNAL CONNECTOR - View from rear of the computer.

Figure 3-8. 100-Pin I/O Connector

4.1 ANALOG INPUTS

The following section provides explanations and helpful hints regarding analog input connections. This section is designed to help you achieve the optimum performance from your CIO-DAS6402 series board.

Prior to jumping into actual connection schemes, you should have at least a basic understanding of Single-Ended/Differential inputs and system grounding/isolation. If you are already comfortable with these concepts you may wish to skip to the next section (on wiring configurations).
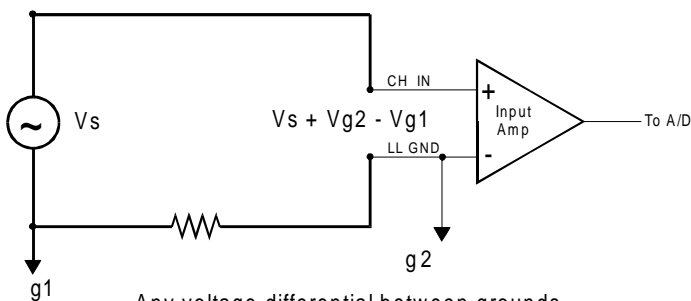
4.1.1 SINGLE-ENDED AND DIFFERENTIAL INPUTS
The CIO-DAS6402 provides either 32 differential or 64 single-ended input channels.

4.1.2 SINGLE-ENDED INPUTS
A single-ended input measures the voltage between the input signal and ground. In this case, in single-ended mode the CIO-DAS6402 measures the voltage between the input channel and LLGND. The single-ended input configuration requires only one physical connection (wire) per channel and allows the CIO-DAS6402 to monitor more channels than the (2-wire) differential configuration using the same connector and onboard multiplexor. However, since the CIO-DAS6402 is measuring the input voltage relative to its own low level ground, single-ended inputs are more susceptible to both EMI (Electro Magnetic Interference) and any ground noise at the signal source. Figure 4-1 shows the theory of single-ended input configuration
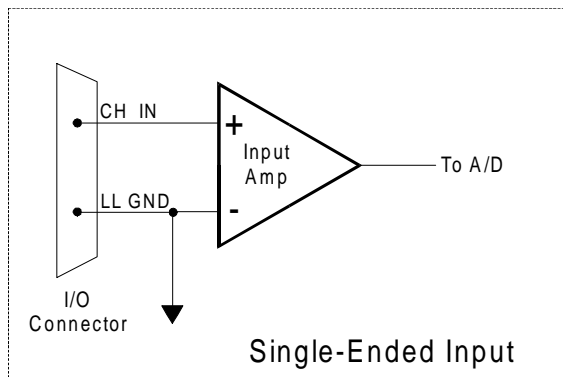
Figure 4-1. Single-Ended Voltage Input Theory

Differential Inputs

Differential inputs measure the voltage between two distinct input signals. Within a certain range (referred to as the common mode range), the measurement is almost independent of signal source to CIO-DAS6402 ground variations. A differential input is also much more immune to EMI than a single-ended one. Most EMI noise induced in one lead is also induced in the other, the input only measures the difference between the two leads, and the EMI common to both is ignored. This effect is a major reason there is twisted pair wire as the twisting assures that both wires are subject to virtually identical external influence. Figure 4-2 below shows a typical differential input configuration.
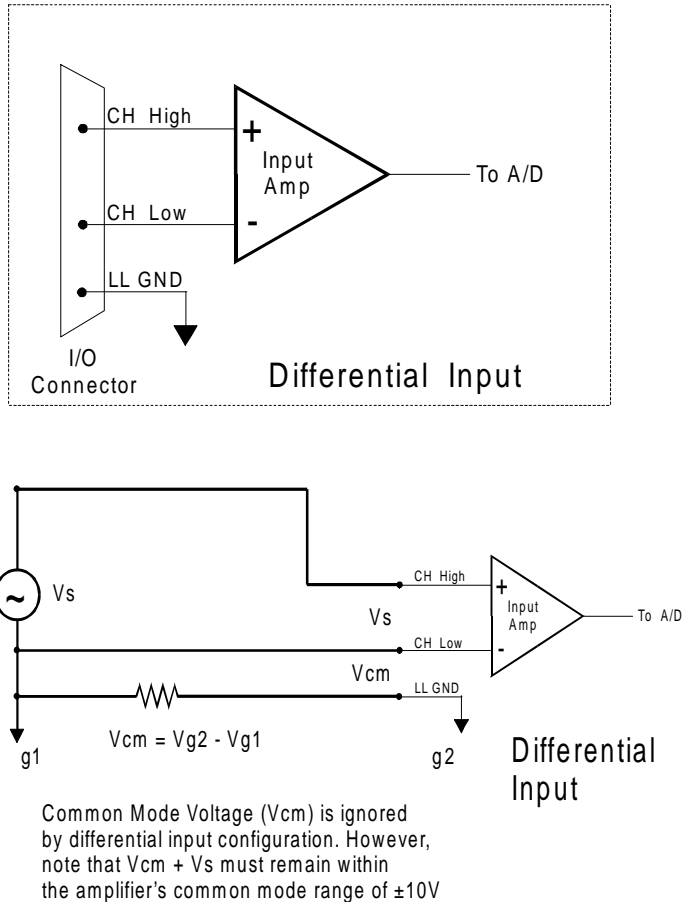
Figure 4-2. Differential input Theory

Before moving on to the discussion of grounding and isolation, it is important to explain the concepts of common mode, and common mode range (CM Range). Common mode voltage is depicted in the diagram above as Vcm. Though differential inputs measure the voltage between two signals, without (almost) respect to the either signal's voltages relative to ground, there is a limit to how far away from ground either signal can go. Though the CIO-DAS6402 has differential inputs, it will not measure the difference between 100V and 101V as 1 Volt (in fact the 100V would destroy the board!). This limitation or common mode range is depicted graphically in Figure 4-3. The CIO-DAS6402 common mode range is +/- 10 Volts. Even in differential mode, no input signal can be measured if it is more than 10V from the board's low level ground (LLGND).
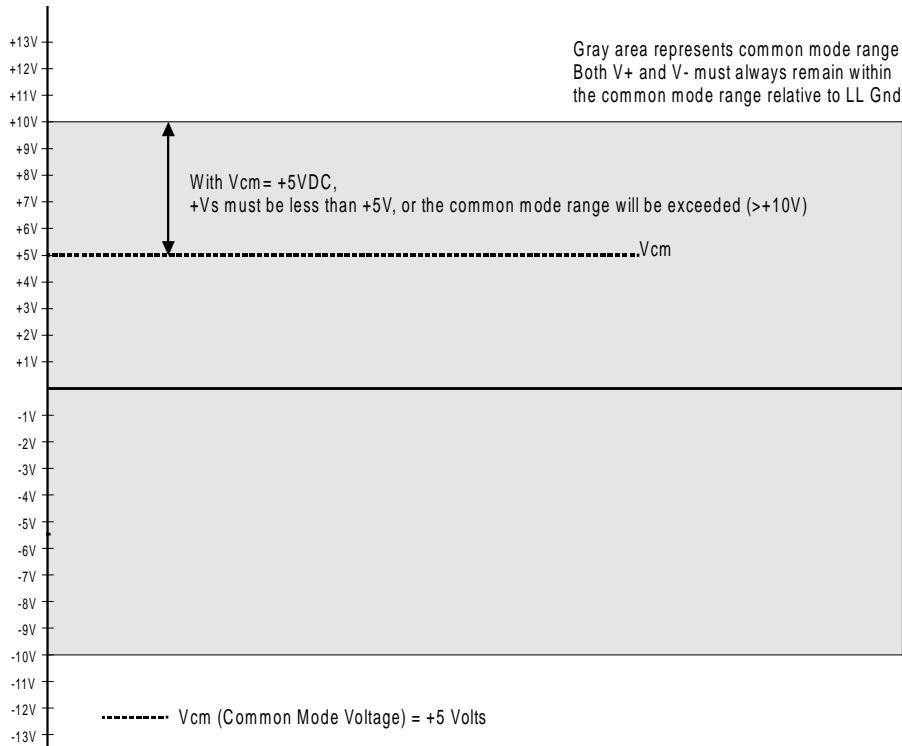
Figure 4-3. Common Mode Range

4.1.3 SYSTEM GROUNDS AND ISOLATION

There are three scenarios possible when connecting your signal source to your CIO-DAS6402 board.

1. The CIO-DAS6402 and the signal source may have the same (or **common**) ground. This signal source may be connected directly to the CIO-DAS6402.

2. The CIO-DAS6402 and the signal source may have an offset voltage between their grounds (AC and/or DC). This offset it commonly referred to a **common mode voltage**. Depending on the magnitude of this voltage, it may or may not be possible to connect the CIO-DAS6402 directly to your signal source. We will discuss this topic further in a later section.

3. The CIO-DAS6402 and the signal source may already have **isolated grounds**. This signal source may be connected directly to the CIO-DAS6402.

Which system do you have?

Try the following test: Using a battery powered voltmeter*, measure the voltage between the ground signal at your signal source and at your PC. Place one voltmeter probe on the PC ground and the other on the signal source ground. Measure both the AC and DC Voltages.

If you do not have access to a voltmeter, skip the experiment and read the following three sections. You may be able to identify your system type from the descriptions provided.

If both AC and DC readings are 0.00 volts, you may have a system with common grounds. However, since voltmeters will average out high frequency signals, there is no guarantee. Please refer to the section below titled ***Common Grounds***.

If you measure reasonably stable AC and DC voltages, your system has an offset voltage between the grounds category. This offset is referred to as a Common Mode Voltage. Please be careful to read the following warning and then proceed to the section describing ***Common Mode*** systems.

If either the AC or DC voltage is greater than 10 volts, do not connect the CIO-DAS6402 to this signal source. You are beyond the boards usable common mode range and will need to either adjust your grounding system or add special Isolation signal conditioning to take useful measurements. A ground offset voltage of more than 30 volts will likely damage the CIO-DAS6402 board and possibly your computer. Note that an offset voltage much greater than 30 volts will not only damage your electronics, but it may also be hazardous to your health.

This is such an important point, that we will state it again. If the voltage between the ground of your signal source and your PC is greater than 10 volts, your board will not take useful measurements. If this voltage is greater than 30 volts, it will likely cause damage, and may represent a serious shock hazard! In this case you will need to either reconfigure your system to reduce the ground differentials, or purchase and install special electrical isolation signal conditioning.

If you cannot obtain a stable DC voltage measurement between the grounds, or the voltage drifts around considerably, the two grounds are most likely isolated. The easiest way to check for isolation is to change your voltmeter to it's ohm scale and measure the resistance between the two grounds. It is recommended that you turn both systems off prior to taking this resistance measurement. If the measured resistance is more than 100 Kohm, it's a fairly safe bet that your system has electrically *isolated grounds*.

Systems with Common Grounds

In the simplest (but perhaps least likely) case, your signal source will have the same ground as the CIO-DAS6402. This would typically occur when providing power or excitation to your signal source directly from the CIO-DAS6402. There may be other common ground configurations, but it is important to note that any voltage between the CIO-DAS6402 ground and your signal ground is a potential error voltage if you set up your system based on a common ground assumption.

As a safe rule of thumb, if your signal source or sensor is not connected directly to an LLGND pin on your CIO-DAS6402, it's best to assume that you do not have a common ground even if your voltmeter measured 0.0 Volts. Configure your system as if there is ground offset voltage between the source and the CIO-DAS6402. This is especially true if you are using either the CIO-DAS6402/16 or the CIO-DAS6402/12 at high gains, since ground potentials in the sub millivolt range will be large enough to cause A/D errors, yet will not likely be measured by your handheld voltmeter.

Systems with Common Mode (ground offset) Voltages

The most frequently encountered grounding scenario involves grounds that are somehow connected, but have AC and/or DC offset voltages between the CIO-DAS6402 and signal source grounds. This offset voltage may be AC, DC or both and may be caused by EMI pickup, resistive voltage drops in ground wiring and connections, etc. Ground offset voltage is a more appropriate term to describe this type of system, but since our goal is to keep things simple, and help you make appropriate connections, we'll stick with our somewhat loose usage of the phrase Common Mode.

Small Common Mode Voltages

If the voltage between the signal source ground and CIO-DAS6402 ground is small, the combination of the ground voltage and input signal will not exceed the CIO-DAS6402's +/-10V common mode range, *(i.e. the voltage between grounds, added to the maximum input voltage, stays within +/-10V)*, This input is compatible with the CIO-DAS6402 and the system may be connected without additional signal conditioning. Fortunately, most systems will fall in this category and have a small voltage differential between grounds.

Large Common Mode Voltages

If the ground differential is large enough, the CIO-DAS6402's +/- 10V common mode range will be exceeded (i.e. the voltage between CIO-DAS6402 and signal source grounds, added to the maximum input voltage you're trying to measure exceeds +/-10V). In this case the CIO-DAS6402 cannot be directly connected to the signal source. You will need to change your system grounding configuration or add isolation signal conditioning. (Please look at our ISO-RACK and ISO-5B-series products to add electrical isolation, or give our technical support group a call to discuss other options.)

Do not rely on the earth prong of a 120VAC receptacle for signal ground connections. Different ground plugs may have large and potentially even dangerous voltage differentials. Remember that the ground pins on 120VAC outlets on different sides of the room may only be connected in the basement. This leaves the possibility that the "ground" pins may have a significant voltage differential (especially if the two 120VAC outlets happen to be on different phases.)

CIO-DAS6402 and signal source already have isolated grounds
Some signal sources will already be electrically isolated from the CIO-DAS6402. The diagram below shows a typical isolated ground system. These signal sources are often battery powered, or are fairly expensive pieces of equipment (since isolation is not an inexpensive proposition), isolated ground systems provide excellent performance, but require some extra effort during connections to assure optimum performance is obtained. Please refer to the following sections for further details.

4.2   WIRING CONFIGURATIONS

Combining all the grounding and input type possibilities provides us with the following potential connection configurations. The combinations along with our recommendations on usage are shown in Table 4-1 below.

Table 4-1. Input vs. Grounding Recommendations

Ground Category	Input Configuration	Our view
Common Ground	Single-Ended Inputs	Recommended
Common Ground	Differential Inputs	Acceptable
Common Mode Voltage < +/-10V	Single-Ended Inputs	Not Recommended
Common Mode Voltage < +/-10V	Differential Inputs	Recommended
Common Mode Voltage > +/- 10V	Single-Ended Inputs	Unacceptable without adding Isolation
Common Mode Voltage > +/-10V	Differential Inputs	Unacceptable without adding Isolation
Already Isolated Grounds	Single-ended Inputs	Acceptable
Already Isolated Grounds	Differential Inputs	Recommended

The following sections depicts recommended input wiring schemes for each of the eight possible input configuration/grounding combinations.

4.2.1   COMMON GROUND / SINGLE-ENDED INPUTS

Single-ended is the recommended configuration for common ground connections. However, if some of your inputs are common ground and some are not, we recommend you use the differential mode. There is no performance penalty (other than loss of channels) for using a differential input to measure a common ground signal source. However the reverse is not true. Figure 4-4 below shows a recommended connection diagram for a common ground / single-ended input system
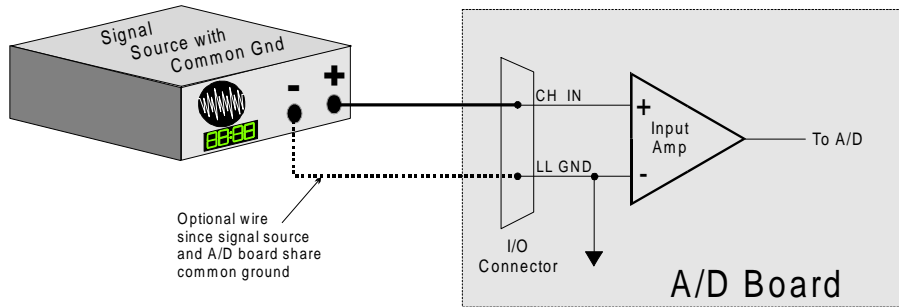
Signal source and A/D board
sharing common ground connected
to single-ended input.

Figure 4-4. Common Ground / Single-Ended Inputs

4.2.2   COMMON GROUND / DIFFERENTIAL INPUTS

The use of differential inputs to monitor a signal source with a common ground is a acceptable configuration though it requires more wiring and offers fewer channels than selecting a single-ended configuration. Figure 4-5 below shows the recommended connections in this configuration.
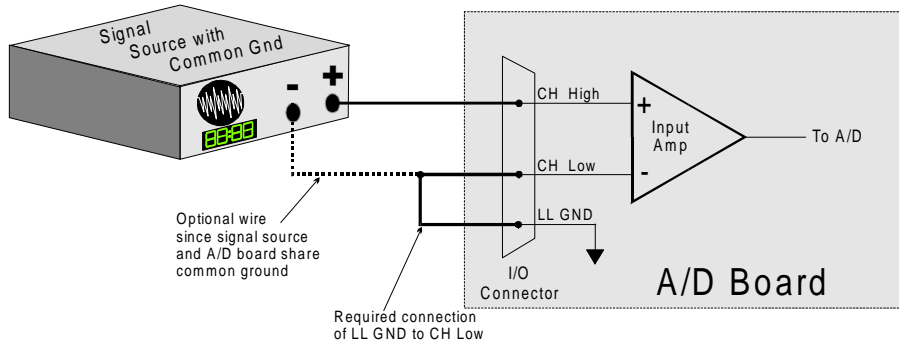
Signal source and A/D board
sharing common ground connected
to differential input.

Figure 4-5. Common Ground / Differential Inputs

4.2.3   COMMON MODE VOLTAGE < +/-10V / SINGLE-ENDED INPUTS

This is not a recommended configuration. In fact, the phrase common mode has no meaning in a single-ended system and this case would be better described as a system with offset grounds. Anyway, you are welcome to try this configuration, no system damage should occur and depending on the overall accuracy you require, you may receive acceptable results.

4.2.4   COMMON MODE VOLTAGE < +/-10V / DIFFERENTIAL INPUTS
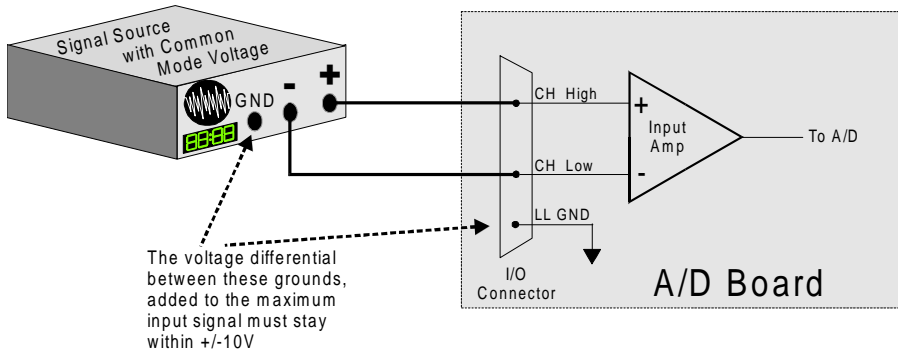
Signal source and A/D board
with common mode voltage
connected to a differential input.

Systems with varying ground potentials should always be monitored in the differential mode. Care is required to assure that the sum of the input signal and the ground differential (referred to as the common mode voltage) does not exceed the common mode range of the A/D board (+/-10V on the CIO-DAS6402). Figure 4-6 below show recommended connections in this configuration.

Figure 4-6. Common Mode Voltage < +/-10V / Differential Inputs

4.2.5 COMMON MODE VOLTAGE > +/-10V

The CIO-DAS6402 will not directly monitor signals with common mode voltages greater than +/-10V. You will either need to alter the system ground configuration to reduce the overall common mode voltage, or add isolated signal conditioning between the source and your board. See Figure 4-7 and 4-8 below.
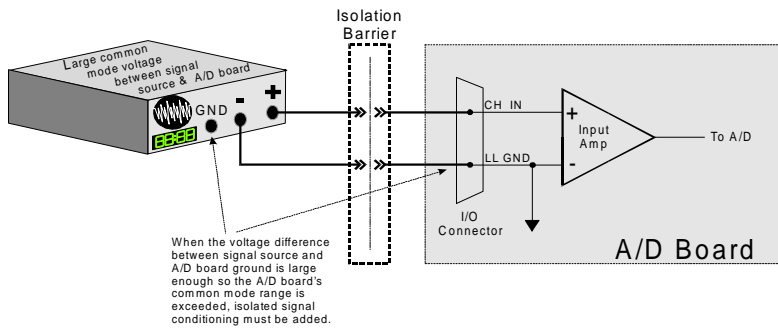
System with a Large Common Mode Voltage,
Connected to a Single-Ended Input

Figure 4-7. Common Mode Voltage > +/-10V. Single-Ended Input
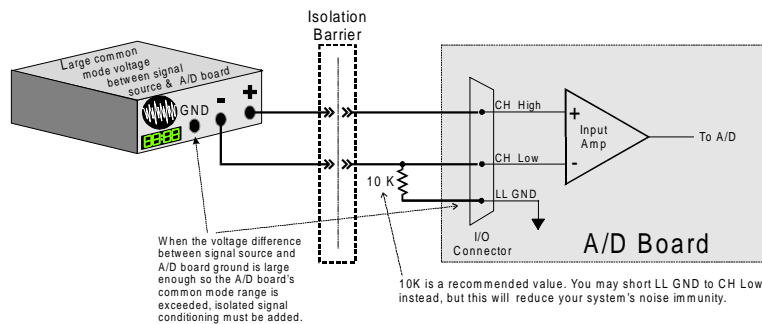
System with a Large Common Mode Voltage,
Connected to a Differential Input

Figure 4-8. Common Mode Voltage > +/-10V. Differential Input

4.2.6 ISOLATED GROUNDS / SINGLE-ENDED INPUTS

Single-ended inputs can be used to monitor isolated inputs, though the use of the differential mode will increase you system's noise immunity. Figure 4-9 below shows the recommended connections is this configuration.
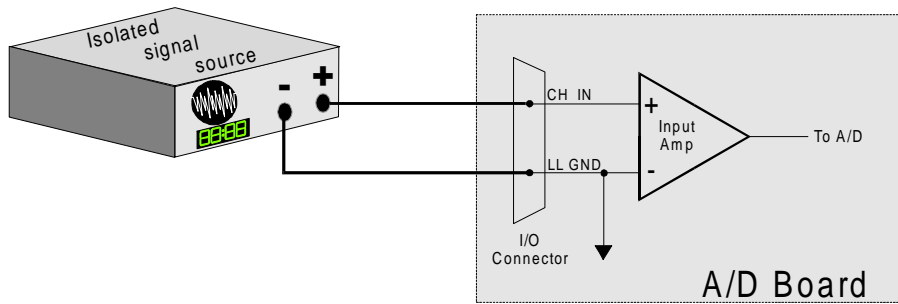
Isolated Signal Source
Connected to a Single-Ended Input

Figure 4-9. Isolated Grounds / Single-Ended Input

4.2.7   ISOLATED GROUNDS / DIFFERENTIAL INPUTS

Optimum performance with isolated signal sources is assured with the use of the differential input setting. Figure 4-10 below shows the recommend connections is this configuration.

These grounds are electrically isolated.

10K is a recommended value. You may short LL GND to CH Low instead, but this will reduce your system's noise immunity.
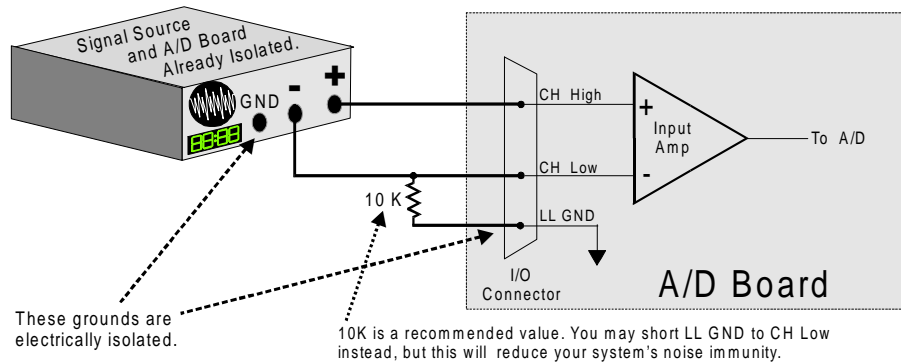
Already isolated signal source
and A/D board connected to
a differential input.

Figure 4-10. Isolated Grounds / Differential Inputs

4.3   ANALOG OUTPUTS

Analog outputs are simple voltage outputs which can be connected to any device which will record, display or be controlled by a voltage. The CIO-DAS6402 analog outputs are 4 quadrant multiplying DACs. This means that they accept an input voltage reference and provide an output voltage which is inverse to the reference voltage and proportional to the digital value in the output register.

For example, the supplied reference of −5V provides a +5V output when the value in the output register is 4095 (full scale at 12-bits of resolution). It provides a value of 2.5V when the value in the output register is 2048.

The output ranges of the CIO-DAS6402/12 are set by software. The output ranges of the CIO-DAS6402/16 are set by dip switch. Please refer to Section 3 for information regarding setting these switches.

5.1   INTRODUCTION

The CIO-DAS6402 is controlled and monitored by reading and writing to 16 I/O addresses. The first address is referred to as the BASE ADDRESS and is set by a bank of switches on the board. All other addresses are located at the BASE ADDRESS plus a specified offset.

Registers are easy to read from and write to, though to create a complete data acquisition software program at the register level is a significant undertaking. Unless there is a specific reason that you need to write your program at the register lever, we recommend using our Universal Library.

In summary form, the registers and their function are listed on the following table. Within each register are eight bits which may constitute a byte of data or be eight individual bit set/read functions.

Table 5-1. DAS6402 I/O Map - COMPATIBLE Mode
(BOLD indicates register definition for DAS6402/16)

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE	A/D bits 0(LSB) - 3 & Channel #	Software Start A/D Conversion
BASE + 1	A/D Bits 4 -11 (MSB)	None
BASE	**A/D bits 0 (LSB) - 7**	**Software Start A/D Conversion**
BASE + 1	**A/D Bits 8 - 15 (MSB)**	**None**
BASE + 2	8/16 Channel Mux	8/16 Channel Mux / Reset FIFO
BASE + 3	Digital Input bits 0-3 / External control	Digital Output Bits 0-3
BASE + 4	None	D/A 0 Bits 0-3
BASE + 5	None	D/A 0 Bits 4-11
BASE + 6	None	D/A 1 Bits 0-3
BASE + 7	None	D/A 1 Bits 4-11
BASE + 8	EOC, UNI/BIP, SEDIFF, Mux	Reset interrupt flip-flop
BASE + 9	DMA Enable, Interrupt, Pacer Source	DMA Enable, Interrupt, Pacer Source
BASE +10	DAC range, TRIG0/CTR0	DAC range, TRIG0/CTR0
BASE +11	DMA, U/B, SEDIFF, MODE, A/D Gain	MODE, A/D Gain Control
BASE +12	Counter 0 Data	Counter 0 Data
BASE +13	CTR 1 Data - A/D Pacer Clock	CTR 1 Data - A/D Pacer Clock
BASE +14	CTR 2 Data - A/D Pacer Clock	CTR 2 Data - A/D Pacer Clock
BASE +15	None. No read back on 8254	8254 Counter Control Register

Table 5-2. DAS6402 I/O Map - ENHANCED Mode
(BOLD indicates register definition for DAS6402/16)

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE	A/D bits 0(LSB) -11 (MSB) (Word)	Software Start A/D Conversion
BASE	**A/D bits 0(LSB) -15 (MSB) (Word)**	**Software Start A/D Conversion**
BASE + 1	*Do not use, use BASE only*	None
BASE + 2	Post-Trigger Index Counter	32/64 Channel Mux (Word) /Reset FIFO
BASE + 3	Digital Input bits 0-7 / External control	Digital Output Bits 0-7
BASE + 4	None	D/A 0 Bits 0-3
BASE + 5	None	D/A 0 Bits 4-11
BASE + 6	None	D/A 1 Bits 0-3
BASE + 7	None	D/A 1 Bits 4-11
BASE + 8	FIFO, Interrupt Status, Clock rate	Extend modes and clear interrupts
BASE + 9	Burst Enable, Interrupt, Pacer Source	Burst Enable, Interrupt, Pacer Source
BASE +10	DAC range, Pacer clock control	DAC range, Pacer clock control
BASE +11	UB,SEDIFF,MODE,Int source, ADGain	UB,SEDIFF,MODE,Int source, ADGain
BASE +12	CTR 0 Data: (Residual/ End of acq)	CTR 0 Data: Preload for residual count
BASE +13	CTR 1 Data - A/D Pacer Clock	CTR 1 Data - A/D Pacer Clock
BASE +14	CTR 2 Data - A/D Pacer Clock	CTR 2 Data - A/D Pacer Clock
BASE +15	None. No read back on 8254	8254 Counter Control Register

5.2   A/D DATA WORD REGISTERS

In Enhanced Mode, two of the data registers are configured for 'Word' reads or writes, as opposed to performing the I/O operation as separate byte reads or writes. These two registers are the A/D Data Register at the BASE+0, and the Channel Mux Hi/Lo Register at BASE+2. Any IO accesses (reads or writes) to either of these registers is interpreted by the board as Word IO.

A/D DATA WORD REGISTER - 12 BIT

BASE + 0   Example, 300h, 768 Decimal
READ/WRITE

Mode	15	14	13	12	11	10	9	8	7	6	5	4	2	3	1	0
ENHANCED	AD11 MSB	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0 LSB	0	0	0	0
COMPATIBLE	AD11 MSB	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0 LSB	MA3	MA2	MA1	MA0

A read/write register. The A/D Data Register is configured as a word because REP INSW can be used to quickly read data from the board, allowing for higher A/D conversion rates than would be possible if using DMA, which accesses the A/D data as two bytes.

READ
On read, the 12-bit ADC value is presented in 'left-justified' format, with the most-significant ADC bit occupying the data word bit position #15; the least-significant ADC bit occupies bit position #4 of the data word.

WRITE
 A write to the base address will cause an A/D conversion, (Bits 0&1 of BASE+9 must be 0.)

ENHANCED MODE: The channel tag is not available in enhanced mode, thus the lowest four bits of the data word will be read back as zero.

COMPATIBLE MODE: The channel tag is available in compatible mode, occupying the lowest four bits of the data word.

A/D DATA WORD REGISTER - 16 BIT

BASE + 0   Example, 300h, 768 Decimal
READ/WRITE

Mode	15	14	13	12	11	10	9	8	7	6	5	4	2	3	1	0
ENHANCED	AD15 MSB	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0 LSB
COMPATIBLE	AD15 MSB	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0 LSB

READ
On read, the 16-bit ADC value is presented in 'left-justified' format, with the most-significant ADC bit occupying the data word bit position #15; the least-significant ADC bit occupies bit position #0 of the data word.

WRITE
 A write to the base address will cause an A/D conversion, (Bits 0&1 of BASE+9 must be 0.)

Whether in ENHANCED or COMPATIBLE MODE, there is no channel tag.

5.3   CHANNEL MUX HI/LO LIMITS WORD REGISTER

BASE ADDRESS +2   Example, 302h, 770 Decimal
WRITE

Mode	15	14	13	12	11	10	9	8	7	6	5	4	2	3	1	0
ENHANCED	-	-	HI 5	HI 4	HI 3	HI 2	HI 1	HI 0	-	-	LO5	LO4	LO3	LO2	LO1	LO0
COMPATIBLE	-	-	-	-	-	-	-	-	8H	4H	2H	1H	8L	4L	2L	1L

WRITE
Writing to this register clears the FIFO.

ENHANCED MODE:
This register is configured as a Word to allow for additional bits, two for the low channel limit and two for the high channel limit, which are used to generate the 6-bit counter sequence. This register cannot be accessed as two separate byte writes, access must be done as an entire word. If a byte write to address 302 is attempted, then the HI0-HI5 data will be undefined. If a byte write to address 303 is attempted, the board will assume that the data is to be written to the DOUT register.
When this register is written, the analog input multiplexers are set to the channel specified in LO0-LO5. After each conversion, the input multiplexers increment to the next channel, reloading to the "LO" channel after the "HI" channel is reached.

READ
Used to return the pre-trigger index value as was done by an 8254 counter.

COMPATIBLE MODE:
READ/WRITE
The mux register operates as the DAS1600 series. The lower eight bits are separated in two nibbles; the upper four bits represent the upper channel and the lower four bits represent the lower channel. For example: to scan channels 2 through 5, write the value 52 to Base + 2. The upper eight bits in this register are written to but cannot be read, and do not affect the mux sequencing circuit.

5.4   8-BIT DIGITAL I/O REGISTERS

BASE ADDRESS +3   Example, 303h, 771 Decimal
READ

7	6	5	4	2	3	1	0
DI7	**DI6**	**DI5**	**DI4**	**DI3**	**DI2** **GATE0**	**DI1** **XTRIG**	**DI0** **XPACER**

The signals present at the 8 digital inputs are read as one byte. Three of the pins have special functions in addition to digital input.:

XPACER/DI0   External Pacer: Starts an A/D Conversion on each active edge.
XTRIG/DI1   External Trigger: Causes an entire acquisition to start or stop.
GATE0/DI2   Gate for CTR0   Used in Compatible mode only.

These special functions are optionally enabled in software, and are explained below. External Interrupt is enabled at BASE +9, External Pacer and External Trigger are enabled at BASE +10. Please see those register descriptions for details.

WRITE

7	6	5	4	2	3	1	0
DO7	**DO6**	**DO5**	**DO4**	**DO3**	**DO2**	**DO1**	**DO0**

All of the eight bits are latched TTL outputs.

5.5   DIGITAL TO ANALOG CONVERTER (ANALOG OUT) REGISTERS

D/A 0 REGISTERS

BASE ADDRESS +4   Example, 304h, 772 Decimal

6402/	7	6	5	4	3	2	1	0
12-BIT	**D/A3**	**D/A2**	**D/A1**	**D/A0**	**0**	**0**	**0**	**0**
16-BIT	**D/A7**	**D/A6**	**D/A5**	**D/A4**	**D/A3**	**D/A2**	**D/A1**	**D/A0**

BASE ADDRESS +5   Example, 305h, 773 Decimal

6402/	7	6	5	4	3	2	1	0
12-BIT	**D/A11**	**D/A10**	**D/A9**	**D/A8**	**D/A7**	**D/A6**	**D/A5**	**D/A4**
16-BIT	**D/A15**	**D/A14**	**D/A13**	**D/A12**	**D/A11**	**D/A10**	**D/A9**	**D/A8**

D/A 1 REGISTERS

BASE ADDRESS +6   Example, 306h, 774 Decimal

6402/	7	6	5	4	3	2	1	0
12-BIT	**D/A3**	**D/A2**	**D/A1**	**D/A0**	**0**	**0**	**0**	**0**
16-BIT	**D/A7**	**D/A6**	**D/A5**	**D/A4**	**D/A3**	**D/A2**	**D/A1**	**D/A0**

BASE ADDRESS +7   Example, 307h, 775 Decimal

6402/	7	6	5	4	3	2	1	0
12-BIT	**D/A11**	**D/A10**	**D/A9**	**D/A8**	**D/A7**	**D/A6**	**D/A5**	**D/A4**
16-BIT	**D/A15**	**D/A14**	**D/A13**	**D/A12**	**D/A11**	**D/A10**	**D/A9**	**D/A8**

WRITE ONLY

6402/12

Each 12 bit D/A output line has two 8-bit registers. The first contains the four least-significant bits of the data and four 'don't-care' bits. The second register contains the eight most significant bits of the data.

Data can be written as two successive bytes or as one word. When two bytes are written, the lower address byte must be written first, and then the higher byte, as the DAC output is updated when the higher byte is written.

When the data is written as a single word, the most significant bit of the DAC data is the most significant bit of the word. The CPU will automatically write the data to the board as two successive bytes, writing the low and then the high byte.

6402/16

Each 16-bit D/A output line has two 8-bit registers. The first contains the eight least significant bits of the data and the second register contains the eight most significant bits of the data. The data is written as two successive bytes - the lower first (or LSB's) followed by the higher byte (or MSB's).

The 6402/16 also has a jumper (HD1) to select either individual update (UPDATE) or simultaneous updating (XFER) of both DAC's. In UPDATE mode, when the higher address is written, that DAC is updated. In XFER mode, after both DAC's are loaded, a Read cycle to any of the DAC registers with update both DAC's simultaneously.

5.6   STATUS REGISTER

BASE ADDRESS + 8   Example, 308h, 776 Decimal

READ

Mode	7	6	5	4	3	2	1	0
ENHANCED	1/10MHz	INDGT	XTRIG	INT	XINT	FFULL	FHALF	FFNE
COMPATIBLE	EOC	UNIBIP	SEDIFF	INT	MA3	MA2	MA1	MA0

Description of Status Register read bits:

ENHANCED MODE:
1/10MHz - Internal Pacer clock source. = 1, Pacer clock is 10MHz, = 0, Pacer clock is 1MHz.

INDGT - Index Gate. Signals when the index counter has been shut off due to FIFO going Half Full. When = 0, index counter active or flip-flop has been reset (by CLRXTR). When = 1, index counter has been shut off.

XTRIG - State of external trigger flop, used when edge-triggering. When =1, the trigger has been activated. When = 0 idle or not active. Cleared by CLRXTR.

INT - State of interrupt flop, from 1 of 4 sources on the board. When = 1, the flip-flop indicates an interrupt condition. When = 0 no interrupt. Cleared by CLRINT. See BASE + 9 for interrupt enable and interrupt level and BASE + 11 for interrupt sources.

XINT - State of external interrupt flop, acts independently of on-board interrupt sources. When = 1, external interrupt occurred, When = 0 no external interrupt. Cleared by CLRXIN.

FFULL - latched status of FIFO Full condition.
         When = 1, FIFO <u>exceeded</u> full state, data may have been lost. When = 0, FIFO has not exceeded full state.

FHALF - indicates if FIFO is above or below half-full. Can be used as an interrupt source for REP INSW ADC.
            When = 1, FIFO is above half-full. When = 0, FIFO is at or below half-full. (not latched)

FFNE - Not empty state of FIFO. Can be used as interrupt for single conversion ADC mode.
            When = 1, FIFO is not empty (contains ADC data). When = 0, FIFO is empty (has no ADC data).

COMPATIBLE MODE:

EOC - End-of-conversion, When 1 = busy. When = 0, conversion complete.

UNIBIP - Analog input Unipolar/Bipolar status, When 1 = unipolar. When 0, = bipolar.

SEDIFF - Analog input channel configuration, 0 = differential, 1 = single ended.

MA3:0 - Analog input channel mux setting (for next conversion).

WRITE

7	6	5	4	3	2	1	0
1/10MHz	POSTMODE	ARMED	EXTEND	-	CLRXIN	CLRXTR	CLRINT

ENHANCED MODE:
The write functions of the status register are to clear certain flip-flop states, and set the Pacer clock to 1 or 10 MHz.

CLRINT - Clear Interrupt flip-flop when = 1. No action when = 0.

CLRXTR - Clear External Trigger flip-flop when = 1. No action when = 0

CLRXIN - Clear External Interrupt flip-flop when = 1. No action when = 0.

(These 'Clear' functions get automatically reset to 0 in 1 to 2 μsec).

EXTEND - Qualifier for bits 5 to 7 data. Must be set to 1 prior to setting the desired bits at 5 to 7.
=0, any data at bits 5 to 7 will be ignored and the state of the bit will not change.
The MODE bit must be = 1 (Enhanced) to change the EXTEND bit.

Example: to set the 1/10MHz bit to set the Pacer time base to 10MHz:

Do each step as separate write operations:
1. Set MODE bit to 1 (base + B, bit 4)
2. Set EXTEND to 1 (base + 8, bit 4)
3. Set 1/10 bit to 1 (base + 8, bit 7), be sure to leave bit 4 set as well, including bits 5/6 if desired to leave them set.
4. Set EXTEND bit to 0, leave the bits in 5 to 7 set as required.
After EXTEND bit is zeroed, any writes to bits 5 to 7 are masked off (doesn't change).

Please note that the clear flip-flop bits in 0 to 2 will be active if their corresponding data bits are high during any write to base+8 in Enhanced Mode.

ARMED - Used with various pre and post-trigger scenarios to gate a 'residual' counter on (CTR0 of the 8254).
Counter 0 operates in Mode 0 and counts conversions, stopping the acquisition process when it reaches terminal count.
When = 0, counting of post-trigger samples is disabled. When =1, counting of post-trigger samples is enabled.
See also **POSTMODE.**

POSTMODE - Used to select whether FifoHalf Full or ADC convert starts Counter 0. Used in conjunction with
PRETRIG to select a strobe to latch the Counter 0 gate. (See BASE + 10 for PRETRIG.) Refer to Table 6-3.
Total # of counts (N) less- than-or-equal-to FIFO 1/2-full is a special case:

Table 5-3. Post-Mode Operations

Gate CTR0:	Pretrig?	**POST-MODE**	Ctr 0 gate strobe:	ARMED bit is set by:
fifo>N>1/2fifo	no 0	0	on last fifo half full	Before acquisition is started
N>fifo	no 0	0	on last fifo half full	Next to last full 'packet'
N <= 1/2 fifo	no 0	1	1st conversion	Before acquisition is started
N> 1/2 fifo	yes 1	0	on fifo half (last interrupt)	ISR on last full 'packet'
N < =1/2 fifo	yes 1	1	on the external trigger	Before acquisition is started

1/10MHz - Sets Pacer clock frequency. .
When bit 7 = 1, Forces Pacer clock to 10 MHz. When = 0, forces Pacer clock to 1 MHz.

COMPATIBLE MODE:

Write to Base + 8 only clears the interrupt flip-flop (sets CLRINT only (= 1)).

5.7   INTERRUPT AND PACER CONTROL REGISTER

BASE ADDRESS +9   Example, 309h, 777 Decimal

READ/WRITE

	7	6	5	4	3	2	1	0
ENH	**INTE**	**HC_IS2**	**HC_IS1**	**HC_IS0**	**XINTE**	**BURSTE**	**HC_PS1**	**HC_PS0**
COM	INTE	HC_IS2	HC_IS1	HC_IS0	XINTE	DMAEN	HC_PS1	HC_PS0

INTE   =1, Analog Interrupts are enabled, =0, interrupts are disabled.
The system interrupt level is determined by the three HC_IS0-2 bits. The interrupt source (Single AD, FIFO Half-Full, End of Burst) is selected by the two Analog Interrupt Source bits HC_AI0 & HC_AI1 (Base + 11). Use of external interrupt (XINTE) also requires that INTE = 1.

HC_IS2, HC_IS1, HC_IS0 will map an enabled interrupt onto a specific ISA bus interrupt level. See Table 6-4 below:

Table 5-4. Interrupt Levels - Enhanced & Compatible

HC_IS2	HC_IS1	HC_IS0	Interrupt Level- Enhanced	Compatible (ref)
0	0	0	none	none
0	0	1	11	none
0	1	0	2	2
0	1	1	3	3
1	0	0	10	none - see Note
1	0	1	5	5
1	1	0	15	6
1	1	1	7	7

Note: Some Interrupt levels in Enhanced Mode are different from Interrupt levels in Compatible Mode. IRQ4 was dropped from the Compatible-mode IRQ's to allow a single GAL to decode all IRQ's, and since COM1 uses IRQ4, the DAS1600 will probably never use it.

XINTE: =1, External Interrupt enabled. =0, External Interrupt disabled. The external interrupt is a direct digital path from the 100-pin connector to the system interrupt. External Interrupt shares the Interrupt Level with the Analog Interrupt path. (Only enabled in Enhanced mode).
BURSTE   When = 1, Burst Mode is enabled. When = 0, Burst Mode is disabled. The number of channels in the burst is determined by the Mux Hi/Lo register.
(BURST Mode also enabled by write to BASE + 406hex bit 6 as on DAS1600 series).

HC_PS1, HC_PS0:   Controls the source of the A/D conversion Pacer according Table 6-5 below:

Table 5-5. Control Source of A/D Conversion Pacer

HC_PS1	HC_PS0	Pacer Source
0	0	Software Convert
0	1	External Pacer Falling Edge
1	0	External Pacer Rising Edge
1	1	Internal Pacer (8254)

5.8   TRIGGER CONTROL/ DAC RANGE SELECT REGISTER

Triggering and Gating are digital means to control pacing. Triggering means that an active edge on the DI1 pin will start the A/D Pacer. When the active edge occurs, the state of the pin is Don't Care. Gating means that a digital level on the DI1 pin will start or stop the A/D Pacer; when the gate is active, A/D conversions are enabled. When the gate is inactive, A/D conversions are suspended but they will resume when the gate returns to its active state. Gating and triggering both share DI1 pin and thus are mutually exclusive. External Pacing, where each A/D conversion is started by an external signal, is tied to the DI0 pin. This means that External Pacing can be combined with a Trigger/Gate function.

BASE ADDRESS +10   Example, 30Ah, 778 Decimal

WRITE

Mode	7	6	5	4	3	2	1	0
ENHANCED	*DAC1R1*	*DAC1R0*	*DAC0R1*	*DAC0R0*	**PRETRIG**	**T/G POL**	**T/G SEL**	**T/G EN**
COMPATIBLE	*DAC1R1*	*DAC1R0*	*DAC0R1*	*DAC0R0*	-	-	**CTR0**	**TRG0**

NOTE: DACxRx ARE USED WITH THE 6402/12 ONLY, (FOR THE 6402/16 THESE BITS HAVE NO FUNCTION - THE DAC'S RANGES ARE SELECTED BY SWITCHES)

DAC#R0:   Output Range select bit for DAC #.   When = 1, range is ±5V or 0 to 5V. When = 0; range is ±10V or 0 to 10V.
DAC#R1:   Output Polarity select bit for DAC #. When = 1, polarity is Unipolar. When = 0, polarity is Bipolar

Table 5-6. Output Range Select Codes

Set DAC Output Range	**DAC#R1**	**DAC#R0**
±5V	0	0
±10V	0	1
0 to 5V	1	0
0 to 10V	1	1

ENHANCED MODE:
T/G EN: Trigger/Gate Enable bit
            When = 1, DI1 pin is enabled for Trigger/Gate function.
            When = 0, Trigger/Gate function is not used. DI1 pin is strictly used for digital input.
            If pretriggering, then set T/G EN to 0 since this will gate in the CTR0OUT clock with ARMED.

T/G SEL: Trigger/Gate Select bit (Requires T/G EN =1)
            When = 0,   DI1 pin functions as a Gate, the active level is determined by the T/G POL bit.
            When = 1,   DI1 pins functions as a Trigger, the active edge is determined by T/G POL bit.

T/G POL: Trigger/Gate Polarity bit (Requires T/G EN =1 or PRETRIG = 1)
            When = 0, if trigger, active edge is rising; if gate, active level is high.
            When = 1, if trigger, active edge is falling; if gate, active level is low.

PRETRIG: Used to stop pacing a certain number of conversions after the trigger occurs.
             When = 1 , Pre-trigger Mode enabled. =0, Pre-trigger Mode disabled.
            8254 Counter 0 is used as the 'Post-Trigger' counter
            (Pre-trigger mode requires that T/G EN = 0, and that T/G SEL = 1 for edge triggering)

Counter 0 clock input is generated from the Conversion Complete pulse to count the number of conversions performed.
A 'Pre-trigger index' counter value can be read (as a Word) from Base + 2 to give the number of conversions that have occurred from the Trigger to the half-full or End-of-Acquisition interrupt. Since current FIFO half-full is 512 conversions this number will be in the range of 0 to 511.

COMPATIBLE MODE:

TRIG0: Trigger/Gate Enable bit

When = 1, Enables DIN0 input to gate the pacer (external trigger/gate).

When = 0, Enables pacer gate preventing external trigger/gate control.

CTR0: Counter 0 input control

When = 1, 100 khz input to counter 0 if external counter 0 input is pulled high (or unconnected since the pin is internally pulled high).

When = 0, external clock input generates pulses to counter 0 clock input.

READ

Mode	7	6	5	4	3	2	1	0
ENHANCED	-	POSTMODE	ARMED	PACERGATE	PRETRIG	T/G POL	T/G SEL	T/G EN
COMPATIBLE	-	POSTMODE	ARMED	PACERGATE	-	-	CTR0	TRG0

ARMED - When = 0, counting of post-trigger samples is disabled. When = 1, counting of post-trigger samples is enabled.

POSTMODE - SEE REGISTER BASE+8 FOR FULL DESCRIPTION.

PACERGATE - When = 0: the Gate for the 8254 PACER is off. When = 1, the Pacer is on.

5.9 COMPATIBLE MODE CONTROL REGISTER

BASE ADDRESS +11   Example, 30Bh, 779 Decimal

READ/WRITE

7	6	5	4	3	2	1	0
DMA1/3	UNI/BIP	SE/DIFF	MODE	HC_AI1	HC_AI0	GAIN1	GAIN0

Since the DAS6402 has no switches or jumpers, certain options must be selectible for Compatible Mode. This is done by placing these selections in the Compatible Mode register. The Mode bit must be set to 1 first to allow the following bits to be changed: **DMA1/3**, **UNI/BIP, SE/DIFF**. The default state for all three bits is 0, which is how the DAS1600 is shipped.

DMA1/3 - When = 1, DMA channel 3 is selected.

When = 0, DMA channel 1 is selected.

DMA is allowed only in Compatible Mode, but the DMA channel selection bit can only be changed when the board is in Enhanced mode. The programmed state will be retained when the board is switched back to Compatible mode.

UNI/BIP - When = 1, Analog Front-End in Unipolar Range

When = 0, Analog Front-End in Bipolar Range

UNI/BIP is used for both Compatible and Enhanced modes, but the bit can only be changed when the board is in Enhanced mode. The programmed state will be retained when the board is switched back to Compatible mode.

SE/DIFF: When = 1, Analog Front-End in Single-ended Mode

When = 0, Analog Front-End in Differential Mode

SE/DIFF is used for both Compatible and Enhanced modes, but the bit can only be changed when the board is in Enhanced mode. In Compatible mode, the number of channels is limited according to the table below. The programmed state will be retained when the board is switched back to Compatible mode.

MODE: When = 1, Board is configured in Enhanced Mode, which in general allows for 64 analog input channels, enhanced triggering, FIFO/REP INSW support, etc..

When = 0, Board is configured in "Compatible" mode, it is software compatible to the DAS1600.

Table 5-7. Comparison of Features: Compatible vs. Enhanced Mode

Feature	MODE	
	Compatible	Enhanced
# Analog Input Channels	16 S-E 8 Diff	64 S-E 32 Diff
# Digital I/O	4 in 4 out	8 in 8 out
External Triggering	Combined w/ Pacing on DIN1, gate only	Separate from Pacing, uses DIN1. Can be gate (level) or trigger (edge)
External Pacing	Combined w/ Trigger on DIN1	Separate from Trigger, uses DIN0
DMA	yes	no
REP INSW	no	yes
Independent Counter at user connector	yes, CTR0	no, CTR0 used for pre-triggering
Burst Mode	Yes	Yes
Interrupts	Single ADC DMA	Single ADC REP INSW End of Burst External
Pre-trigger	No	Yes

In Enhanced mode, **HC_AI1, HC_AI0** select the interrupt source, which also will determine the acquisition mode the board is to be operated under. These bits are 0 in Compatible mode. Refer to Table 6-8.

Table 5-8. Interrupt Source Coding - Enhanced Mode

HC_AI1	HC_AI0	ADC Acquisition Mode	Interrupt Source
0	0	Single ADC polled	none
0	1	Single ADC interrupt	FIFO Not Empty
1	0	Fifo REP INSW (512 samples)	FIFO ½ Full
1	1	Burst REP INSW (2-64 samples)	End of Burst

If pre-trigger is enabled, (allowed during a REP INSW mode, HC_AI1=1) then an End-of-Acquisition interrupt will be enabled. This interrupt occurs a pre-determined number of conversions after the trigger. Counter 0 is programmed to count conversions after the trigger and will cause the interrupt when it counts down and reaches Terminal Count.

GAIN1, GAIN0 select the front end gain (Table 5-9). They are valid for Enhanced or Compatible Mode.

Table 5-9. Front-End Gain Coding

GAIN1	GAIN0	Analog Input Gain	Analog Input Voltage Range
0	0	1	0 to 10V or ±10V
0	1	2	0 to 5V or ±5V
1	0	4	0 to 2.5V or ±2.5V
1	1	8	0 to 1.25V or ±1.25V

5.10 PACER CLOCK DATA AND CONTROL REGISTERS

8254 COUNTER 0 DATA - POST TRIGGER CONVERSION COUNTER

BASE + 12   Example, 30Ch, 780 decimal

READ/WRITE

7	6	5	4	2	3	1	0
D8	D7	D6	D5	D4	D3	D2	D1

Counter 0 is used to count conversions to stop the acquisition when a known number of samples have occurred. It essentially is gated on when only a 'residual' number of conversions remain. The main counting of samples is done by the Interrupt Service Routine, which will increment each time by 'packets' equal to Fifo 1/2-full (Fifo 1/2-full is 512 for DAS6400). Generally the value loaded into Counter 0 is N mod 512, where N is the total count, or the post trigger count, since Total count is not known when pre-trigger is active. Counter 0 will be enabled by use of the **ARMED** bit (Base+8) when the next-to-last 1/2-full interrupt is processed.
Counter 0 is to operated in Mode 0.

8254 COUNTER 1 DATA - PACER DIVIDER LOWER

BASE + 13   Example, 30Dh, 781 decimal

READ/WRITE

7	6	5	4	2	3	1	0
D8	D7	D6	D5	D4	D3	D2	D1

8254 COUNTER 2 DATA - PACER DIVIDER UPPER

BASE + 14   Example, 30Eh, 782 decimal

READ/WRITE

7	6	5	4	2	3	1	0
D8	D7	D6	D5	D4	D3	D2	D1

Counter 1 is the lower 16 bits of the 32-bit pacer clock divider. It's output is fed to the clock input of Counter 2 which is the upper 16-bits of the pacer clock divider. The clock input to Counter 1 is a precision oscillator source, selected by software to be 1MHz or 10MHz
Counter 2's output is called the 'Internal Pacer' and can be selected by software to the be the A/D Pacer source. Counters 1 & 2 should be configured to operate in 8254 Mode 2.

8254 CONTROL REGISTER

BASE + 15   Example, 30Fh, 783 decimal
WRITE ONLY

7	6	5	4	2	3	1	0
D8	D7	D6	D5	D4	D3	D2	D1

The control register is used to set the operating Modes of 8254 Counters 0,1 & 2. A counter is configured by writing the correct Mode information to the Control Register, then the proper count data must be written to the specific Counter Register. The Counters on the 8254 are 16-bit devices. Since the interface to the 8254 is only eight bits wide, Count data is written to the Counter Register as two successive bytes. First the low byte is written, then the high byte. The Control Register is eight bits wide. Further information can be obtained on the 8254 data sheet, available from Intel or Harris.

6 CALIBRATION AND TEST

Every board was fully tested and calibrated before being placed in finished goods inventory at the factory. For normal environments a calibration interval of 6 months to one year is recommended. If frequent variations in temperature or humidity are common then recalibrate at least once every three months. It takes less than 20 minutes to calibrate a CIO-DAS6402.

6.1 REQUIRED EQUIPMENT

Ideally, you will need a precision voltage source, a 4 1/2 digit digital voltmeter (5 ½ digit for the CIO-DAS-6402/16), a calculator and some wire. If you do not have a precision voltage source, you will need a non-precision source and have to make a few calculations.

You will not need an extender card to calibrate the board but you will need to have the cover off you computer with the power on, so trim pots can be adjusted during calibration. For that reason a plastic screwdriver has been supplied with your CIO-DAS6402. In the event that the screwdriver is dropped into the PC, no damage will result from short circuits.

6.2 CALIBRATING THE A/D & D/A CONVERTERS

The A/D is calibrated by applying a known voltage to an analog input channel and adjusting trim pots for offset and gain. There are four trim pots requiring adjustment to calibrate the analog input section of the CIO-DAS6402. The entire procedure is described in detail in the *Insta*Cal™, calibration routine.

The CIO-DAS6402 should be calibrated for the range you intend to use it in. When the range is changed, slight variation in Zero and Full Scale may result. These variations can be measured and removed in software if necessary.

7 SIGNAL CONDITIONING CIRCUITS

7.1 VOLTAGE DIVIDERS

An alternative method of measuring a signal which varies over a range greater than the input range of a digital input, is to use a voltage divider. When correctly designed, it can drop the voltage of the input signal to a safe level the digital input can accept.

Ohm's law states:
>   Voltage = Current x Resistance

Kirkoff's law states:
>   The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.

In a voltage divider, the voltage across one resistor in a series circuit is proportional to the total resistance divided by the one resistor (see formula below).

The object in a voltage divider is to choose two resistors having the proportions of the maximum voltage of the input signal to the maximum allowed input voltage.

The formula for attenuation is:

$$\text{Attenuation} = \frac{R1 + R2}{R2}$$

$$2 = \frac{10K + 10K}{10K}$$

For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the attenuation (A) is 2:1 or just 2.

R1 = (A-1) x R2   For a given attenuation, pick a resistor and call it
                         R2, the use this formula to calculate R1.

Digital inputs often require the use of voltage dividers. For example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to a digital input. The voltage must be dropped to 5 volts max when on. The attenuation is 24:5 or 4.8.

Using the equation above, if R2 is 1K, R1 = (4.8−1) x 1000 = 3.8K.

Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

NOTE

The resistors, R1 and R2, are going to dissipate power in the divider circuit according to the equation $W = I^2 \times R$; (Current (I) = Voltage/Resistance). The higher the value of the resistance (R1 + R2), the less power dissipated by the divider circuit. Here is a simple rule:

For attenuation of <5:1, no resistor should be less than 10K.

For attenuation of > 5:1, no resistor should be less than 1K.

7.2   LOW PASS FILTERS

A low pass filter is placed on the signal wires between a signal and an A/D board. It stops frequencies greater than the cutoff frequency from entering the A/D board's analog or digital inputs.

The cutoff frequency is that frequency above which no variation of voltage with respect to time may enter the circuit. For example, if a low pass filter had a cutoff frequency of 30 Hz, the kind of interference associated with line voltage (60 Hz) would be filtered out but a signal of 25 Hz would be allowed to pass.

In a digital circuit, a low-pass filter is often used to filter an input from a momentary contact button or relay.

A simple low-pass filter may be constructed from one resistor (R) and one capacitor (C). The cutoff frequency is determined according to the formulas below: (Use π= 3.14, R = ohms, C = Farads.)

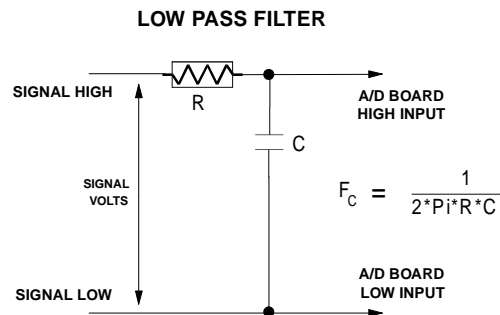$$Fc = \frac{1}{2 * \pi * R * C}$$

$$R = \frac{1}{2 * \pi * C * Fc}$$

LOW PASS FILTER

SIGNAL HIGH

R

C

$$F_C = \frac{1}{2*Pi*R*C}$$

SIGNAL VOLTS

A/D BOARD HIGH INPUT

A/D BOARD LOW INPUT

SIGNAL LOW

Figure 7-2. Low-Pass Filter Theory

8.1 CIO-DAS6402/16

Typical for 25 DegC unless otherwise specified.

Power consumption
Icc: Operating	1.17 A typical, 1.67 A max

Analog input section
A/D converter type	AD976A, successive-approximation
Resolution	16 bits
Programmable ranges	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
A/D pacing	Programmable: internal counter or external source (DIN0, rising edge)
Data transfer	Compatible: Byte wide, interrupt, software polled, DMA
	Enhanced: Word wide, interrupt, software polled, REP INSW
	Above via 1 kilo sample FIFO
	Burst Mode (programmable option) @ 100 kHz
Polarity	Unipolar/Bipolar, software selectable
Number of channels	Compatible: 8 differential or 16 single-ended, software-selectable
	Enhanced: 32 differential or 64 single-ended, software-selectable
Interrupts	Programmable levels 2, 3, 5, 7, 10, 11, 15
	Positive-edge triggered
Interrupt enable	Programmable interrupt enable for internal and external interrupt
Interrupt sources	End-of-conversion, FIFO not empty, FIFO half full, end-of-burst, external
Trigger sources	Compatible: External hardware/software (DIN0)
	Enhanced: External trigger/gate (DIN1), edge/level,polarity/edge programmable.
A/D Triggering Modes	Digital:
	Software configurable for Edge (triggered) or level-activated (gated).
	Programmable polarity (rising/falling edge trigger, high/low gate).
	Pre-trigger:
	Unlimited pre- and post-trigger samples. Total # of samples must be > 512.
A/D conversion time	5 μs
Throughput	100 kHz min
Integral Linearity error	±2 LSB max
No missing codes guaranteed	16 bits
Gain drift (A/D specs)	±7 ppm/°C, all ranges
Zero drift (A/D specs)	±2 ppm/°C, all ranges
Input leakage current (@25 Deg C)	200 nA
Input impedance	Min 10 Meg Ohms
Absolute maximum input voltage	±15V

Analog Output
Resolution	16 bits
Number of channels	2 Voltage Outputs
D/A type	AD660BN
Voltage Ranges	±2.5, ±5, ±10, 0 to 2.5, 0 to 5, 0 to 10, switch-selectable
Offset error	Adjustable to zero by potentiometer
Gain error	Adjustable to zero by potentiometer
Differential nonlinearity	±1LSB max
Integral nonlinearity	±1LSB max
Monotonicity	Guaranteed monotonic to 15 bits over temperature
Gain drift	±15 ppm/°C max
Bipolar offset drift	±5 ppm/°C max
Unipolar offset drift	±3 ppm/°C max
D/A pacing	Software
D/A trigger modes	N/A
Data transfer	Byte or word update
Throughput	System-dependent (software-paced)
Settling time (20V step to ±½LSB)	12 µs typ, 19 us max
Settling time (10V step to ±½LSB)	6 µs typ, 9 us max
Slew Rate	2.8 V/uS Typical
Current Drive	±5 mA min
Output short-circuit duration	40 mA min Continuous
Output Coupling	DC
Amp Output Impedance (OP-27)	0.1 Ohms max
Miscellaneous	Double buffered output latches
	Update DACs individually or simultaneously (jumper selectable)
	Power up and reset, all DAC's cleared to 0 volts (switch selects bipolar or unipolar zero)

Digital Input / Output
Digital Type	Output: 74LS244
	Input: 74LS273
Configuration	Compatible: Two dedicated ports, 4 inputs and 4 outputs
	Enhanced: Two dedicated ports, 8 inputs and 8 outputs
Output High	2.7 volts @ -0.4 mA min
Output Low	0.4 volts @ 8 mA min
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, - 0.5 volts absolute min

Counter section
> Counter type 82C54
> Configuration 3 down-counters, 16 bits each

> > Counter 0
> > > Compatible mode - Independent
> > > > Source: Programmable external (CTR0 CLK) or 100 kHz internal source).
> > > > Gate: Available at connector (DIN2).
> > > > Output: Available at connector (CTR0 OUT).
> > > Enhanced mode - ADC residual sample counter
> > > > Source: ADC Clock.
> > > > Gate: Internal use.
> > > > Output: End-of-Acquisition interrupt.

> > Counter 1 - ADC Pacer Lower Divider
> > > Source: 10 MHz oscillator
> > > Gate: Tied to Counter 2 gate, programmable source.
> > > Output: Chained to Counter 2 Clock.

> > Counter 2 - ADC Pacer Upper Divider
> > > Source: Counter 1 Output.
> > > Gate: Tied to Counter 1 gate, programmable source.
> > > Output: ADC Pacer clock, available at user connector.

Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental
Operating temperature range	0 to 70°C
Storage temperature range	- 40 to 100°C
Humidity	0 to 90% non-condensing

8.2   CIO-DAS6402/12

Typical for 25°C unless otherwise specified.

Power consumption
    Icc: Operating   1.05 A typical, 1.6 A max

Analog input section
    A/D converter type   ADS7800, Successive Approximation
    Resolution   12 bits
    Programmable ranges   ±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
    A/D pacing   Programmable: internal counter or external source (DIN0, rising edge)
    Data transfer   Compatible: Byte wide, interrupt, software polled, DMA
                                    Enhanced: Word wide, interrupt, software polled, REP INSW
                                    Above via 1k sample FIFO
                                    Burst Mode (programmable option) @ 250 kHz

    Polarity   Unipolar/Bipolar, software-selectable
    Number of channels   Compatible: 8 differential or 16 single-ended, software-selectable
                                    Enhanced: 32 differential or 64 single-ended, software-selectable

    Interrupts   Programmable levels 2, 3, 5, 7, 10, 11, 15
                                    Positive-edge triggered
    Interrupt enable   Programmable interrupt enable for internal and external interrupt
    Interrupt sources   End-of-conversion, FIFO not empty, FIFO half full, end-of-burst, external
    Trigger sources   Compatible: External hardware/software (DIN0)
                                    Enhanced: External trigger/gate (DIN1), edge/level, polarity/edge programmable.

    A/D Triggering Modes   Digital:
                                    Software configurable for Edge (triggered) or level-activated (gated).
                                    Programmable polarity (rising/falling edge trigger, high/low gate).
                                    Pre-trigger:
                                    Unlimited pre- and post-trigger samples. Total # of samples must be > 512.

    A/D conversion time   3 μs
    Throughput   333 kHz min
    Differential Linearity error   ±.75 LSB
    Integral Linearity error   ±.5 LSB

    No missing codes guaranteed   12 bits
    Gain drift (A/D specs)   ±6 ppm/°C, all ranges
    Zero drift (A/D specs)   ±1 ppm/°C, all ranges
    Input leakage current (@25 Deg C)   200 nA
    Input impedance   Min 10Meg Ohms
    Absolute maximum input voltage   ±15V

Analog Output:

Resolution	12 bits
Number of channels	2 Voltage Output
D/A type	AD7237
Voltage Ranges	±10V, ±5V, 0 to 5V, 0 to 10V. Software-programmable
Offset error	Adjustable to zero by potentiometer
Gain error	Adjustable to zero by potentiometer
Differential nonlinearity	±1LSB max
Integral nonlinearity	±1LSB max
Monotonicity	Guaranteed monotonic over temperature
D/A Gain drift	±15 ppm/$^\circ$C max
D/A Bipolar offset drift	±5 ppm/$^\circ$C max
D/A Unipolar offset drift	±3 ppm/$^\circ$C max
D/A pacing	Software
D/A trigger modes	N/A
Data transfer	Byte or word update
Throughput	System dependent (software paced)
Settling time (20V step to $\pm\frac{1}{2}$LSB)	5 µs typ, 8 µs max
Slew Rate	4V/µs typ
Current Drive	±2 mA min
Output short-circuit duration	25 mA indefinite
Output Coupling	DC
Amp Output Impedance (AD711)	0.1 Ohms max
Miscellaneous	Double-buffered output latches
	Power up and reset, all DAC's cleared to 0 volts

Digital Input / Output

Digital Type	Output: 74LS244
	Input: 74LS273
Configuration	Compatible: Two dedicated ports, 4 inputs and 4 outputs
	Enhanced: Two dedicated ports, 8 inputs and 8 outputs
Output High	2.7 volts @ -0.4 mA min
Output Low	0.4 volts @ 8 mA min
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, - 0.5 volts absolute min

Counter section
    Counter type   82C54
    Configuration   3 down-counters, 16 bits each

Counter 0
Compatible mode - Independent
    Source: Programmable external (CTR0 CLK) or 100kHz internal source).
    Gate: Available at connector (DIN2).
    Output: Available at connector (CTR0 OUT).
Enhanced mode - ADC residual sample counter
    Source: ADC Clock.
    Gate: Internal use.
    Output: End-of-Acquisition interrupt.

Counter 1 - ADC Pacer Lower Divider
    Source: 10 MHz oscillator
    Gate: Tied to Counter 2 gate, programmable source.
    Output: Chained to Counter 2 Clock.

Counter 2 - ADC Pacer Upper Divider
    Source: Counter 1 Output.
    Gate: Tied to Counter 1 gate, programmable source.
    Output: ADC Pacer clock, available at user connector.

Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental
Operating temperature range	0 to 70°C
Storage temperature range	- 40 to 100°C
Humidity	0 to 90% non-condensing

For your notes.

For your notes.

EC Declaration of Conformity

We, Measurement Computing Corp., Inc., declare under sole responsibility that the product:

Part Number	Description
CIO-DAS6402/12	12-Bit Analog I/O Board
CIO-DAS6402/16	16-Bit Analog I/O Board

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance