USB-QUAD08

Eight-channel Quadrature Encoder Input Device

User's Guide

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MEASUREMENT COMPUTING™

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Table of Contents

About this User's Guide

What you will learn from this user's guide

This user's guide describes the Measurement Computing USB-QUAD08 data acquisition device and lists device specifications.

Conventions in this user's guide

For more information

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

bold text — **Bold** text is used for the names of objects on a screen, such as buttons, text boxes, and check boxes.

italic text — *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase.

Where to find more information

Additional information about the USB-QUAD08 is available on our website at www.mccdaq.com. You can also contact Measurement Computing Corporation by phone, fax, or email with specific questions.

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

Introducing the USB-QUAD08

The USB-QUAD08 is a USB 2.0 high-speed device supported under popular Microsoft® Windows® operating systems. The device is compatible with both USB 1.1 and USB 2.0 ports.

The USB-QUAD08 provides the following features:

- Eight counter inputs (quadrature/non-quadrature mode)
  - Simultaneous input and decoding of up to eight incremental quadrature encoders.
  - High-speed pulse counter for general counting applications; multiple counting modes supported
  - Configurable as single-ended or differential
  - 10 MHz, 16-, 32-, 48-bit resolution, ±12 volt input range
  - Indicator LEDs show the status of each counter/encoder input
  - 16 debounce settings
- Eight digital I/O bits
  - Configurable as input or output
  - Digital input bits accept voltage inputs up to 50VDC (42.4Vpk)
  - Digital output bits are open collector, with clamping diodes for CEMF (counter-electromotive force) suppression
- Internal/external pacing
- Internal software trigger and external digital trigger

I/O connections are made to ten banks of detachable screw terminals or 37-pin D-type connectors. The 37-pin connectors are pin-compatible with the PCI-QUAD04 for upgrade/migration from a PCI bus, although software migration is required.

The USB-QUAD08 is powered by the +5 volt USB supply from your computer. When operating in encoder mode, the USB-QUAD08 passes an external supply of up to 50 VDC (current rated at 1.5 A @ 5 VDC) through the ENC+ IN screw terminal to all connected ENC+ terminals.

Installing the USB-QUAD08

What comes with your USB-QUAD08 shipment?

As you unpack your USB-QUAD08, verify that the following components are included.

Hardware

- USB-QUAD08
- USB cable (2-meter length)

Documentation

In addition to this hardware user's guide, you should also receive the *Quick Start Guide*. This booklet provides an overview of the MCC DAQ software you received with the device, and includes information about installing the software. Please read this booklet completely before installing any software or hardware.

Optional components

If you ordered any of the following products with your board, they should be included with your shipment.

- Cables
  - C37F-4X9F-1M
  - C37FFS-x
  - C37FF-x
- Signal termination accessories

  MCC provides signal termination products for use with the USB-QUAD08. Refer to Signal termination on page 14 for a list of compatible accessory products.
- ACC-202 DIN-rail kit

Unpacking the USB-QUAD08

As with any electronic device, take care while handling to avoid damage from static electricity. Before removing the USB-QUAD08 from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

If the device is damaged, notify Measurement Computing Corporation immediately by phone, fax, or e-mail.

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

For international customers, contact your local distributor. Refer to the International Distributors section on our web site at www.mccdaq.com/International.

Installing the software

Install the MCC DAQ software before you install your board. The driver needed to run the USB-QUAD08 is installed with the MCC DAQ software. Refer to the *Quick Start Guide* for instructions on installing the software on the MCC DAQ CD. This booklet is available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Be sure you are using the latest system software

Before you install your USB-QUAD08, run Windows Update to update your operating system with the latest USB drivers.

Configuring the channel input mode

The counter inputs are configurable as single-ended (±12 V) or differential (±12 V; differential input ±14 Vmax) mode via on-board switches (see Figure 1).

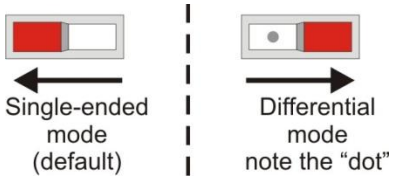


Figure 1. Channel input mode switch

Figure 2 shows the locations for the counter input mode switches and the counter LEDs. Using the board orientation shown in Figure 2, slide the switch to the left (toward the USB connector) for single-ended mode, or to the right (towards the 37-pin connector) for differential mode. Note that the "dot" is visible on the switch when configured for differential mode, regardless of the board orientation.

By default, the board is shipped with the counter inputs configured for single-ended operation (as shown in Figure 2).

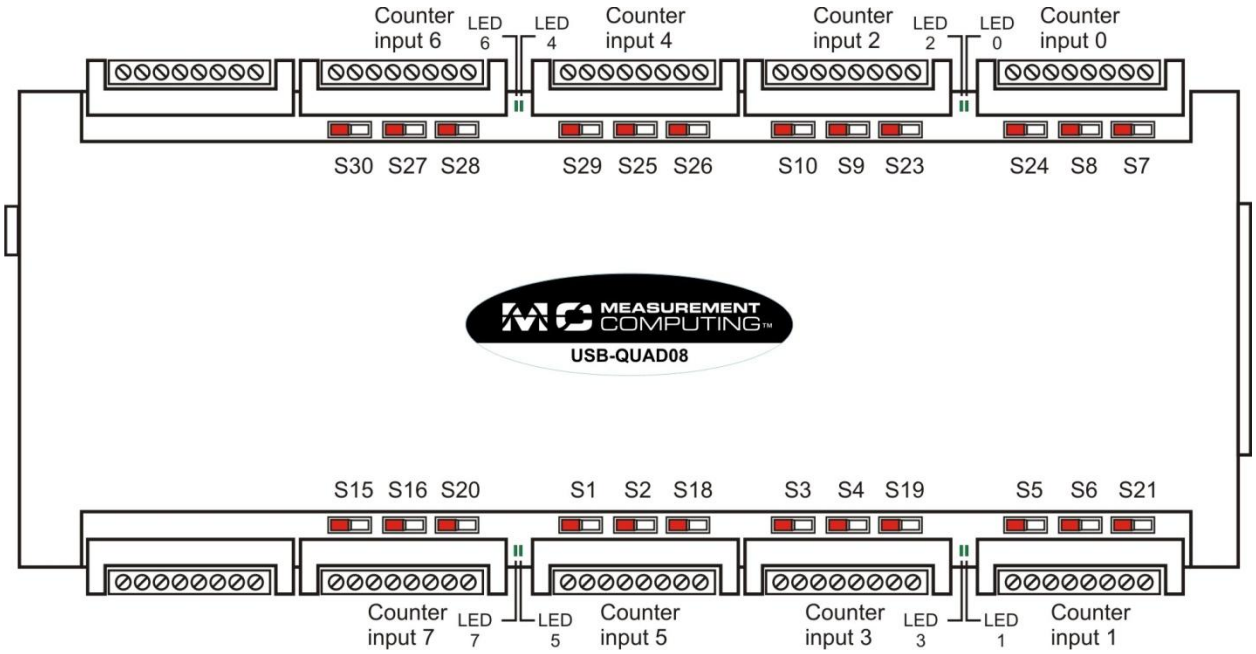


Figure 2. Input mode switch and LED locations

The following table lists the counter input channel associated with each switch.

	Counter input channel							
Input	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Phase A	S7	S5	S23	S3	S26	S1	S28	S15
Phase B	S8	S6	S9	S4	S25	S2	S27	S16
Index	S24	S21	S10	S19	S29	S18	S30	S20

Installing the hardware

Install the MCC DAQ software before you install your board

The driver needed to run your board is installed with the MCC DAQ software. Therefore, you need to install the MCC DAQ software before you install your board. Refer to the *Quick Start Guide* for instructions on installing the software.

Connecting the USB-QUAD08 to your system

To connect the USB-QUAD08 to your system, turn on your computer and connect the USB cable to an available USB port on the computer or to an external USB hub connected to the computer. Connect the other end of the USB cable to the USB connector on the device.

When you connect the device for the first time, a **Found New Hardware** dialog opens when the operating system detects the device. Two drivers will be loaded — "MCC USB" and "USB-QUAD08". The installation is complete after the drivers are loaded and the dialog closes. The Status LED on the USB-QUAD08 should blink and then remain on, indicating that communication between the device and the computer is established.

The **Power** LED blinks during device detection and initialization, and then remains on. When first powered on, a momentary delay may occur before the Power LED begins to blink or become solid.

If the Status LED turns off

If the Status LED turns on but then turns off, the computer has lost communication with the USB-QUAD08. To restore communication, disconnect the USB cable from the computer, and then reconnect it. This should restore communication, and the LED should turn on.

Signal connections

The USB-QUAD08 has 10 screw terminals and two 37-pin connectors. The table below lists the board connectors, applicable cables, and accessory products compatible with the USB-QUAD08.

Board connectors, cables, and accessory equipment

Connectors, cables, and accessories	Description
Connector type	10 banks of detachable screw terminals Two 37-pin D type connectors — J12 (external) and J50 (internal)
Compatible cables with the 37-pin connectors	C37F-4X9F-1M C37FF-x C37FFS-x
Compatible accessory products with the C37FF-x cable or C37FFs-x cable	CIO-MINI37 SCB-37 CIO-MINI37/DST CIO-MINI37-VERT CIO-MINI37-VERTDST CIO-TERMINAL
Wire gauge range for screw terminals	16 AWG to 28 AWG

Caution! Be sure to correctly phase the encoder according to the manufacturer instructions.

Screw terminal pinout

Pin assignments for differential mode are shown in Figure 3.

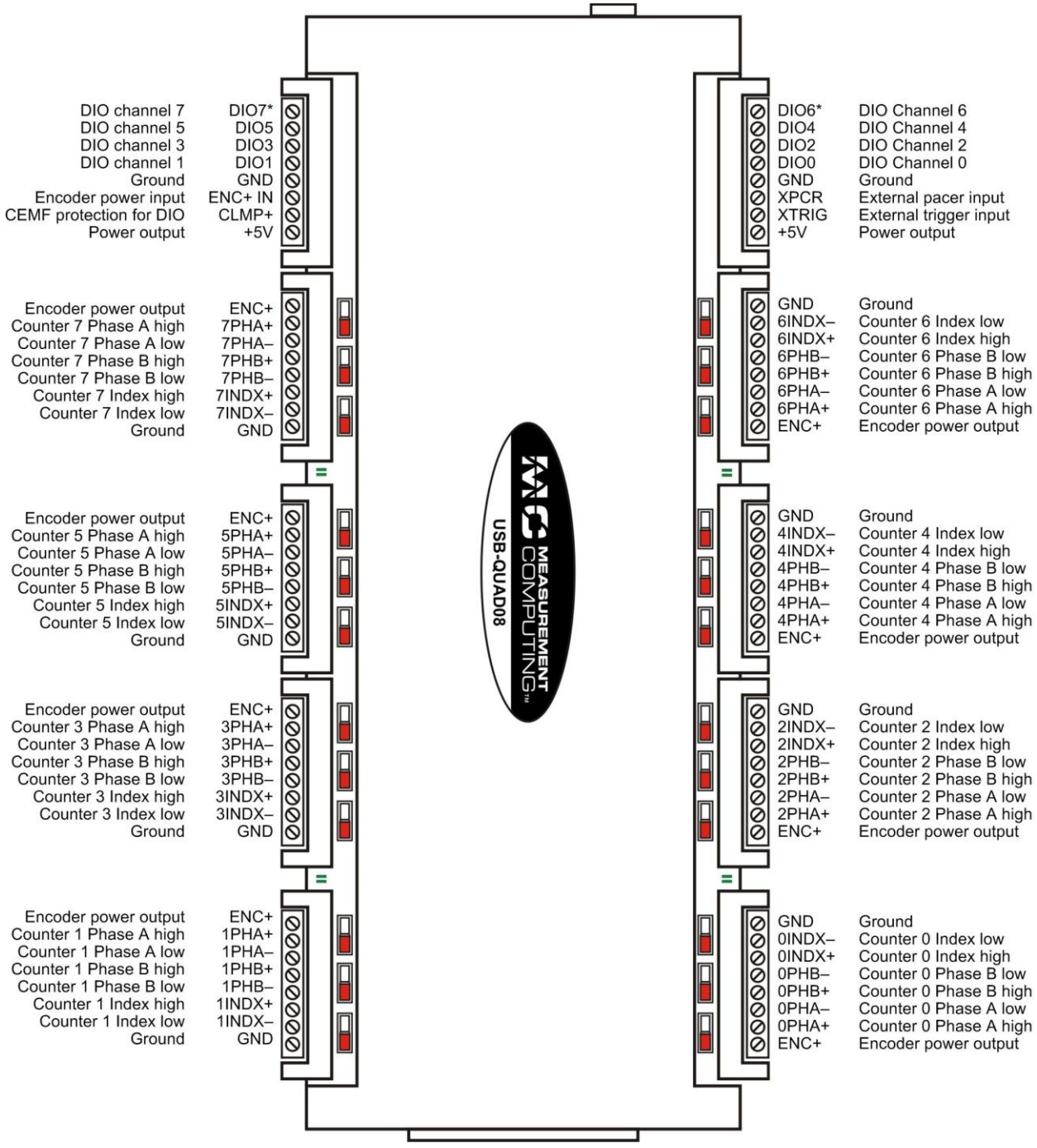


Figure 3. Differential mode pinout

Pin assignments for single-ended mode are shown in Figure 4.

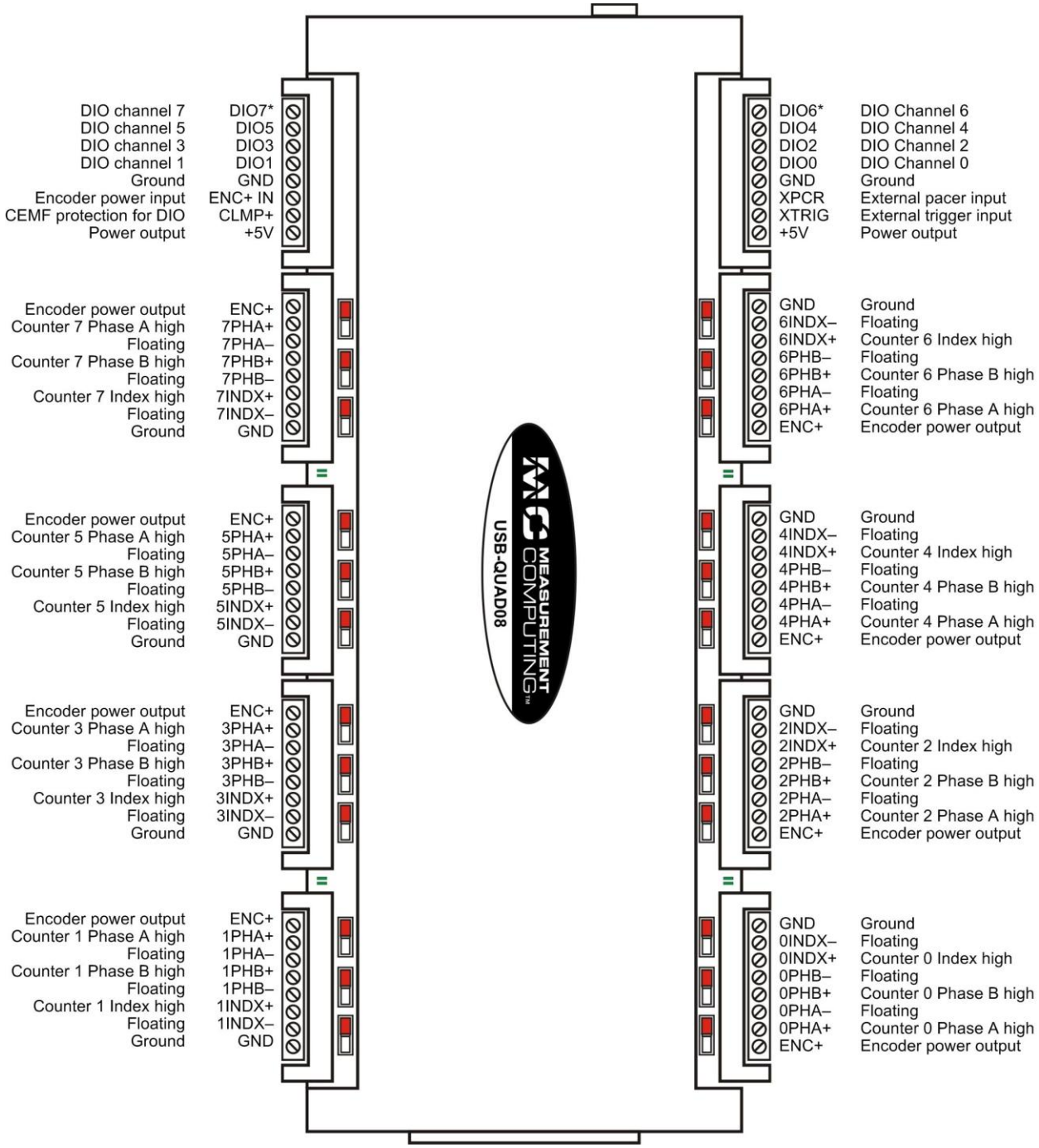


Figure 4. Single-ended mode pinout

Notes

- When operating in quadrature counter mode, the **ENC+** output terminals are used to power encoders. The external supply input to **ENC+ IN** is passed to all of the **ENC+** outputs. When operating in normal counter mode, the **ENC+ IN** and **ENC** terminals provide no function.
- Terminals **DIO6** and **DIO7** can also function as Timer Output 0 and Timer Output 1, respectively.
- The **CLMP+** terminal is used to protect the digital outputs from counter-electro-motive force (CEMF). Refer to page 26 for more information about CEMF.

37-pin connector pinout (J12 and J50)

The USB-QUAD08 has two 37-pin connectors. One connector (**J12**) is on the device right panel, and the other connector (**J50**) is internal to the device. Pin assignments for differential mode are shown in Figure 5.

Caution! Be sure to correctly phase the encoder according to the manufacturer's instructions.

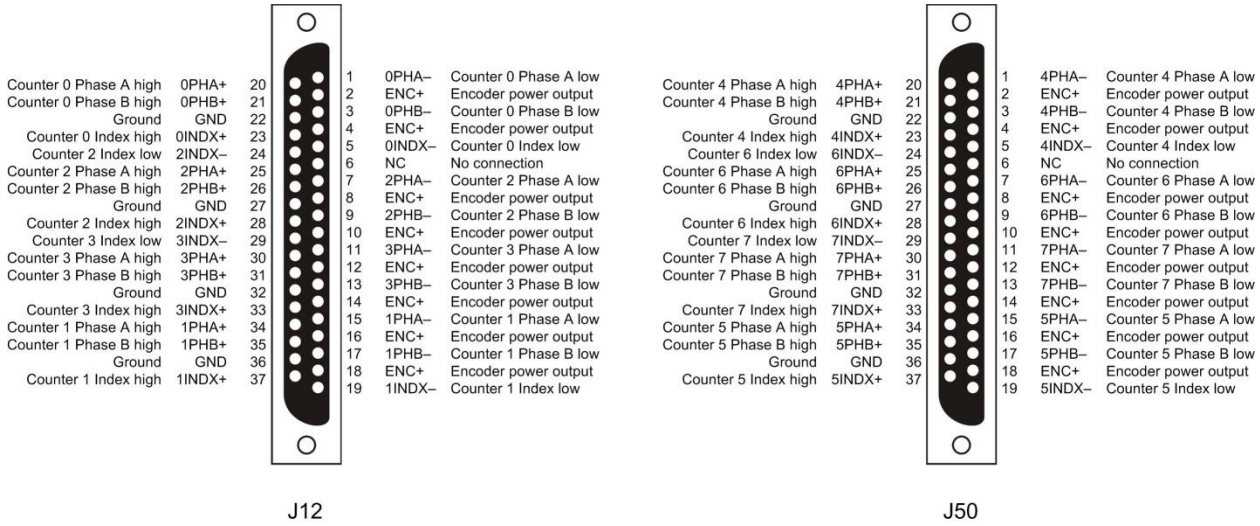


Figure 5. Differential mode pinout

Pin assignments for single-ended mode are shown in Figure 6.

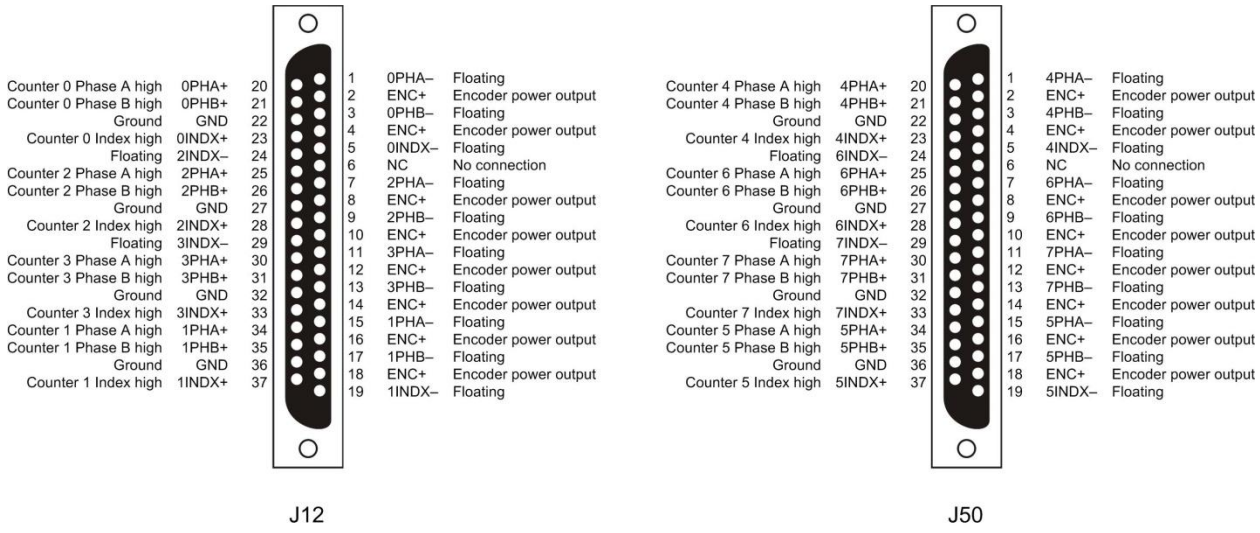


Figure 6. Single-ended mode pinout

Cables

C37F-4X9F-1M cable to 37-pin connector pinout

Connections between the 37-pin connectors (J12 and J50) to the C37F-4X9F-1M cable are shown in Figure 8. To power the encoders, the USB-QUAD08 passes an external supply from the **ENC+ IN** power input terminal to connected **ENC+** power output screw terminals.

Figure 7. C37F-4X9F-1M cable

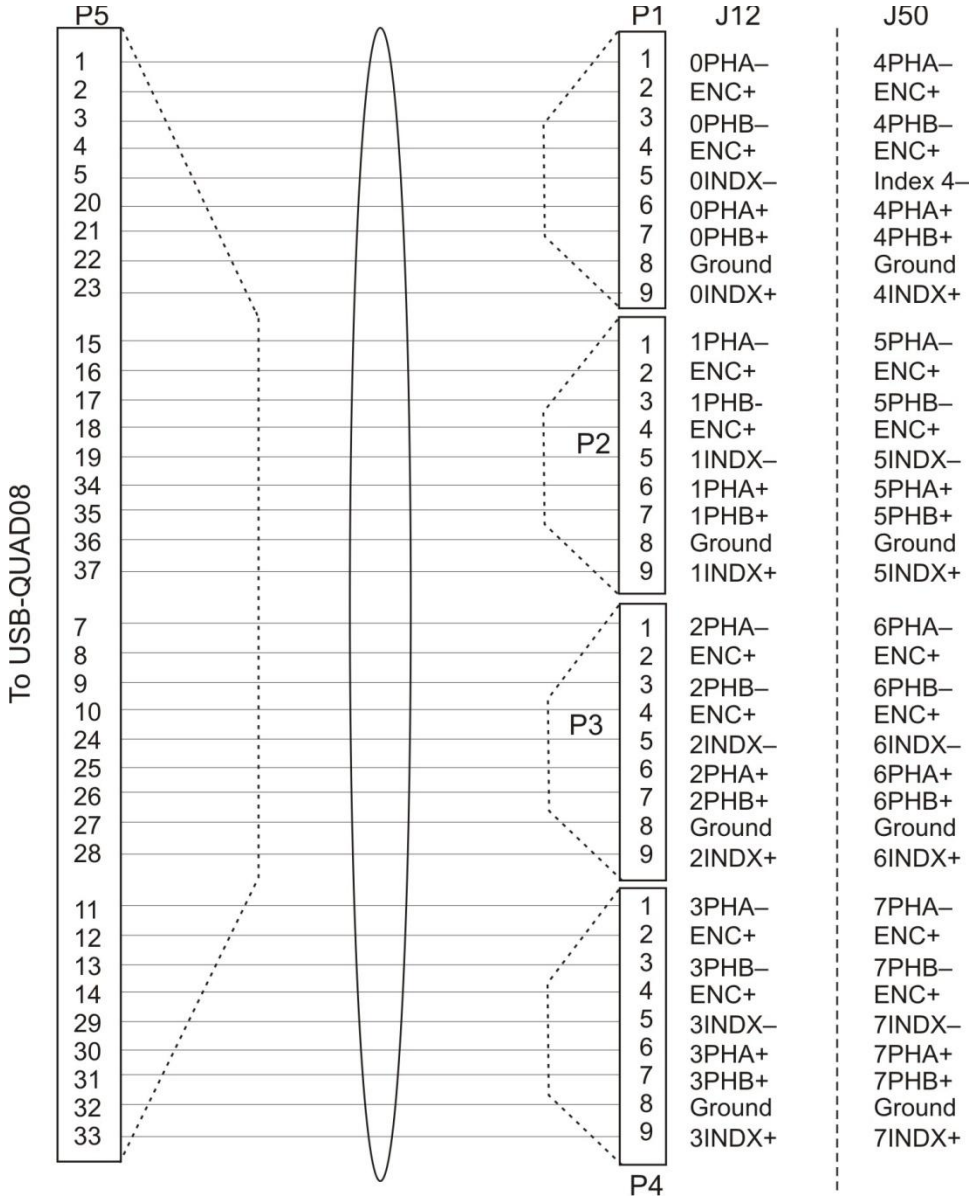


Figure 8. 37-pin connector to the C37F-4X9F-1M cable pinout

C37FFS-x and C37FF-x pinout

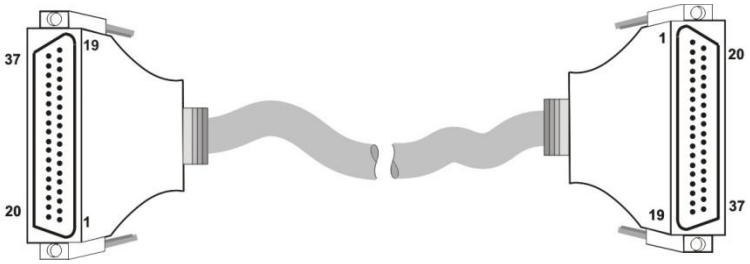


Figure 9. C37FFS-x cable

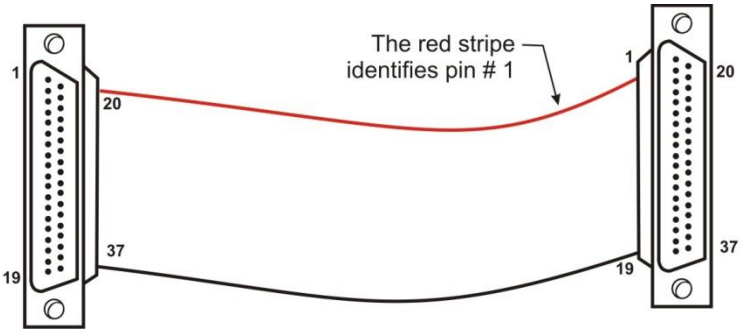


Figure 10. C37FF-x cable

Signal termination

You can connect the USB-QUAD08 to the following accessory boards using the C37FF-x or C37FFS-x cable.

- SCB-37 — Signal connection box, 37-conductor, shielded.
- CIO-MINI37 — Universal screw terminal board, 37-pin.
- CIO-MINI37/DST — Universal screw terminal board, 37-pin, detachable screw terminals.
- CIO-MINI37-VERT — Universal screw terminal board, 37-pin D male connector, vertical.
- CIO-MINI37-VERTDST — Universal screw terminal board, 37-pin D male connector, vertical, detachable screw terminals.
- CIO-TERMINAL— Universal screw terminal board, prototyping area 37 terminals.

Details on these products are available on our web site at www.mccdaq.com/products/screw_terminal_bnc.aspx.

DIN-rail mounting

Use the ACC-202 DIN-rail kit used for mounting a USB-QUAD08 to a standard DIN rail. Use the thread-forming screws to attach the DIN rail clip to your device.

Figure 11. ACC-202 DIN-rail kit

Details on this product are available on our web site at www.mccdaq.com/daq-accessory/acc-202.aspx.

Connecting the USB-QUAD08 to an encoder

Up to eight encoders can be connected to the screw terminals (*n*PHA, *n*PHB, and *n*INDX, where *n* is the number of the encoder (0 to 7) on the screw terminal). Up to four encoders can be connected to each 37-pin connector (external J12 and internal J50).

Encoder inputs are configurable in differential or single-ended mode. Each A and B signal can be made as a single-ended connection with respect to the ±12V to common ground (GND).

To connect the USB-QUAD08 to an encoder, make the following connections:

- Connect encoder signals A, B, and Z to the A, B, and Index pins on the screw terminal or 37-pin connector.
- Connect the encoder ground to a ground (GND) terminal.
- Connect the encoder power supply input to an **ENC+** screw terminal.

  To power the encoders, the USB-QUAD08 passes an external supply of up to 50 VDC (current rated 1.5 A @ 5 VDC) through the **ENC+ IN** encoder power input terminal to the **ENC+** encoder power output terminals. Diodes protect against reverse polarity.
- Connect the supply return to a ground (GND) terminal.

Caution! Ensure that the signals are connected such that there is no potential between PC ground and signal ground. Make sure that the current output specification is not exceeded.

Figure 12 shows the differential input connections to one encoder.

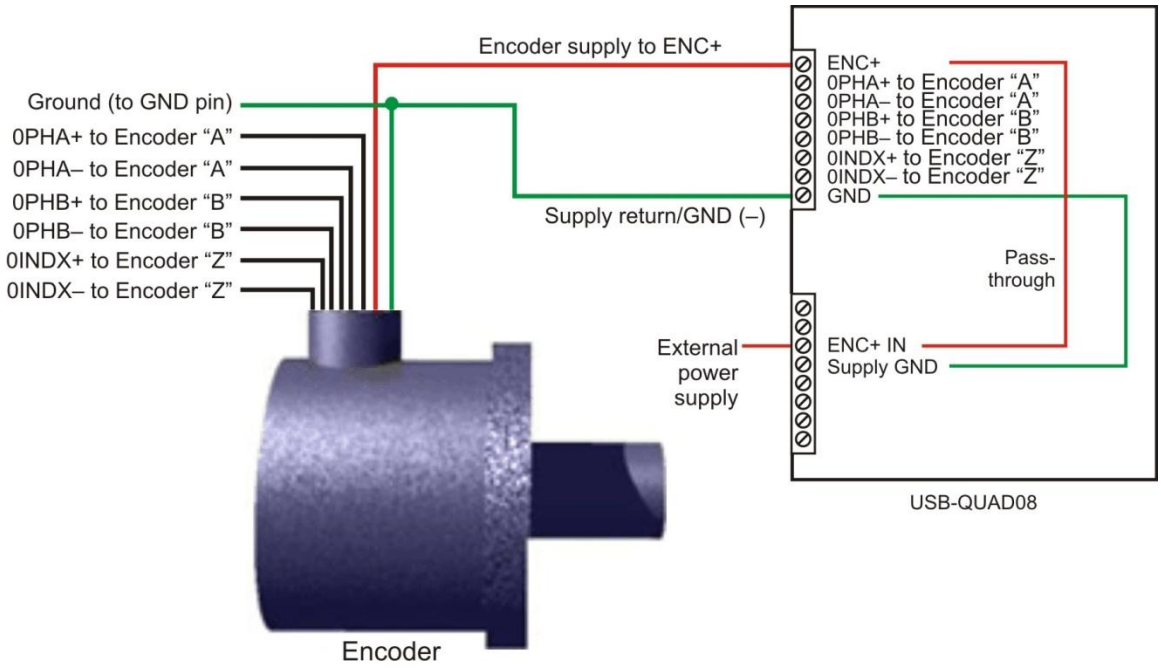


Figure 12. Differential encoder connections to the screw terminal or 37-pin connector

Figure 13 shows the single-ended input connections to one encoder.

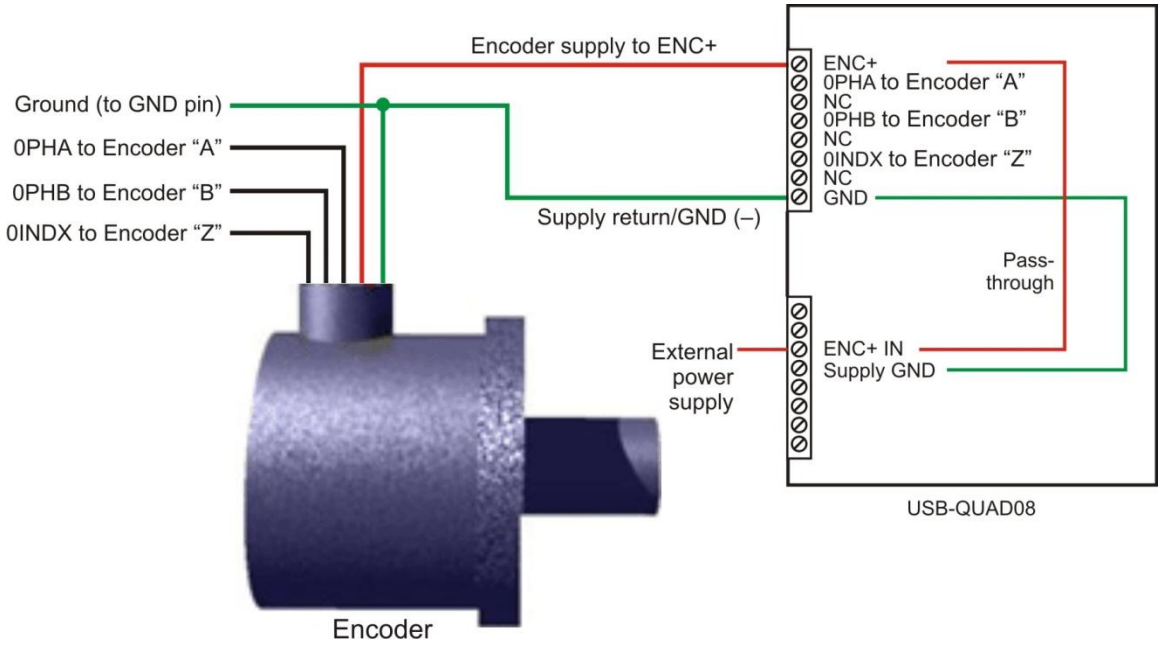


Figure 13. Single-ended encoder connections to the screw terminal or 37-pin connector

Functional Details

USB-QUAD08 block diagram

USB-QUAD08 functions are illustrated in the block diagram shown here.

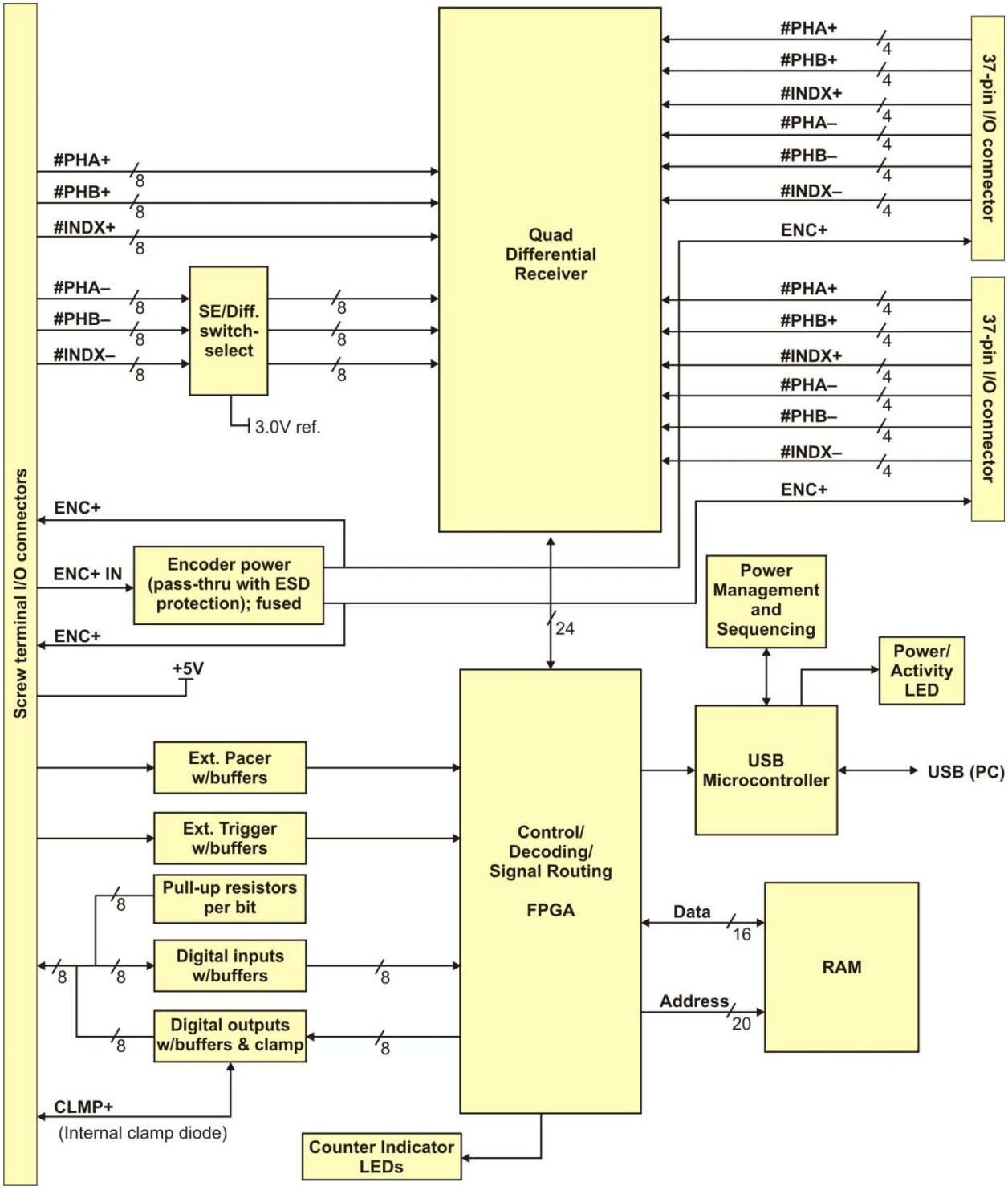
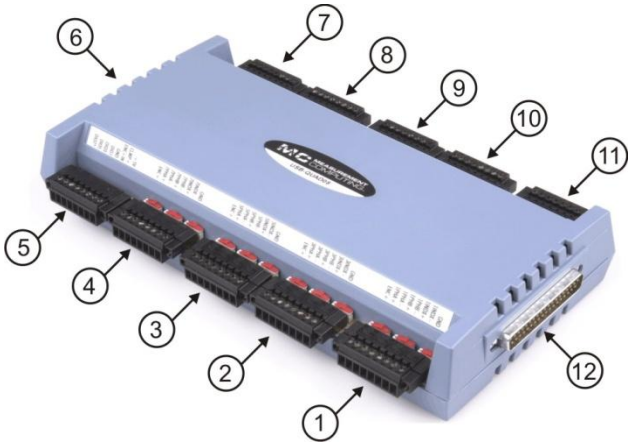


Figure 14. USB-QUAD08 functional block diagram

External components

The USB-QUAD08 has the following external components, as shown in Figure 15.

- 10 Screw terminal banks
- 37-pin I/O connector (J12)
- Device Power and Status LEDs
- USB connector
- Counter/encoder channel LEDs (not shown below, refer to Figure 2 on page 8 for each location)



1	Counter input 1 connections	7	DIO2, 4, 6, 8, trigger, pacer, and power connections
2	Counter input 3 connections	8	Counter input 6 connections
3	Counter input 5 connections	9	Counter input 4 connections
4	Counter input 7 connections	10	Counter input 2 connections
5	DIO1, 3, 5, 7, ENC+ IN, power connections	11	Counter input 0 connections
6	USB connector and LEDs (Figure 16)	12	37-pin I/O connector (J12)

Figure 15. USB-QUAD08 external components

The LEDs and USB connector locations are shown in Figure 16.

1	Power LED (top) and Status LED (bottom)	2	USB connector

Figure 16. Power/Status LEDs, USB connector (device left side)

Screw terminals

The device has ten banks of detachable screw terminals that provide the following connections:

- Eight encoder/counter inputs
- Eight DIO, or six DIO and two timer outputs
- Clamp for CEMF suppression
- External trigger input
- External pacer input
- External encoder power input
- Eight encoder power outputs
- Power outputs
- Ground

37-pin connectors (J12, J50)

The USB-QUAD08 has two 37-pin D-type connectors (J12 and J50). Each connector provides Phase A, B, and Index connections for up to four quadrature encoder inputs. Connector pinouts are shown 12.

Connector J12 is on the right side of the device (as shown in Figure 15 on page 18). Connector J50 is internal; you must remove the board from the housing to access connector J50.

LED indicators

The USB-QUAD08 has LEDs for power and communication status (see Figure 16). Additionally, each encoder/counter channel has an associated status LED adjacent to its screw terminal bank (see Figure 2 on page 8.)

- **Power** LED: indicates that the device microcontroller has power and is running.
- **Status** LED: indicates that the USB is configured; blinks to indicate USB traffic.
- **Channel** LEDs: indicates that the encoder/counter is receiving a valid signal on any of the inputs

USB connector

The USB connector provides +5 V power and communication.

Counter input modes

The USB-QUAD08 supports the following counter input modes:

- Counter – Quadrature or Totalize mode
- Period measurement
- Pulse-width measurement

Counter operation modes are programmable with software. Some modes make use of a user-configurable value called the MAXLIMIT value. This value doesn't directly affect the current count, but sets a limit used in some modes to determine counter behavior.

All counter modes use the phase A input. Some modes also make use of the phase B and Index inputs.

Each mode supports additional sub-modes for counter operations. Refer to the discussion of each counter mode in the pages that follow for specific information.

Quadrature counter mode

The USB-QUAD08 can simultaneously decode signals from up to eight encoders. Quadrature encoders with 16-bit, 32-bit, or 48-bit counters, 10 MHz maximum pulse frequency, and X1, X2, and X4 count modes are supported.

The USB-QUAD08 provides Phase A (±), Phase B (±), and Index (±) inputs for each encoder connected (0°, 90°, and zero). Phase A and Phase B are generated at a 90° phase shift with respect to each other. Phase A and B signals are used to determine system position (counts), velocity (counts per second), and direction of rotation. The Index signal can be programmed to gate, latch the current count, decrement, or clear/reload the counter with the MAXLIMIT value.

The Index signal may be used to establish an absolute reference position within one count of the encoder rotation (360°). This signal can be used to reload the position counter, which is useful at system startup when the incremental encoder cannot determine the starting position of the motor.

The Terminal count / MAXLIMIT status can be output to the DIO terminals.

Each input can be debounced from 500 ns to 25.5 ms (total of 16 selections) to eliminate extraneous noise, or to switch induced transients. Encoder input signals must be within –12 V to +12 V, and the switching threshold is 200 mV differential or 200 mV above 3.0 V and 50 mV, typical, hysteresis. Refer to page 22 for additional information about Debounce mode.

The following table lists the options supported in Quadrature mode.

Quadrature counter mode options

Counter mode	Description
Count mode	Select X1, X2, or X4. Count modes provide different levels of accuracy with respect to the encoder position. ▪ X1: counts rising edges on phase A (512 pulses). In X1 mode the encoder position is accurate to within 360° ÷ 512. ▪ X2: counts rising edges and falling edges on phase A (1024 pulses total). In X2 mode the encoder position is accurate to within 360 ° ÷ 1024. ▪ X4: count rising and falling edges on both phase A and phase B (1024 pulses on both phase A and phase B). In X2 mode the encoder position is accurate to within 360° ÷ 2048.
Range limit	When counting up: The counter stops when the maximum count (specified by the MAXLIMIT value) is reached. Counting resumes if direction is reversed or the counter is cleared. When counting down: The counter will count down to 0 and then stop. Counting resumes if direction is reversed or the counter is cleared.
Non-recycle	The counter is disabled if a count overflow or underflow occurs or the MAXLIMIT value is reached. A clear command (via software or Index input) is required to re-enable the counter.
Modulo-N	Counting up: When the maximum count (specified by the MAXLIMIT value) is reached, the counter rolls over to 0 and continues counting up. Counting down: When the count reaches 0, the counter rolls over to the maximum count (specified by the MAXLIMIT value) and continues counting down.

Quadrature mode options that are specific to the Index signal are listed below.

Index input mode options (Quadrature mode)

Counter mode	Description
Clear on Z	The counter is cleared on the rising edge of the Index signal.
Latching	Latching mode allows the count to be latched by the Index signal.

Totalize counter mode

The USB-QUAD08 can be used as a high speed pulse counter for general counting applications. The counters can concurrently monitor time periods, frequencies, pulses, and other event driven incremental occurrences directly from pulse-generators, limit switches, proximity switches, and magnetic pick-ups.

Each counter can be configured with software as a 16, 32, or 48-bit counter. The counters can accept frequency inputs up to 10 MHz.

In Totalize mode, phase A is used as the primary counter input. Phase B can be used to set the count direction in up/down counting— by default, the counter counts up when phase B is high (1), and counts down when phase B is low (0). The Index input can be used to gate, latch, decrement the counter, or clear/reload the counter with the MAXLIMIT value. Counter inputs can be read either asynchronously or synchronously as part of a digital scan group.

The following table lists the options supported in Totalize mode.

Totalize counter mode options

Counter mode	Description
Clear on read	The counter is cleared after each asynchronous read. The value of the counter before it was cleared is latched and returned.
Range limit	When counting up: The counter stops when the maximum count (specified by the MAXLIMIT value) is reached. Counting resumes if direction is reversed or the counter is reloaded. When counting down: The counter will count down to 0 and then stop. Counting resumes if direction is reversed or the counter is reloaded.
Non-recycle	The counter is disabled if a count overflow or underflow occurs or the MAXLIMIT value is reached. A clear command (via software or Index input) is required to re-enable the counter.

Counter mode	Description
Modulo-N	Counting up: When the maximum count (specified by the MAXLIMIT value) is reached, the counter rolls over to 0 and continues counting up. Counting down: When the count reaches 0, the counter rolls over to the maximum count (specified by the MAXLIMIT value) and continues counting down.
Up/down	Up/down counting mode uses phase A as the pulse source and phase B as the direction. By default, the counter counts up when phase B=1 (high), and counts down when phase B=0 (low).

Totalize mode options that are specific to the Index signal are listed below.

Index input mode options (Totalize mode)

Counter mode	Description
Gating	Gating mode allows the index input to gate the counter. By default, the counter is enabled when the Index signal is high. When the Index signal is low the counter is disabled, but holds the count value.
Latching	Latching mode allows the count to be latched by the Index signal.
Clear/Reload	Clear/Reload mode allows the Index signal to reload the counter with the MAXLIMIT value.
Decrement	Decrement mode allows the Index signal to decrement the counter.

Period measurement mode

Use period mode to measure the period of a signal at a counter channel's phase A input. You can measure x1, x10, x100 or x1000 periods, 16-bit, 32-bit, or 48-bit values. Four resolutions are available — 20.83 ns, 208.3 ns, 2.083 µs, or 20.83 µs. All period measurement mode options are software-selectable. The 48 MHz system clock is used as the timing source. Periods from sub-microsecond to many seconds can be measured.

Counter channel inputs are read synchronously using period mode.

Pulse width measurement mode

Use pulse width mode to measure the time from the rising edge to the falling edge, or vice versa, on a signal on a phase A counter input. Four resolutions are available (20.83 ns, 208.3 ns, 2.083 µs, or 20.83 µs). All pulse width measurement mode options are software selectable. The 48 MHz system clock is used as the timing source. Pulse widths from sub-microsecond to many seconds can be measured..

Counter channel inputs are read synchronously using pulse width mode.

Synchronous/asynchronous scanning

Counter inputs can be read asynchronously under program control, or synchronously as part of a digital scan group.

Synchronous scanning

When read synchronously, the count of each channel counter is set to 0 and latched at the beginning of the synchronous acquisition. Each clock pulse (*start-of-scan* signal) initiates a scan of all channels specified. Each time the USB-QUAD08 receives a *start-of-scan* signal, the counter values are latched and are available to the device. The values returned during scan period 1 are always zero. The values returned during scan period 2 reflect what happened during scan period 1. The scan period defines the timing resolution. To achieve a higher timing resolution shorten the scan period.

Use of terminal count outputs is not recommended in conjunction with synchronous reads

When scanning is initiated, the counters are reset to 0 and disarmed until the scan begins. This has the following affects on the terminal count outputs:

- The terminal count output timing is affected by the reset when scanning is initiated.

- When using an external trigger to initiate the synchronous acquisition, the counter is disarmed on all channels included in the scan until the trigger occurs.

- Reloading the MAXLIMIT register interrupts the TC outputs.

Asynchronous scanning

When read asynchronously, counters can be configured so that they get set to 0 after each read, count up or down repeatedly, or count until the 16, 32, 48-bit, or a user-set limit has been reached. Refer to the counter mode descriptions below.

Debounce mode

The USB-QUAD08 has debounce circuitry which eliminates switch-induced transients that are typically associated with electro-mechanical devices including relays, proximity switches, and encoders.

All debounce options are software selectable. You can select a debounce time, debounce mode, and rising-edge or falling-edge sensitivity. Each channel can be debounced with 16 programmable debounce times in the range of 500 ns to 25.5 ms.

Two debounce modes (*trigger after stable* and *trigger before stable*) and a debounce bypass are shown in Figure 17. The signal from the buffer can be inverted before it enters the debounce circuitry. The inverter is used to make the input rising-edge or falling-edge sensitive.

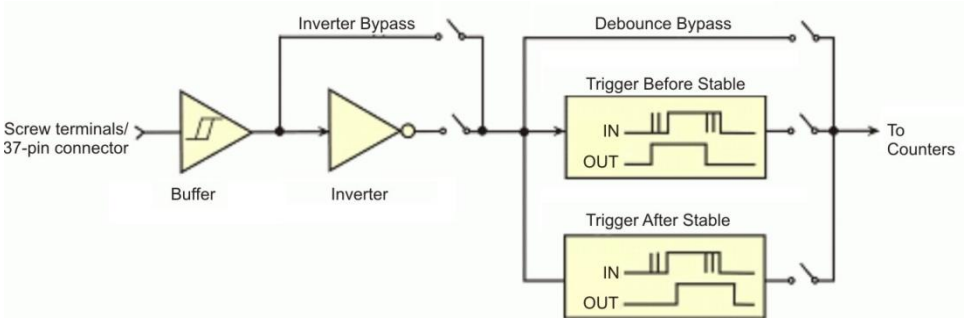


Figure 17. Debounce block diagram

Edge selection is available with or without debounce. In this case, the debounce time setting is ignored and the input signal goes straight from the inverter or inverter bypass to the counter module.

The two debounce modes are *trigger after stable* and *trigger before stable*. In either mode, the selected debounce time determines how fast the signal can change and still be recognized.

Trigger after stable mode

In the *trigger after stable* mode, the output of the debounce module does not change state until a period of stability has been achieved. This means that the input has an edge, and then must be stable for a period of time equal to the debounce time. Refer to Figure 18.

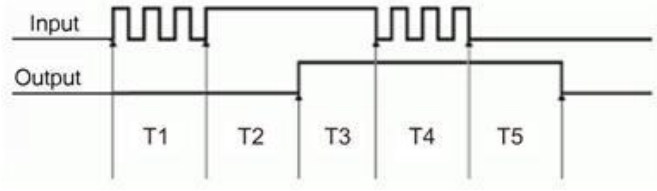


Figure 18. Trigger after stable mode

T1 through T5 indicate time periods. In trigger after stable mode, the input signal to the debounce module is required to have a period of stability after an incoming edge, in order for that edge to be accepted (passed through to the counter module.) For this example, the debounce time is equal to T2 and T5.

- T1 – In Figure 18, the input signal goes high at the beginning of time period T1, but never stays high for a period of time equal to the debounce time setting (equal to T2 for this example.)

- T2 – At the end of time period T2, the input signal has transitioned high and stayed there for the required amount of time—therefore the output transitions high. If the input signal does not stabilize in the high state long enough, no transition would have appeared on the output and the entire disturbance on the input would have been rejected.
- T3 – During time period T3, the input signal remained steady. No change in output is seen.
- T4 – During time period T4, the input signal has more disturbances and does not stabilize in any state long enough. No change in the output is seen.
- T5 – At the end of time period T5, the input signal has transitioned low and stayed there for the required amount of time—therefore the output goes low.

Trigger before stable mode

In the *trigger before stable* mode, the output of the debounce module immediately changes state, but will not change state again until a period of stability has passed. For this reason the mode can be used to detect glitches. Refer to Figure 19.

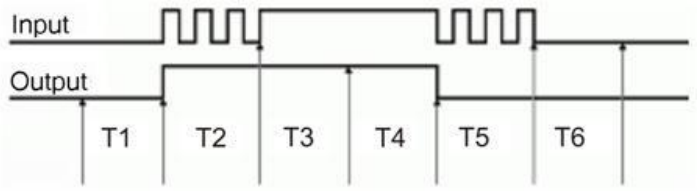


Figure 19. Trigger Before Stable mode

"T1" through "T5" in Figure 19 indicate time periods:

- T1 – The input signal is low for the debounce time (equal to T1); therefore when the input edge arrives at the end of time period T1, it is accepted and the output (of the debounce module) goes high. Note that a period of stability must precede the edge in order for the edge to be accepted.
- T2 – During time period T2, the input signal is not stable for a length of time equal to T1 (the debounce time setting for this example.) Therefore, the output stays "high" and does not change state during time period T2.
- T3 – During time period T3, the input signal is stable for a time period equal to T1, meeting the debounce requirement. The output is held at the high state. This is the same state as the input.
- T4 – At anytime during time period T4, the input can change state. When this happens, the output will also change state. At the end of time period T4, the input changes state, going low, and the output follows this action [by going low].
- T5 – During time period T5, the input signal again has disturbances that cause the input to not meet the debounce time requirement. The output does not change state.
- T6 – After time period T6, the input signal has been stable for the debounce time and therefore any edge on the input after time period T6 is immediately reflected in the output of the debounce module.

Debounce mode comparisons

Figure 20 shows how the two modes interpret the same input signal, which exhibits glitches. Notice that the *trigger before stable* mode recognizes more glitches than the *trigger after stable* mode. Use the **bypass** option to achieve maximum glitch recognition.

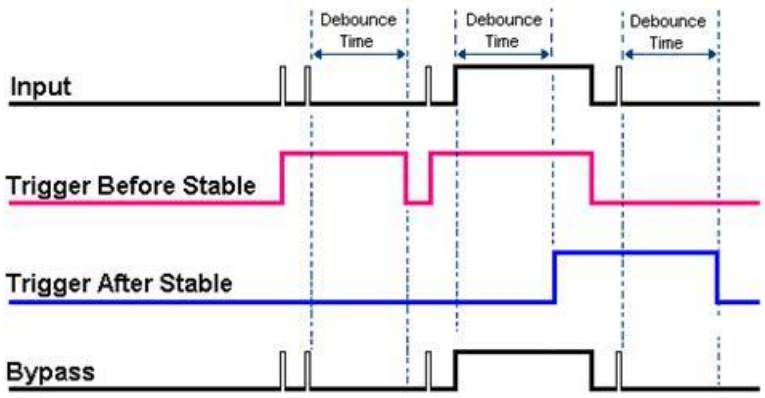


Figure 20. Example of two debounce modes interpreting the same signal

Set the debounce time according to the amount of instability expected in the input signal. Setting a debounce time that is too short may result in unwanted glitches clocking the counter. Setting a debounce time that is too long may result in an input signal being rejected entirely. Some experimentation may be required to find the appropriate debounce time for a particular application.

To see the effects of different debounce time settings, view the analog waveform along with the counter output. This can be done by connecting the source to an analog input.

Use *trigger before stable* mode when the input signal has groups of glitches and each group is to be counted as one. The trigger before stable mode recognizes and counts the first glitch within a group but rejects the subsequent glitches within the group if the debounce time is set accordingly. Set the debounce time to encompass one entire group of glitches, as shown in Figure 21.

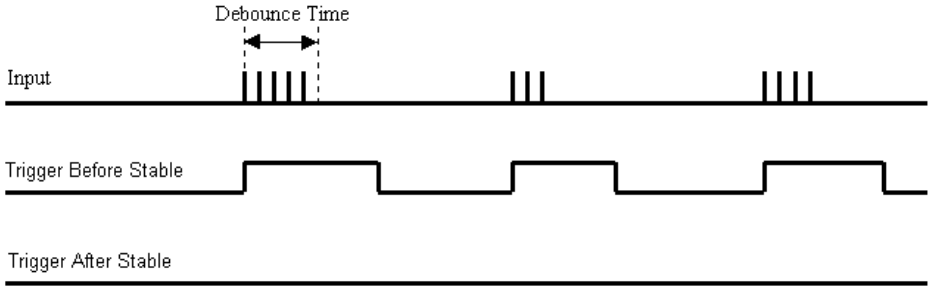


Figure 21. Optimal debounce time for "trigger before stable" mode

Trigger after stable mode behaves more like a traditional debounce function: rejecting glitches and only passing state transitions after a required period of stability. *Trigger after stable* mode is used with electro-mechanical devices like encoders and mechanical switches to reject switch bounce and disturbances due to a vibrating encoder that is not otherwise moving.

The debounce time should be set short enough to accept the desired input pulse but longer than the period of the undesired disturbance, as shown in Figure 22.

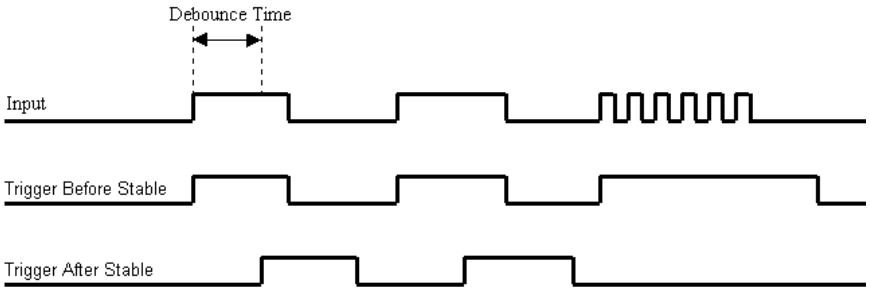


Figure 22. Optimal debounce time for "trigger after stable" mode

Digital I/O

You can connect up to eight digital IO lines to the **DIO0** to **DIO7** screw terminals. Each digital bit can be independently configured as a digital input, a digital output, or as a terminal count output for the corresponding counter channel. In addition, DIO6 and DIO7 can be configured as timer outputs with variable pulse width. When a digital channel is configured for terminal count or timer output, it cannot be used for DIO functions.

Digital input

Digital bits configured for input can accept high voltage inputs up to 42.4 V_{pk} or 50 VDC. The digital inputs are pulled high at power-up with a 10 kΩ series resistor to +5V with diode protection. This allows higher voltage inputs from the sourcing current to the USB-QUAD08. Digital input bits are read asynchronously.

Digital output

Digital bits configured for output are open collector with an inductive diode clamped to the **CLMP+** terminal for CEMF (counter electromotive force) suppression. DO bits can withstand 50 volts, and can operate via software control (asynchronous). The asynchronous digital output throughput is 4000 updates/second, typical.

Terminal count output

When used as terminal count outputs, **DIO0** to **DIO7** indicate the count status for each corresponding counter channel. The output state will go high for the period of time that the count is equal to the terminal count value or the values specified as the MAXLIMIT.

For example, assume DIO0 is set for terminal count output. If counter 0 is configured for Range limit mode with MAXLIMIT set to 4,096, the output of DIO0 will go high when the count reaches 4,096 (counting up) or 0 (counting down). The output remains high until counting resumes, either by a direction change or by a counter reload.

Similarly, if configured for Modulo-N counting, the same behavior applies except that a reset or direction change is not required to change the output state, since this mode rolls over when the MAXLIMIT value is reached. Once the count moves off of MAXLIMIT (counting up) or 0 (counting down), the terminal count output will go low.

Timer output

You can use **DIO6** and **DIO7** as 16-bit timer outputs. Each timer can generate a programmable pulse width wave with a programmable frequency in the range of 0. 01123 Hz to 5 MHz. At higher frequencies, the timer output frequency and duty cycle are dependent on the load impedance and the supply (refer to Driving digital outputs on page 26 for more information). The duty cycle is programmable.

The timer output rate and pulse width can be updated asynchronously at any time, however, doing so results in a pulse stream that is not seamless.

Driving digital outputs

The outputs are open-collector, effectively sinking current. The USB-QUAD08 has weak 10 kΩ resistors pulled up to +5V with over-voltage protection. Using this default configuration may not provide adequate drive for your application.

If minimum current is required, install a 250 Ω resistor from a digital output bit sinking from a +5V terminal. Do not exceed 20 mA.

If a stronger drive strength is required, use an external supply with a series resistor up to 500 mA load per digital output pin. Do not exceed 2.5 A for the device.

Counter-electro-motive force (CEMF) suppression

Counter-electromotive force is the voltage, or electromotive force, that is induced into an inductor due to an alternating or pulsating current. CEMF is caused by a changing electromagnetic field, and is always in polarity opposite to that of the applied voltage. The USB-QUAD08 provides a **CLMP+** screw terminal to suppress CEMF. For CEMF protection, attach an external supply to the **CLMP+** terminal directly — do not install the supply after the series resistor.

Caution! Each output can sink up to 500 mA. Ensure that the entire device (up to 5 outputs) sinks less than 2.5 A. Alternately, all outputs can sink 300 mA.

Figure 23 below shows the digital output/timer output circuit.

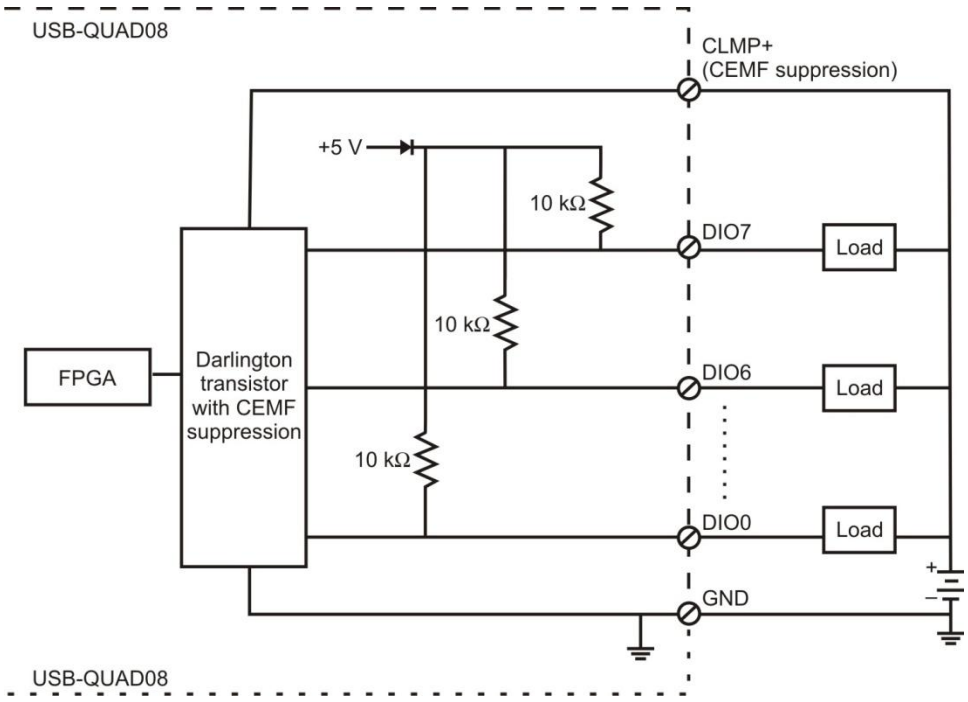


Figure 23. Digital/timer output channel circuit

Triggering

You can trigger a synchronous acquisition of counter data internally with software or externally using the **XTRIG** digital trigger input screw terminal.

The **XTRIG** input allows TTL-level triggering with latencies guaranteed to be less than 1 µs. The acquisition can be triggered on a rising or falling edge, or on a high or low level. The trigger input is TTL logic . Latency is one sample period, maximum. The input signal range is –0.5 V to 7 V maximum. The logic level (1 or 0) and the rising or falling edge for the discrete trigger input are software selectable.

Pacing

You can pace synchronous acquisition of counter data by the onboard clock or by an external clock connected to the **XPCR** external pacer input terminal.

Power

The total supply current at the +5V terminal is 480 mA, maximum, including DIO. The total supply current shared between the +5V terminals is 20 mA, maximum.

You can use the +5V terminal to supply power to external devices or circuitry.

Caution! The +5V terminals are outputs. Do not connect to an external power supply or you may damage the USB-QUAD08 and possibly the computer.

The maximum total output current that can be drawn from all USB-QUAD08 connections (power, analog, and digital outputs) is 480 mA. This maximum applies to most personal computers and self-powered USB hubs. Bus-powered hubs and notebook computers may limit the maximum available output current to 100 mA.

The total current requirements of the USB-QUAD08 is 225 mA, typical. The maximum available excess current is the difference between the allowed current draw of the computer platform and the total output current requirement of the device. For an application running on a computer or powered hub, the maximum available excess current at the +5V screw terminals is calculated as follows:

Maximum excess current = 480 mA – 225 mA = 255 mA

If the current requirement of the device exceeds the current available from the computer, connect to a self-powered hub or power the computer with an external power adapter.

Encoder power

When operating in Quadrature counter mode, the USB-QUAD08 passes an external supply of up to 50 VDC (current rated 1.5 A @ 5 VDC) through the **ENC+ IN** encoder input power terminal to the **ENC+** encoder power output terminals. Each **ENC+** terminal provides power to one encoder.

When operating in normal counter mode, the **ENC+ IN** and **ENC** terminals provide no function.

Ground

The ground (**GND**) connections provide a common ground for the digital, counter, and power connections.

Caution! Ensure that the signals are connected such that there is no potential between PC ground and signal ground.

Mechanical Drawings

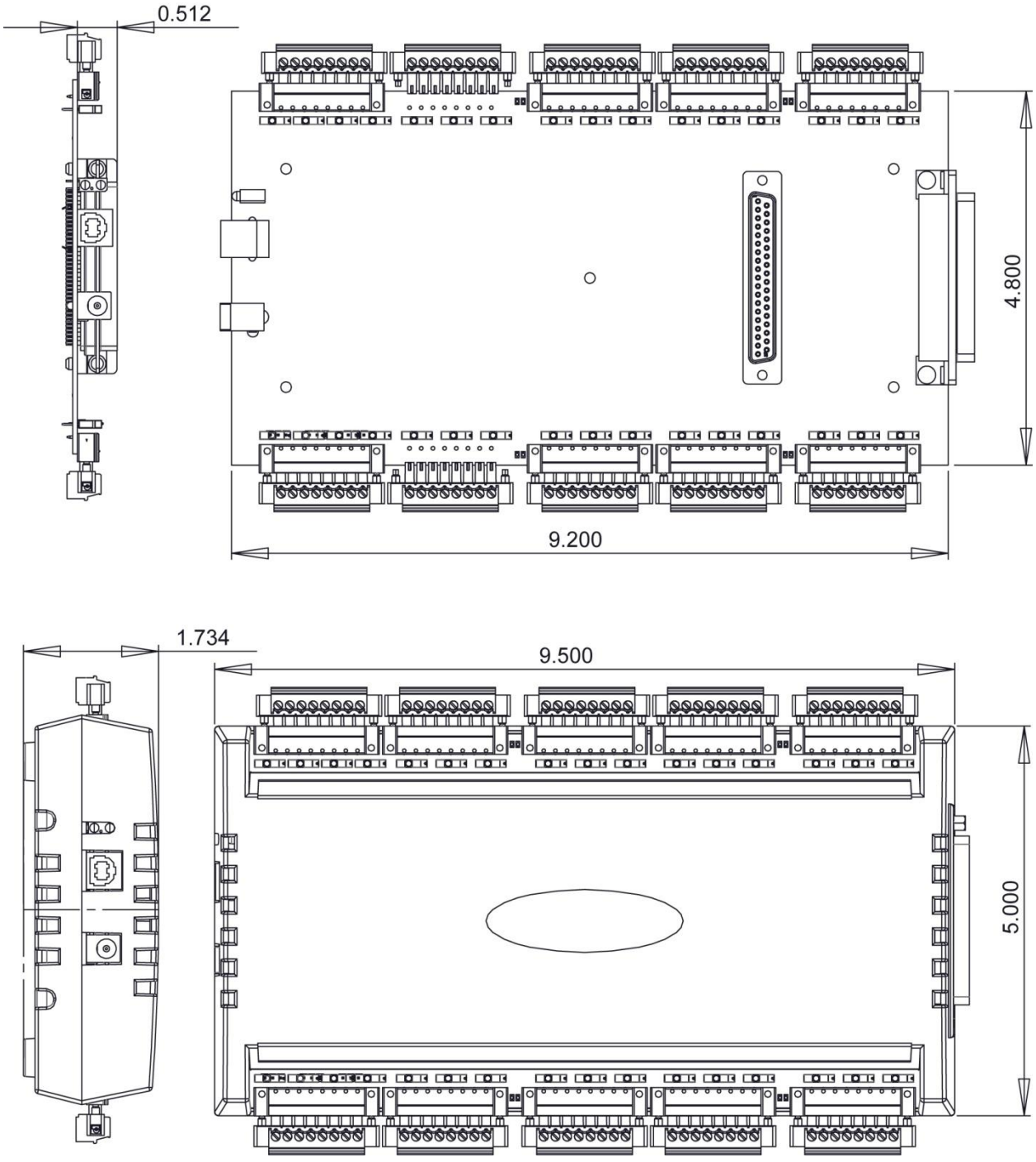


Figure 24. USB-QUAD08 circuit board (top) and enclosure dimensions

Specifications

All specifications are subject to change without notice.
Typical for 25 °C unless otherwise specified.
Specifications in *italic text* are guaranteed by design.

Counter

Table 1. Counter specifications

Parameter	Specification
Counter type	FPGA
Counters	8 (quadrature or normal)
Counter input modes	Quadrature (x1, x2, x4)/Totalize, Pulse width, Period
Mode options	Non-Recycle, Range Limit, Clear on Read, Modulo-N, Up/Down, Decrement
Index options	Latch, Clear|Reload, Decrement, Gate; mode dependent.
Resolution	16, 32 or 48-bit counters
Quadrature mode input frequency	10/5/2.5 MHz, max, in x1/x2/x4
Normal mode input frequency	10 MHz, max
De-bounce times	16 steps from 500 ns to 25 ms; positive or negative edge sensitive; glitch detect mode or de-bounce mode; software-selectable.
Time-base and accuracy	48 MHz (24 MHz – 30 ppm with a 2xDLL (delay locked loop))
Counter read pacer	Internal or external scan pacer up to 8 MHz
Period/pulse width resolution	20.83 ns; 208.3 ns; 2.083 µs; or 20.83 µs

Input

Table 2. Input specifications

Parameter	Specification
Receiver type	SN75ALS175 quad differential receiver
Configuration	8 channels. Each channel consists of PhaseA input, PhaseB input and Index input; each input is selectable as single-ended or differential.
	Differential: ▪ PhaseA, PhaseB and Index (+) inputs at the user connector are routed to the (+) inputs of differential receiver. ▪ PhaseA, PhaseB and Index (–) inputs at the user connector are routed to the (–) inputs of the differential receiver.
	Single-ended: ▪ PhaseA, PhaseB and Index (+) inputs at the user connector are routed to the (+) inputs of the differential receiver. ▪ PhaseA, PhaseB and Index (–) inputs at the user connector are left floating. The (–) inputs of the differential receiver are routed to the +3 V reference.
Common mode input voltage range	*±12 V*
Differential input voltage range	*±12 V*
Input sensitivity	*±200 mV*
Input hysteresis	*50 mV, typ*
Input impedance	*12 kΩ, min*
Absolute maximum input voltage	*±14 V, max*
Miscellaneous	▪ *Meets or exceeds ANSI EIA/TIA-422-B, EIA/TIA-423-B, RS-485.* ▪ *Meets ITU recommendations V.10, V.11, X.26, X.27.* ▪ *Designed for multipoint busses on long lines and in noisy environments.*

Digital I/O – Timer outputs – Terminal count outputs

Table 3. Output specifications

Parameter	Specification
Number of I/O	8 independent
Configurable	Timer outputs (DIO6, DIO7 only), Terminal count/Modulo, Input/Output (default)
Input:	
Input characteristics	Weak 10 kΩ resistor pulled-up to 5V with protection diode (+V_{USB} – diode drop).
Input high	*+2.0 V to 42.4 V_{pk} 50 VDC*
Input low	*0 V to 0.8 V*
Output:	
Output characteristics	Open-collector Darlington transistors with CEMF suppression diodes (ULN2803)
Output logic supply	User voltage supply up to 50 VDC (42.4 V_{pk}) for strong drive.
CEMF Supply (CLMP+)	Connect to logic supply positive terminal up to *50 VDC (42.4 V_{pk})*
Output high	*2.0 VDC to 50 VDC (42.4 V_{pk}); dependent upon logic supply.*
Output low	<0.8 V
Output sink current	*500 mA per pin, 2.5 A max. per device* (parallel connections for higher current needs) requires external supply.
Output generation	Counter events or timer outputs (bits 6 and 7); asynchronous generation
Asynchronous throughput	4000 updates/second, typ (tested on Windows XP and Windows Vista32)
Timer outputs:	
Number of channels	Two 16-bit ▪ Timer Output 0 (DIO6) ▪ Timer Output 1 (DIO7)
Effective frequency range	0.01123 Hz to 5 MHz

Trigger and pacer

Table 4. Trigger and pacer specifications

Parameter	Specification
Digital type	Edge/level sensitive; software-selectable.
Trigger types	Start acquisition process
Pacer	Latch counter values for read back
Trigger and pacer inputs	▪ Internal (software) ▪ External
Trigger and pacer input	–0.5 V to 7.0 V
External pacer frequency	8 MHz, max

Indicator LEDs

Table 5. LED specifications

Parameter	Specification
Power LED	Indicates that the device's microcontroller has power and is running.
Status LED	Indicates that the USB is configured; blinks to indicate USB traffic.
Channel LEDs	Indicates that the encoder/counter is receiving a valid signal on any of the inputs.

Power

Table 6. Power specifications

Parameter	Condition	Specification
V_{USB} (+5V) (Note 1)	▪ Connected to self-powered hub ▪ Connected to externally-powered root port hub	4.5 V to 5.25 V 480 mA max; 225 mA typ
V_{USER} (+5V) current	4.5 V to 5.25 V; 20 mA max	
Encoder supply	External supply of 1.5 A @ 5 VDC fused up to 42.4 V_{pk} (50 V_{DC}) @ 2 A Protection diodes (30BQ060, 0.5V_{max} drop) protecting against reverse polarity.	
Encoder supply fuse	0452002. - Littelfuse 2A NANO2® Slo-Blo® Subminiature Surface Mount Fuse	

Note 1: "Self-powered hub" refers to a USB hub with an external power supply. Self-powered hubs allow a connected USB device to draw up to 500 mA. "Root port hubs" reside in the PC USB host Controller. The USB port(s) on your PC are root port hubs. All externally-powered root port hubs (desktop PC) provide up to 500 mA of current for a USB device. Battery-powered root port hubs provide 100 mA or 500 mA, depending upon the manufacturer. A laptop PC that is not connected to an external power adapter is an example of a battery-powered root port hub. If your laptop PC is constrained to the 100 mA max, use a self-powered hub.

Environmental

Table 7. Environmental specifications

Parameter	Specification
Operating temperature range	0 °C to 60 °C
Storage temperature range	–40 °C to 85 °C
Humidity	0% to 90% non-condensing

Mechanical

Table 8. Mechanical specifications

Parameter	Specification
Dimensions (L × W × H)	245 × 146 × 50 mm (9.6 × 5.7 × 2.0 in.)

USB specifications

Table 9. USB specifications

Parameter	Specification
Device type	USB 2.0 high-speed mode (480 Mbps) if available (recommended), otherwise, USB 1.1 full-speed mode (12 Mbps)
Device compatibility	USB 2.0 (recommended) or USB 1.1
USB cable type	*A-B cable, UL type AWM 2725 or equivalent. (min 24 AWG VBUS/GND, min 28 AWG D+/D–)*
USB cable length	3 meters, max (9.84 feet)

I/O connectors

Table 10. I/O Connector specifications

Parameter	Specification
Connector type	▪ Screw terminals: 10 banks; detachable ▪ 37-pin D type: J12(external) and J50 (internal)
Wire gauge range for screw terminals	16 AWG to 28 AWG
Compatible cable with the 37-pin connectors	C37F-4X9F-1M C37FF-x C37FFS-x
Compatible accessory products with the 37-pin connectors	SCB-37 CIO-MINI37 CIO-MINI37/DST CIO-MINI37-VERT CIO-MINI37-VERTDST CIO-TERMINAL

Screw terminal connectors

Table 11. Differential mode pinout

Signal name	Terminal description	Signal name	Terminal description
ENC+	Encoder power output (Note 2)	GND	Ground
0PHA+	Counter 0 Phase A high	1INDX–	Counter 1 Phase A high
0PHA–	Counter 0 Phase A low	1INDX+	Counter 1 Phase A low
0PHB+	Counter 0 Phase B high	1PHB–	Counter 1 Phase B high
0PHB–	Counter 0 Phase B low	1PHB+	Counter 1 Phase B low
0INDX+	Counter 0 Index high	1PHA–	Counter 1 Index high
0INDX–	Counter 0 Index low	1PHA+	Counter 1 Index low
GND	Ground	ENC+	Encoder power output (Note 2)
ENC+	Encoder power output (Note 2)	GND	Ground
2PHA+	Counter 2 Phase A high	3INDX–	Counter 3 Phase A high
2PHA–	Counter 2 Phase A low	3INDX+	Counter 3 Phase A low
2PHB+	Counter 2 Phase B high	3PHB–	Counter 3 Phase B high
2PHB–	Counter 2 Phase B low	3PHB+	Counter 3 Phase B low
2INDX+	Counter 2 Index high	3PHA–	Counter 3 Index high
2INDX–	Counter 2 Index low	3PHA+	Counter 3 Index low
GND	Ground	ENC+	Encoder power output (Note 2)
ENC+	Encoder power output (Note 2)	GND	Ground
4PHA+	Counter 4 Phase A high	5INDX–	Counter 5 Phase A high
4PHA–	Counter 4 Phase A low	5INDX+	Counter 5 Phase A low
4PHB+	Counter 4 Phase B high	5PHB–	Counter 5 Phase B high
4PHB–	Counter 4 Phase B low	5PHB+	Counter 5 Phase B low
4INDX+	Counter 4 Index high	5PHA–	Counter 5 Index high
4INDX–	Counter 4 Index low	5PHA+	Counter 5 Index low
GND	Ground	ENC+	Encoder power output (Note 2)
ENC+	Encoder power output (Note 2)	GND	Ground
6PHA+	Counter 6 Phase A high	7INDX–	Counter 7 Phase A high
6PHA–	Counter 6 Phase A low	7INDX+	Counter 7 Phase A low
6PHB+	Counter 6 Phase B high	7PHB–	Counter 7 Phase B high
6PHB–	Counter 6 Phase B low	7PHB+	Counter 7 Phase B low
6INDX+	Counter 6 Index high	7PHA–	Counter 7 Index high
6INDX–	Counter 6 Index low	7PHA+	Counter 7 Index low
GND	Ground	ENC+	Encoder power output (Note 2)
+5V	Power output	+5V	Power output
XTRIG	External trigger input	CLMP+	CEMF protection for DIO (Note 5)
XPCR	External pacer input	ENC+ IN	Encoder power input(Note 2)
GND	Ground	GND	Ground
DIO0	DIO channel 0	DIO1	DIO channel 1
DIO2	DIO channel 2	DIO3	DIO channel 3
DIO4	DIO channel 4	DIO5	DIO channel 5
DIO6*	DIO channel 6 (Note 3)	DIO7*	DIO channel 7 (Note 4)

Note 2: External supply when operating in encoder mode. ENC+ IN is passed to all ENC+ lines with optional protection diodes to prevent reverse connection.

Note 3: DIO6 can also function as Timer Output 0.

Note 4: DIO7 can also function as Timer Output 1.

Note 5: CEMF protection to the DIO supply; it is not a source.

Table 12. Single-ended mode pinout

Signal name	Terminal description	Signal name	Terminal description
ENC+	Encoder power output (Note 6)	GND	Ground
0PHA+	Counter 0 Phase A	1INDX–	Floating (Note 7)
0PHA–	Floating (Note 7)	1INDX+	Counter 1 Phase A
0PHB+	Counter 0 Phase B	1PHB–	Floating (Note 7)
0PHB–	Floating (Note 7)	1PHB+	Counter 1 Phase B
0INDX+	Counter 0 Index	1PHA–	Floating (Note 7)
0INDX–	Floating (Note 7)	1PHA+	Counter 1 Index
GND	Ground	ENC+	Encoder power output (Note 6)
ENC+	Encoder power output (Note 6)	GND	Ground
2PHA+	Counter 2 Phase A	3INDX–	Floating (Note 7)
2PHA–	Floating (Note 7)	3INDX+	Counter 3 Phase A
2PHB+	Counter 2 Phase B	3PHB–	Floating (Note 7)
2PHB–	Floating (Note 7)	3PHB+	Counter 3 Phase B
2INDX+	Counter 2 Index	3PHA–	Floating (Note 7)
2INDX–	Floating (Note 7)	3PHA+	Counter 3 Index
GND	Ground	ENC+	Encoder power output (Note 6)
ENC+	Encoder power output (Note 6)	GND	Ground
4PHA+	Counter 4 Phase A	5INDX–	Floating (Note 7)
4PHA–	Floating (Note 7)	5INDX+	Counter 5 Phase A
4PHB+	Counter 4 Phase B	5PHB–	Floating (Note 7)
4PHB–	Floating (Note 7)	5PHB+	Counter 5 Phase B
4INDX+	Counter 4 Index	5PHA–	Floating (Note 7)
4INDX–	Floating (Note 7)	5PHA+	Counter 5 Index
GND	Ground	ENC+	Encoder power output (Note 6)
ENC+	Encoder power output (Note 6)	GND	Ground
6PHA+	Counter 6 Phase A	7INDX–	Floating (Note 7)
6PHA–	Floating (Note 7)	7INDX+	Counter 7 Phase A
6PHB+	Counter 6 Phase B	7PHB–	Floating (Note 7)
6PHB–	Floating (Note 7)	7PHB+	Counter 7 Phase B
6INDX+	Counter 6 Index	7PHA–	Floating (Note 7)
6INDX–	Floating (Note 7)	7PHA+	Counter 7 Index low
GND	Ground	ENC+	Encoder power output (Note 6)
+5V	Power output	+5V	Power output
XTRIG	External trigger input	CLMP+	CEMF protection for DIO (Note 10)
XPCR	External pacer input	ENC+ IN	Encoder power input (Note 6)
GND	Ground	GND	Ground
DIO0	DIO channel 0	DIO1	DIO channel 1
DIO2	DIO channel 2	DIO3	DIO channel 3
DIO4	DIO channel 4	DIO5	DIO channel 5
DIO6*	DIO channel 6 (Note 8)	DIO7*	DIO channel 7 (Note 9)

Note 6: External supply when operating in encoder mode. ENC+ IN is passed to all ENC+ lines with optional protection diodes to prevent reverse connection.

Note 7: In single-ended mode, the PhaseA, PhaseB and Index (–) inputs at the user connector are left floating. The (–) inputs of the differential receiver are routed to +3 V reference.

Note 8: DIO6 can also function as Timer Output 0.

Note 9: DIO7 can also function as Timer Output 1.

Note 10: CEMF protection to the DIO supply; it is not a source.

37-pin connectors

J12

Table 13. Differential mode pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	0PHA –	Counter 0 Phase A low	20	0PHA+	Counter 0 Phase A high
2	ENC+	Encoder power output	21	0PHB+	Counter 0 Phase B high
3	0PHB–	Counter 0 Phase B low	22	GND	Ground
4	ENC+	Encoder power output	23	0INDX+	Counter 0 Index high
5	0INDX–	Counter 0 Index low	24	2INDX–	Counter 2 Index low
6	NC	No connection	25	2PHA+	Counter 2 Phase A high
7	2PHA–	Counter 2 Phase A low	26	2PHB+	Counter 2 Phase B high
8	ENC+	Encoder power output	27	GND	Ground
9	2PHB–	Counter 2 Phase B low	28	2INDX+	Counter 2 Index high
10	ENC+	Encoder power output	29	3INDX–	Counter 3 Index low
11	3PHA–	Counter 3 Phase A low	30	3PHA+	Counter 3 Phase A high
12	ENC+	Encoder power output	31	3PHB+	Counter 3 Phase B high
13	3PHB–	Counter 3 Phase B low	32	GND	Ground
14	ENC+	Encoder power output	33	3INDX+	Counter 3 Index high
15	1PHA–	Counter 1 Phase A low	34	1PHA+	Counter 1 Phase A high
16	ENC+	Encoder power output	35	1PHB+	Counter 1 Phase B high
17	1PHB–	Counter 1 Phase B low	36	GND	Ground
18	ENC+	Encoder power output	37	1INDX+	Counter 1 Index high
19	1INDX–	Counter 1 Index low			

Table 14. Single-ended mode pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	0PHA –	Floating (Note 11)	20	0PHA+	Counter 0 Phase A
2	ENC+	Encoder power output	21	0PHB+	Counter 0 Phase B
3	0PHB–	Floating (Note 11)	22	GND	Ground
4	ENC+	Encoder power output	23	0INDX+	Counter 0 Index
5	0INDX–	Floating (Note 11)	24	2INDX–	Floating (Note 11)
6	NC	No connection	25	2PHA+	Counter 2 Phase A
7	2PHA–	Floating (Note 11)	26	2PHB+	Counter 2 Phase B
8	ENC+	Encoder power output	27	GND	Ground
9	2PHB–	Floating (Note 11)	28	2INDX+	Counter 2 Index
10	ENC+	Encoder power output	29	3INDX–	Floating (Note 11)
11	3PHA–	Floating (Note 11)	30	3PHA+	Counter 3 Phase A
12	ENC+	Encoder power output	31	3PHB+	Counter 3 Phase B
13	3PHB–	Floating (Note 11)	32	GND	Ground
14	ENC+	Encoder power output	33	3INDX+	Counter 3 Index high
15	1PHA–	Floating (Note 11)	34	1PHA+	Counter 1 Phase A
16	ENC+	Encoder power output	35	1PHB+	Counter 1 Phase B
17	1PHB–	Floating (Note 11)	36	GND	Ground
18	ENC+	Encoder power output	37	1INDX+	Counter 1 Index
19	1INDX–	Floating (Note 11)			

Note 11: In single-ended mode, the PhaseA, PhaseB and Index (–) inputs at the user connector are left floating. The (–) inputs of the differential receiver are routed to +3 V reference.

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Table 15. Differential mode pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	4PHA –	Counter 4 Phase A low	20	4PHA+	Counter 4 Phase A high
2	ENC+	Encoder power output	21	4PHB+	Counter 4 Phase B high
3	4PHB–	Counter 4 Phase B low	22	GND	Ground
4	ENC+	Encoder power output	23	4INDX+	Counter 4 Index high
5	4INDX–	Counter 4 Index low	24	6INDX–	Counter 6 Index low
6	NC	No connection	25	6PHA+	Counter 6 Phase A high
7	6PHA–	Counter 6 Phase A low	26	6PHB+	Counter 6 Phase B high
8	ENC+	Encoder power output	27	GND	Ground
9	6PHB–	Counter 6 Phase B low	28	6INDX+	Counter 6 Index high
10	ENC+	Encoder power output	29	7INDX–	Counter 7 Index low
11	7PHA–	Counter 7 Phase A low	30	7PHA+	Counter 7 Phase A high
12	ENC+	Encoder power output	31	7PHB+	Counter 7 Phase B high
13	7PHB–	Counter 7 Phase B low	32	GND	Ground
14	ENC+	Encoder power output	33	7INDX+	Counter 7 Index high
15	5PHA–	Counter 5 Phase A low	34	5PHA+	Counter 5 Phase A high
16	ENC+	Encoder power output	35	5PHB+	Counter 5 Phase B high
17	5PHB–	Counter 5 Phase B low	36	GND	Ground
18	ENC+	Encoder power output	37	5INDX+	Counter 5 Index high
19	5INDX–	Counter 5 Index low			

Table 16. Single-ended mode pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	4PHA –	Floating (Note 12)	20	4PHA+	Counter 4 Phase A
2	ENC+	Encoder power output	21	4PHB+	Counter 4 Phase B
3	4PHB–	Floating (Note 12)	22	GND	Ground
4	ENC+	Encoder power output	23	4INDX+	Counter 4 Index
5	4INDX–	Floating (Note 12)	24	6INDX–	Floating (Note 12)
6	NC	No connection	25	6PHA+	Counter 6 Phase A
7	6PHA–	Floating (Note 12)	26	6PHB+	Counter 6 Phase B
8	ENC+	Encoder power output	27	GND	Ground
9	6PHB–	Floating (Note 12)	28	6INDX+	Counter 6 Index
10	ENC+	Encoder power output	29	7INDX–	Floating (Note 12)
11	7PHA–	Floating (Note 12)	30	7PHA+	Counter 7 Phase A
12	ENC+	Encoder power output	31	7PHB+	Counter 7 Phase B
13	7PHB–	Floating (Note 12)	32	GND	Ground
14	ENC+	Encoder power output	33	7INDX+	Counter 7 Index
15	5PHA–	Floating (Note 12)	34	5PHA+	Counter 5 Phase A
16	ENC+	Encoder power output	35	5PHB+	Counter 5 Phase B
17	5PHB–	Floating (Note 12)	36	GND	Ground
18	ENC+	Encoder power output	37	5INDX+	Counter 5 Index
19	5INDX–	Floating (Note 12)			

Note 12: In single-ended mode, the PhaseA, PhaseB and Index (–) inputs at the user connector are left floating. The (–) inputs of the differential receiver are routed to +3 V reference.

CE Declaration of Conformity

Manufacturer:	Measurement Computing Corporation
Address:	10 Commerce Way Suite 1008 Norton, MA 02766 USA
Category:	Electrical equipment for measurement, control and laboratory use.

Measurement Computing Corporation declares under sole responsibility that the product

USB-QUAD08

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EC EMC Directive 2004/108/EC: General Requirements, EN 61326-1:2006 (IEC 61326-1:2005).

Emissions:

- EN 55011 (2007) / CISPR 11(2003): Radiated emissions: Group 1, Class A
- EN 55011 (2007) / CISPR 11(2003): Conducted emissions: Group 1, Class A

Immunity: EN 61326-1:2006, Table 3.

- IEC 61000-4-2 (2001): Electrostatic Discharge immunity.
- IEC 61000-4-3 (2002): Radiated Electromagnetic Field immunity.

To maintain compliance to the standards of this declaration, the following conditions must be met.

- The host computer, peripheral equipment, power sources, and expansion hardware must be CE compliant.
- All I/O cables must be shielded, with the shields connected to ground.
- I/O cables must be less than 3 meters (9.75 feet) in length.
- The host computer must be properly grounded.
- The host computer must be USB 2.0 compliant.
- Equipment must be operated in a controlled electromagnetic environment as defined by Standards EN 61326-1:2006, or IEC 61326-1:2005.

Note: Data acquisition equipment may exhibit noise or increased offsets when exposed to high RF fields (>1V/m) or transients.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in May, 2009. Test records are outlined in Chomerics Test Report #EMI5334.09.

We hereby declare that the equipment specified conforms to the above Directives and Standards.

Carl Haapaoja, Director of Quality Assurance

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