USB-1602HS-2AO

Multifunction Synchronous Data Acquisition Board

User's Guide

MEASUREMENT COMPUTING™

USB-1602HS-2AO

Multifunction Synchronous Data Acquisition Board

User's Guide

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Table of Contents

About this User's Guide

What you will learn from this user's guide

This user's guide explains how to install, configure, and use the USB-1602HS-2AO so that you get the most out of its synchronous data acquisition features.

This user's guide also refers you to related documents available on our web site, and to technical support resources.

Conventions in this user's guide

For more information on …

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

<#:#> Angle brackets that enclose numbers separated by a colon signify a range of numbers, such as those assigned to registers, bit settings, etc.

bold text **Bold** text is used for the names of objects on the screen, such as buttons, text boxes, and check boxes. For example:
1. Insert the disk or CD and click the **OK** button.

italic text *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase. For example:
The *InstaCal* installation procedure is explained in the Quick Start Guide.
Never touch the exposed pins or circuit connections on the board.

Where to find more information

For additional information relevant to the operation of your hardware, refer to the Documents subdirectory where you installed the MCC DAQ software (C:\Program Files\Measurement Computing\DAQ by default), or search for your device on our website at www.mccdaq.com.

Introducing the USB-1602HS-2AO

Overview: USB-1602HS-2AO features

The USB-1602HS-2AO is a multifunction high-speed measurement and control board supported under popular Microsoft® Windows® operating systems. The device is compatible with both USB 1.1 and USB 2.0 ports, (although the speed of the module maybe limited when using USB 1.1 ports).

The USB-1602HS-2AO provides the following features:

- Two single-ended 16-bit analog inputs, with one A/D converter per channel.

  The maximum sampling rate is 2 MS/s per channel.

  The input range is software programmable for ±10 V, ±2.5 V, or ±500 mV.
- Two synchronous 16-bit ±10 V analog outputs can generate waveforms at 1 MS/s per channel.
- 16 synchronous digital inputs and 16 synchronous digital outputs
- Four 16-bit or 32-bit counters (can be configured to be gated)
- Two timer/pulse generators with pulse width (duty cycle) control
- Three 16-bit or 32-bit quadrature detectors to measure linear and rotary position

A 68-pin SCSI connector provides connections for all inputs and outputs except for the two analog inputs. Four BNC connectors provide connections for the two analog inputs, and alternate connections for the external pacer clock and external digital trigger input.

The USB-1602HS-2AO samples all analog inputs, digital inputs, and counter inputs simultaneously. You can synchronize AI, AO, and DIO operations at rates of up to 1 MS/s (million samples per second), with aggregate throughput up to 8 MS/s.

You can pace operations with an internal or external clock.

A 500 VDC isolation barrier between the field wiring and USB interface reduces signal noise and protects the board and your computer from ground spikes. The USB 2.0 high-speed driver transfers data at rates up to 480 Mbps.

The device is powered by a 10 Watt regulated external power supply that is included with shipment. Factory and self-calibration tables are stored onboard in EEPROM.

Software features

For information on the features of *Insta*Cal and the other software included with your USB-1602HS-2AO, refer to the *Quick Start Guide* that shipped with your device.

Installing the USB-1602HS-2AO

What comes with your USB-1602HS-2AO shipment?

Hardware

- USB-1602HS-2AO

- USB cable (2-meter length)

- External power supply and cord – 5 volts, 10 watt AC power adapter. MCC part number PS-5V2AEPS

Optional components

Cables

- Standard BNC cable
- CA-68-3R cable
- CA-68-3S (3 foot shielded cable)
- CA-68-6S (6 foot shielded cable)

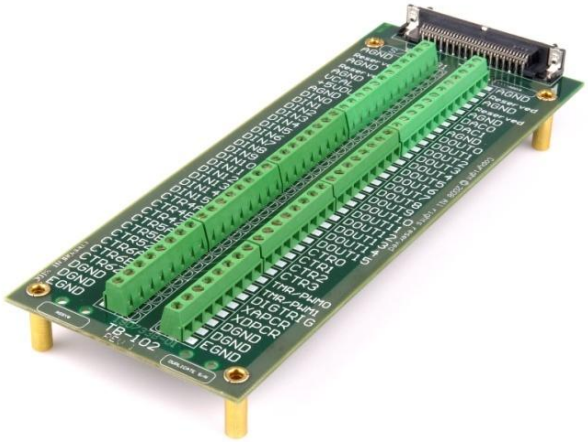
CA-68-3R (3-feet)

CA-68-3S (3-feet)

CA-68-6S (6-feet)

Screw termination board with screw terminals

- TB-102



Additional documentation

In addition to this hardware user's guide, you should also receive the *Quick Start Guide* (available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf). This booklet supplies a brief description of the software you received with your USB-1602HS-2AO and information regarding installation of that software. Please read this booklet completely before installing any software or hardware.

Signal conditioning accessories

MCC provides signal termination products for use with the USB-1602HS-2AO. Refer to the "Field wiring and signal termination" section for a complete list of compatible accessory products.

Unpacking the USB-1602HS-2AO

As with any electronic device, take care while handling to avoid damage from static electricity. Before removing the USB-1602HS-2AO from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

If the USB-1602HS-2AO is damaged, notify Measurement Computing Corporation immediately by phone, fax, or e-mail.

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

For international customers, contact the local distributor where you purchased the USB-1602HS-2AO. Click on this link www.measurementcomputing.com/sales.asp to locate your distributor.

Installing the software

Refer to the *Quick Start Guide* for instructions on installing the software on the *Measurement Computing Data Acquisition Software CD*. This booklet is available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Installing the hardware

Power to the USB-1602HS-2AO is provided with the 10 watt AC power adapter (PS-5V2AEPS). The power supply ships with a U.S. plug. Optional interchangeable plugs for international locations are available.

Connecting the external power supply

Connect the AC power adapter cord to the **EXT. PWR** connector on the device's rear panel, and plug the adapter into an electrical outlet.

The **POWER** LED on the front panel turns on when the device is detected by the system.

Connect external power before connecting the USB cable to the computer

Connect the external power cable to the USB-1602HS-2AO before connecting the USB cable to the computer. This allows the USB-1602HS-2AO to inform the host computer (when the USB cable is connected) that the board requires minimal power from the computer's USB port.

Connecting the USB-1602HS-2AO to your system

To connect the USB-1602HS-2AO to your system, turn the computer on, and connect a USB cable from the **USB** connector on the rear panel to either a USB port on the computer or external USB hub connected to the computer.

When you connect the USB-1602HS-2AO for the first time, a **Found New Hardware** message opens as the device is detected. When the message closes, the installation is complete.

Configuring the USB-1602HS-2AO

All hardware configuration options on the USB-1602HS-2AO are software controlled with the exception of the digital pull-up / pull-down (described below), which is set for pull-up by default. You can select some of the configuration options using *Insta*Cal, such as the analog input range and the trigger source. Once selected, any program that uses the Universal Library will initialize the hardware according to these selections.

Connecting the board for I/O operations

Connectors, cables, and accessory products

The following table lists the board connectors, applicable cables, and compatible accessory products for the USB-1602HS-2AO.

Board connectors, cables, and compatible hardware

Parameter	Specification
Connector types	▪ Four standard BNC female connectors for analog input, clock input, and digital trigger input ▪ 68-pin SCSI connector
Compatible cable for the BNC connectors	Standard BNC cable
Compatible cables for the 68-pin SCSI connector	▪ CA-68-3R ▪ CA-68-3S or CA-68-6S shielded cable
Compatible accessory products using the CA-68-3R, CA-68-3S, or CA-68-6S cables	TB-102 screw terminal board

BNC connectors

The USB-1602HS-2AO has four BNC connectors used to connect the analog input signals, external pacer clock input, and external digital trigger input.

Figure 1. BNC connectors

The signal names for the BNC connectors are listed below:

BNC Label	Signal connection
CH0	Analog input 0
CH1	Analog input 1
EXT TRG	External digital trigger input
EXT CLK	External pacer clock input

EXT TRG is equivalent to the DIG TRIG signal on the SCSI connector. EXT CLK is equivalent to the XAPCR signal on the SCSI connector. Connect your signals using a standard BNC cable.

68-pin SCSI connector

The signals that are available on the 68-pin SCSI connector are listed below.

68-pin SCSI connector pin out

Signal name	Pin		Pin	Signal name
DGND	68	• •	34	DGND
(external pacer clock output) XDPCR	67	• •	33	CTR6 Z
(external pacer clock input) XAPCR	66	• •	32	CTR6 B
DIG TRIG	65	• •	31	CTR6 A
TMR/PWM1	64	• •	30	CTR5 Z
TMR/PWM0	63	• •	29	CTR5 B
CTR3	62	• •	28	CTR5 A
CTR2	61	• •	27	CTR4 Z
CTR1	60	• •	26	CTR4 B
CTR0	59	• •	25	CTR4 A
DOUT15	58	• •	24	DIN15
DOUT14	57	• •	23	DIN14
DOUT13	56	• •	22	DIN13
DOUT12	55	• •	21	DIN12
DOUT11	54	• •	20	DIN11
DOUT10	53	• •	19	DIN10
DOUT9	52	• •	18	DIN9
DOUT8	51	• •	17	DIN8
DOUT7	50	• •	16	DIN7
DOUT6	49	• •	15	DIN6
DOUT5	48	• •	14	DIN5
DOUT4	47	• •	13	DIN4
DOUT3	46	• •	12	DIN3
DOUT2	45	• •	11	DIN2
DOUT1	44	• •	10	DIN1
DOUT0	43	• •	9	DIN0
AGND	42	• •	8	AGND
DAC 1	41	• •	7	+5VPWR
DAC 0	40	• •	6	VCAL (reserved for calibration)
AGND	39	• •	5	AGND
Reserved	38	• •	4	Reserved
AGND	37	• •	3	AGND
Reserved	36	• •	2	Reserved
AGND	35	• •	1	AGND

Connect your signals using a CA-68-3R cable, or CA-68-3S or CA-68-6S shielded cable.

Cabling

Use a CA-68-3R 68-pin ribbon expansion cable (Figure 2), or a CA-68-3S (3-foot) or CA-68-6S (6-foot) 68-pin shielded expansion cable (Figure 3) to connect signals to the USB-1602HS-2AO's 68-pin SCSI connector.

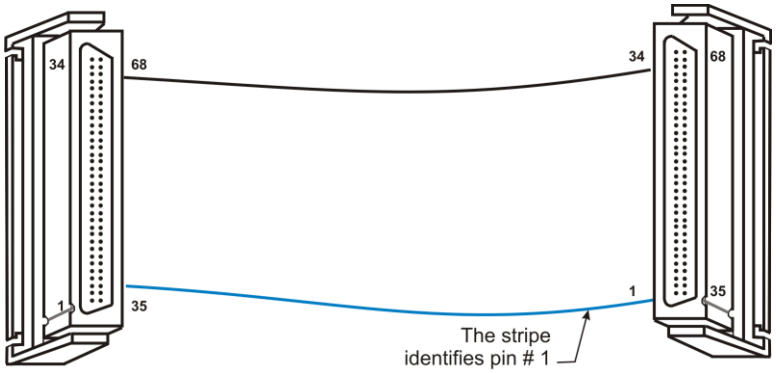


Figure 2. CA-68-3R cable

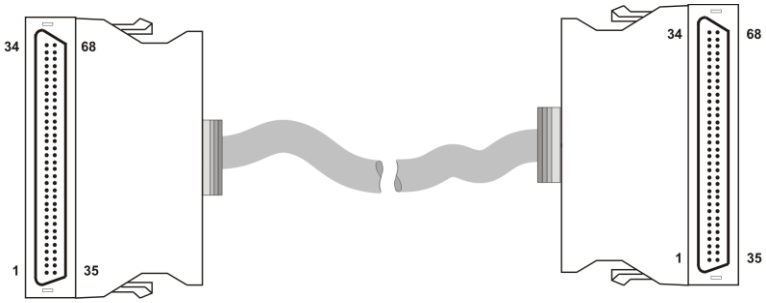


Figure 3. CA-68-3S and CA-68-6S shielded cable

Details on these cables are available at www.mccdaq.com/usb-data-acquisition/USB-1604HS-2AO.aspx.

Field wiring and signal termination

You can use the following Measurement Computing screw terminal board to terminate field signals and route them into the USB-1602HS-2AO board using the CA-68-3R, CA-68-3S, or CA-68-6S cable:

- **TB-102**: Termination board with screw terminals. Details on this product are available on our web site at www.mccdaq.com/products/screw_terminal_bnc.aspx.

  A 19-inch rack mount kit (**RM-TB-102)** for the TB-102 termination board is also available.

TB-102 screw terminal board connector to SCSI connector pin out

The TB-102 terminal board is shown here. The table below lists how signals on the TB-102 are mapped to the signals on the 68-pin SCSI connector.

Pin mapping between the TB-102 terminal board and the 68-pin SCSI connector

TB1 screw terminals	SCSI pin	TB2 screw terminals	SCSI pin
AGND	1	AGND	35
Reserved	2	Reserved	36
AGND	3	AGND	37
Reserved	4	Reserved	38
AGND	5	AGND	39
VCAL	6	DAC0	40
+5VOUT	7	DAC1	41
AGND	8	AGND	42
DIN0	9	DOUT0	43
DIN1	10	DOUT1	44
DIN2	11	DOUT2	45
DIN3	12	DOUT3	46
DIN4	13	DOUT4	47
DIN5	14	DOUT5	48
DIN6	15	DOUT6	49
DIN7	16	DOUT7	50
DIN8	17	DOUT8	51
DIN9	18	DOUT9	52
DIN10	19	DOUT10	53
DIN11	20	DOUT11	54
DIN12	21	DOUT12	55
DIN13	22	DOUT13	56
DIN14	23	DOUT14	57
DIN15	24	DOUT15	58
CTR4A	25	CTR0	59
CTR4B	26	CTR1	60
CTR4Z	27	CTR2	61
CTR5A	28	CTR3	62
CTR5B	29	TMR/PWM0	63
CTR5Z	30	TMR/PWM1	64
CTR6A	31	DIGTRIG	65
CTR6B	32	XAPCR	66
CTR6Z	33	XDPCR	67
DGND	34	DGND	68
DGND	*	DGND	*
EGND	**	EGND	**

* Extra digital ground connectors

** EGND is connected to the SCSI connector shell.

Functional Details

Front panel

Figure 4. USB-1602HS-2AO front panel

BNC connectors

The USB-1602HS-2AO has four BNC connectors that provide connections for the following signals:

- Two single-ended analog inputs
- External digital trigger input
- External pacer clock input

These signals are also available on the 68-pin SCSI connector.

Status LEDs

The **POWER** LED lights up after the device is enumerated by the system. The **ACTIVE** LED lights up when the USB-1602HS-2AO is transmitting or receiving data.

Rear panel

Figure 5. USB-1602HS-2AO rear panel

SCSI connector

The 68-pin SCSI connector provides connections for all I/O signals except for analog input: Refer to page 12 for the connector pin out.

- Two analog outputs (DAC0 and DAC1)
- 16 digital inputs (DIN1 to DIN15)
- 16 digital outputs (DOUT1 to DOUT15)
- Four counters (CTR0 to CTR3). Two counters may be gated.
- Three quadrature detectors (CTR4 A, B, and Z to CTR6 A, B, and Z)
- Two timer/pulse outputs (TMR/PWM0 to TMR/PWM1)
- Digital trigger input (DIG TRIG)
- Input pacer clock (XAPCR)
- Output pacer clock (XDPCR)
- Analog ground (AGND)
- Digital ground (DGND)
- Calibration (VCAL)
- +5V PWR

External power connector (EXT PWR)

The USB-1602HS-2AO requires external power. Connect the PS-5V2AEPS power supply to the EXT PWR connector. This power supply provides 5 VDC, 2 A power, and plugs into a standard 120 VAC outlet.

USB connector

The USB connector provides communication with the host PC.

Analog common

The analog ground reference for the analog inputs and analog outputs.

Mechanical drawing

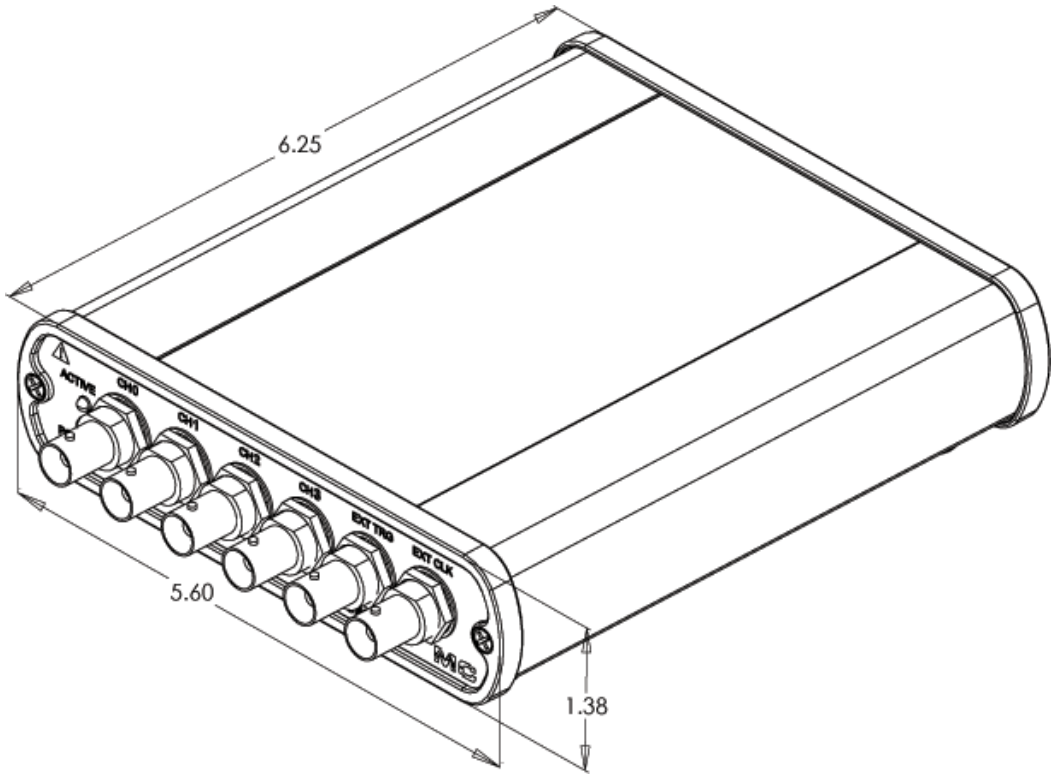


Figure 6. USB-1602HS-2AO case dimensions

Block diagram

USB-1602HS-2AO functions are illustrated in the block diagram shown here.

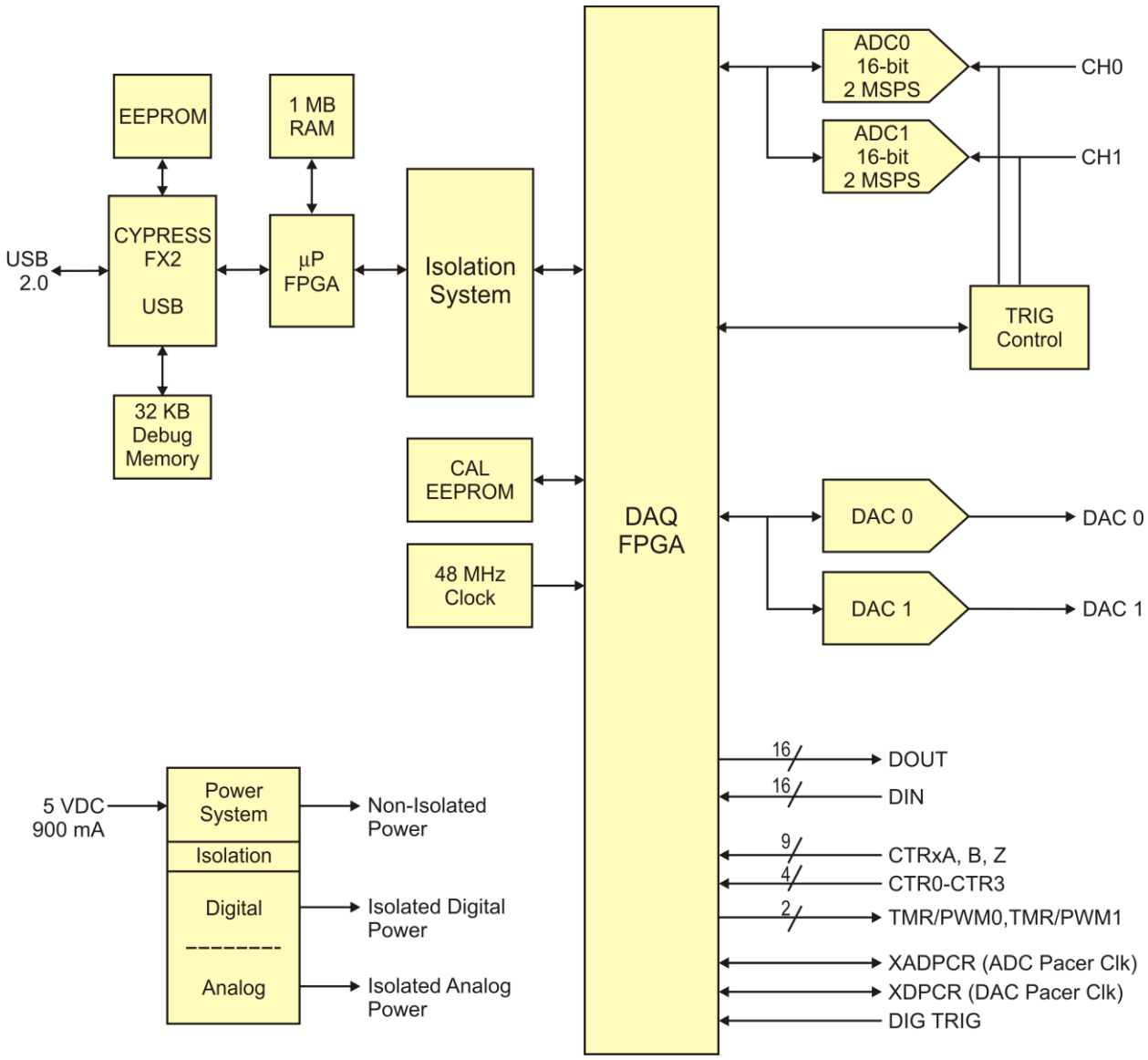


Figure 7. USB-1602HS-2AO functional block diagram

Synchronous analog, digital, and counter sampling

The USB-1602HS-2AO samples all analog, digital, and counter inputs simultaneously, while also generating up to two analog outputs and digital pattern outputs at the same time.

The maximum analog input sampling rate is 2 MS/s. Digital channels (digital input and counter channels) can be sampled at rates up to 8 MS/s for one channel when no analog channels are sampled, and rates of up to 2 MS/s when analog channels are also sampled.

Input clock pacing

Analog, digital, and counter inputs can be sampled based on either an internal programmable input pacer or with an external clock source (**XAPCR** pin on the SCSI connector or the **EXT CLK** BNC connector). Analog channels can be paced from 0. 5 µs to 1000 seconds in 20.83 ns steps. Digital and counter inputs can be paced from 250 ns to 1 second in 20.83 ns steps.

The clock rate is 8 MHz maximum for both the internal pacer clock and external input scan clock.

Output clock pacing

Analog, digital, and timer operations can be paced using the internal output pacer clock (independent of the internal pacer clock), an external output pacer clock connected to the XDPCR pin on the SCSI connector, the internal programmable input pacer, or an external input pacing clock connected to either the XAPCR pin on the SCSI connector or the **EXT CLK** BNC connector.

The clock rate is 1 MHz maximum for analog output operations, and 8 MHz maximum for digital operations in which no analog channels are enabled.

Analog inputs

The USB-1602HS-2AO has two single-ended analog inputs. Each input has a dedicated 16 bit A/D converter that provides true simultaneous sampling at rates of up to 2 MHz per channel. The input range is software selectable for ±10 V, ±2.5 V, or ±500 mV.

You can pace analog input operations with the internal A/D pacer clock or with an external clock source. When using an external input scan clock, connect the clock source to the **XAPCR** pin on the SCSI connector or the **EXT CLK** BNC connector.

Analog outputs

The USB-1602HS-2AO has two independent, 16-bit, analog output channels. The analog output range is -10V to +10V.

Each DAC channel can continuously output a waveform at up to 1 MHz. You can clock the DAC channels with the internal DAC scan clock or with an external DAC input clock. The internal analog input pacer clock can pace both the DAC output and the analog input simultaneously.

When using an external output scan clock, connect the clock source to the **XDPCR** pin on the SCSI connector or the **EXT CLK** BNC connector.

Digital I/O

The USB-1602HS-2AO has 32 CMOS digital I/O lines configured as 16 digital inputs and 16 digital outputs. You can pace digital operations with the onboard scan clock or an external source. The maximum DIO transfer rate is 8 MS/s (software paced).

Digital input scanning

Digital input ports can be read synchronously along with analog channels in a scan, or asynchronously before, during, or after an analog input scan.

The digital inputs can sustain rates of up to 8 MS/s for one channel when no analog channels are sampled, and rates of up to 2 MS/s when analog channels are also sampled.

Internal pull-up/pull-down capability (J14)

Unconnected inputs are pulled high to +3.3V through 100 k resistors via a 4-pin jumper on the PCB board (**J14**). To configure these inputs to pull low (0 V), do the following:

1. Remove the 4 screws from the rear panel.

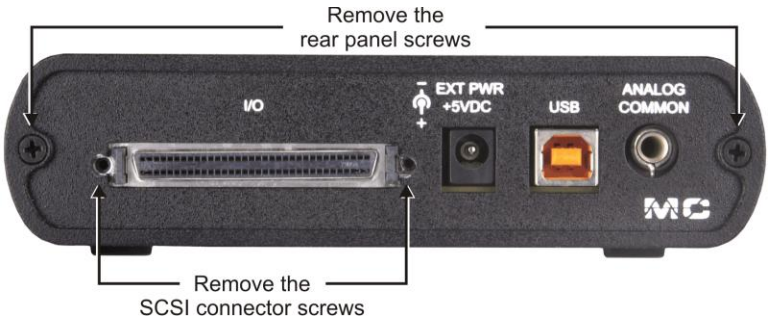


Figure 8. Location of rear panel screws

2. Slide the board out of the housing and locate jumper **J14**.

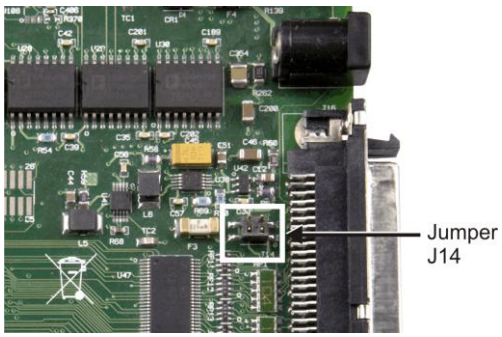


Figure 9. Location of J14

3. Configure jumper J14 for either pull-up or pull-down configuration (refer to Figure 10).
   - For pull-up, place the J14 shorting block across pins 1 and 2.
   - For pull-down, place the J14 shorting block across pins 3 and 4.

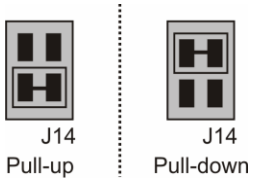


Figure 10. J14 configuration

4. Slide the board into the housing.
5. Replace the 4 screws on the rear panel.

Digital outputs and pattern generation

Digital outputs can be updated asynchronously at any time before, during, or after an acquisition. The USB-1602HS-2AO can generate a digital pattern at up to 4 MS/s.

Digital pattern generation is clocked with either the internal D/A scan clock or with an external D/A input clock. Digital patterns can be generated along with D/A waveforms. They are paced by the same selected clock. The on-board programmable clock generates updates ranging from once every 1000 seconds to 1 MHz, independent of the acquisition rate.

The digital outputs are driven low at power up and reset.

Triggering

Triggering can be the most critical aspect of a data acquisition application. A trigger event occurs and data acquisition begins when specified conditions are met. You select the trigger mode and set up its parameters with software.

The USB-1602HS-2AO supports both hardware-based and software-based triggers. With a hardware-based trigger, an output value is compared in hardware to an input level on a specified channel. With software-based triggers, the analog, digital, and/or counter readings are checked by the PC in order to detect the trigger event.

The USB-1602HS-2AO supports the following trigger sources:

- Hardware-based triggers:
  - Analog input hardware
  - External digital trigger input
- Software-based triggers:
  - Analog software trigger
  - Digital pattern
  - Counter/totalizer

Hardware-based triggering

With a hardware-based trigger, an output value is compared in hardware to an input level on a specified channel.

Analog input hardware

In this mode, the acquisition is triggered when a specified input level is achieved. The USB-1602HS-2AO uses true analog triggering in which the trigger level you program sets an analog DAC, which is then compared in hardware to the analog input level on the selected channel. This ensures an analog trigger latency that is less than 1.5 µs.

You can select any analog channel as the trigger channel, but the selected channel must be the first channel in the scan. You can program the trigger level, the rising or falling edge, and hysteresis level. The trigger level can be any value within the voltage range for the selected trigger channel.

External digital trigger input

A separate digital trigger input line (**DIG TRIG**) allows TTL-level triggering with latencies guaranteed to be no less than 100 nS. The acquisition is triggered when a rising or falling edge is detected .

The trigger level is set at TTL sensitive. Latency is one sample period, maximum. The input signal range is ±15 V. The trigger edge, logic level (1 or 0), and the rising or falling edge for the discrete trigger input are software selectable.

Software-based triggering

The three software-based trigger modes differ from hardware analog triggering and digital triggering because the analog, digital, or counter readings are checked by the PC in order to detect the trigger event.

Analog software

The acquisition is triggered when the computer issues a software command. You can select any analog channel in the scan as the trigger channel. The trigger level, the rising or falling edge, and hysteresis are software programmable. The trigger level can be any value within the range of the trigger channel. Latency is one sample period, maximum.

Digital pattern

The acquisition is triggered with a digital input channel pattern. You can select any scanned digital input channel pattern to trigger an acquisition, including the ability to mask or ignore specific bits.

You can program to trigger the conversion when equal to, not equal to, above, or below a value. Latency is one sample period, maximum.

Counter/Totalizer

The acquisition is triggered with the counter/totalize inputs. You can program triggering to occur on a frequency, or on total counts that are equal, not equal, above, below, or below a value, or that are within/outside of a window rising/falling edge. Latency is one sample period, maximum. You can select of the included counter channels as the trigger source.

Software-based triggering usually results in a long period of inactivity between the trigger condition being detected and the data being acquired. However, the USB-1602HS-2AO avoids this situation by using pre-trigger data. When software-based-triggering is used, and the PC detects the trigger condition — which may be thousands of readings after the actual occurrence of the signal — the USB-1602HS-2AO driver automatically looks back to the location in memory where the actual trigger-causing measurement occurred, and presents the acquired data that begins at the point where the trigger-causing measurement occurs. The maximum inactive period in this mode equals one scan period.

Set the trigger value > 0 when using a counter input as the trigger source

When using a counter for a trigger source, set the trigger value to 1 or greater. Since all counters start at zero with the first scan, there is no valid reference in regard to rising or falling edge. Setting the trigger value to 1 or greater ensures that a valid reference value is present, and that the first trigger will be legitimate.

Stop trigger modes

You can use any of the software trigger modes explained previously to stop an acquisition. For example, you can program an acquisition to begin on one event, such as a voltage level, and then stop on another event, such as a digital pattern.

Pre-triggering and post-triggering modes

The USB-1602HS-2AO supports four modes of pre-triggering and post-triggering. When using pre-trigger, you must use software-based triggering to initiate an acquisition.

No pre-trigger, post-trigger stop event

In this mode, data acquisition starts when the trigger is received, and the acquisition stops when the stop-trigger event is received.

Fixed pre-trigger with post-trigger stop event

In this mode, you set the number of pre-trigger readings to acquire. The acquisition continues until a stop-trigger event occurs.

No pre-trigger, infinite post-trigger

In this mode, no pre-trigger data is acquired. Instead, data is acquired beginning with the trigger event, and is terminated when you issue a command to halt the acquisition.

Fixed pre-trigger with infinite post-trigger

You set the amount of pre-trigger data to acquire. Then, the system continues to acquire data until the program issues a command to halt acquisition.

Counter inputs

The USB-1602HS-2AO has four counters that can accept frequency inputs up to 20 MHz. The counter channels can be read as 16 or 32-bit counters. A counter can also be configured to be gated by one of the other counter inputs mapped as a gate input (refer to Mapped channels, on page 22). The input type is TTL, rising-edge triggered.

The counters can concurrently monitor time periods, frequencies, pulses, and other event driven incremental occurrences directly from pulse-generators, limit switches, proximity switches, and magnetic pick-ups.

Counter inputs can be read asynchronously under program control, or synchronously as part of an analog or digital scan group.

When reading synchronously, all counters are set to zero at the start of an acquisition. When reading asynchronously, counters may be cleared on each read, count up continually, or count until the 16-bit or 32-bit limit has been reached. See the counter mode descriptions below.

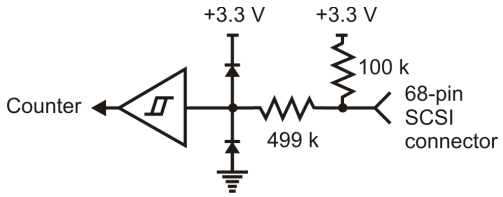


Figure 11. Typical USB-1602HS-2AO counter channel

Mapped channels

A *mapped channel* is one of four counter input signals (CTR0 to CTR3) that can get multiplexed into a counter module. The mapped channel can participate with the counter's input signal by gating the counter, latching the counter, and so on. The four possible choices for the mapped channel are the four counter input signals (post-debounce).

A mapped channel can be used to:

- gate the counter
- decrement the counter
- latch the current count to the count register

Usually, all counter outputs are latched at the beginning of each scan within the acquisition. However, you can use a second channel — known as the mapped channel — to latch the counter output.

Counter input modes

The USB-1602HS-2AO supports the following modes:

- Counter
- Period
- Pulse width measurement
- Timing

Program the counter operation mode with software.

Counter mode

A counter can be asynchronously read with or without *clear on read*. The asynchronous read-signals strobe when the lower 16-bits of the counter are read by software. The software can read the counter's high 16-bits some time later after reading the lower 16-bits. The full 32-bit result reflects the timing of the first asynchronous read strobe.

The following counter mode options are selectable with software.

Counter mode	Description
Totalize	This mode allows the basic use of a 32-bit counter. The channel input increments the counter upward. ▪ When used as a 16-bit counter (counter low), one channel can be scanned up to an 8 MHz rate. ▪ When used as a 32-bit counter (counter high), two sample times are used to return the full 32-bit result. Therefore, a 32-bit counter can only be sampled at a 4 MHz maximum rate. The counter counts up and does not clear on every new sample. However, it does clear at the start of a new scan command. The counter rolls over on the 16-bit (counter low) boundary, or on the 32-bit (counter high) boundary.
Clear on read	The counter counts up and is cleared after each read. By default, the counter counts up and only clears the counter at the start of a new scan command. The value of the counter before it was cleared is latched and returned.
Rollover	The counter continues to count upward, rolling over on the 16 or 32-bit boundary.
Stop at top	The counter stops at the top of its count. The top of the count is FFFF hex (65,535) for the 16-bit mode, and FFFFFFFF hex (4,294,967,295) for the 32-bit mode.
16-bit or 32-bit	Sets the counter type to either 16-bits or 32-bits. The type of counter only matters if the counter is using the Stop at all FFFFs mode; otherwise, this option is ignored. The 16 bit mode requires less bandwidth for higher channels count and higher sample rates.

Period mode

This mode allows for period measurement of the channel input.

You can measure x1, x10, x100 or x1000 periods, and 16-bit (counter low) or 32-bit (counter high) values. Four timebase, or tick-size, values are available (20.83 ns, 208.3 ns, 2.083 µs, or 20.83 µs). These values are based on the 48 MHz system clock. Any other channel can gate the period measurement. All period mode options are selectable with software.

Pulse width measurement mode

This mode is used to measure a channel's pulse width.

You can measure 16-bit or 32-bit values. Four timebase, or tick-size, values are available (20.83 ns, 208.3 ns, 2.083 µs, or 20.83 µs). These values are based on the 48 MHz system clock. Any other channel can gate the pulse width measurement. All pulse width options are selectable with software.

Timing mode

This mode is used to measure the time between two subsequent events, such as the edge of one channel with respect to the edge of another channel.

You can measure 16-bit or 32-bit values. Four timebase, or tick-size, values are available (20.83 ns, 208.3 ns, 2.083 µs, or 20.83 µs) . All timing options are selectable with software.

Debounce function

The USB-1602HS-2AO has debounce circuitry which eliminates switch-induced transients that are typically associated with electro-mechanical devices including relays, proximity switches, and encoders.

All debounce options are selectable with software. You can select a debounce time, debounce mode, and rising-edge or falling-edge sensitivity.

Each channel's output can be debounced with 16 programmable debounce times in the range of 500 ns to 25.5 ms).

There are two debounce modes, as well as a debounce bypass, as shown in Figure 12. The signal from the buffer can be inverted before it enters the debounce circuitry. The inverter is used to make the input rising-edge or falling-edge sensitive.

Edge selection is available with or without debounce. In this case the debounce time setting is ignored and the input signal goes straight from the inverter or inverter bypass to the counter module.

The two debounce modes are *trigger after stable* and *trigger before stable*. In either mode, the selected debounce time determines how fast the signal can change and still be recognized.

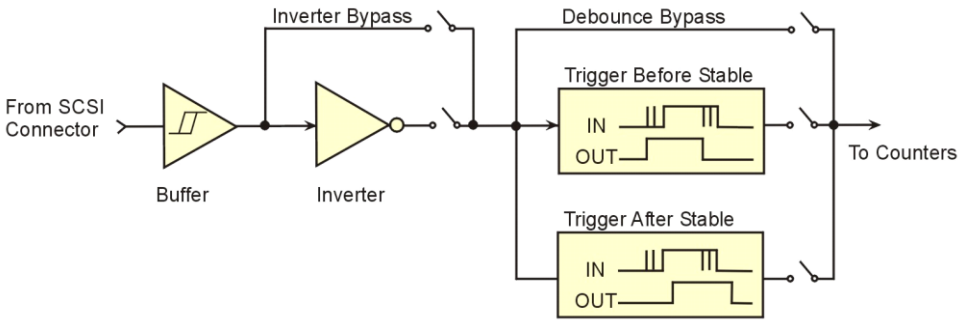


Figure 12. Debounce model block diagram

Trigger after stable mode

In the *trigger after stable* mode, the output of the debounce module does not change state until a period of stability has been achieved. This means that the input has an edge, and then must be stable for a period of time equal to the debounce time.

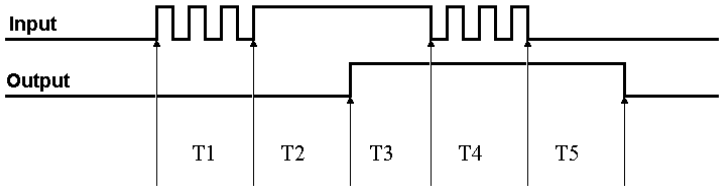


Figure 13. Debounce module – trigger after stable mode

T1 through T5 indicate time periods. In *trigger after stable* mode, the input signal to the debounce module is required to have a period of stability after an incoming edge, in order for that edge to be accepted (passed through to the counter module.) For this example, the debounce time is equal to T2 and T5.

- T1 – In Figure 13, the input signal goes high at the beginning of time period T1, but never stays high for a period of time equal to the debounce time setting (equal to T2 for this example.)
- T2 – At the end of time period T2, the input signal has transitioned high and stayed there for the required amount of time—therefore the output transitions high. If the input signal does not stabilize in the high state long enough, no transition would have appeared on the output and the entire disturbance on the input would have been rejected.
- T3 – During time period T3, the input signal remained steady. No change in output is seen.
- T4 – During time period T4, the input signal has more disturbances and does not stabilize in any state long enough. No change in the output is seen.
- T5 – At the end of time period T5, the input signal has transitioned low and stayed there for the required amount of time—therefore the output goes low.

Trigger before stable mode

In the *trigger before stable* mode, the output of the debounce module immediately changes state, but will not change state again until a period of stability has passed. For this reason the mode can be used to detect glitches.

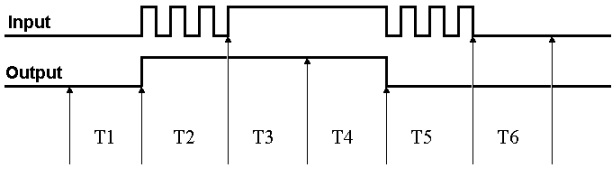


Figure 14. Debounce module – Trigger before stable mode

T1 through T5 indicate time periods.

- T1 – In Figure 14, the input signal is low for the debounce time (equal to T1); therefore when the input edge arrives at the end of time period T1, it is accepted and the output (of the debounce module) goes high. Note that a period of stability must precede the edge in order for the edge to be accepted.

- T2 – During time period T2, the input signal is not stable for a length of time equal to T1 (the debounce time setting for this example.) Therefore, the output stays "high" and does not change state during time period T2.
- T3 – During time period T3, the input signal is stable for a time period equal to T1, meeting the debounce requirement. The output is held at the high state. This is the same state as the input.
- T4 – At anytime during time period T4, the input can change state. When this happens, the output will also change state. At the end of time period T4, the input changes state, going low, and the output follows this action [by going low].
- T5 – During time period T5, the input signal again has disturbances that cause the input to not meet the debounce time requirement. The output does not change state.
- T6 – After time period T6, the input signal has been stable for the debounce time and therefore any edge on the input after time period T6 is immediately reflected in the output of the debounce module.

Debounce mode comparisons

Figure 15 shows how the two modes interpret the same input signal, which exhibits glitches. Notice that the *trigger before stable* mode recognizes more glitches than the *trigger after stable* mode. Use the *bypass* option to achieve maximum glitch recognition.

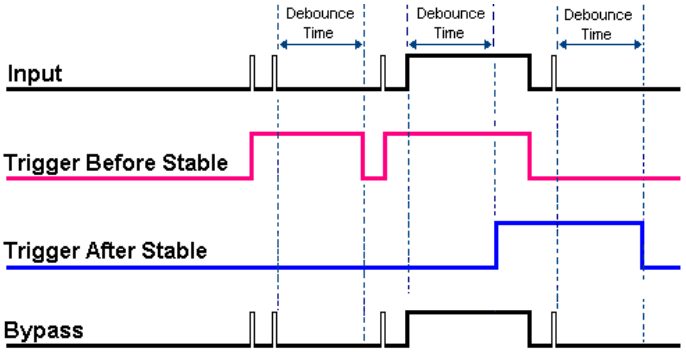


Figure 15. Example of two debounce modes interpreting the same signal

Set the debounce time according to the amount of instability expected in the input signal. Setting a debounce time that is too short may result in unwanted glitches clocking the counter. Setting a debounce time that is too long may result in an input signal being rejected entirely. Some experimentation may be required to find the appropriate debounce time for a particular application.

To see the effects of different debounce time settings, view the analog waveform along with the counter output. This can be done by connecting the source to an analog input.

Use *trigger before stable* mode when the input signal has groups of glitches and each group is to be counted as one. The trigger before stable mode recognizes and counts the first glitch within a group but rejects the subsequent glitches within the group if the debounce time is set accordingly. The debounce time should be set to encompass one entire group of glitches as shown in the following diagram.

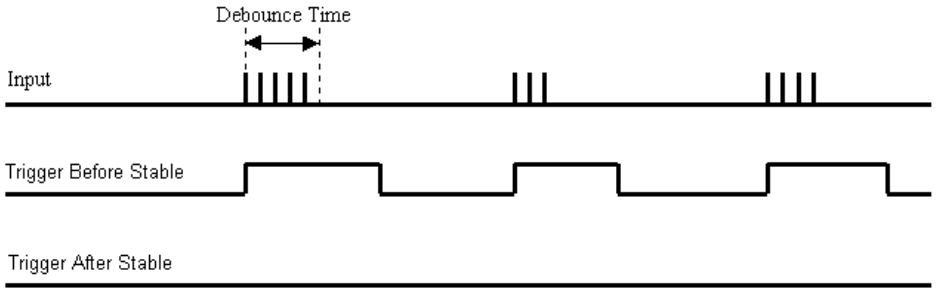


Figure 16. Optimal debounce time for trigger before stable mode

Trigger after stable mode behaves more like a traditional debounce function: rejecting glitches and only passing state transitions after a required period of stability. *Trigger after stable* mode is used with electro-mechanical devices like encoders and mechanical switches to reject switch bounce and disturbances due to a vibrating encoder that is not otherwise moving. The debounce time should be set short enough to accept the desired input pulse but longer than the period of the undesired disturbance as shown in Figure 17.

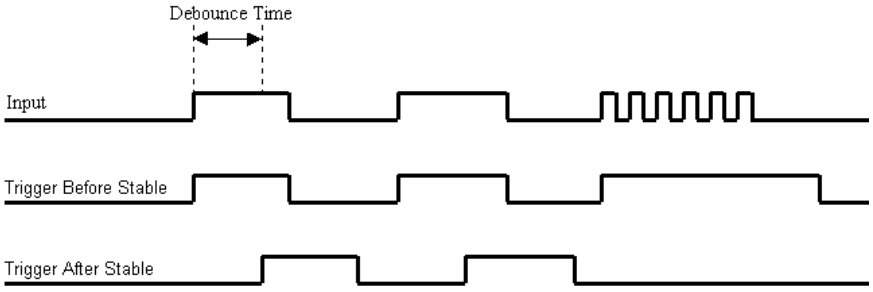


Figure 17. Optimal debounce time for trigger after stable mode

Quadrature detectors

Overview

Quadrature detectors are used to calculate the relative or absolute position of a quadrature encoder, and to determine its rotational speed. Each quadrature detector supports phase A, B, and Z input signals (0°, 90°, and zero). When reading phase A, phase B, and index Z signals, the positioning, direction, and velocity data can be calculated.

Quadrature encoders generally have three outputs: A, B, and Z. The A and B signals are pulse trains driven by an optical sensor inside the encoder. As the encoder shaft rotates, a laminated optical shield rotates inside the encoder. The shield has three concentric circular patterns of alternating opaque and transparent windows through which an LED shines. There is one LED and one phototransistor for each of the concentric circular patterns. One phototransistor produces the A signal, another phototransistor produces the B signal and the last phototransistor produces the Z signal. The concentric pattern for A has 512 window pairs (or 1024, 4096, etc.)

When using a counter for a trigger source, use a trigger value of at least 1. Since all counters start at zero with the initial scan, there is no valid reference in regard to rising or falling edge. Setting a pre-trigger to 1 or more ensures that a valid reference value is present, and that the first trigger is legitimate.

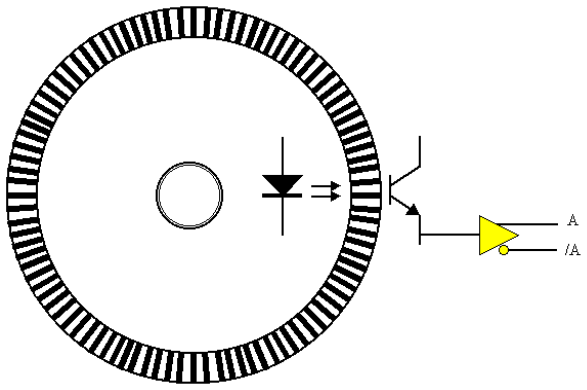


Figure 18. Concentric pattern for output A

The concentric pattern for B has the same number of window pairs as A, except that the entire pattern is rotated by ¼ of a window-pair. Thus the B signal is always 90º out of phase from the A signal. The A and B signals pulse 512 times (or 1024, 4096, etc.) per complete rotation of the encoder.

The concentric pattern for the Z signal has only one transparent window and therefore pulses only once per complete rotation. Representative signals are shown in Figure 19.

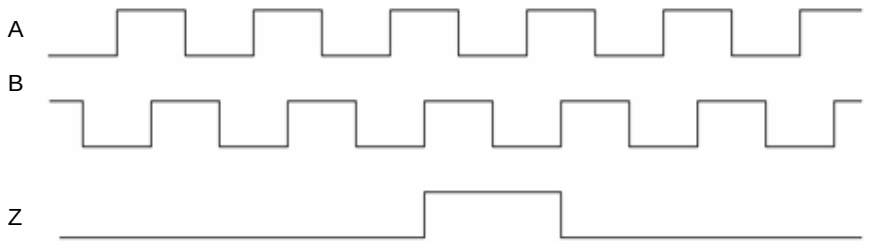


Figure 19. Representation of quadrature encoder outputs A, B, and Z

As the encoder rotates, the A (or B) signal indicates the distance the encoder has traveled. The frequency of A (or B) indicates the velocity of rotation of the encoder. If the Z signal is used to zero a counter (that is clocked by A) then that counter gives the number of pulses the encoder has rotated from its reference. The Z signal is a reference marker for the encoder. It should be noted that when the encoder is rotating clockwise (as viewed from the back), A will lead B and when the encoder is rotating counterclockwise, A lags behind B. If the counter direction control logic is such that the counter counts upward when A leads B and counts downward when A lags B, then the counter gives direction control as well as distance from the reference.

Maximizing encoder accuracy

If there are 512 pulses on A, then the encoder position is accurate to within 360°/512.

You can get even greater accuracy by counting not only rising edges on A but also falling edges on A, giving position accuracy to 360°/1024.

You get maximum accuracy counting rising and falling edges on A and on B (since B also has 512 pulses.) This gives a position accuracy of 360°/2048. These different modes are known as X1, X2, and X4.

Connecting the USB-1602HS-2AO to an encoder

You can connect up to three quadrature encoders to the USB-1602HS-2AO. Quadrature encoders with a 16-bit (counter low) or a 32-bit (counter low + counter high) counter, 6 MHz maximum pulse frequency, and X1, X2, and X4 count modes are supported.

The SCSI connector provides six counter pins that are dedicated to performing encoder functions:

- CTR4 A, CTR4 B, CTR4 Z
- CTR5 A, CTR5 B, CTR5 Z
- CTR6 A, CTR6 B, CTR6 Z

The encoder input pins are dedicated for encoder counting, and cannot be mapped for other functions. Input A is a direct counter input. Input B functions as the B phase for encoder counting, and Input Z functions as the Z phase of the encoder.

Each A and B signal is made as a single-ended connection with respect to common ground. To connect an encoder to the USB-1602HS-2AO, do the following:

- Connect signals A, B, and Z to the CTR4 A, B, and Z through CTR6 A, B, and Z pins on the SCSI connector.
- Connect each encoder ground to GND.

Figure 20 shows the connections for one encoder to the 68-pin SCSI connector on a USB-1602HS-2AO.

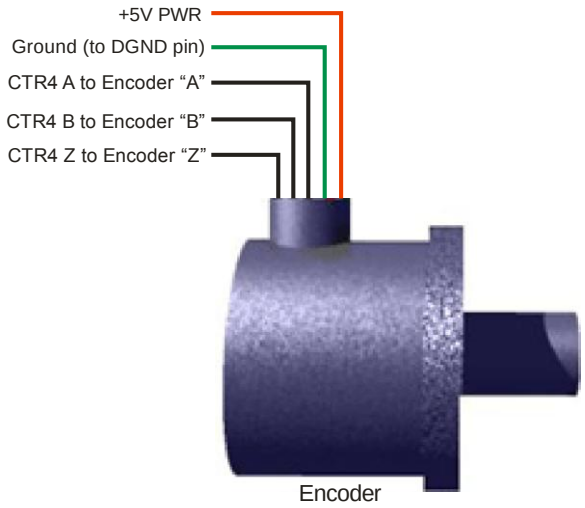


Figure 20. Encoder connections to the SCSI connector*

* Connections can alternately be made to the associated screw-terminals of a connected TB-102 terminal connector.

You can get the relative position and velocity from the encoder. However, during an acquisition, you cannot get data that is relative to the Z-position until the encoder locates the Z-reference.

Debounce feature

Each input can be debounced from 500 ns to 25.5 ms (total of 16 selections) to eliminate extraneous noise, or to switch induced transients. Encoder input signals must be within 0 and 5.5 volts and the switching threshold is typically 1.5 volts. If the encoder stops rotating, but continues to generate signals (due to it being mounted to a vibrating or noisy machine), you can use the debounce feature to eliminate false edges. Choose an appropriate debounce time and apply it to each encoder channel. Refer to the "Debounce function" section on page 23 for additional information regarding debounce times.

Scan period values

The USB-1602HS-2AO clears all counter channels at the beginning of the acquisition, so the values returned during scan period 1 are always zero. The values returned during scan period 2 reflect what happened during scan period 1. In general, the output of each channel’s counter is latched at the beginning of each scan period (called the *start-of-scan*.) Every time the USB-1602HS-2AO receives a *start-of-scan* signal, the counter values are latched and are available to the USB-1602HS-2AO.

The scan period defines the timing resolution for the USB-1602HS-2AO. If you need a higher timing resolution, shorten the scan period.

Timer/pulse generators

The USB-1602HS-2AO has two timer/pulse generator signals (**TMR/PWM0** and **TMR/PWM1**) with programmable duty cycle. Each timer is capable of generating a programmable pulse width wave with a programmable frequency in the range of 0.01123 Hz to 24 MHz. The pulse and period range is 20.83 ns to 89 seconds.

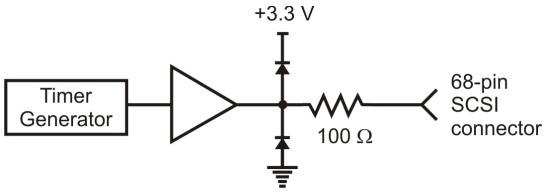


Figure 21. Typical timer/pulse generator channel

The timer outputs can be updated asynchronously at any time, however, doing so results in a pulse stream that is not seamless.

Using detection setpoints for output control

You can configure a detection setpoint for each analog input channel. Each setpoint can update the following channels, allowing for real-time control based on acquisition data:

- The upper 8-bits of the digital output port with a data byte and mask byte
- analog outputs (DAC 0, DAC 1)

You can configure each detection setpoint as one of the following:

- **Single point referenced** – Above, below, or equal to the defined setpoint.
- **Window (dual point) referenced** – Inside or outside the window.
- **Window (dual point) referenced, hysteresis mode** – *Outside the window high* forces one output (designated as Output 2); *outside the window low* forces another output (designated as Output 1).

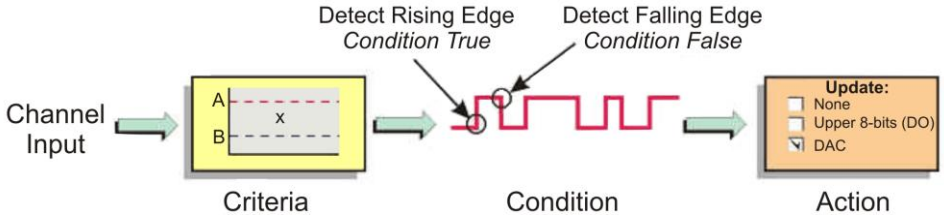


Figure 22. Setpoint configuration

A digital detect signal is used to indicate when a signal condition is *True* or *False*. A signal condition is true if the signal has met defined criteria, and false if the signal has not met defined criteria. The detect signals can be measured as any other input channel, thus allowing real time data analysis during an acquisition.

The detection module looks at the 16-bit data being returned on a channel and generates another signal for each channel with a setpoint applied (*Detect1* for Channel 1, *Detect2* for Channel 2, and so on; see Figure 23). These signals serve as data markers for each channel's data. It does not matter whether that data is volts or counts.

A channel's detect signal shows a rising edge and is *True* (1) when the channel's data meets the setpoint criteria. The detect signal shows a falling edge and is *False* (0) when the channel's data does not meet the setpoint criteria. The *True* and *False* states for each setpoint criteria appear in the setpoint status register; refer to "Using the setpoint status register" section on page 36 for more information.

Criteria – input signal is equal to X		**Action - driven by condition**
Compare X to:	**Setpoint definition**	**Update conditions**
Limit A or Limit B	▪ Equal to A (X = A) ▪ Below A (X < A) ▪ Above B (X > B) (choose one)	*True* only: ▪ If *True*, then output value 1 ▪ If *False*, then perform no action *True* and *False*: ▪ If *True*, then output value 1 ▪ If *False*, then output value 2

Criteria – input signal is equal to X		Action - driven by condition
Window* (non-hysteresis mode)	▪ Inside (B < X < A) ▪ Outside: B > X; or X > A (choose one)	*True* only: ▪ If *True*, then output value 1 ▪ If *False*, then perform no action *True* and *False:* ▪ If *True*, then output value 1 ▪ If *False*, then output value 2
Window* (hysteresis mode)	▪ Above A (X > A) ▪ Below B (X < B) (both conditions are checked in hysteresis mode)	Hysteresis mode (forced update): ▪ If X > A is *True*, then output value 2 until X < B is *True*, then output value 1. ▪ If X < B is *True*, then output value 1 until X > A is *True*, then output value 2. This is saying: (a) If the input signal is outside the window *high*, then output value 2 until the signal goes outside the window *low*, and (b) if the signal is outside the window *low*, then output value 1 until the signal goes outside the window *high*. There is no change to the detect signal while within the window.

* Value A defines the upper limit of the Window, and Value B defines the lower limit.

The detect signal has the timing resolution of the scan period, as shown in Figure 23. The detect signal can change no faster than the scan frequency (1/sampling period.)

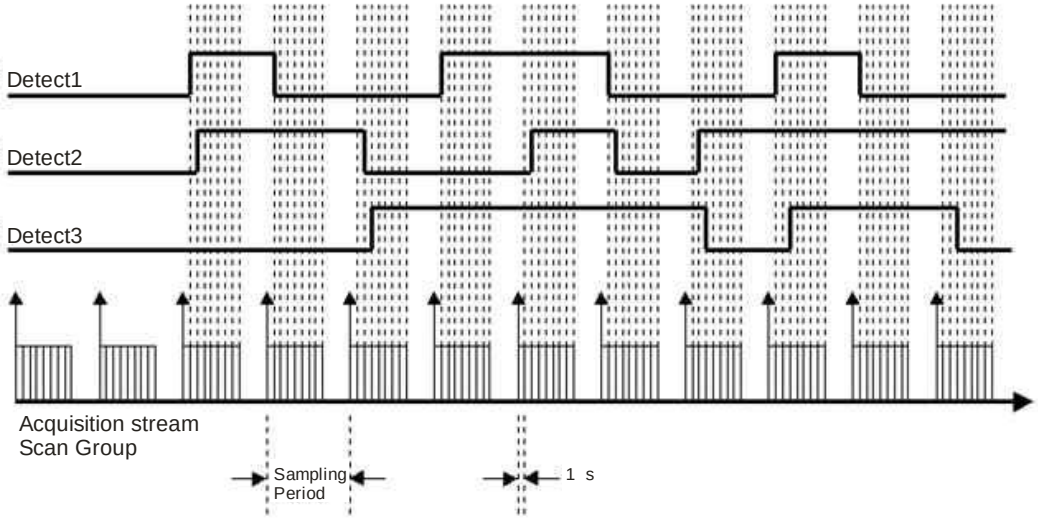


Figure 23. Detection signals for channels 1, 2, and 3

Each channel in the scan group can have one detection setpoint. There can be no more than 16 total setpoints total applied to channels within a sampling group.

Detection setpoints act on 16-bit data only. When reading the counters as 32-bit, data is returned 16-bits at a time. The lower word, the higher word, or both lower and higher words can be part of the scan group. Each counter input channel can have one detection setpoint for the counter's lower 16-bit value, and one detection setpoint for the counter's higher 16-bit value.

Setpoint configuration

You program all setpoints as part of the pre-acquisition setup, similar to setting up an external trigger. Each setpoint acts on 16-bit data, so each has two 16-bit compare values: a high limit (*limit A*) and a low limit (*limit B*). These limits define the *setpoint window*.

You can set the 16-bit high limit (*limit A*) and the 16-bit low limit (*limit B*) with software.

The setpoint conditions (criteria) and update modes are summarized below.

Setpoint criteria

Inside window	The signal is below the 16-bit high limit (limit A) **and** above the 16-bit low limit (limit B).
Outside window	The signal is above the 16-bit high limit (limit A), **or** below the 16-bit low limit (limit B).
Greater than value	The signal is above the 16-bit low limit. The 16-bit high limit (limit A) is not used.
Less than value	The signal is below the 16-bit high limit. The 16-bit low limit (limit B) is not used.
Equal to value	The signal is equal to the 16-bit high limit. The 16-bit low limit (limit B) is not used. This mode is intended for use when the counter or digital input channels are the source channel. Only use this mode with counter or digital input channels as the channel source. To have similar functionality for analog channels, use the *inside window* mode.
Hysteresis mode	*Outside the window high* forces output 2 until an *outside the window low* condition exists, then output 1 is forced. Output 1 continues until an *outside the window high* condition exists. This cycle repeats as long as the acquisition is running in hysteresis mode.

Setpoint output channel

- None
- Update the upper 8-bits of the digital output port
- Update the analog output channels (DAC0, DAC1)

Update modes

- Update on *True* only
- Update on *True* and *False*
- None – Do not update

Setpoint values for output

- 16-bit DAC value or the most significant byte (MSB) of the digital output port when the input *does* meets criteria.
- 16-bit DAC value or the most significant byte (MSB) of the digital output port when the input *does not* meet criteria.

Note: When using setpoints with triggers other than immediate, hardware analog, or TLL, the setpoint criteria evaluation begins immediately upon triggering the acquisition.

Examples of control outputs

Detection on analog input, DAC, and digital port MSB updates

Example 1:

Update mode: Update on *True* and *False*

Criteria: Channel 1 — *below limit*

In this example, channel 1 is programmed with reference to one setpoint (*limit A*), defining a low limit.

Channel	Condition	State of detect signal	Action
1	Below limit A (for channel 1)	*True*	When the channel 1 analog input voltage is below limit A, update DAC1 with the output value 0.0 V.
		False	When the above condition is *false*, update DAC1 with the output value of *minus* 1.0 V.

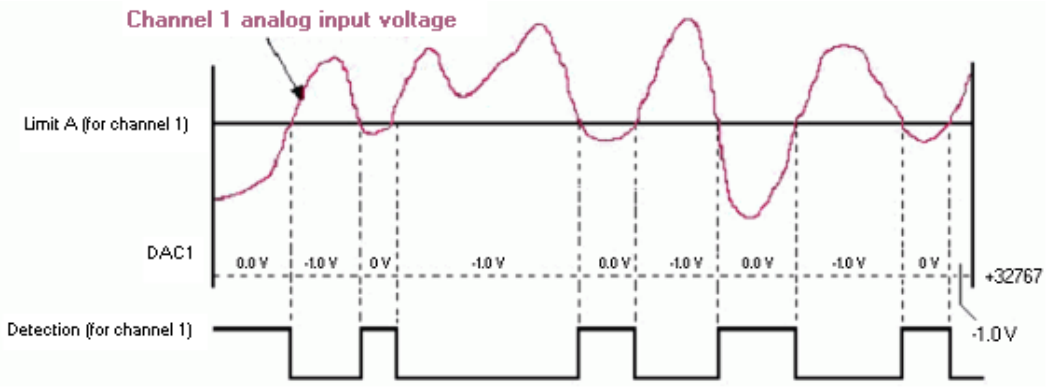


Figure 24. Channel 1 input with setpoint update on *True* and *False*

The setpoint placed on analog Channel 1 updated DAC1 with 0.0 V. The update occurred when the channel 1 input was less than setpoint limit A. When the value of the channel 1 input was above setpoint limit A, the condition of less than limit A was *false*, and DAC1 was updated with –1.0 V.

Example 2:

Update mode: Update on *True* and *False*

Criteria: Channel 0 — *inside window*

In this example, Channel 0 is programmed with reference to two setpoints (limit A and limit B) which define a window for that channel.

Channel	Condition	State of detect signal	Action
0	Within window (between limit A and limit B) for channel 0	*True*	When Channel 0 analog input voltage is within the window, update the digital output port's MSB with 70h.
		False	When the above condition is *false* (channel 0 analog input voltage is outside the window), update the digital output port's MSB with 30h.

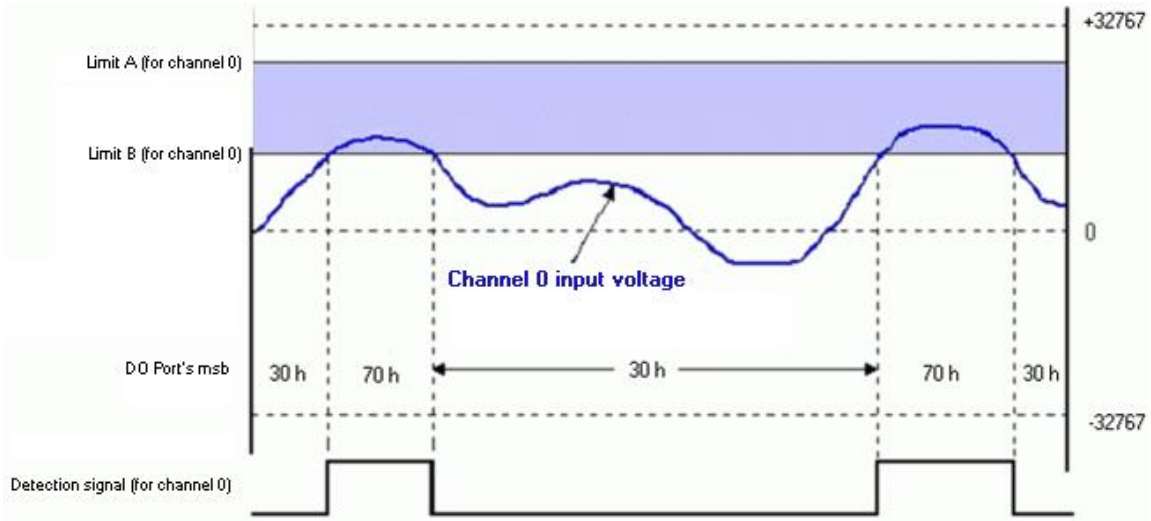


Figure 25. Channel 0 input with setpoint update on *True* and *False*

You can program control outputs on each setpoint. Detection for channel 0 can be used to update the digital output port's most significant byte with one value when the analog input voltage is within the shaded region (70 h), and update with a different value when the analog input voltage is outside the shaded region (30 h).

Using the hysteresis function

Update mode: N/A, the hysteresis option has a forced update built into the function

Criteria used: Window criteria for above and below the set limits

Figure 26 shows analog input Channel 1 with a setpoint which defines two 16-bit limits — Limit A (High) and Limit B (Low). These limits are applied in the hysteresis mode and DAC channel 0 is updated accordingly.

In this example, Channel 1's analog input voltage is used to update DAC0, as follows:

- When outside the window, low (below limit B) DAC0 is updated with 3.0 V. This update remains in effect until the analog input voltage goes above Limit A.
- When outside the window, high (above limit A), DAC0 is updated with 7.0 V. This update remains in effect until the analog input signal falls below limit B. At that time we are again outside the limit "low" and the update process repeats itself.

Hysteresis mode can also be done with the digital output port's most significant byte instead of a DAC.

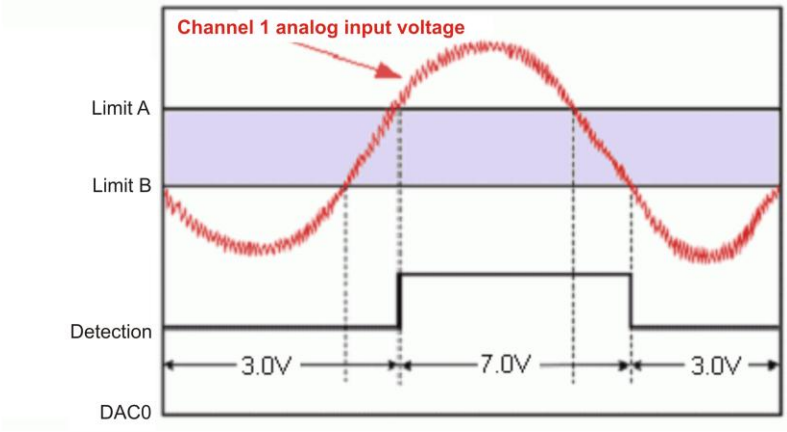


Figure 26. Channel 1 in hysteresis mode

Using multiple inputs to control one DAC output

Update mode: Rising edge, for each of two channels

Criteria used: Inside window, for each of two channels

Figure 27 shows how multiple inputs can update one output. In this figure, analog output channel DAC1 is being updated. Analog input Channel 1 has an inside-the-window setpoint applied. Whenever Channel 1's input goes inside the programmed window, DAC1 will be updated with 3.0 V.

Analog input Channel 2 also has an inside-the-window setpoint applied. Whenever channel 2's input goes inside the programmed window, DAC1 is updated with –7.0 V.

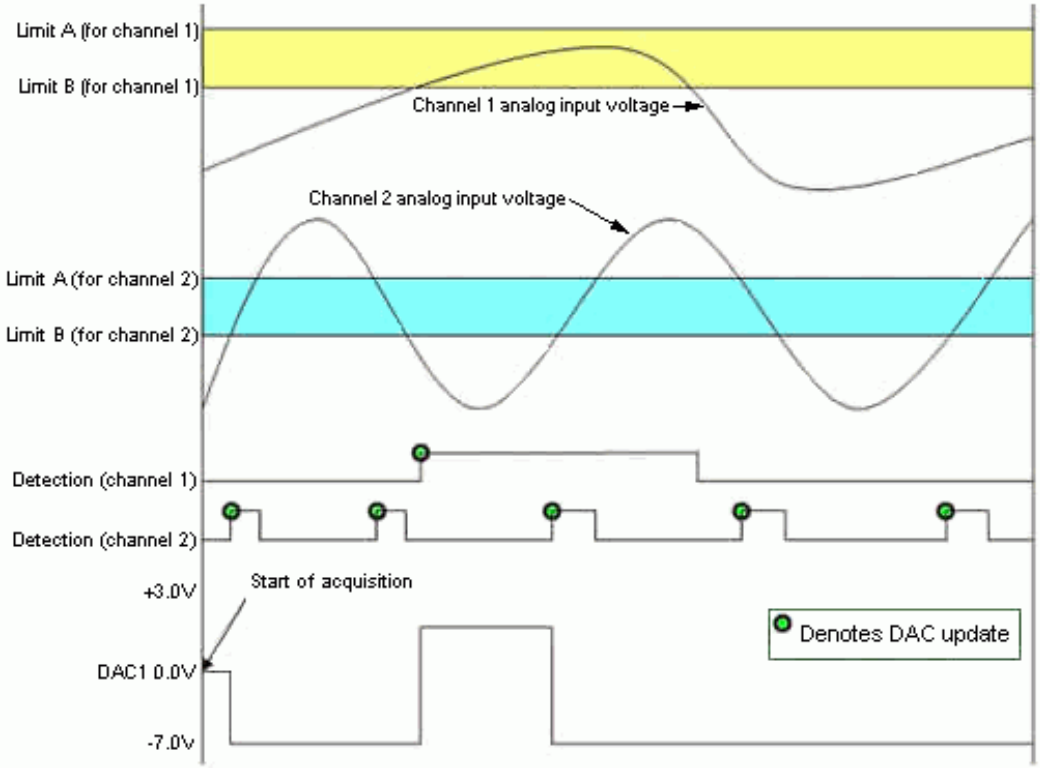


Figure 27. Using two criteria to control an output

The update on *True* only mode was selected, and therefore the updates for DAC1 only occur when the criteria is met. However, in the above figure we see that there are two setpoints acting on one DAC. We can also see that the two criteria can be met simultaneously. When both criteria are *True* at the same time, the DAC1 voltage is associated with the criteria that has been *most recently met*.

Setpoint detection on a totalizing counter

In Figure 28, CTR1 is a counter channel in totalize mode. Two setpoints define a point of change for Detect 1 as the counter counts upward. The detect output is high when inside the window (greater than limit B (low limit)) but less than limit A (the high limit).

In this case, the CTR1 setpoint is defined for the 16 lower bits of channel 1's 32-bit value. The digital output port's MSB could be updated on a *True* condition (the rising edge of the detection signal). You can also update one of the DAC output channels with a value.

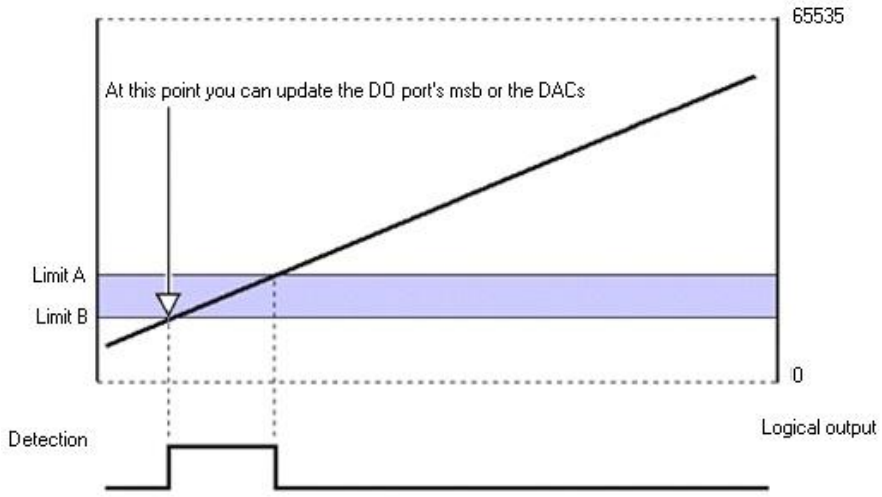


Figure 28. CTR1 in totalizing counter mode, inside the window setpoint

Controlling analog and digital outputs

You can program each setpoint with an 8-bit digital output byte and corresponding 8-bit mask byte. When the setpoint criteria is met, the digital output port's most significant byte (MSB) can be updated with the given byte and mask. You can also program each setpoint with a 16-bit DAC update value. Either DAC output can be updated in real time.

In *hysteresis mode*, each setpoint has two forced update values. Each update value can drive one DAC or the digital output port's most significant byte. *In hysteresis mode, the outputs do not change when the input values are inside the window*. One update value gets applied when the input values are less than the window, and a different update value gets applied when the input values are greater than the window.

Update on *True* and *False* uses two update values. The update values can drive DACs or the digital output port's most significant byte.

The digital output port's most significant byte is updated one sample period after the detection setpoint channel is sampled, plus up to 250 ns for data transfer from the detection setpoint channels. DAC output is updated one sample period after the detection setpoint channel is sampled, plus up to 1 µs for data transfer from the detection setpoint channels and data shifting out to the D/A converter. Update latencies can be improved with an increased sample rate.

When using setpoints to control the DAC outputs, increased latencies may occur if attempting to stream data to DACs or pattern digital output at the same time. The increased latency can be as long as the period of the DAC pacer clock. For these reasons, **avoid streaming outputs on any DAC or pattern digital output when using setpoints to control DACs**.

Update latency

USB-1602HS-2AO channels are read almost immediately. The response for a channel input detection does not occur until the next reading is taken, during the next tick of the acquisition clock. The maximum update latency is one sample period plus 250 ns for the most significant byte (MSB) of the digital output port, and 1 µs for DAC updates.

The detection circuit works on data that is put into the acquisition stream at the sample rate. This data is acquired according to the pre-acquisition setup (sampling group, sample period, etc.) and returned to the PC. Counters are latched into the acquisition stream when sampling begins. The actual counters may be counting much faster than the sample rate, and therefore only every 10^{th}, 100^{th}, or n^{th} count shows up in the acquisition data.

As a result, you can set a small detection window on a totalizing counter channel and have the detection setpoint "stepped over" since the sample period was too long. Even though the counter value stepped into and out of the detection window, the actual values going back to the PC may not. This is true no matter what mode the counter channel is in.

When setting a detection window, keep a sample period in mind. This applies to analog inputs and counter inputs. Quickly changing analog input voltages can step over a setpoint window if not sampled often enough, resulting in missed setpoint event.

There are three possible solutions for overcoming this problem:

- Shorten the sample period to give more timing resolution on the counter values or analog values.
- Widen the setpoint window by increasing limit A and/or lowering limit B.
- A combination of both of the above solutions could be made.

Using the setpoint status register

You can use the setpoint status register to check the current state of the 16 possible setpoints. In the register, Setpoint 0 is the least significant bit, and setpoint 15 is the most significant bit. Each setpoint is assigned a value of 0 or 1.

- A value of 0 indicates that the setpoint criteria is not met — the condition is *False*.
- A value of 1 indicates that the criteria is met — the condition is *True*.

In the following example, the criteria for setpoints 0, 1, and 4 is satisfied (*True*), but the criteria for the other 13 setpoints is not met.

Setpoint #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
True (1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1
False (0)	<<< Most significant bit							Least significant bit >>>								

From the above table we have 10011 binary, or 19 decimal; it is derived as follows:

- Setpoint 0, having a *True* state, shows 1, giving us decimal 1.
- Setpoint 1, having a *True* state, shows 1, giving us decimal 2.
- Setpoint 4, having a *True* state, shows 1, giving us decimal 16.

For proper operation, the setpoint status register must be the last channel sampled.

Calibrating the USB-1602HS-2AO

Every range of a USB-1602HS-2AO device is calibrated at the factory using a NIST traceable calibration process. Correction factors for each range are stored on the unit at the time of calibration.

The analog input calibration can be adjusted in the field without destroying the factory calibration. This is accomplished by having two independent calibration tables in the on-board EPROM: one table contains the original factory calibration, and the other table is used to store field calibration constants.

You can perform field calibration automatically in seconds with *Insta*Cal and without the use of external hardware or instruments. Field calibration traceability is derived through an on-board reference which has a stability of 0.005% per year. A two-year calibration period is recommended for the USB-1602HS-2AO.

Calibrate the USB-1602HS-2AO using *Insta*Cal after the board has fully warmed up. The recommended warm-up time is 15 minutes. For best results, calibrate the board immediately before making critical measurements. The high resolution analog components on the board are somewhat sensitive to temperature. Pre-measurement calibration ensures your board is operating at peak accuracy.

Specifications

All specifications are subject to change without notice.
Typical for 25 °C unless otherwise specified.
All signal names refer to 68 pin SCSI connector, unless otherwise specified.

Analog input

Table 1. Analog input specifications

Parameter	Conditions	Specification
A/D converter type		16-bit successive approximation type
Number of AI channels		2 SE simultaneous
Input configuration		Single-ended
Sampling method		Simultaneous; individual A/D per channel
Input ranges		±10 V, ±2.5 V, ±500 mV
Absolute maximum input voltage		*±30 V maximum (power on)* *±20 V maximum (power off)*
Input impedance		10 MΩ (typical, power on)
Input bias current		< 2 µA
Input bandwidth (-3 dB)		3 MHz, typical
Crosstalk	Remaining inputs grounded	100 dB (at 100 kHz)
Pacer sources		▪ Onboard A/D clock or external digital source (XAPCR or EXT CLK BNC) ▪ External pacing (XAPCR or EXT CLK BNC) See Table 12 for additional information.
Trigger sources and modes		See Table 11
Sampling rate		0.01 S/s to 2 MS/s each channel, software programmable
Clock sources		Internal, software programmable or external pacing
Resolution		16-bits
INL (integral non-linearity)		±2.0 LSB
DNL (differential non-linearity)		±1.0 LSB

Table 2. Calibrated accuracy

Range	Accuracy
±10 V	±1 mV
±2.5 V	±0.5 mV
±500 mV	±0.15 mV

Table 3. Noise performance, note 1

Range	Typical counts	LSB rms
±10 V	8	1.3
±2.5 V	11	1.6
±500 mV	17	2.5

Note 1: Noise distribution is determined by gathering 50,000 samples with inputs tied to ground at the BNC connectors. Samples are gathered at the maximum specified rate.

Table 4. SINAD (signal to noise and distortion) performance, note 2

Range	Typical SINAD, dB
±10 V	84
±2.5 V	82
±500 mV	77

Note 2: Calibrated and measured with a 10 kHz signal at 0.95 FSR, at the maximum sampling rate.

Table 5. ENOB (effective number of bits) performance, note 3

Range	Typical ENOB, Bits
±10 V	14
±2.5 V	13
±500 mV	13

Note 3: Calibrated and measured with a 10 kHz signal at 0.95 FSR, at the maximum sampling rate.

Table 6. SFDR (spurious-free dynamic range) performance, note 4

Range	Typical SFDR, dB
±10 V	95
±2.5 V	95
±500 mV	95

Note 4: SFDR is measured at the maximum sampling rate.

Analog output

Table 7. Analog output specifications

Parameter	Conditions	Specification
Number of channels		Two independent
Resolution		16-bits
Output range		±10 V
Throughput	Two channel	1 MS/s each channel
Pacer sources		▪ Internal pacing ▪ External pacing ▪ Pacing slaved to analog input pacing See Table 12 for additional information.
Monotonicity		16-bits
Glitch energy		< 12 nV/s
Current output		±5 mA maximum
Output coupling		DC
Power up state		DACs clear to midscale, (0 V, ±20 mV)
Output noise		3 mV rms maximum
Settling time (to .01%FS)	10 V output step, (R_L=5 kΩ, C_L=200 pf)	5 µS
Slew rate		10 V/µs
Gain error		±0.01% of FSR
Zero error		±0.0045 V maximum
INL		< 2 LSBs
DNL		< 1 LSB
Offset error drift		±10 ppm/°C
Gain error drift		±10 ppm/°C

Analog input calibration

Table 8. Analog input calibration specifications

Parameter	Specification
Recommended warm-up time	15 minutes minimum
Calibration methods	Software system calibration and self-calibration
Self-calibration	yes
System calibration interval	1 year
System calibration references	+8.192 V, +2.048 V, +0.4096 V ±5 mV. Actual measured values stored in EEPROM
	Tempco: 5 ppm/°C maximum
	Long term stability: 30 ppm/1000 h

Digital inputs

Table 9. Digital input specifications

Parameter	Specification
Number	16 inputs (DIN0-DIN15)
Digital type	3.3V CMOS (5V tolerant)
Digital input transfer rate (H/W-paced)	Up to 8 MHz — DIO-only operation 2 MHz — if configured for AI operations
Input high voltage	2.0 V minimum, 5.5 V maximum
Input low voltage	0.8 V maximum, 0 V minimum
Absolute maximum input voltage	15 V (power-on and power-off conditions)
DIN pacing	On-board or external clock (XAPCR)
Pacer sources	▪ Internal pacer clock or external digital source (XAPCR or EXT CLK BNC). ▪ External pacer clock (XAPCR or EXT CLK BNC) See Table 12 for additional information.
DIN trigger modes and sources	See Table 11
Input pull-ups	100 kΩ (consult factory for alternative options)
Latency, software paced	115 ms, typical (system dependant)

Digital outputs

Table 10. Digital output specifications

Parameter	Specification
Number	16 outputs (DOUT0-DOUT15)
Digital output rate	8 MHz maximum if no analog outputs are enabled, (1 MHz maximum if analog outputs are enabled)
Digital type	3.3 V CMOS
Output high voltage (IOH = –2.5 mA)	2.4 V minimum, 3.4 V maximum
Output low voltage (IOL = 2.5 mA)	0.4 V maximum, 0 V minimum
Output current	2.5 mA maximum per pin
DOUT pacing	On-board or external clock (XDPCR)
Pacer sources	▪ Internal pacing ▪ External pacing ▪ Pacing slaved to analog input pacing See table 12 for additional information.
Outputs at power on and reset	Low
Latency, software paced	115 ms, typical (system dependant)

Trigger sources

Table 11. External trigger specifications

Parameter	Specification
Available trigger sources	▪ Analog input hardware ▪ Analog software trigger ▪ External digital input ▪ Digital pattern ▪ Counter/totalizer
Trigger source details	
Analog input (hardware) trigger (CH0 – CH1)	Input signal range: entire span of selected voltage range Channel selectable Trigger level: Programmable (12-bit resolution) Hysteresis: Programmable (12-bit resolution) Latency: 1.25 uS typical Accuracy: ±2% of reading, ±10 mV offset maximum
Analog software trigger (CH0 – CH1)	Trigger range: Anywhere within range of the trigger channel Trigger level: Programmable (16-bit resolution) Latency: one sample period (maximum)
External digital: ▪ (EXT TRIG — BNC or ▪ DIG TRIG — SCSI	Input signal range: –15 V to +15 V maximum Trigger level: TTL level sensitive Minimum pulse width: 50 ns high, 50 ns low Latency: 100ns maximum
Digital pattern triggering DIN0-15	▪ 16-bit pattern triggering on the digital port, DIN0-DIN15 ▪ Programmable for trigger on equal, not equal, above, or below a value. ▪ Individual bits can be masked for "don't care" condition. ▪ Latency: One sample period, maximum
Counter/totalizer triggering: (CTR0-3)	Counter/totalizer inputs (CTR0-3) can trigger an acquisition. User can select to trigger on a frequency or on total counts that are equal, not equal, above, or below a value, or within/outside of a window rising/falling edge. Latency: One sample period, maximum

Pacing sources

Table 12. Pacing specifications

Parameter	Specification
Pacer clocks (2) ▪ Input pacer ▪ Output pacer	Input pacer: ▪ For pacing A/D, DIN and Counter signals ▪ Can be internally generated or externally supplied (XAPCR) ▪ XAPCR is accessible from front BNC or rear SCSI connector Output pacer: ▪ For pacing DAC, DOUT and Timer/PWM signals ▪ Can be internally generated or externally supplied (XDPCR)
Input pacer clock sources (2) ▪ Internal, programmable ▪ External (XAPCR)	Internal, programmable: ▪ Analog channels from 500 ns to 1000s in 20.83 ns steps. ▪ DIN channels and counters from 125 ns* to 100 s in 20.83 ns steps. ▪ Can be configured to pace AO and/or DOUT channels External, TTL level input (XAPCR): ▪ A/D channels down to 500 ns minimum ▪ DIN channels and counters down to 125 ns* minimum ▪ Can be configured to pace DAC and/or DOUT channels
Input pacer rate Internal or external, (XAPCR) source	Analog: 2 MHz maximum Digital: 8 MHz if no analog channels are enabled. 2 MHz with analog channels enabled.
Pacer input high voltage	2.0 V minimum, 5.5 V maximum
Pacer input low voltage	0.8 V maximum, 0 V minimum
Minimum pulse width	50 ns high, 50 ns low
Output pacer clock sources (4)	▪ Internal output pacer clock, (independent of input pacer clock) ▪ External output pacer clock, XDPCR ▪ Internal input pacing clock ▪ External input pacing clock, XAPCR
Output pacer rate Internal or external, (XDPCR) source	Analog: 1.0 MHz maximum Digital: 8 MHz, if no analog outputs are enabled, (1 MHz if DAC outputs are enabled)
Internal pacer routed to BNC or SCSI conn. ▪ Output high voltage (IOH = –2.5 mA): ▪ Output low voltage (IOL = 2.5 mA):	XAPCR or XDPCR ▪ 2.4 V minimum ▪ 0.4 V maximum

Counters

Table 13. Counter specifications

Parameter	Specification
Number of channels	4 independent CTRL 0,1,2,3 (may be configured as gated if desired)
Modes	Counter, Period, Pulse width, Timing
Counter mode options	Totalize, Clear on Read, Rollover, Stop at top, 16-bit or 32-bit, any other channel can decrement the counter
Period mode options	Measure x1, x10, x100, or x1000 periods, 16-bit or 32-bit, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 µs, 20.83 µs), any other channel can gate the period measurement
Pulse width mode options	16-bit or 32-bit values, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 µs, 20.83 µs), any other channel can gate the pulse width measurement
Timing mode options	16-bit or 32-bit values, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 µs, 20.83 µs)
Resolution	16 or 32-bits
Maximum input frequency	20 MHz
Input type	TTL, rising edge triggered
Absolute maximum input voltage	15V
De-bounce function	16 selections, from 500ns to 25.5ms, pos or neg edge, glitch detect and/or de-bounce modes
Required input current	*±5 µA*
Minimum pulse width	*25 nS high, 25 ns low*
Input high voltage	2.0 V minimum, 5.5 V maximum
Input low voltage	0.8 V maximum, 0 V minimum

Timers

Table 14. Timer specifications

Parameter	Conditions	Specification
Number of channels		Two: TMR/PWM0, TMR/PWM1
Effective frequency range		0.0112 Hz to 24 MHz
Period resolution		20.83 nS
Pulse width resolution		20.83 nS
Output high voltage (IOH = –2.5 mA)		2.4 V minimum
Output low voltage (IOL = 2.5 mA)		0.4 V maximum
Output current		2.5 mA maximum per pin

Quadrature decoders

Table 15. Quadrature decoder specifications

Parameter	Conditions	Specification
Number of decoders		3 (CTR4A, B, Z; CTR5 A, B, Z; CTR6 A, B, Z)
Signals per decoder		A, B and Z
Resolution		16 or 32-bits
Maximum frequency		6 MHz
Minimum pulse width		*25 nS high, 25 ns low*
De-bounce function		16 selections, from 500 ns to 25.5 ms, positive or negative edge, glitch detect, and/or de-bounce modes
Input high voltage		2.0 V minimum, 5.5 V maximum
Input low voltage		0.8 V maximum, 0 V minimum
Absolute maximum input voltage		15 V

Power

Table 16. Power specifications

Parameter	Conditions	Specification
Supply current	Continuous mode	1.5 Amp maximum
+5V EXT output voltage range		4.75 V to 5.25 V
Isolation	Measurement system to PC	500 VDC minimum
AC power adapter specifications (MCC part number PS-5V2AEPS)		
Output voltage		5V, ±5%
Output power		10 watts
Power jack configuration		Two conductor, barrel
Power jack barrel diameter		6.3 mm
Power jack pin diameter		2.0 mm
Power jack polarity		Center positive

USB specifications

Table 17. USB specifications

Parameter	Specification
USB device type	USB 2.0 (high-speed)
USB device compatibility	USB 1.1, 2.0
USB cable length	Three meters maximum.
USB cable type	A-B cable, UL type AWM 2527 or equivalent (minimum 24 AWG VBUS/GND, minimum 28 AWG D+/D-).

Environmental

Table 18. Environmental specifications

Parameter	Specification
Operating temperature range	0 to 55 °C maximum
Storage temperature range	-40 to 85 °C maximum
Humidity	0 to 90% non-condensing

Mechanical

Table 19. Mechanical specifications

Parameter	Specification
Dimensions	142.2 mm W x 180.3 mm D x 38.1 mm H (5.6" x 7.1" x 1.5")
Weight	675 g (1.5 lbs)

I/O cables, connectors and accessories

Table 20. Cables, connectors and accessory specifications

Parameter	Specification
I/O connector type	68-pin standard "SCSI TYPE III" female connector
Compatible cables (for the 68-pin SCSI connector)	▪ CA-68-3R — 68-pin ribbon cable; 3 feet. ▪ CA-68-3S — 68-pin shielded round cable; 3 feet. ▪ CA-68-6S — 68-pin shielded round cable; 6 feet.
Compatible accessory products (for the 68-pin SCSI connector)	▪ TB-102 termination board with screw terminals ▪ RM-TB-100, 19-inch rack mount kit for TB-102

Signal I/O connectors

BNC connectors

Table 21. BNC connectors pin out

BNC signals	Function
CH0	Analog input CH0
CH1	Analog input CH1
EXT TRIG	BNC connection for DIG TRIG*
EXT CLK	BNC connection for XAPCR clock*

*These signals also available at SCSI connector

68-pin SCSI connector

Table 22. 68-pin SCSI connector pin out

Pin No.	Signal	Pin No.	Signal
1	AGND	35	AGND
2	RESERVED	36	RESERVED
3	AGND	37	AGND
4	RESERVED	38	RESERVED
5	AGND	39	AGND
6	VCAL	40	DAC 0
7	+5V PWR	41	DAC 1
8	AGND	42	AGND
9	DIN0	43	DOUT0
10	DIN1	44	DOUT1
11	DIN2	45	DOUT2
12	DIN3	46	DOUT3
13	DIN4	47	DOUT4
14	DIN5	48	DOUT5
15	DIN6	49	DOUT6
16	DIN7	50	DOUT7
17	DIN8	51	DOUT8
18	DIN9	52	DOUT9
19	DIN10	53	DOUT10
20	DIN11	54	DOUT11
21	DIN12	55	DOUT12
22	DIN13	56	DOUT13
23	DIN14	57	DOUT14
24	DIN15	58	DOUT15
25	CTR4 A	59	CTR0
26	CTR4 B	60	CTR1
27	CTR4 Z	61	CTR2
28	CTR5 A	62	CTR3
29	CTR5 B	63	TMR/PWM0
30	CTR5 Z	64	TMR/PWM1
31	CTR6 A	65	DIG TRIG
32	CTR6 B	66	XAPCR
33	CTR6 Z	67	XDPCR
34	DGND	68	DGND

CE Declaration of Conformity

Manufacturer: Measurement Computing Corporation
Address: 10 Commerce Way
Suite 1008
Norton, MA 02766
USA

Category: Electrical equipment for measurement, control and laboratory use.

Measurement Computing Corporation declares under sole responsibility that the product

USB-1602HS-2AO

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EC EMC Directive 2004/108/EC: General Requirements, EN 61326-1:2006 (IEC 61326-1:2005).

Emissions:

- EN 55011 (2007) / CISPR 11(2003): Radiated emissions: Group 1, Class A
- EN 55011 (2007) / CISPR 11(2003): Conducted emissions: Group 1, Class A

Immunity: EN 61326-1:2006, Table 3.

- IEC 61000-4-2 (2001): Electrostatic Discharge immunity.
- IEC 61000-4-3 (2002): Radiated Electromagnetic Field immunity.
- IEC 61000-4-4 (2004): Electric Fast Transient Burst Immunity.
- IEC 61000-4-5 (2001): Surge Immunity.
- IEC 61000-4-6 (2003): Radio Frequency Common Mode Immunity.
- IEC 61000-4-11 (2004): Voltage Interrupts.

To maintain compliance to the standards of this declaration, the following conditions must be met.

- The host computer, peripheral equipment, power sources, and expansion hardware must be CE compliant.
- All I/O cables must be shielded, with the shields connected to ground.
- I/O cables must be less than 3 meters (9.75 feet) in length.
- The host computer must be properly grounded.
- Equipment must be operated in a controlled electromagnetic environment as defined by Standards EN 61326-1:2006, or IEC 61326-1:2005.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in February, 2009. Test records are outlined in Chomerics Test Report #EMI5276.09.

We hereby declare that the equipment specified conforms to the above Directives and Standards.

Carl Haapaoja, Director of Quality Assurance

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