

# PCI-DAS1001

## Specifications



**MEASUREMENT  
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# Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

## Analog input

Table 1. Analog input specifications

Parameter	Specification
<i>A/D converter type</i>	7800
Resolution	12 bits
Number of channels	8 differential or 16 single-ended, software selectable
Input ranges	$\pm 10$ V, $\pm 1$ V, $\pm 0.1$ V, $\pm 0.01$ V, 0 to 10 V, 0 to 1 V, 0 to 0.1 V, 0 to 0.01 V. Fully programmable
Polarity	Unipolar/bipolar, software selectable
A/D pacing	Programmable: internal counter or external source (A/D External Pacer, positive or negative edge selectable by software), or software polled
Burst mode	Software selectable option, rate = 6.67 $\mu$ s
A/D trigger sources	External digital (A/D External Trigger)
A/D triggering modes	Digital: Software enabled, rising edge, hardware trigger Pre-trigger: Unlimited pre- and post-trigger samples. Total # of samples must be > 512.
Data transfer	From 1024 sample FIFO via REPINSW, interrupt or software polled
<i>A/D conversion time</i>	3 $\mu$ s
Throughput	150 kHz
Relative accuracy	$\pm 1.5$ LSB
Differential linearity error	$\pm 0.75$ LSB
Integral linearity error	$\pm 0.5$ LSB typ, $\pm 1.5$ LSB max
Gain error (relative to calibration reference)	0.01 V range: $\pm 0.4\%$ of reading, max All other ranges: $\pm 0.02\%$ of reading, max
<i>No missing codes guaranteed</i>	12 bits
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM
<i>Gain drift (A/D specs)</i>	$\pm 6$ ppm/ $^{\circ}$ C
<i>Zero drift (A/D specs)</i>	$\pm 1$ ppm/ $^{\circ}$ C
Common mode range	$\pm 10$ V
CMRR @ 60 Hz	70 dB
<i>Input leakage current</i>	200 nA
<i>Input impedance</i>	10 MOhms, min
<i>Absolute maximum input voltage</i>	$\pm 35$ V
Noise distribution	Rate = 1-150 kHz, average # bins 10 V ranges: 3 bins 1 V ranges: 4 bins 0.1 V ranges: 10 bins Bipolar 0.01 V range: 20 bins Unipolar 0.01 V range: 32 bins

## Analog output

Table 2. Analog output specifications

Parameter	Specification
<i>D/A type</i>	AD7847AR
<i>Resolution</i>	12 bits
<i>Number of channels</i>	2
<i>Output ranges</i>	±10 V, ±5 V, 0 to 5 V, 0 to 10 V. Each channel independently programmable.
<i>D/A pacing</i>	Software
<i>Data transfer</i>	Programmed I/O
<i>Offset error</i>	±600 µV max, all ranges (calibrated)
<i>Gain error</i>	±0.02% FSR max (calibrated)
<i>Differential nonlinearity</i>	±1 LSB max
<i>Integral nonlinearity</i>	±1 LSB max
<i>Monotonicity</i>	12 bits
<i>D/A gain drift</i>	±2 ppm/°C max
<i>D/A bipolar offset drift</i>	±5 ppm/°C max
<i>D/A unipolar offset drift</i>	±5 ppm/°C max
<i>Throughput</i>	PC dependent
<i>Settling time (to 0.01% of 10 V step)</i>	4 µs typ
<i>Slew rate</i>	7 V/µS
<i>Current drive</i>	±5 mA min
<i>Output short-circuit duration</i>	25 mA indefinite
<i>Output coupling</i>	DC
<i>Amp output impedance</i>	0.1 Ohms max
<i>Miscellaneous</i>	Power up and reset, all DACs cleared to 0 V, ±200 mV

## Digital input/output

Table 3. DIO specifications

Parameter	Specification
<i>Digital type</i>	82C55A
<i>Configuration</i>	2 banks of 8, 2 banks of 4, programmable by bank as input or output
<i>Number of channels</i>	24 I/O (FIRSTPORTA 0 through FIRSTPORTC 7)
<i>Output high</i>	3.0 V, min @ -2.5 mA
<i>Output low</i>	0.4 V, max @ 2.5 mA
<i>Input high</i>	2.0 V, min, +5.5 V absolute, max
<i>Input low</i>	0.8 V, max, -0.5 V absolute, min
<i>Power-up / reset state</i>	Input mode (high impedance)
<i>Interrupts</i>	INTA# - mapped to IRQn via PCI BIOS at boot-time
<i>Interrupt enable</i>	Programmable
<i>Interrupt sources</i>	Residual counter, end-of-channel-scan, AD-FIFO-not-empty, AD-FIFO-half-full

## Counter section

Table 4. Counter specifications

Parameter		Specification
<i>Counter type</i>		82C54
<i>Configuration</i>		Two 82C54 devices. 3 down counters per 82C54, 16 bits each
82C54A:	Counter 0 - ADC residual sample counter	<ul style="list-style-type: none"> <li>▪ Source: ADC Clock.</li> <li>▪ Gate: Internal programmable source.</li> <li>▪ Output: End-of-Acquisition interrupt.</li> </ul>
	Counter 1 - ADC pacer lower divider	<ul style="list-style-type: none"> <li>▪ Source: 10 MHz oscillator</li> <li>▪ Gate: tied to counter 2 gate, programmable source.</li> <li>▪ Output: chained to counter 2 clock.</li> </ul>
	Counter 2 - ADC pacer upper divider	<ul style="list-style-type: none"> <li>▪ Source: counter 1 output.</li> <li>▪ Gate: Tied to counter 1 gate, programmable source.</li> <li>▪ Output: ADC pacer clock (if software selected), available at user connector.</li> </ul>
82C54B:	Counter 0 - pretrigger mode	<ul style="list-style-type: none"> <li>▪ Source: ADC clock</li> <li>▪ Gate: external trigger</li> <li>▪ Output: End-of-Acquisition interrupt</li> </ul>
	Counter 0 - user counter 4 (when in non-pretrigger mode)	<ul style="list-style-type: none"> <li>▪ Source: User input at 100-pin connector (CLK4) or internal 10 MHz (software selectable)</li> <li>▪ Gate: user input at 100-pin connector (GATE4)</li> <li>▪ Output: available at 100-pin connector (OUT4)</li> </ul>
	Counter 1 - user counter 5	<ul style="list-style-type: none"> <li>▪ Source: user input at 100-pin connector (CLK5)</li> <li>▪ Gate: user input at 100-pin connector (GATE5)</li> <li>▪ Output: available at 100-pin connector (OUT5)</li> </ul>
	Counter 2 - user counter 6	<ul style="list-style-type: none"> <li>▪ Source: user input at 100-pin connector (CLK6)</li> <li>▪ Gate: user input at 100-pin connector (GATE6)</li> <li>▪ Output: available at 100-pin connector (OUT6)</li> </ul>
<i>Clock input frequency</i>		10 MHz max
<i>High pulse width (clock input)</i>		30 ns min
<i>Low pulse width (clock input)</i>		50 ns min
<i>Gate width high</i>		50 ns min
<i>Gate width low</i>		50 ns min
<i>Input low voltage</i>		0.8 V max
<i>Input high voltage</i>		2.0 V min
<i>Output low voltage</i>		0.4 V max
<i>Output high voltage</i>		3.0 V min

## Power consumption

Table 5. Power consumption specifications

Parameter	Specification
+5 V operating (A/D converting to FIFO)	0.8 A typical, 1.0 A max

## Environmental

Table 6. Environmental specifications

Parameter	Specification
<i>Operating temperature range</i>	<i>0 to 70 °C</i>
<i>Storage temperature range</i>	<i>-40 to 100 °C</i>
<i>Humidity</i>	<i>0 to 90% non-condensing</i>

## Main connector and pin out

Connector type	100-pin high density Robinson Nugent	
Compatible cable	C100FF-x, unshielded ribbon cable. x = length in feet	
Compatible accessory products (with C100FF-x cable)	ISO-RACK16/P ISO-DA02/P CIO-ERB24 (DADP-5037 adaptor required) CIO-SERB24 (DADP-5037 adaptor required) SSR-RACK24 (DADP-5037 adaptor required)	BNC-16SE BNC-16DI CIO-MINI50 (2 required) CIO-TERM100 (1 required) SCB-50 (1 required)

### 8-channel differential mode pin out

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0
2	CH0 IN HI	52	FIRSTPORTA Bit 1
3	CH0 IN LO	53	FIRSTPORTA Bit 2
4	CH1 IN HI	54	FIRSTPORTA Bit 3
5	CH1 IN LO	55	FIRSTPORTA Bit 4
6	CH2 IN HI	56	FIRSTPORTA Bit 5
7	CH2 IN LO	57	FIRSTPORTA Bit 6
8	CH3 IN HI	58	FIRSTPORTA Bit 7
9	CH3 IN LO	59	FIRSTPORTB Bit 0
10	CH4 IN HI	60	FIRSTPORTB Bit 1
11	CH4 IN LO	61	FIRSTPORTB Bit 2
12	CH5 IN HI	62	FIRSTPORTB Bit 3
13	CH5 IN LO	63	FIRSTPORTB Bit 4
14	CH6 IN HI	64	FIRSTPORTB Bit 5
15	CH6 IN LO	65	FIRSTPORTB Bit 6
16	CH7 IN HI	66	FIRSTPORTB Bit 7
17	CH7 IN LO	67	FIRSTPORTC Bit 0
18	LLGND	68	FIRSTPORTC Bit 1
19	N/C	69	FIRSTPORTC Bit 2
20	N/C	70	FIRSTPORTC Bit 3
21	N/C	71	FIRSTPORTC Bit 4
22	N/C	72	FIRSTPORTC Bit 5
23	N/C	73	FIRSTPORTC Bit 6
24	N/C	74	FIRSTPORTC Bit 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	CTR6 CLK
31	N/C	81	CTR6 GATE
32	N/C	82	CTR6 OUT
33	N/C	83	N/C
34	N/C	84	N/C
35	D/A GND 0	85	CTR5 CLK
36	D/A OUT 0	86	CTR5 GATE
37	D/A GND 1	87	CTR5 OUT
38	D/A OUT 1	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	N/C	93	N/C
44	N/C	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	N/C
47	N/C	97	N/C
48	PC +5V	98	N/C
49	N/C	99	N/C
50	GND	100	GND

**16-channel single-ended mode pin out**

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0
2	CH0 IN	52	FIRSTPORTA Bit 1
3	CH8 IN	53	FIRSTPORTA Bit 2
4	CH1 IN	54	FIRSTPORTA Bit 3
5	CH9 IN	55	FIRSTPORTA Bit 4
6	CH2 IN	56	FIRSTPORTA Bit 5
7	CH10 IN	57	FIRSTPORTA Bit 6
8	CH3 IN	58	FIRSTPORTA Bit 7
9	CH11 IN	59	FIRSTPORTB Bit 0
10	CH4 IN	60	FIRSTPORTB Bit 1
11	CH12 IN	61	FIRSTPORTB Bit 2
12	CH5 IN	62	FIRSTPORTB Bit 3
13	CH13 IN	63	FIRSTPORTB Bit 4
14	CH6 IN	64	FIRSTPORTB Bit 5
15	CH14 IN	65	FIRSTPORTB Bit 6
16	CH7 IN	66	FIRSTPORTB Bit 7
17	CH15 IN	67	FIRSTPORTC Bit 0
18	LLGND	68	FIRSTPORTC Bit 1
19	N/C	69	FIRSTPORTC Bit 2
20	N/C	70	FIRSTPORTC Bit 3
21	N/C	71	FIRSTPORTC Bit 4
22	N/C	72	FIRSTPORTC Bit 5
23	N/C	73	FIRSTPORTC Bit 6
24	N/C	74	FIRSTPORTC Bit 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	CTR6 CLK
31	N/C	81	CTR6 GATE
32	N/C	82	CTR6 OUT
33	N/C	83	N/C
34	N/C	84	N/C
35	D/A GND 0	85	CTR5 CLK
36	D/A OUT 0	86	CTR5 GATE
37	D/A GND 1	87	CTR5 OUT
38	D/A OUT 1	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	N/C	93	N/C
44	N/C	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	N/C
47	N/C	97	N/C
48	PC +5V	98	N/C
49	N/C	99	N/C
50	GND	100	GND

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