SPECIFICATIONS

CIO-DAS800

Analog Input & Digital I/O

Revision 2, October, 2000

Power consumption

+5V quiescent	450 mA typical, 600 mA max

Analog input section

A/D converter type	AD674A, Successive Approximation
Resolution	12 bits
Number of channels	8
Input Ranges	±5V fixed
Polarity	Bipolar fixed
A/D pacing	Programmable: internal counter or external source (IR Input / XCLK, falling edge) or software-polled
A/D Trigger sources	External hardware (Digital In 1 / Trig, rising edge)
Data transfer	Interrupt or software-polled from 256 sample FIFO buffer
Channel configuration	Single-ended
DMA	None
A/D conversion time	20 µs
Throughput	50 kHz
Accuracy	±0.01% of full scale ±1 LSB typ, ±0.05% of full scale ±1 LSB max
Differential Linearity error	±0.5 LSB max
Integral Linearity error	±1 LSB
No missing codes (guaranteed)	12 bits
Gain drift (A/D specs)	±50 ppm/°C
Zero drift (A/D specs)	±10 ppm/°C
Common Mode Range	±10V
CMRR @ 60 Hz	70 dB min
Input leakage current (@ 25deg C)	± 30 nA
Input leakage current (over temp.)	±250 nA
Input impedance	>1000 MegOhm typical
Absolute maximum input voltage	±35V

Digital I/O section

Digital type	FPGA
Configuration	Two ports, 3 input and 4 output
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.32V max (IOL = 4 mA)
Output high voltage	3.86V min (IOH = –4 mA)
Absolute max. input voltage	–0.5V, +5.5V
Interrupts	Jumper selectable: levels 2, 3, 4, 5, 6, 7 or not connected Positive-edge triggered
Interrupt enable:	Programmable
Interrupt sources:	Ext. (IR Input / XCLK), A/D End-of-Conv., A/D FIFO Half-Full

Counter section

Counter type	82C54
Configuration	3 down-counters , 16 bit resolution

Counter 0 - independent user counter

Source:	external, user connector (Counter 0 In)
Gate:	external, user connector (Gate 0)
Output:	user connector (Counter 0 Out)

Counter 1 - ADC Pacer Lower Divider or independent user counter

Source:	user connector (Counter 1 In) and optionally, Counter 2 Out, selectable by software
Gate:	Programmable, disabled or user connector (Gate 1)
Output:	User connector (Counter 1 Out) and optionally to A/D start convert, software-selectable

Counter 2 - ADC Pacer Upper Divider

Source:	Internal 1 MHz oscillator
Gate:	Programmable, disabled or user connector (Gate 2)
Output:	User connector (Counter 2 Out) and optionally to counter 1 input, software selectable

Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min
Crystal oscillator	
Frequency	1 MHz
Frequency accuracy	100 ppm

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	–20 to 70°C
Humidity	0 to 90% non-condensing

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