

SPECIFICATIONS

CIO-DAS08-AOH

CIO-DAS08-AOM

CIO-DAS08-AOL

Analog Input & Digital I/O



**MEASUREMENT
COMPUTING™**

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Power consumption

+5V: 670 mA typical, 840 mA max

Analog Input Section

| | |
|-----------------------------------|---|
| A/D converter type | 574AJ |
| Resolution | 12 bits |
| Number of channels | 8 differential (configurable as quasi-differential via installation of SIP resistor) |
| Input Ranges | |
| CIO-DAS08-AOH | $\pm 10V, \pm 5V, \pm 1V, \pm 0.5V, \pm 0.1V, \pm 0.05V, \pm 0.01V, \pm 0.005V, 0$ to 10V, 0 to 1V, 0 to 0.1V, 0 to 0.01V software-selectable |
| CIO-DAS08-AOL | $\pm 10V, \pm 5V, \pm 2.5V, \pm 1.25V, \pm 0.625V, 0$ to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V software selectable |
| CIO-DAS08-AOM | $\pm 10V, \pm 5V, \pm 0.5V, \pm 0.05V, \pm 0.01V, 0$ to 10V, 0 to 1V, 0 to 0.1V, 0 to 0.01V software selectable |
| Polarity | Unipolar/Bipolar, software selectable |
| A/D pacing | Internal counter or external source (Interrupt Input, jumper selectable, rising edge) or software polled |
| A/D Trigger sources | External hardware/software (Digital In 1) |
| Data transfer | Interrupt or software-polled |
| DMA | None |
| A/D conversion time | 25 μ s |
| Throughput | 20 KHz, PC dependent |
| Accuracy | $\pm 0.01\%$ of reading ± 1 LSB |
| $\pm 0.05\%$ of full scale | |
| Differential Linearity error | ± 1 LSB |
| Integral Linearity error | ± 0.5 LSB |
| No missing codes guaranteed | 12 bits |
| Gain drift (A/D specs) | ± 25 ppm/ $^{\circ}$ C |
| Zero drift (A/D specs) | ± 10 μ V/ $^{\circ}$ C |
| Common Mode Range | $\pm 10V$ |
| CMRR | 72 dB |
| Input leakage current (@25 Deg C) | 100 nA |
| Input impedance | 10 Meg Ohms min |
| Absolute maximum input voltage | $\pm 35V$ |

Analog Output:

| | |
|---------------------------|--|
| D/A converter type | AD7237 dual DAC |
| Resolution | 12 bits |
| Number of channels | 2 |
| Output Ranges | $\pm 10V, \pm 5V, \pm 2.5V, \pm 1.67V, 0$ to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.67V Each channel independently switch selectable |
| Offset error | ± 1 LSB max (adjustable to 0 with potentiometer) |
| Gain error | ± 1 LSB max (adjustable to 0 with potentiometer) |
| Differential nonlinearity | ± 0.9 LSB max |
| Integral nonlinearity | ± 1 LSB max |
| Monotonicity | Guaranteed monotonic to 12 bits over temperature |

| | |
|--|--------------------------------|
| D/A Gain drift | ±3 ppm/°C max |
| D/A Bipolar offset drift | ±30 ppm/°C max |
| D/A Unipolar offset drift | ±50 ppm/°C max |
| D/A pacing | Software paced |
| D/A trigger modes | Software |
| Data transfer | Programmed I/O |
| Settling time (D/A converter) (full scale step to ±0.5 LSB) | 8 µs max |
| Slew Rate (OP07) | 0.3V/µs |
| Current Drive | ±5 mA |
| Output short-circuit duration | indefinite |
| Output coupling | DC |
| Output impedance | 0.1 Ohms max |
| Miscellaneous | Double buffered output latches |
| Update DACs individually or simultaneously (jumper selectable) | |

Digital Input / Output

| | |
|--------------------------------------|---|
| Digital Type (main connector) | |
| Output: | 74LS273 |
| Input: | 74LS244 |
| Configuration | 4 fixed output bits, 3 fixed input bits |
| Number of channels | 4 out, 3 in |
| Output High | 2.7 volts min @ -0.4 mA |
| Output Low | 0.4 volts max @ 8 mA |
| Input High | 2.0 volts min, 7 volts absolute max |
| Input Low | 0.8 volts max, -0.5 volts absolute min |
| Output power-up / reset state | low |
| Digital Type (Digital I/O connector) | 82C55 |
| Configuration | 2 banks of 8, 2 banks of 4, programmable by bank as input or output |
| Number of channels | 24 I/O |
| Output High | 3.0 volts min @ -2.5mA |
| Output Low | 0.4 volts max @ 2.5mA |
| Input High | 2.0 volts min, 5.5 volts absolute max |
| Input Low | 0.8 volts max, -0.5 volts absolute min |
| Power-up / reset state | Input mode (high impedance) |
| Interrupts | 2 through 7, jumper-selectable |
| Interrupt enable | Programmable |
| Interrupt sources | External (Interrupt In), rising edge |

Counter section

| | |
|--|---------------------------------|
| Counter type | 82C54 |
| Configuration | 3 down-counters, 16 bits each |
| Counter 0 - independent, user configurable | |
| Source: | user connector (Counter 0 In) |
| Gate: | tied high through 10k (enabled) |
| Output: | user connector (Counter 0 Out) |

Counter 1 - independent, user configurable

Source: user connector (Counter 1 In)
Gate: user connector (Gate 1)
Output: user connector (Counter 1 Out)

Counter 2 - independent, user configurable

Source: 1MHz (from 10MHz Xtal via divide-by-ten) or PC SysClk (via divide by 2 circuit) selectable by jumper
Gate: user connector (Gate 2)
Output: user connector (Counter 2 Out)

| | |
|--------------------------------|------------|
| Clock input frequency | 10 Mhz max |
| High pulse width (clock input) | 30 ns min |
| Low pulse width (clock input) | 50 ns min |
| Gate width high | 50 ns min |
| Gate width low | 50 ns min |
| Input low voltage | 0.8V max |
| Input high voltage | 2.0V min |
| Output low voltage | 0.4V max |
| Output high voltage | 3.0V min |

Environmental

| | |
|-----------------------------|-------------------------|
| Operating temperature range | 0 to 50°C |
| Storage temperature range | -20 to 70°C |
| Humidity | 0 to 95% non-condensing |

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