# SPECIFICATIONS

# CIO-DAC04/12-HS

# Quad 12-bit Analog Outputs

## Power Consumption

| | |
|---|---|
| +5V supply | 520 mA typ, 610 mA max. |

## Analog Output

| | |
|---|---|
| Resolution | 12 bits |
| Number of channels | 4 Voltage Output |
| D/A type | AD7948BN |
| Voltage Ranges | $\pm2.5$, $\pm5$, $\pm10$, 0 to 2.5, 0 to 5, 0 to 10, switch-selectable, each channel independently |
| D/A Pacing | Internal or external clock (EXTPACER) on falling edge or software-paced |
| D/A Gating | External (EXTGATE), active high |
| Data Transfer | Programmed I/O |
| | From 1024 FIFO via programmed I/O or REP-OUTSW interrupt |
| Offset error | Adjustable to zero |
| Gain error | Adjustable to zero |
| Differential nonlinearity | $\pm0.5$ LSB max. |
| Integral nonlinearity | $\pm0.5$ LSB max. |
| Monotonicity | Guaranteed monotonic to 12 bits over temperature |
| D/A Gain drift | 5 ppm FSR/°C max. |
| Throughput | PC-dependent, 250 kHz max. |
| Settling time (20V step to .01%) | 1µs typical, 1.5µs max |
| Slew rate | 32V/µs typical |
| Current Drive | $\pm5$ mA typical |
| Output short-circuit duration | 20 mA min Continuous |
| Output Coupling | DC |
| Miscellaneous | Double buffered output latches |
| | Update DACs individually or simultaneously (software-selectable) |

Simultaneous mode requires that channel 3 is always included in the channels to be updated.

State of analog outputs at power-up is un-defined.

When using the internal pacer, the user must physically disconnect any signal connected to the EXTPACER input on the User Connector.

## Digital Input / Output

| | |
|---|---|
| Digital Type | |
| Input: | 74LS244 |
| Output: | 74LS273 |
| Configuration | 2 banks of 8, 1 bank as input, 1 bank as output |
| Number of channels | 16 |
| Output High | 2.7 volts min @ −0.4 mA |
| Output Low | 0.4 volts max @ 8 mA |
| Input High | 2.0 volts min, 7 volts absolute max |
| Input Low | 0.8 volts max, −0.5 volts absolute min |
| Power up, reset state of outputs | Logic low |
| Interrupt | IRQ 2 - 7, Software-selectable |
| Interrupt enable | Programmable |
| Interrupt sources | D/A FIFO-half-full |

## Counters Section

| | |
|---|---|
| Configuration | 82C54 device. 3 down-counters, 16 bits each, chained to form a 48-bit counter |

Counter 0 - Internal Pacer - First divider

| | |
|---|---|
| Source: | 10 MHz oscillator |
| Gate: | Internal PGATE (FPGA control signal) |
| Output: | Chained to Counter 1 clock input |

Counter 1 - Internal Pacer - Second divider

| | |
|---|---|
| Source: | Counter 0 output |
| Gate: | Internal PGATE (FPGA control signal) |
| Output: | Chained to Counter 2 clock input |

Counter 2 - Internal Pacer - Third divider

| | |
|---|---|
| Source: | Counter 1 output |
| Gate: | Internal PGATE (FPGA control signal) |
| Output: | Pacer control logic |

| | |
|---|---|
| Clock input frequency | 10 MHz max |
| High pulse width (clock input) | 30 ns min |
| Low pulse width (clock input) | 50 ns min |
| Gate width high | 50 ns min |
| Gate width low | 50 ns min |
| Input low voltage | 0.8V max |
| Input high voltage | 2.0V min |
| Output low voltage | 0.4V max |
| Output high voltage | 3.0V min |

## Environmental

| | |
|---|---|
| Operating temperature range | 0 to 70°C |
| Storage temperature range | −40 to 100°C |
| Humidity | 0 to 90% non-condensing |