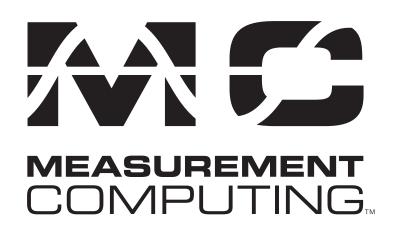
SPECIFICATIONS CIO-DAC04/12-HS

Quad 12-bit Analog Outputs



Revision 5, October, 2000 © Copyright 2000, MEASUREMENT COMPUTING CORPORATION

Power Consumption

+5V supply

Analog Output

Resolution Number of channels D/A type Voltage Ranges

D/A Pacing

D/A Gating Data Transfer

Offset error Gain error Differential nonlinearity Integral nonlinearity Monotonicity D/A Gain drift Throughput Settling time (20V step to .01%) Slew rate Current Drive Output short-circuit duration Output Coupling 520 mA typ, 610 mA max.

12 bits 4 Voltage Output AD7948BN ±2.5, ±5, ±10, 0 to 2.5, 0 to 5, 0 to 10, switch-selectable, each channel independently

Internal or external clock (EXTPACER) on falling edge or software-paced External (EXTGATE), active high Programmed I/O From 1024 FIFO via programmed I/O or REP-OUTSW interrupt

Adjustable to zero Adjustable to zero ±0.5 LSB max. ±0.5 LSB max. Guaranteed monotonic to 12 bits over temperature 5 ppm FSR/°C max. PC-dependent, 250 kHz max. 1µs typical, 1.5µs max 32V/µs typical ±5 mA typical 20 mA min Continuous DC

Miscellaneous

Double buffered output latches Update DACs individually or simultaneously (softwareselectable)

Simultaneous mode requires that channel 3 is always included in the channels to be updated. State of analog outputs at power-up is un-defined.

When using the internal pacer, the user must physically disconnect any signal connected to the EXTPACER input on the User Connector.

Digital Input / Output

Interrupt enable

Interrupt sources

Digital Type	
Input:	74LS244
Output:	74LS273
Configuration	2 banks of 8, 1 bank as input, 1 bank as output
Number of channels	16
Output High	2.7 volts min @ -0.4 mA
Output Low	0.4 volts max @ 8 mA
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min
Power up, reset state of outputs	Logic low
Interrupt	IRQ 2 - 7, Software-selectable

IRQ 2 - 7, Software-selectable Programmable D/A FIFO-half-full

Counters Section

Configuration

Counter 0 - Internal Pacer - First divider

Gate: Output: Counter 1 - Internal Pacer - Second divider Source: Gate: Output: Counter 2 - Internal Pacer - Third divider Source: Gate: Output:

Clock input frequency High pulse width (clock input) Low pulse width (clock input) Gate width high Gate width low Input low voltage Input high voltage Output low voltage Output high voltage

82C54 device. 3 down-counters, 16 bits each, chained to form a 48-bit counter

10 MHz oscillator

Source: Internal PGATE (FPGA control signal) Chained to Counter 1 clock input

Counter 0 output Internal PGATE (FPGA control signal) Chained to Counter 2 clock input

Counter 1 output Internal PGATE (FPGA control signal) Pacer control logic

Environmental

Operating temperature range Storage temperature range Humidity

0 to 70°C -40 to 100°C 0 to 90% non-condensing

10 MHz max

30 ns min

50 ns min

50 ns min

50 ns min

0.8V max

2.0V min

0.4V max

3.0V min

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