PCIM-DAS16JR/16

Specifications

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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Power consumption

+5V quiescent	500 mA typical, 750 mA max. Does not include the current consumed through 37-pin I/O connector.
+5V available at 37-pin I/O connector	1 A max, protected with re-settable fuse

Analog input

A/D converter type	LTC1605ACSW
Resolution	16 bits
Number of channels	16 single-ended / 8 differential, switch selectable
Input ranges ▪ Gain is software selectable ▪ Unipolar / bipolar polarity is software selectable	±10 V, ±5 V, ±2.5 V, ±1.25 V 0 to 10 V, 0 to 5 V, 0 to 2.5 V, 0 to 1.25 V
A/D Pacing (software programmable)	Internal counter - 82C54. Positive or negative edge, jumper selectable.
	External source (pin 25), Positive or negative edge, software selectable.
	Software polled
A/D Trigger (only available when internal pacing selected, software enable/disable)	External edge trigger (pin 25), Positive or negative edge, software selectable.
A/D Gate (only available when internal pacing selected, software enable/disable)	External gate (pin 25), High or Low level, software selectable.
Simultaneous Sample and Hold trigger	TTL output (pin 26) Logic 0 = Hold, Logic 1 = Sample Compatible with CIO-SSH16
Burst mode	Software selectable option, burst interval = 10 µS
Data transfer	From 1024 sample FIFO via interrupt w/ REPINSW
	Interrupt
	Software polled
Interrupt	INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable through PLX9030
Interrupt polarity	Active high level or active low level, programmable through PLX9030
Interrupt sources (software programmable)	▪ End of conversion ▪ FIFO not Empty ▪ End of Burst ▪ End of Acquisition ▪ FIFO Half Full
A/D conversion time	*10 µs max.*
Throughput	100 kS/s
Input coupling	*DC*
Input bandwidth (all ranges)	*325 kHz*
Common mode range	±10 V min.
CMRR @ 60 Hz	-100 dB typ., -80 dB min
Recommended warm-up time	15 minutes

Input bias current	*±3 nA max.*
Input impedance	*10 M Ohms min.*
Absolute maximum input voltage	*+55/-40V fault protected via input mux.*

Accuracy

Typical accuracy	±2.3 LSB
Absolute accuracy	±5.0 LSB
Accuracy components	
Gain Error	Trimmable by potentiometer to 0
Offset Error	Trimmable by potentiometer to 0
PGA linearity error	*±1.3 LSB typ., ±10.0 LSB max.*
Integral Linearity Error	±0.5 LSB typ., ±3.0 LSB max.
Differential Linearity Error	*±0.5 LSB typ., ±2.0 LSB max.*

Each PCIM-DAS16JR/16 is tested at the factory to ensure the board's overall accuracy error does not exceed ±5 LSB. Total board error is a combination of gain, offset, differential linearity and integral linearity error. The theoretical absolute accuracy of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

Analog input drift

Range	Analog Input Full-Scale Gain drift	Analog Input Zero drift	Overall Analog Input drift
±10.00 V	2.2 LSB/°C max.	1.8 LSB/°C max.	4.0 LSB/°C max.
±5.000 V	2.2 LSB/°C max.	1.9 LSB/°C max.	4.1 LSB/°C max.
±2.500 V	2.2 LSB/°C max.	2.0 LSB/°C max.	4.2 LSB/°C max.
±1.250 V	2.2 LSB/°C max.	2.3 LSB/°C max.	4.5 LSB/°C max.
0 - 10.00 V	4.1 LSB/°C max.	1.9 LSB/°C max.	6.0 LSB/°C max.
0 - 5.000 V	4.1 LSB/°C max.	2.1 LSB/°C max.	6.2 LSB/°C max.
0 - 2.500 V	4.1 LSB/°C max.	2.4 LSB/°C max.	6.5 LSB/°C max.
0 - 1.250 V	4.1 LSB/°C max.	3.0 LSB/°C max.	7.1 LSB/°C max.

Absolute error change per °C temperature change is a combination of the gain and offset drift of many components. The theoretical worst case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and are causing error in the same direction.

Noise performance

The following table summarizes the worst case noise performance for the PCIM-DAS16JR/16. Noise distribution is determined by gathering 50000 samples with inputs tied to ground at the PCIM-DAS16JR/16 main connector. Data represents both single-ended and differential modes of operation.

Range	LSBrms	Typical Counts
±10.00 V	1.30	12
±5.000 V	1.30	12
±2.500 V	1.30	12
±1.250 V	1.30	13
0 - 10.00 V	1.80	15
0 - 5.000 V	1.80	15
0 - 2.500 V	1.80	15
0 - 1.250 V	1.80	16

Settling time

Settling time is defined here as the time required for a channel to settle to within a specified accuracy in response to a full-scale (FS) step. Two channels are scanned at a specified rate with a –FS DC signal presented to channel 1 and a +FS DC signal presented to channel 0.

Condition	Range	Accuracy			
			±0.00076% (±4 LSB)	±0.0015% (±8 LSB)	±0.0061% (±16 LSB)
Same range to same range	±10 V	Typ.	400 µS	100 µS	10 µS
	±5 V	Typ.	100 µS	20 µS	10 µS
	±2.5 V	Typ.	60 µS	12 µS	10 µS
	±1.25 V	Typ.	50 µS	10 µS	
	0 to 10 V	Typ.	400 µS	100 µS	10 µS
	0 to 5 V	Typ.	100 µS	20 µS	10 µS
	0 to 2 V	Typ.	60 µS	12 µS	10 µS
	0 to 1.25 V	Typ.	50 µS	10 µS	

Digital input / output

Main connector

Digital output type	5V/TTL compatible
Digital input type	5V/TTL compatible, pulled to logic high via 10 K resistor network
Number of I/O	8
Configuration	4 fixed input, 4 fixed output
Output high voltage	*3.8 volts min. @ -32 mA*
Output low voltage	*0.55 volts max. @ 32 mA*
Input high voltage	*2.0 volts min., 7 volts absolute max.*
Input low voltage	*0.8 volts max., -0.5 volts absolute min.*
Data transfer	Programmed I/O
Power-up / reset state	DIG OUT [3:0] - TTL logic low state

Counter

Counter type	82C54
Configuration	3 down counters, 16-bits each
Counter 1 source (software selectable)	▪ External source from main connector (pin 21*) ▪ 100 kHz internal source
Counter 1 gate	External gate from main connector (pin 24*)
Counter 1 output	Available at main connector (pin 2)
Counter 2 source (jumper selectable at P2)	▪ Internal 1 MHz ▪ Internal 10 MHz
Counter 2 gate (software enable/disable)	External source from main connector (pin 25*)
Counter 2 output	Internal only, chained to counter 3 source
Counter 3 source	Counter 2 output
Counter 3 gate (software enable/disable)	External source from main connector (pin 25*)
Counter 3 output	Available at main connector (pin 20). Programmable as ADC Pacer clock.
Clock input frequency	*10 MHz max.*
High pulse width (clock input)	*30 ns min.*
Low pulse width (clock input)	*50 ns min.*
Gate width high	*50 ns min.*
Gate width low	*50 ns min.*
Input high	*2.0 volts min., 5.5 volts absolute max.*
Input low	*0.8 volts max., -0.5 volts absolute min.*
Output high	*3.0 volts min. @ -2.5 mA*
Output low	*0.4 volts max. @ 2.5 mA*
Crystal oscillator frequency	10 MHz
Frequency accuracy	50 ppm

* Pins 21, 24, and 25 are pulled to logic high via 10 K resistors.

Environmental

Operating temperature range	0 to 70 °C
Storage temperature range	-40 to 100 °C
Humidity	0 to 95% non-condensing

Mechanical

Card dimensions	PCI half card: 136.5 mm (L) x 106.9 mm (W) x 11.65 mm (H)
Form factor	Universal PCI keying. Compatible with 3.3 V/5 V 32-bit, 33 MHz back planes.

Main connector and pin out

Connector type	37-pin male "D" connector
Connector compatibility	Identical to the CIO-DAS16JR/16 connector
Compatible accessory products	CIO-MINI37 CIO-SCB37 CIO-SSH-16
Compatible cables	C37FF-x C37FFS-x

8-channel differential mode pin out

Pin	Signal Name	Pin	Signal Name
1	+5V PC BUS POWER	20	CTR 3 OUT
2	CTR 1 OUT	21	CTR 1 CLOCK IN
3	DIG OUT 3	22	DIG OUT 2
4	DIG OUT 1	23	DIG OUT 0
5	DIG IN 3	24	DIG IN 2 / CTR1 GATE
6	DIG IN 1	25	DIG IN 0 / EXT TRIG / EXT PACER / EXT GATE
7	DIG GND	26	SS&H OUT
8	NC	27	NC
9	NC	28	AGND
10	NC	29	AGND
11	CH7 LO	30	CH7 HIGH
12	CH6 LO	31	CH6 HIGH
13	CH5 LO	32	CH5 HIGH
14	CH4 LO	33	CH4 HIGH
15	CH3 LO	34	CH3 HIGH
16	CH2 LO	35	CH2 HIGH
17	CH1 LO	36	CH1 HIGH
18	CH0 LO	37	CH0 HIGH
19	AGND		

16-channel single-ended mode pin out

Pin	Signal Name	Pin	Signal Name
1	+5V PC BUS POWER	20	CTR 3 OUT
2	CTR 1 OUT	21	CTR 1 CLOCK IN
3	DIG OUT 3	22	DIG OUT 2
4	DIG OUT 1	23	DIG OUT 0
5	DIG IN 3	24	DIG IN 2 / CTR1 GATE
6	DIG IN 1	25	DIG IN 0 / EXT TRIG / EXT PACER / EXT GATE
7	DIG GND	26	SS&H OUT
8	NC	27	NC
9	NC	28	AGND
10	NC	29	AGND
11	CH15 HIGH	30	CH7 HIGH
12	CH14 HIGH	31	CH6 HIGH
13	CH13 HIGH	32	CH5 HIGH
14	CH12 HIGH	33	CH4 HIGH
15	CH11 HIGH	34	CH3 HIGH
16	CH10 HIGH	35	CH2 HIGH
17	CH9 HIGH	36	CH1 HIGH
18	CH8 HIGH	37	CHO HIGH
19	AGND		

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