7210-TQFP-R

IEEE 488.2 Controller chip – replacement for NEC µPD7210

7210-TQFP-R

- RoHS-compliant
- Pin-compatible with NEC µPD7210
- Software-compatible with NEC µPD7210
- Low power consumption
- Meets all IEEE 488.2 requirements:
  - Bus line monitoring
  - Preferred implementation of requesting service
  - Sends no messages when there are no listeners
- Performs all IEEE 488.1 interface functions SH1, AH1, T5 or TE5, L3 or LE3, SR1, RL1, PP1, PP2, DC1, DT1, C1, C2, C3, C4, C5
- Reduces driver overhead
- Does not lose a data byte if ATN is asserted while transmitting data
- Static interrupt status bits that do not clear when read
- Programmable data transfer rate
- (T1 delays of 350 ns, 500 ns, 1.1 µs, and 2 µs)
- Automatic EOS and/or NL message detection
- Direct memory access (DMA)
- Automatically processes IEEE 488 commands and reads undefined commands
- Programmable compatible with bus transceivers (T1, National Semiconductor, Motorola, and Intel)
- TTL-compatible CMOS device
- Programmable clock rate up to 20 MHz

Overview

Measurement Computing Corporation's 7210-TQFP-R is a 44-pin DIP replacement part for the NEC µPD7210. The 7210-TQFP-R is 100% register-compatible and pin-compatible with the NEC µPD7210 on power up. The 7210-TQFP-R performs all of the interface functions defined by the ANSI/IEEE Standard 488.1-1987, and it meets the additional requirements and recommendations of ANSI/IEEE Standard 488.2-1987. The 7210-TQFP-R performs complete IEEE 488 talker, listener, and controller functions.

On power up, the 7210-TQFP-R contains the complete register set of the NEC µPD7210, but can perform complete IEEE 488.2 controller functions through software.

If you are an instrument developer, you can take advantage of IEEE 488.2 with minimal software modifications yet keep the 44-pin hardware configuration. The default clock input is 8 MHz, but increased performance is available from the 7210-TQFP-R through software-selectable input values up to 20 MHz.

If you are an IEEE 488 instrument manufacturer looking for alternatives to existing NEC µPD7210 chip suppliers or planning to upgrade your designs to IEEE 488.2 without hardware changes, consider using the 7210-TQFP-R. Because the 7210-TQFP-R accepts faster clock inputs, performance increases without many firmware changes.

General

The 7210-TQFP-R manages the IEEE 488 bus. You program the IEEE 488 bus by writing control words into the appropriate registers. CPU-readable status registers supply operational feedback. The 7210-TQFP-R mode determines the function of these registers. When in 7210 mode, the registers resemble the µPD7210 register set with additional registers that supply extra functionality and IEEE 488.2 compatibility. In this mode, the 7210-TQFP-R is completely pin-compatible with the NEC µPD7210. Figure 1 shows the key components of the 7210-TQFP-R.

RoHS Compliance

The 7210-TQFP-R is available from MCC as a RoHS-compliant chip. The chip is marked with an e3 inside an ellipse to indicate a matte pure tin finish on the leads, in accordance with the marking recommendations defined in JEDEC JESD97.

The RoHS-compliant 7210-TQFP-R meets industry requirements for baking and maximum solder reflow temperature. The baking requirements are outlined in JEDEC J-STD-033. MCC recommends using the solder reflow profile as shown in IPC/JEDEC J-STD-020C with a peak temperature of 260 °C, the maximum temperature they can withstand.

Ordering Information

RoHS-compliant chip	MCC Part number
44-pin LQFP package	7210-TQFP-R

Block Diagram

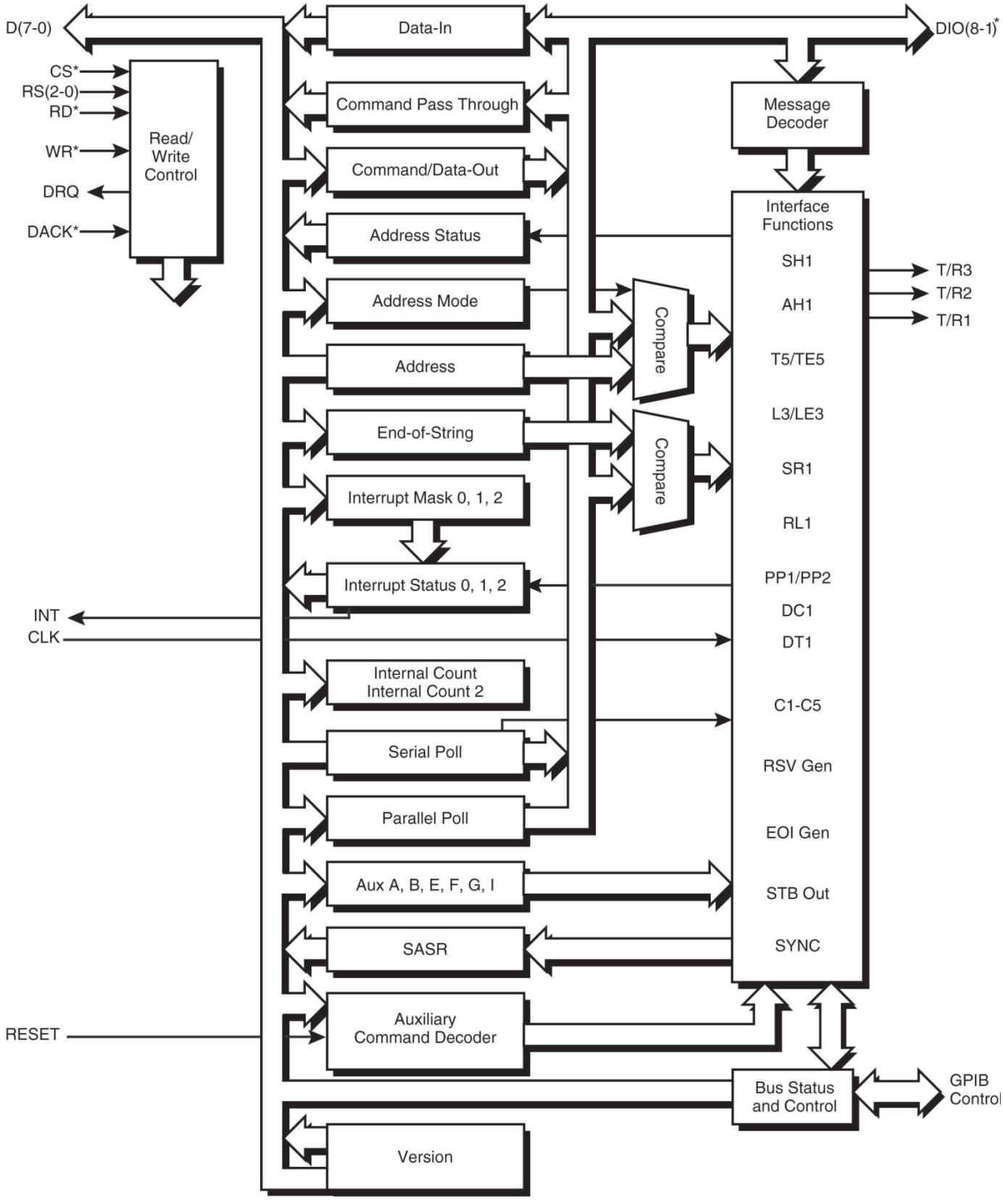


Figure 1. 7210-TQFP-R block diagram

Pin Descriptions

The following table describes the 7210-TQFP-R pins.

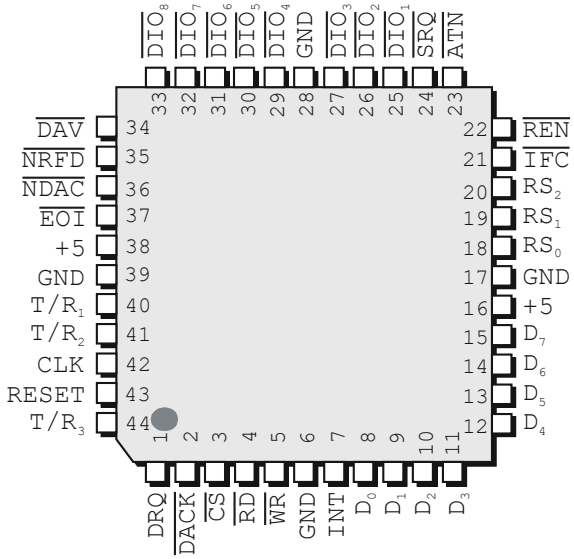


Figure 2. 7210-TQFP-R pin configuration

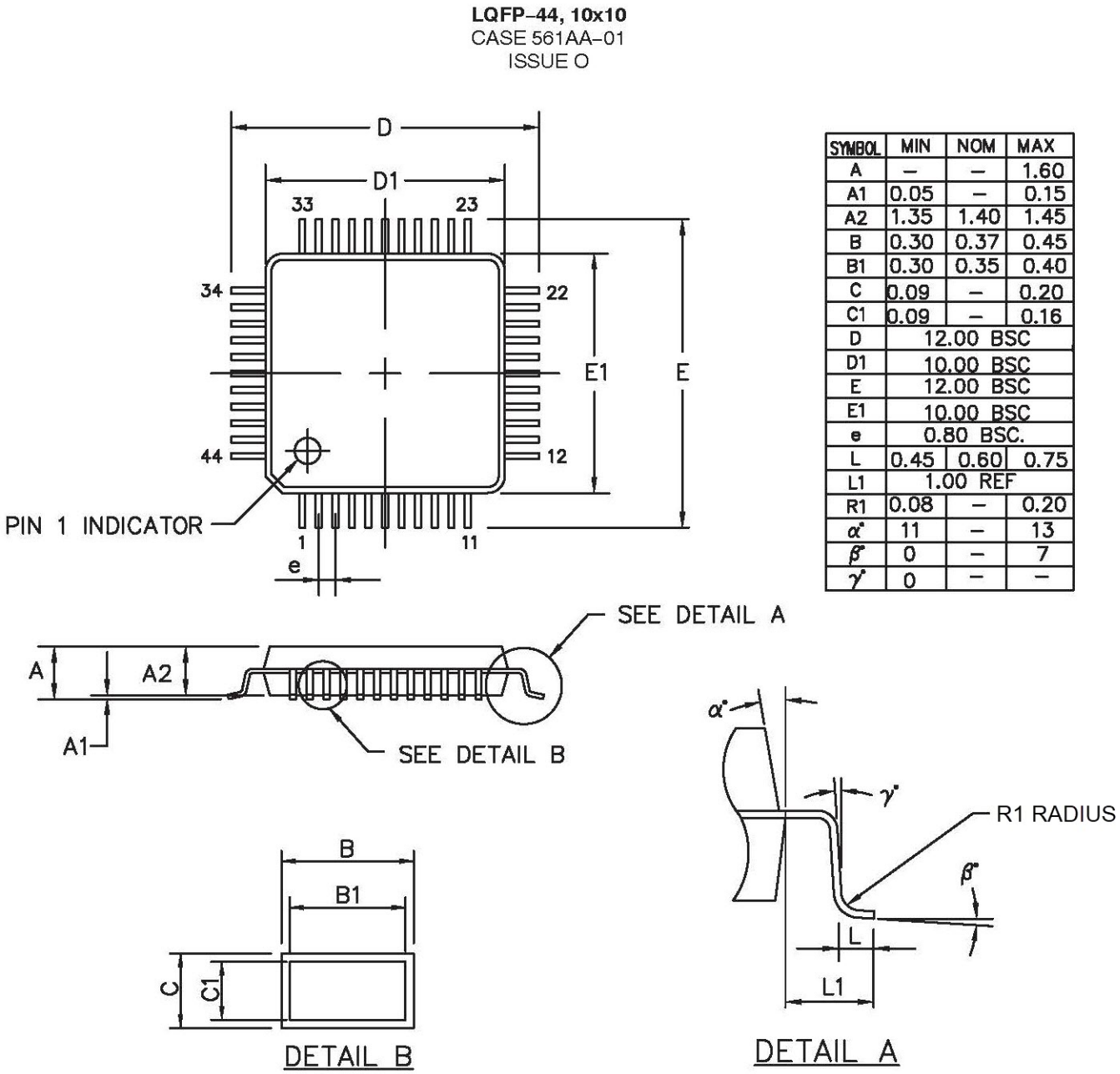
Pin Identification

Table 1. 7210-TQFP-R pin configuration

Pin #	Mnemonic	I/O	Description
1	DRQ	O	**DMA Request**. Requests data transfer. Becomes low on input of DMA acknowledge signal DACK.
2	$\overline{\text{DACK}}$	I	**DMA Acknowledge**. (Active low) Signal connects the computer system data bus to the data register of the 7210-TQFP-R.
3	$\overline{\text{CS}}$	I	**Chip Select**. (Active low) Enables access to the register selected by RS_0-RS_2 (read or write operation).
4	$\overline{\text{RD}}$	I	**Read**. (Active low) Places contents of read register specified RS_0-RS_2 on D_0-D_7 (computer bus).
5	$\overline{\text{WR}}$	I	**Write**. (Active low) Writes data on D_0-D_7 into the write register specified by RS_0-RS_2.
6, 17, 28, 39	GND		**Ground**
7	INT	O	**Interrupt Request**. (Active high/low) Becomes active due to any 1 of 13 internal interrupt conditions (unmasked). Active state software configurable. Active high on chip reset.
8-15	D_0-D_7	I/O	**Data Bus**. 8-bit bidirectional data bus for interface to the computer system.
16, 38	+5 (V_{CC})	I/O	+5 VDC (±5%)
18-20	RS_0-RS_2	I	**Register Select**. These lines select one of eight read (write) registers during a read (write) operation.
21	$\overline{\text{IFC}}$	I/O	**Interface Clear**. Control line used for clearing the interface functions.
22	$\overline{\text{REN}}$	I/O	**Remote Enable**. Control line used to enable remote operation of the devices.
23	$\overline{\text{ATN}}$	I/O	**Attention**. Control line which indicates whether data on DIO lines is an interface message or device dependent message.
24	$\overline{\text{SRQ}}$	I/O	**Service Request**. Control line used to request service from the controller.
25-33	$\overline{\text{DIO}}_1$- $\overline{\text{DIO}}_8$	I/O	**Data Input/Output**. 8-bit bi-directional bus for transfer of message.
34	$\overline{\text{DAV}}$	I/O	**Data Valid**. Handshake line indicating that data on DIO lines is valid.
35	$\overline{\text{NRFD}}$	I/O	**Ready for Data**. Handshake line indicating that device is ready for data.
36	$\overline{\text{NDAC}}$	I/O	**Data Accepted**. Handshake line indicating completion of message reception.
37	$\overline{\text{EOI}}$	I/O	**End or Identity**. Control line used to indicate the end of multiple byte transfer sequence or to execute a parallel polling in conjunction with ATN.
40	T/R_1	O	**Transmit/Receive Control**. Input/output control signal for the GPIB bus transceivers.
41	T/R_2	O	**Transmit/Receive Control**. The values of T/R_2 and T/R_3 are determined by the values of the Address Mode register bits TRM1, and TRM0.
42	CLK	I	**Clock**. 1 MHz to 20 MHz reference clock for generating the state change prohibit times T_1, T_6, T_7, T_9 specified in IEEE Standard 488.2-1992.
43	RESET	I	**Reset**. Resets the 7210-TQFP-R to an idle state when high (active high).
44	T/R_3	O	**Transmit/Receive Control**. See T/R_2 (pin 41).

Mechanical Data

Controlling dimensions are in millimeters.



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
B	0.30	0.37	0.45
B1	0.30	0.35	0.40
C	0.09	–	0.20
C1	0.09	–	0.16
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.80 BSC.		
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	–	0.20
α°	11	–	13
β°	0	–	7
γ°	0	–	–

Figure 3. Package outline

7210 Mode Registers

In 7210 mode, the 7210-TQFP-R registers include all the NEC µPD7210 registers plus two types of additional registers – extra auxiliary registers and paged-in registers. You write the extra auxiliary registers in the same way as standard µPD7210 auxiliary registers. Upon issuing an auxiliary page-in command, the paged-in registers appear at the same offsets as existing µPD7210 registers. At the end of the next CPU access, the chip pages out the paged-in registers. The following table lists the registers in the 7210 mode register set.

7210 Register Set

Register	Page-In	A(2-0)	WR*	RD*	CS*	DACK*
Data-in	U	0 0 0	1	0	0	1
Data-in	X	X X X	1	0	X	0
Command/data-out	U	0 0 0	0	1	0	1
Command/data-out	X	X X X	0	1	X	0
Interrupt status[1]	U	0 0 1	1	0	0	1
Interrupt mask[1]	U	0 0 1	0	1	0	1
Interrupt status[2]	U	0 1 0	1	0	0	1
Interrupt mask[2]	U	0 1 0	0	1	0	1
Serial poll status	N	0 1 1	1	0	0	1
Serial poll mode	N	0 1 1	0	1	0	1
Version	P	0 1 1	1	0	0	1
Initial counter[2]	P	0 1 1	0	1	0	1
Address status	U	1 0 0	1	0	0	1
Address mode	U	1 0 0	0	1	0	1
Command pass through	N	1 0 1	1	0	0	1
Auxiliary mode	U	1 0 1	0	1	0	1
Source/acceptor status†	P	1 0 1	1	0	0	1
Address 0	N	1 1 0	1	0	0	1
Address	N	1 1 0	0	1	0	1
Interrupt status 0†	P	1 1 0	1	0	0	1
Interrupt mask 0†	P	1 1 0	0	1	0	1
Address†	N	1 1 1	1	0	0	1
End-of-string	N	1 1 1	0	1	0	1
Bus status†	P	1 1 1	1	0	0	1
Bus control†	P	1 1 1	0	1	0	1

Notes for the Page-In column:

U = The page-in auxiliary command does not affect the register.

N = The register offset is always valid except for immediately after a page-in auxiliary command.

P = The register is valid only immediately after a page-in auxiliary command.

The † symbol indicates features that are not available in the µPD7210, such as register and auxiliary commands.

DC Characteristics

Parameter	Symbol	Limits		Unit	Test Conditions
		Min	Max		
Voltage input low	VIL	-0.5	+0.8	V	
Voltage input high	VIH	+2.0	VCC	V	
Voltage output low	VOL	0	0.4	V	
Voltage output high	VOH	+2.4	VCC	V	
Input/output leakage current		-10	+10	µA	w/o internal pull-up
Input/output leakage current		-200	+200	µA	with internal pull-up
Supply Current			45	mA	
Output current low (all pins except T/R_1)	IOL	2		mA	VOL=0.4 V
T/R_1	IOL	4		mA	VOL=0.4 V
Input current low/high	IIL		-0.5	mA	
Output current high	IOH	-1		mA	V0H=VCC-0.5 V
Supply voltage	VCC	4.75	5.25	V	

Capacitance

TA_0 to 70 °C; V_{cc}= 5 V ±5%

Parameter	Symbol	Limits		Unit	Test Conditions
		Min	Max		
Input capacitance	Cin		10	pF	
Output capacitance	Cout		10	pF	
I/O capacitance	CI/O		10	pF	

Absolute Maximum Ratings

Property	Test Conditions
Supply voltage, VCC	-0.5 to +6.0 V
Input voltage, VI	-0.5 to VCC +0.5
Operating temperature, TOPR	0 to +70 °C
Storage temperature, TSTG	-40 to +125 °C
Caution: Exposing the device to stresses above those listed could cause permanent damage. The device is not meant to be operated under conditions outside the operational limits. Exposure to absolute maximum rating conditions for extended periods may affect reliability.	

AC Characteristics

TA0 to 70 °C; Vcc= 5 V ±5%

Parameter	Sym.	Limits		Unit	Test Conditions
		Min	Max		
Address hold from $\overline{RD}\uparrow$ $\overline{WR}\uparrow$	t_{AH}	0		ns	
Address setup to $\overline{RD}\downarrow$ $\overline{WR}\downarrow$	t_{AS}	0		ns	
Data float from $\overline{RD}\uparrow$	t_{DF}		25	ns	
Data delay from $\overline{RD}\downarrow$	t_{DR}		80	ns	DACK=0
DRQ unassertion	t_{DU}		25	ns	
Data delay from $\overline{RD}\downarrow$	t_{RD}	85	ns	CS=0	
RD recovery width	t_{RR}	120		ns	
RD pulse width	t_{RW}	85		ns	
Data setup to $\overline{WR}\uparrow$	t_{WS}	60		ns	
Data hold from $\overline{WR}\uparrow$	t_{WH}	0		ns	

Timing Waveforms

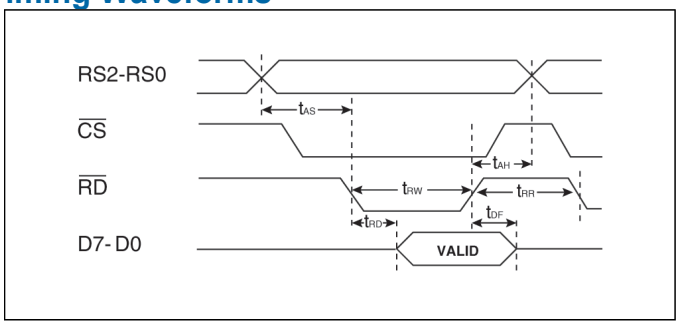


Figure 4. CPU Read

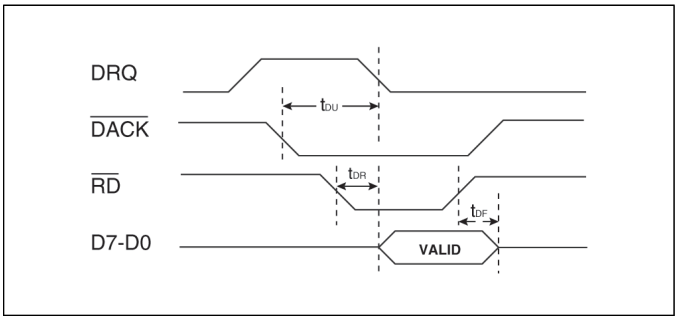


Figure 5. DMA Read

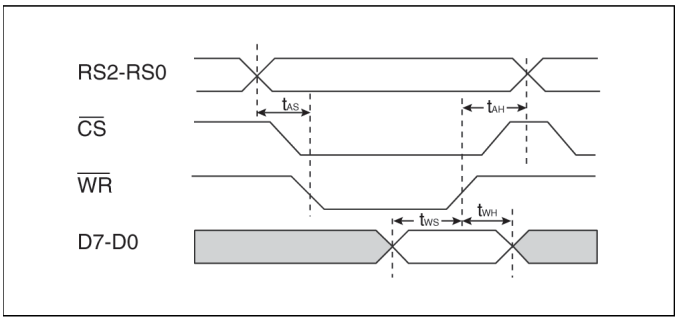


Figure 6. CPU Write

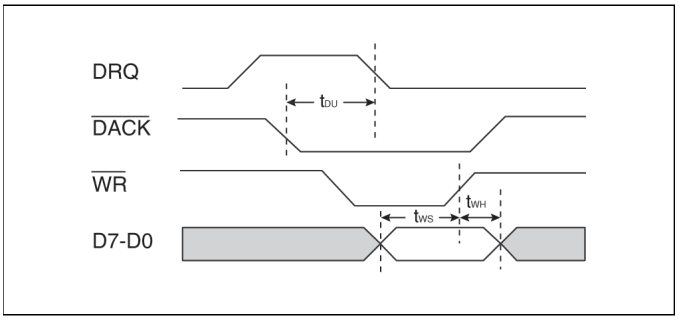


Figure 7. DMA Write

Source Handshake

Parameter	Sym.	Limits		Test Conditions
		Min	Max	
$\overline{NDAC}\uparrow$ to $\overline{DAV}\uparrow$	t_{ND}		40	
$\overline{NDAC}\uparrow$ to $\overline{INT}\uparrow$ or $\overline{DRQ}\uparrow$	t_{NI}		40	INT (DO IE Bit = 1) DRQ (DMAO Bit = 1)
$\overline{WR}\uparrow$ to $\overline{DAV}\downarrow$	t_{WD}	2,000	2,125	2 µs T1 (8 MHz, 50% duty)
$\overline{WR}\uparrow$ to $\overline{DAV}\downarrow$	t_{WD}	1,125	1,250	1.1 µs T1 (8 MHz, 50% duty)
$\overline{WR}\uparrow$ to $\overline{DAV}\downarrow$	t_{WD}	500	625	500 ns T1 (8 MHz, 50% duty)
$\overline{WR}\uparrow$ to $\overline{DAV}\downarrow$	t_{WD}	375	500	350 ns T1 (8 MHz, 50% duty)

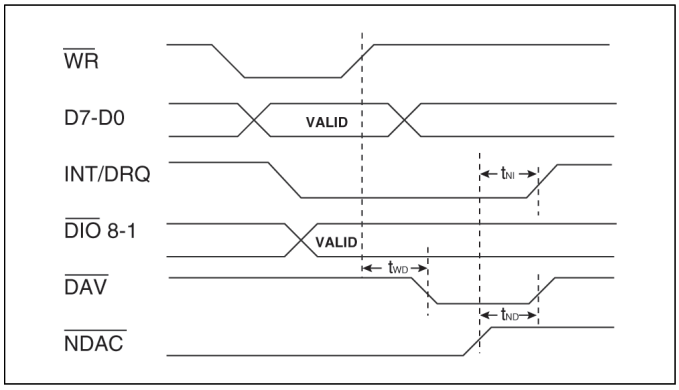


Figure 8. Source Handshake

Acceptor Handshake

Parameter	Sym.	Limits		Test Conditions
		Min	Max	
$\overline{DAV}\downarrow$ to $\overline{NDAC}\uparrow$	t_{DD}		225	8 MHz, 50% duty
$\overline{DAV}\uparrow$ to $\overline{NDAC}\downarrow$	t_{DD}		20	
$\overline{DAV}\downarrow$ to $\overline{INT}\uparrow$ or $\overline{DRQ}\uparrow$	t_{NI}		116	INT (DIIE Bit = 1) DRQ (DMAI Bit = 1)
$\overline{DAV}\downarrow$ to $\overline{NRFD}\downarrow$	t_{DR}		25	
$\overline{RD}\uparrow$ to $\overline{NRFD}\uparrow$	t_{NR}		30	Read of DIR, not in Holdoff state

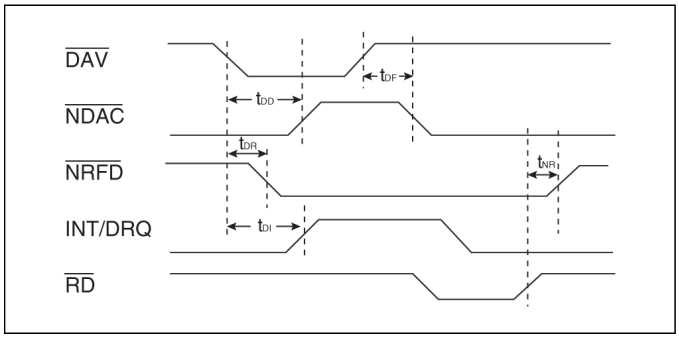


Figure 9. Acceptor Handshake

Response to ATN

Parameter	Sym.	Limits		Test Conditions
		Min	Max	
$\overline{ATN}\uparrow$ to $\overline{NRFD}\downarrow$	$t_{\Delta F}$		35	Acceptor handshake Holdoff
$\overline{ATN}\downarrow$ to $\overline{NDAC}\downarrow$	t_{AN}		35	AIDS → ANRS
$\overline{ATN}\downarrow$ to $\overline{TE}\downarrow$	t_{AT}		30	TACS → TADS

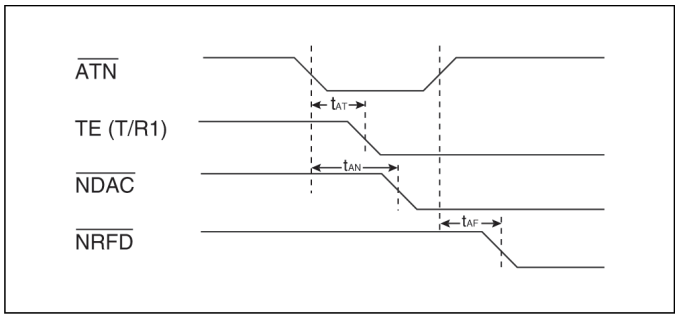


Figure 10. Response to ATN

Parallel Poll

Parameter	Sym.	Limits		Test Conditions
		Min	Max	
$\overline{EOI}\downarrow$ to $\overline{DIO}$ valid	t_{FD}		90	PPSS › PPAS
$\overline{EOI}\downarrow$ to $\overline{TE}\uparrow$	t_{ET}		25	PPSS › PPAS
$\overline{EOI}\uparrow$ to $\overline{TE}\downarrow$	t_{TE}		25	PPAS › PPSS

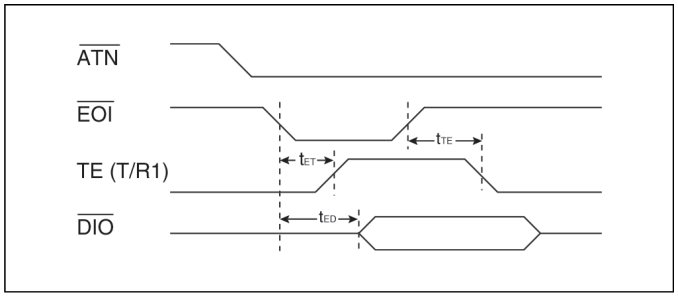


Figure 11. Parallel Poll

Typical System

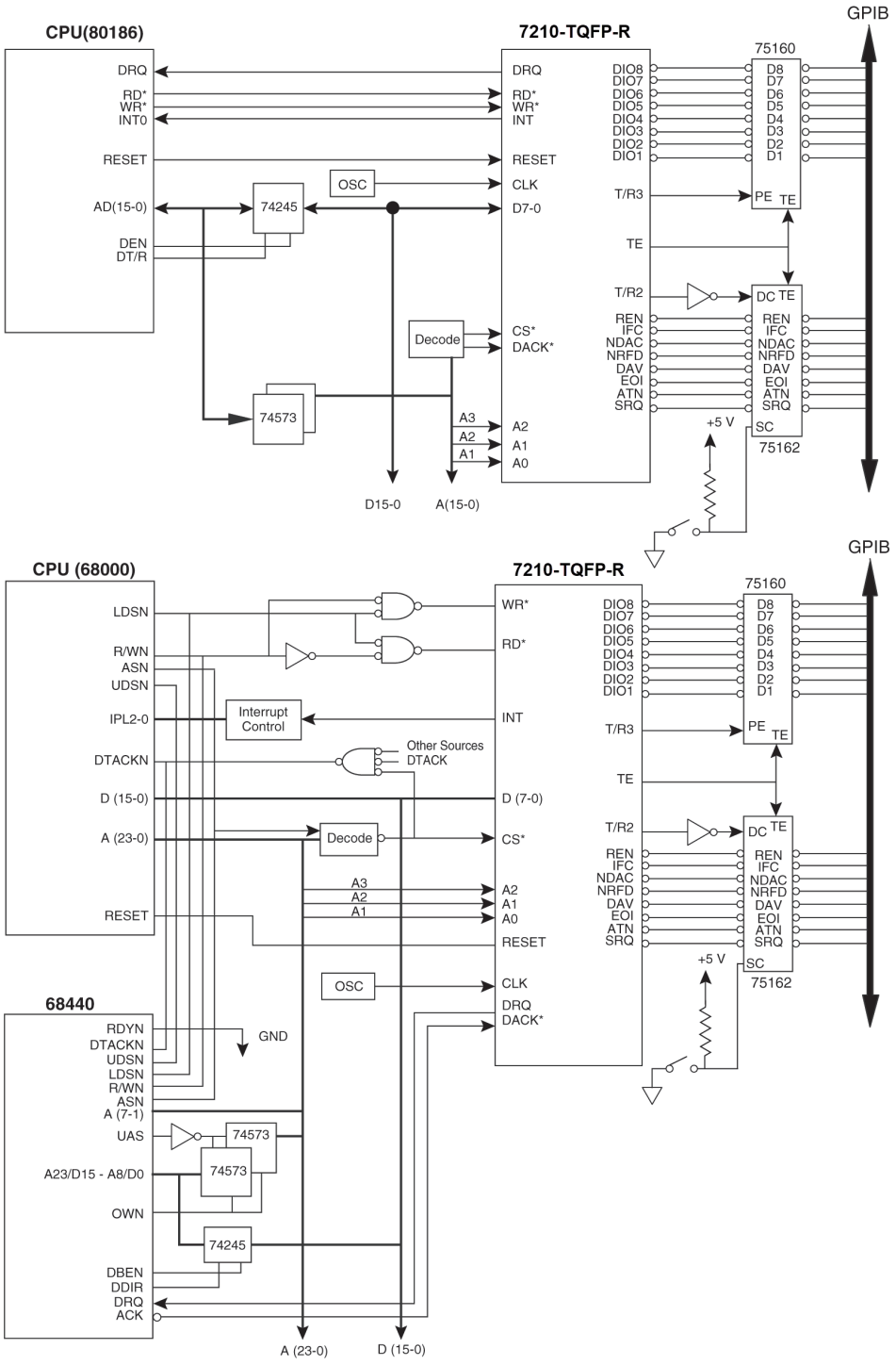


Figure 12. Typical CPU System with the 7210-TQFP-R

Contact us

Contact us if you need assistance in developing the interface to your particular system. Our engineering staff will work with you to ensure that your 7210-TQFP-R interface is simple, efficient and allows access to all chip features.

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

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