

A

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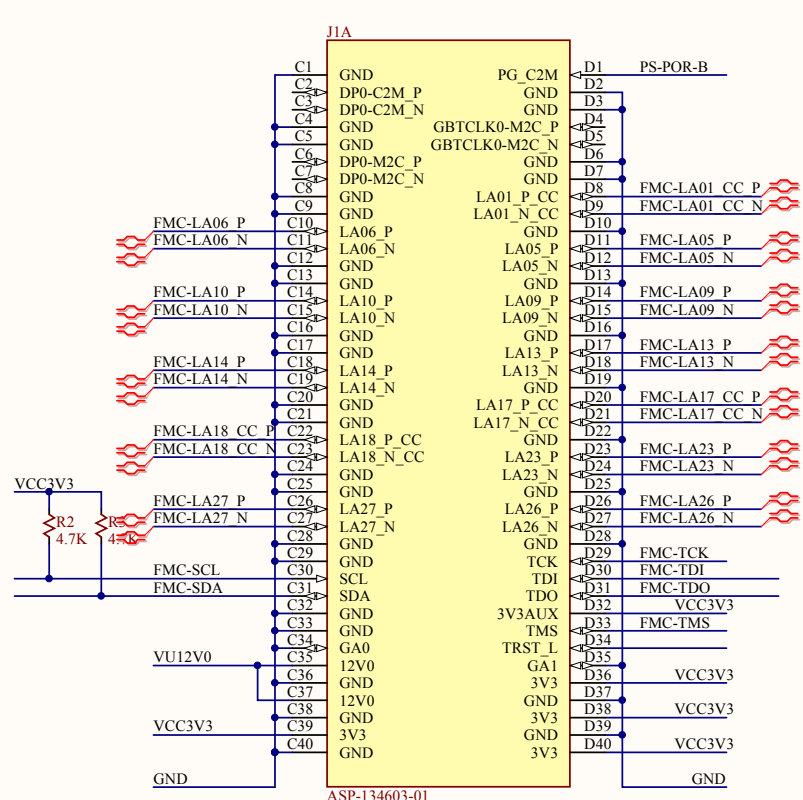
D

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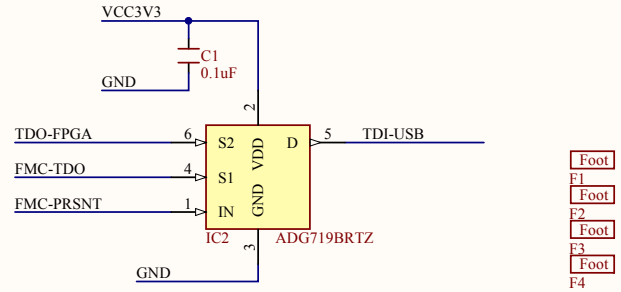
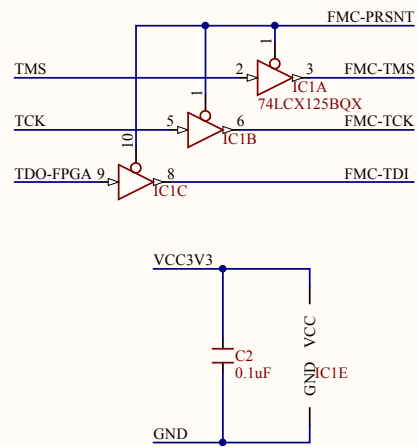
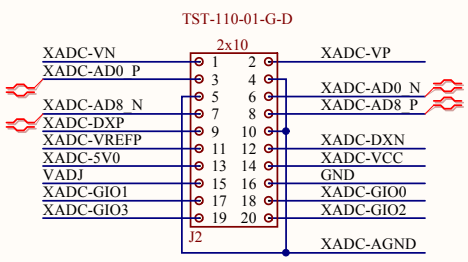
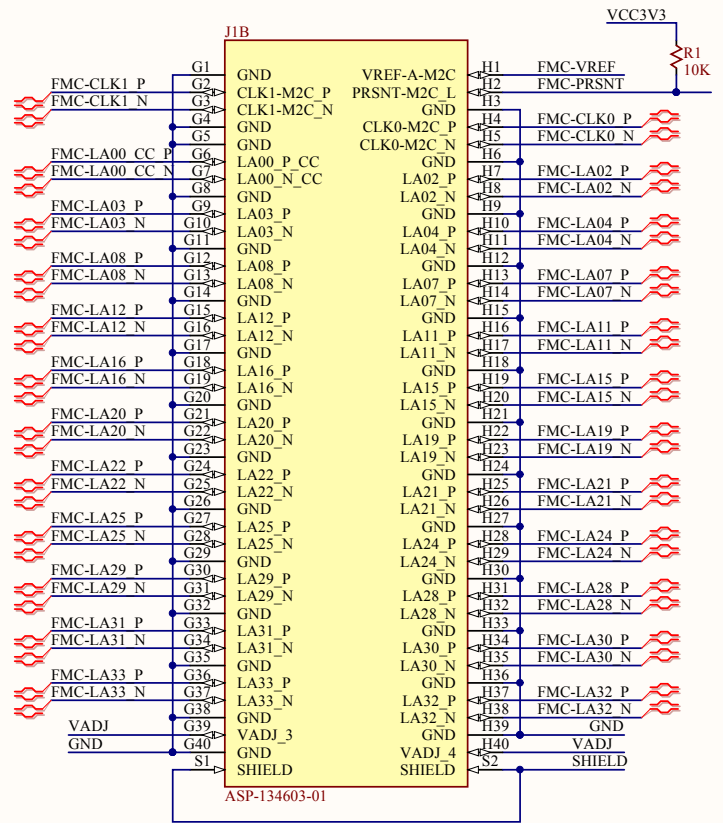
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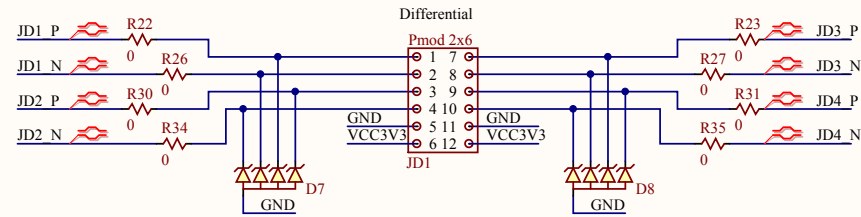
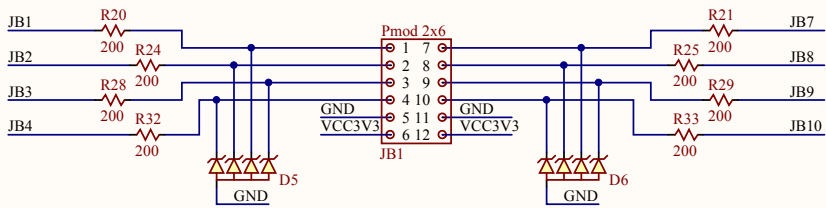
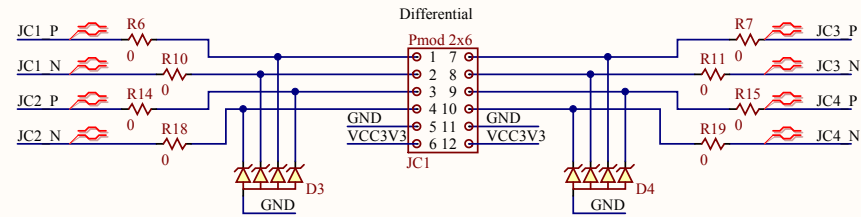
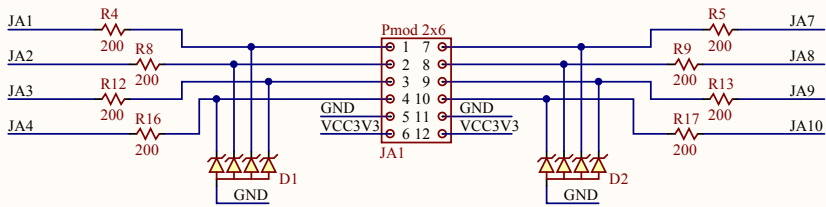
C

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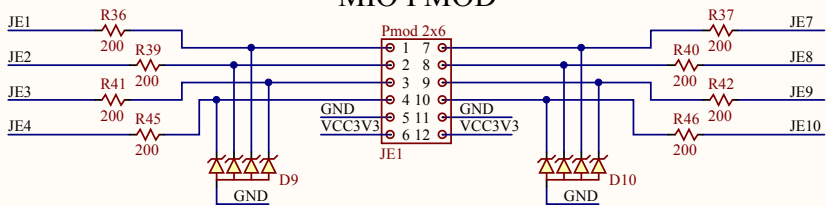


FMC and AMS Connector - SHEET 1
 PMODS, General I/O - SHEET 2
 Audio Codec - SHEET 3
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 DDR and MIO Ports - SHEET 9
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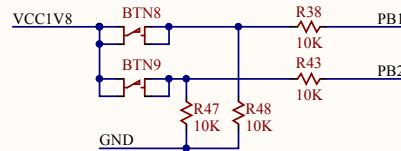




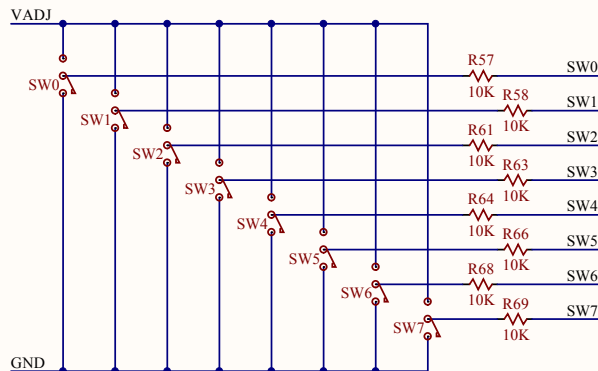
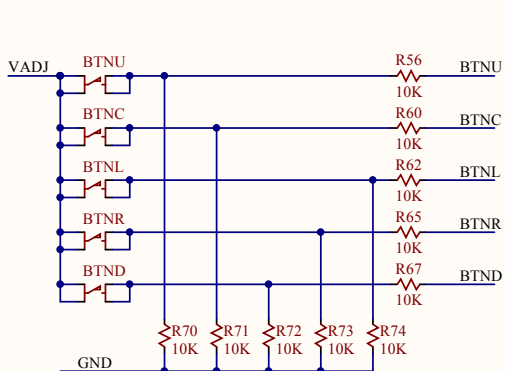
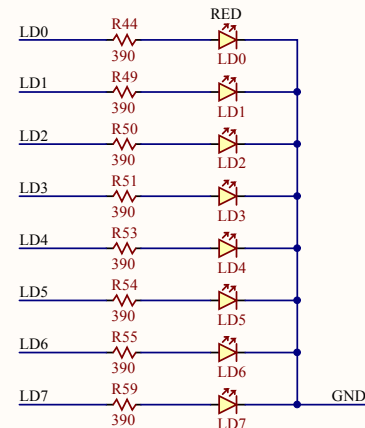
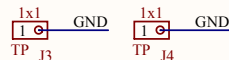
MIO PMOD




MIO BUTTON

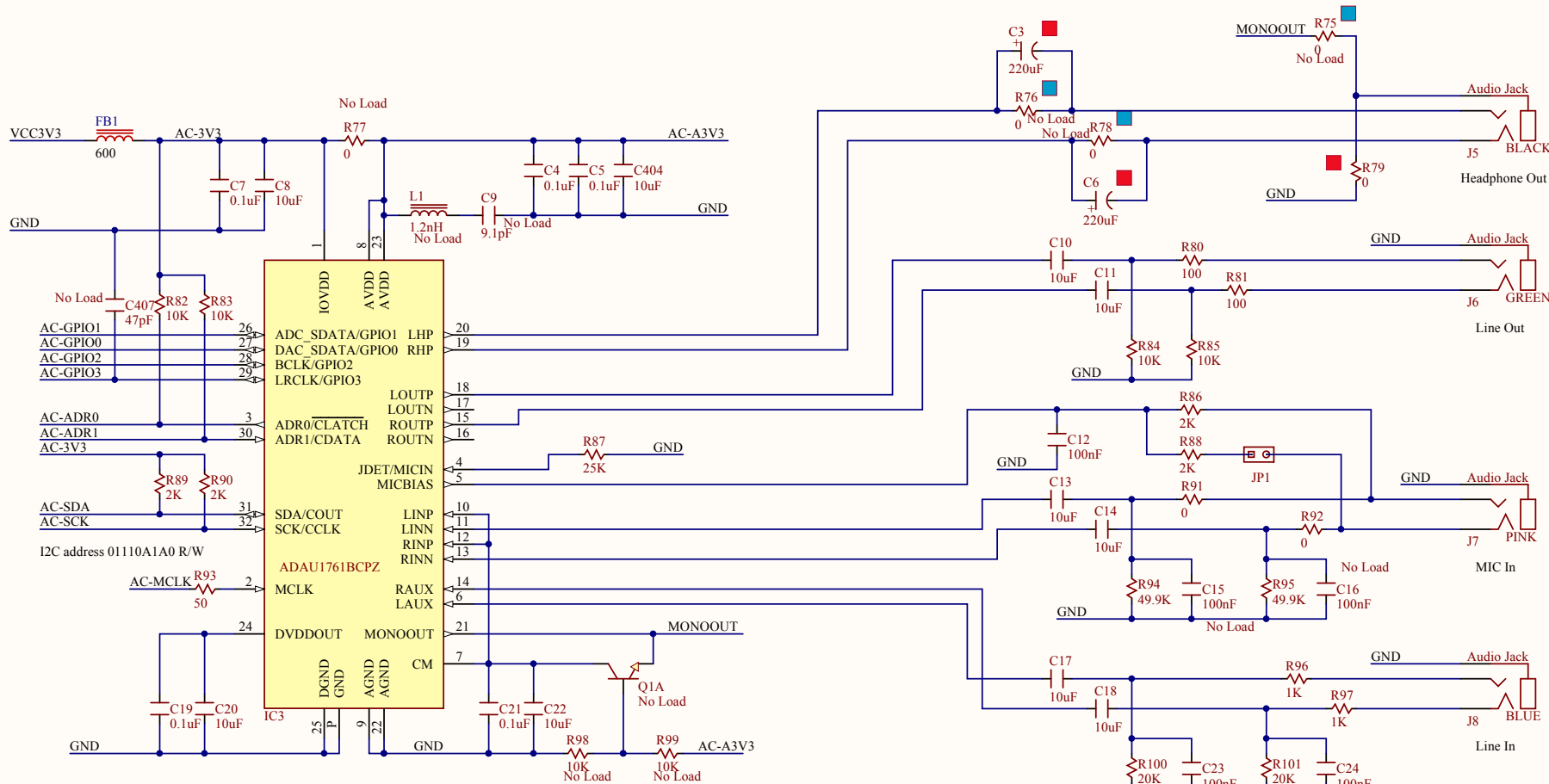


MIO LED

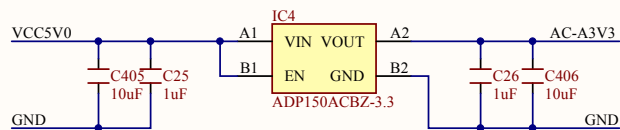


Title ZED		Rev C.1
Circuit PMods and General I/O		Copyright 2012
Doc# 500-248		
Engineer EG		
Author GMA		
Date 6/20/2012		
Sheet# 2 out of 16		

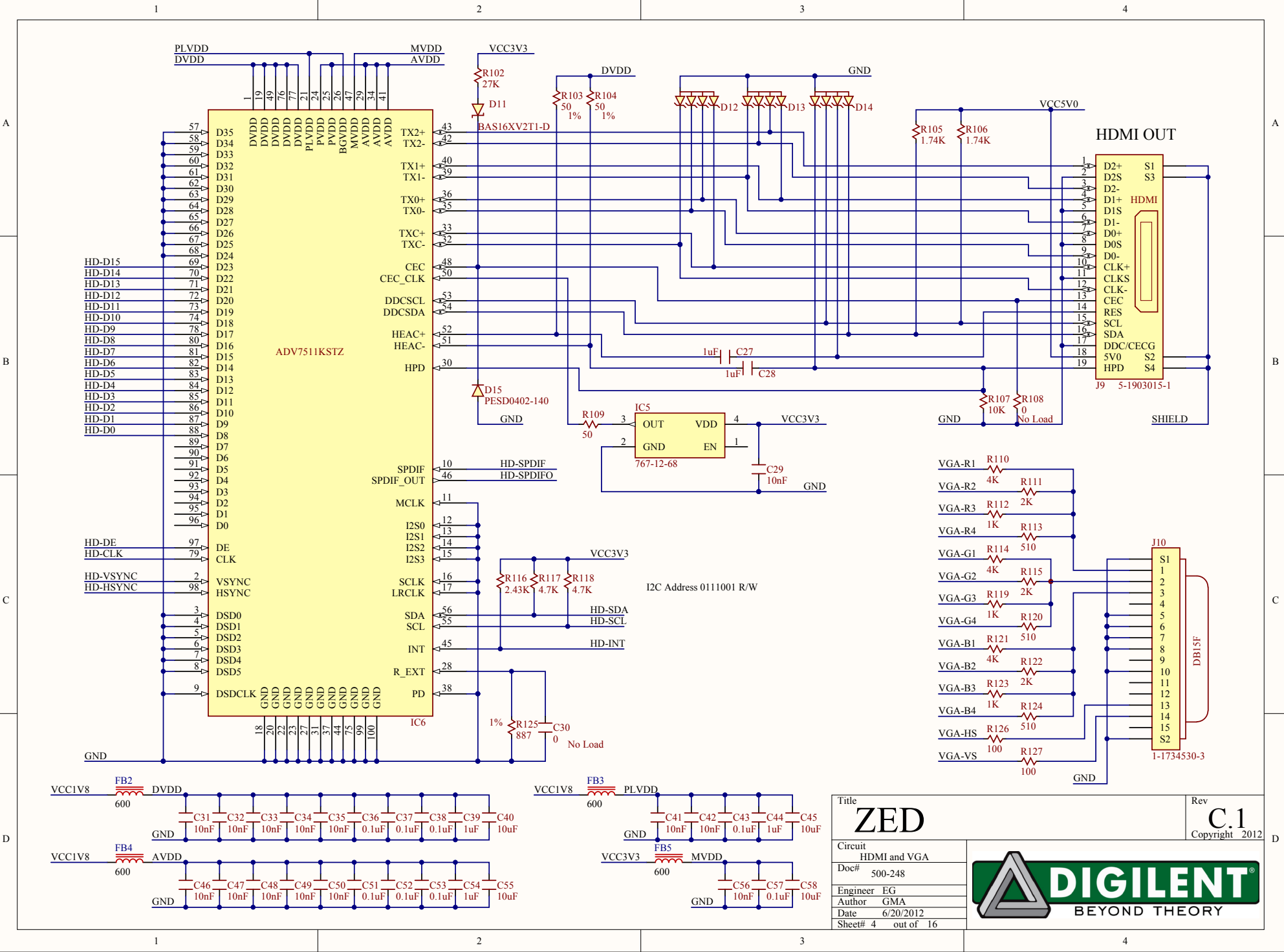
NOTE: Load No Load
 Capless Headphone ■ ■
 AC-Coupled Headphone ■ ■

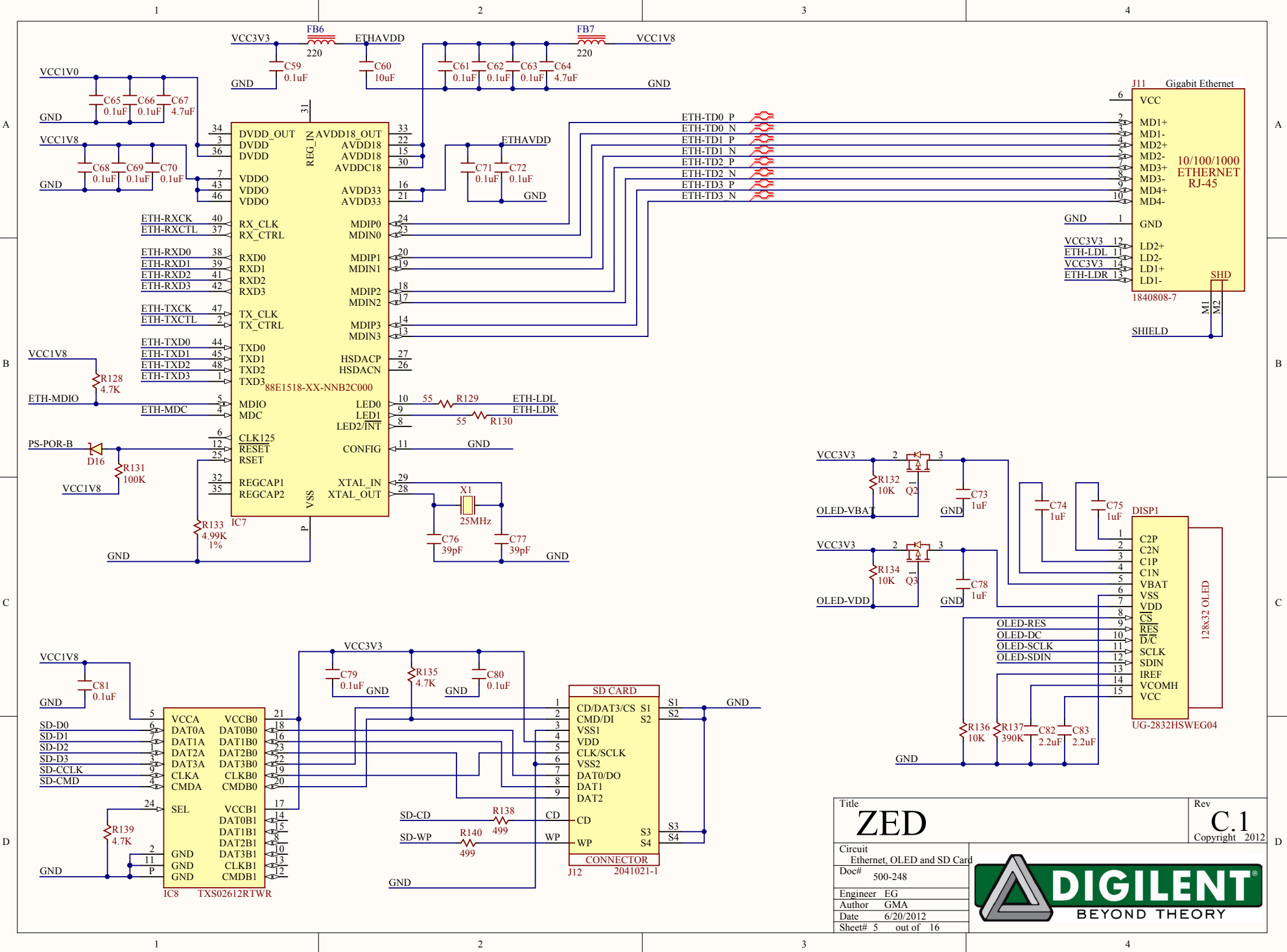



NOTE: AGND and GND pins must connect at single point under ADP150



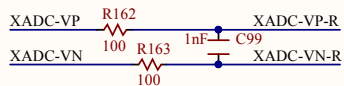
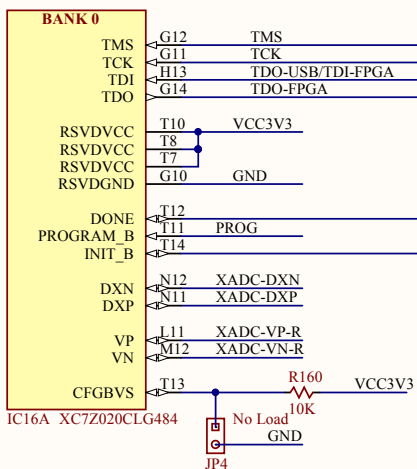
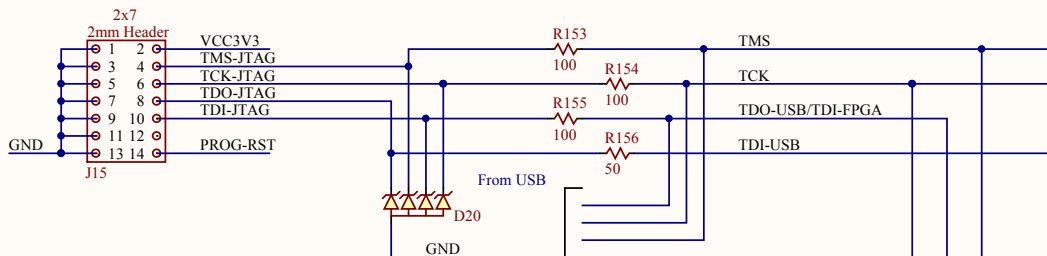
Title ZED		Rev C.1
Circuit Audio Codec		Copyright 2012
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Engineer	EG	
Author	GMA	
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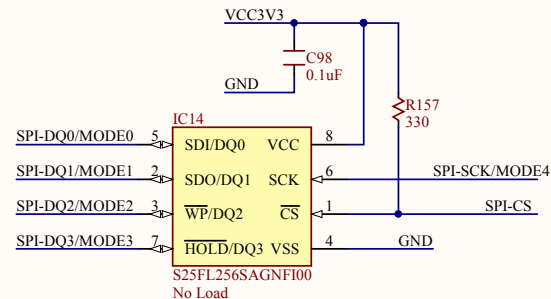
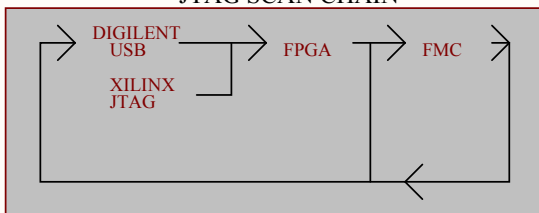


Title		Rev	
ZED		C.1	
Circuit		Ethernet, OLED and SD Card	
Doc#		500-248	
Engineer		EG	
Author		GMA	
Date		6/20/2012	
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		Copyright 2012	
		BEYOND THEORY	

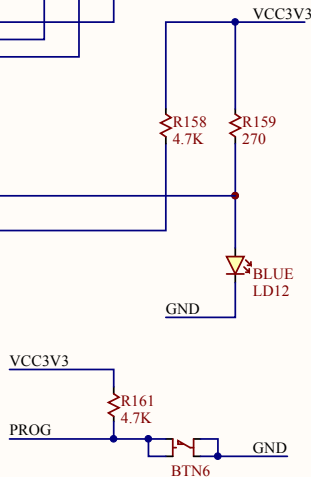
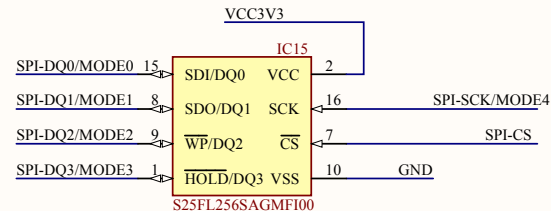
Xilinx JTAG Header



JTAG SCAN CHAIN



Note: Load either package, not both. Default SOIC16



Title ZED		Rev C.1
Circuit FPGA Configuration		Copyright 2012
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Author	GMA	
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VCC3V3

VCC3V3

VADJ

VADJ

BANK 13		
IO_0	R7	FMC-SCL
IO_25	R7	FMC-SDA
IO_L1N_T0	R9	JB9
IO_L1P_T0	R10	JB3
IO_L2N_T0	W8	JB4
IO_L2P_T0	W8	JB10
IO_L3N_T0_DQS	W10	JB8
IO_L3P_T0_DQS	W11	JB2
IO_L4N_T0	W12	JB1
IO_L4P_T0	W12	JB7
IO_L5N_T0	U11	OLED-VBAT
IO_L5P_T0	U12	OLED-VDD
IO_L6N_T0_VREF	U9	OLED-RES
IO_L6P_T0	U10	OLED-DC
IO_L7N_T1	AB12	OLED-SCLK
IO_L7P_T1	AA12	OLED-SDIN
IO_L8N_T1	AB11	JA7
IO_L8P_T1	AA11	JA2
IO_L9N_T1_DQS	AB9	JA9
IO_L9P_T1_DQS	AB10	JA8
IO_L10N_T1	V10	JA3
IO_L10P_T1	V11	JA1
IO_L11N_T1_SRCC	AA8	JA10
IO_L11P_T1_SRCC	AA9	JA4
IO_L12N_T1_MRCC	R8	AC-GPIO0
IO_L12P_T1_MRCC	R9	GCLK
IO_L13N_T2_MRCC	R5	AC-ADR1
IO_L13P_T2_MRCC	R6	AC-GPIO3
IO_L14N_T2_SRCC	AA6	AC-GPIO2
IO_L14P_T2_SRCC	AA7	AC-GPIO1
IO_L15N_T2_DQS	AB1	AC-ADR0
IO_L15P_T2_DQS	AB2	AC-MCLK
IO_L16N_T2	AB4	AC-SCK
IO_L16P_T2	AB5	AC-SDA
IO_L17N_T2	AB6	JC1 N
IO_L17P_T2	AB7	JC1 P
IO_L18N_T2	AA4	JC2 N
IO_L18P_T2	AA4	JC2 P
IO_L19N_T3_VREF	R4	JC3 N
IO_L19P_T3	R6	JC3 P
IO_L20N_T3	U4	JC4 N
IO_L20P_T3	U4	JC4 P
IO_L21N_T3_DQS	V4	JD2 N
IO_L21P_T3_DQS	V5	JD2 P
IO_L22N_T3	U5	JD4 N
IO_L22P_T3	U6	JD4 P
IO_L23N_T3	W7	JD1 N
IO_L23P_T3	W7	JD1 P
IO_L24N_T3	W5	JD3 N
IO_L24P_T3	W6	JD3 P

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BANK 33		
IO_0	U19	LD6
IO_25	U14	LD7
IO_L1N_T0	U21	LD3
IO_L1P_T0	U21	LD1
IO_L2N_T0	U22	LD2
IO_L2P_T0	U22	LD0
IO_L3N_T0_DQS	W22	LD5
IO_L3P_T0_DQS	W22	LD4
IO_L4N_T0	W21	
IO_L4P_T0	W20	VGA-R1
IO_L5N_T0	U20	VGA-R2
IO_L5P_T0	V19	VGA-R3
IO_L6N_T0_VREF	V18	VGA-R4
IO_L6P_T0	AB22	VGA-G1
IO_L7N_T1	AA22	VGA-G2
IO_L7P_T1	AB21	VGA-G3
IO_L8N_T1	AA21	VGA-G4
IO_L8P_T1	U21	VGA-B1
IO_L9N_T1_DQS	V20	VGA-B2
IO_L9P_T1_DQS	AB20	VGA-B3
IO_L10N_T1	AB19	VGA-B4
IO_L10P_T1	AA19	VGA-HS
IO_L11N_T1_SRCC	V19	VGA-VS
IO_L11P_T1_SRCC	AA18	HD-SCL
IO_L12N_T1_MRCC	V18	HD-SPDIF0
IO_L12P_T1_MRCC	V18	HD-CLK
IO_L13N_T2_MRCC	W17	HD-VSYNC
IO_L13P_T2_MRCC	W16	HD-SDA
IO_L14N_T2_SRCC	W16	HD-INT
IO_L14P_T2_SRCC	U16	HD-DE
IO_L15N_T2_DQS	U15	HD-SPDIF
IO_L15P_T2_DQS	V17	HD-HSYNC
IO_L16N_T2	U17	HD-D13
IO_L16P_T2	AB17	HD-D7
IO_L17N_T2	AA17	HD-D8
IO_L17P_T2	AB16	HD-D5
IO_L18N_T2	AA16	HD-D6
IO_L18P_T2	V15	HD-D12
IO_L19N_T3_VREF	V14	HD-D14
IO_L19P_T3	W13	HD-D10
IO_L20N_T3	V13	HD-D15
IO_L20P_T3	V15	HD-D9
IO_L21N_T3_DQS	W15	HD-D11
IO_L21P_T3_DQS	AA14	HD-D2
IO_L22N_T3	V14	HD-D3
IO_L22P_T3	AA13	HD-D1
IO_L23N_T3	V13	HD-D0
IO_L23P_T3	AB15	HD-D4
IO_L24N_T3	U14	FMC-PRSN1
IO_L24P_T3	AB14	FMC-PRSN1

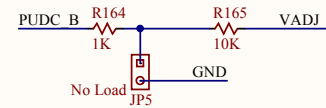
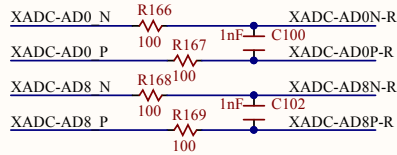
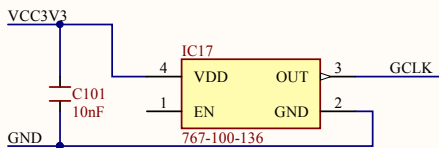
IC16C XC7Z020CLG484

BANK 34		
IO_0	H15	XADC-GIO0
IO_25	R15	XADC-GIO1
IO_L1N_T0	R15	XADC-GIO2
IO_L1P_T0	R15	XADC-GIO3
IO_L2N_T0	R17	FMC-LA15_N
IO_L2P_T0	R16	FMC-LA15_P
IO_L3N_T0_DQS	R16	OTG-VBUSOC
IO_L3P_T0_DQS	R16	PUDC B
IO_L4N_T0	M17	FMC-LA13_N
IO_L4P_T0	L17	FMC-LA13_P
IO_L5N_T0	N18	FMC-LA11_N
IO_L5P_T0	N17	FMC-LA11_P
IO_L6N_T0_VREF	M16	FMC-VREF
IO_L6P_T0	M15	SW7
IO_L7N_T1	R18	FMC-LA05_N
IO_L7P_T1	R18	FMC-LA05_P
IO_L8N_T1	R22	FMC-LA08_N
IO_L8P_T1	R21	FMC-LA08_P
IO_L9N_T1_DQS	R21	FMC-LA16_N
IO_L9P_T1_DQS	R20	FMC-LA16_P
IO_L10N_T1	R22	FMC-LA06_N
IO_L10P_T1	R21	FMC-LA06_P
IO_L11N_T1_SRCC	R20	FMC-LA14_N
IO_L11P_T1_SRCC	R19	FMC-LA14_P
IO_L12N_T1_MRCC	R19	FMC-CLK0_N
IO_L12P_T1_MRCC	R18	FMC-CLK0_P
IO_L13N_T2_MRCC	M20	FMC-LA00_CC_N
IO_L13P_T2_MRCC	M19	FMC-LA00_CC_P
IO_L14N_T2_SRCC	N20	FMC-LA01_CC_N
IO_L14P_T2_SRCC	N19	FMC-LA01_CC_P
IO_L15N_T2_DQS	M22	FMC-LA04_N
IO_L15P_T2_DQS	M21	FMC-LA04_P
IO_L16N_T2	R22	FMC-LA03_N
IO_L16P_T2	R22	FMC-LA03_P
IO_L17N_T2	R21	FMC-LA09_N
IO_L17P_T2	R20	FMC-LA09_P
IO_L18N_T2	R21	FMC-LA12_N
IO_L18P_T2	R20	FMC-LA12_P
IO_L19N_T3_VREF	R15	FMC-VREF
IO_L19P_T3	N15	BTNL
IO_L20N_T3	R18	FMC-LA02_N
IO_L20P_T3	R17	FMC-LA02_P
IO_L21N_T3_DQS	R17	FMC-LA07_N
IO_L21P_T3_DQS	R16	FMC-LA07_P
IO_L22N_T3	R19	FMC-LA10_N
IO_L22P_T3	R18	FMC-LA10_P
IO_L23N_T3	R18	BTNU
IO_L23P_T3	R16	BTNR
IO_L24N_T3	R16	BTND
IO_L24P_T3	R16	BTNC

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BANK 35		
IO_0	H17	SW6
IO_25	H18	SW5
IO_L1N_T0_AD0N	E16	XADC-AD0N-R
IO_L1P_T0_AD0P	E16	XADC-AD0P-R
IO_L2N_T0_AD8N	D17	XADC-AD8N-R
IO_L2P_T0_AD8P	D16	XADC-AD8P-R
IO_L3N_T0_DQS_AD1N	D15	FMC-LA23_N
IO_L3P_T0_DQS_AD1P	E15	FMC-LA23_P
IO_L4N_T0	G16	FMC-LA19_N
IO_L4P_T0	G15	FMC-LA19_P
IO_L5N_T0_AD9N	E18	FMC-LA26_N
IO_L5P_T0_AD9P	F18	FMC-LA26_P
IO_L6N_T0_VREF	F17	FMC-VREF
IO_L6P_T0	G17	OTG-RESETN
IO_L7N_T1_AD2N	B15	FMC-LA30_N
IO_L7P_T1_AD2P	C15	FMC-LA30_P
IO_L8N_T1_AD10N	B17	FMC-LA31_N
IO_L8P_T1_AD10P	B16	FMC-LA31_P
IO_L9N_T1_DQS_AD3N	A17	FMC-LA28_N
IO_L9P_T1_DQS_AD3P	A16	FMC-LA28_P
IO_L10N_T1_AD11N	A19	FMC-LA24_N
IO_L10P_T1_AD11P	A18	FMC-LA24_P
IO_L11N_T1_SRCC	C18	FMC-LA29_N
IO_L11P_T1_SRCC	C17	FMC-LA29_P
IO_L12N_T1_MRCC	D19	FMC-CLK1_N
IO_L12P_T1_MRCC	D18	FMC-CLK1_P
IO_L13N_T2_MRCC	B20	FMC-LA17_CC_N
IO_L13P_T2_MRCC	B19	FMC-LA17_CC_P
IO_L14N_T2_AD4N_SRCC	C20	FMC-LA18_CC_N
IO_L14P_T2_AD4P_SRCC	D20	FMC-LA18_CC_P
IO_L15N_T2_DQS_AD12N	A22	FMC-LA32_N
IO_L15P_T2_DQS_AD12P	A21	FMC-LA32_P
IO_L16N_T2	C22	FMC-LA25_N
IO_L16P_T2	D22	FMC-LA25_P
IO_L17N_T2_AD5N	D21	FMC-LA27_N
IO_L17P_T2_AD5P	E21	FMC-LA27_P
IO_L18N_T2_AD13N	B22	FMC-LA33_N
IO_L18P_T2_AD13P	B21	FMC-LA33_P
IO_L19N_T3_VREF	H20	FMC-VREF
IO_L19P_T3	H19	SW4
IO_L20N_T3_AD6N	F19	FMC-LA22_N
IO_L20P_T3_AD6P	G19	FMC-LA22_P
IO_L21N_T3_DQS_AD14N	E20	FMC-LA21_N
IO_L21P_T3_DQS_AD14P	E19	FMC-LA21_P
IO_L22N_T3_AD7N	G21	FMC-LA20_N
IO_L22P_T3_AD7P	G20	FMC-LA20_P
IO_L23N_T3	F22	SW0
IO_L23P_T3	F21	SW3
IO_L24N_T3_AD15N	G22	SW1
IO_L24P_T3_AD15P	H22	SW2

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Circuit		Copyright 2012
FPGA Banks		
Doc#	500-248	
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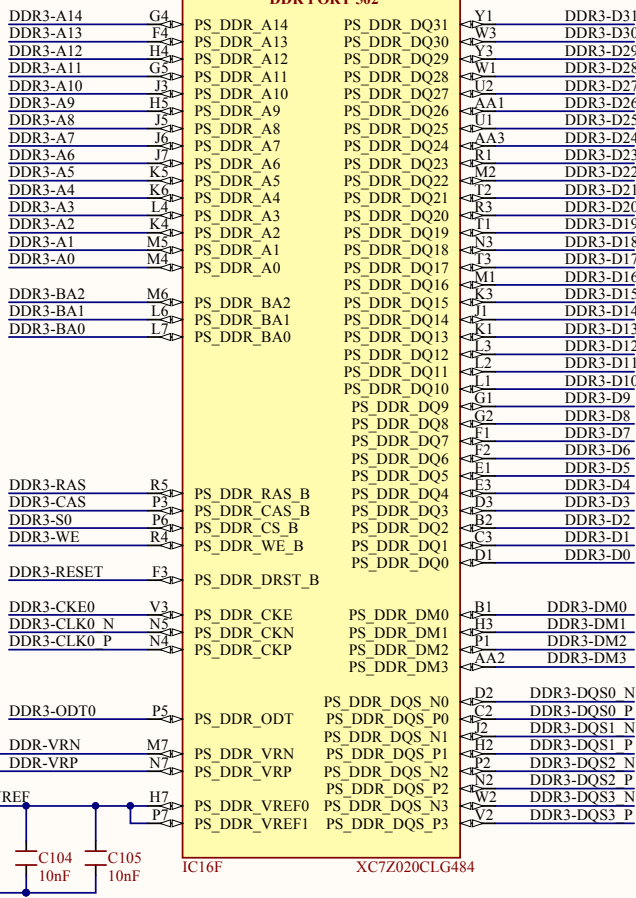
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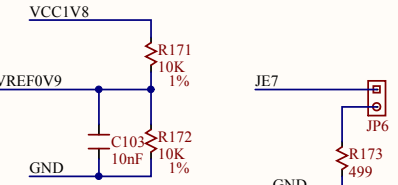
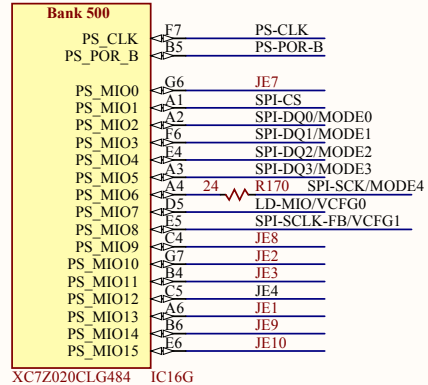
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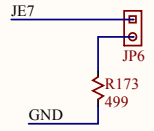
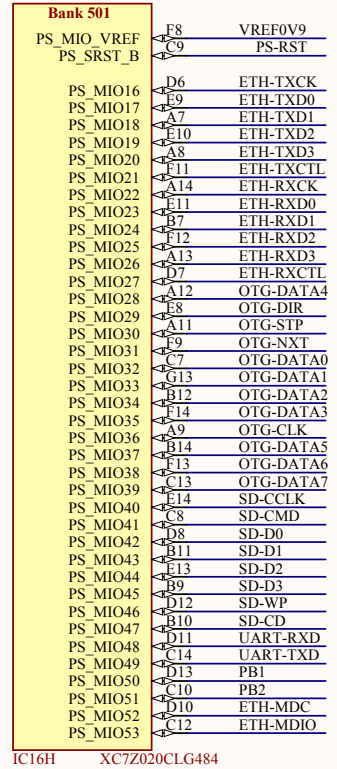
DDR1V5



VCC3V3

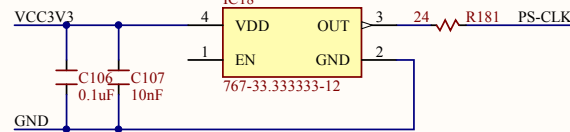
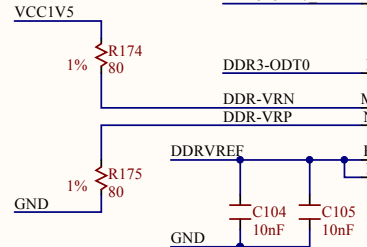
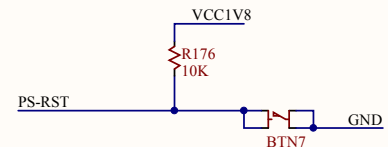
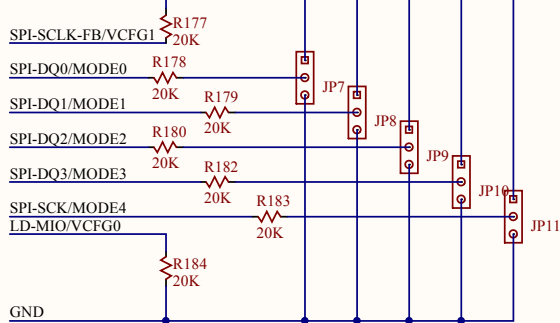


VCC1V8

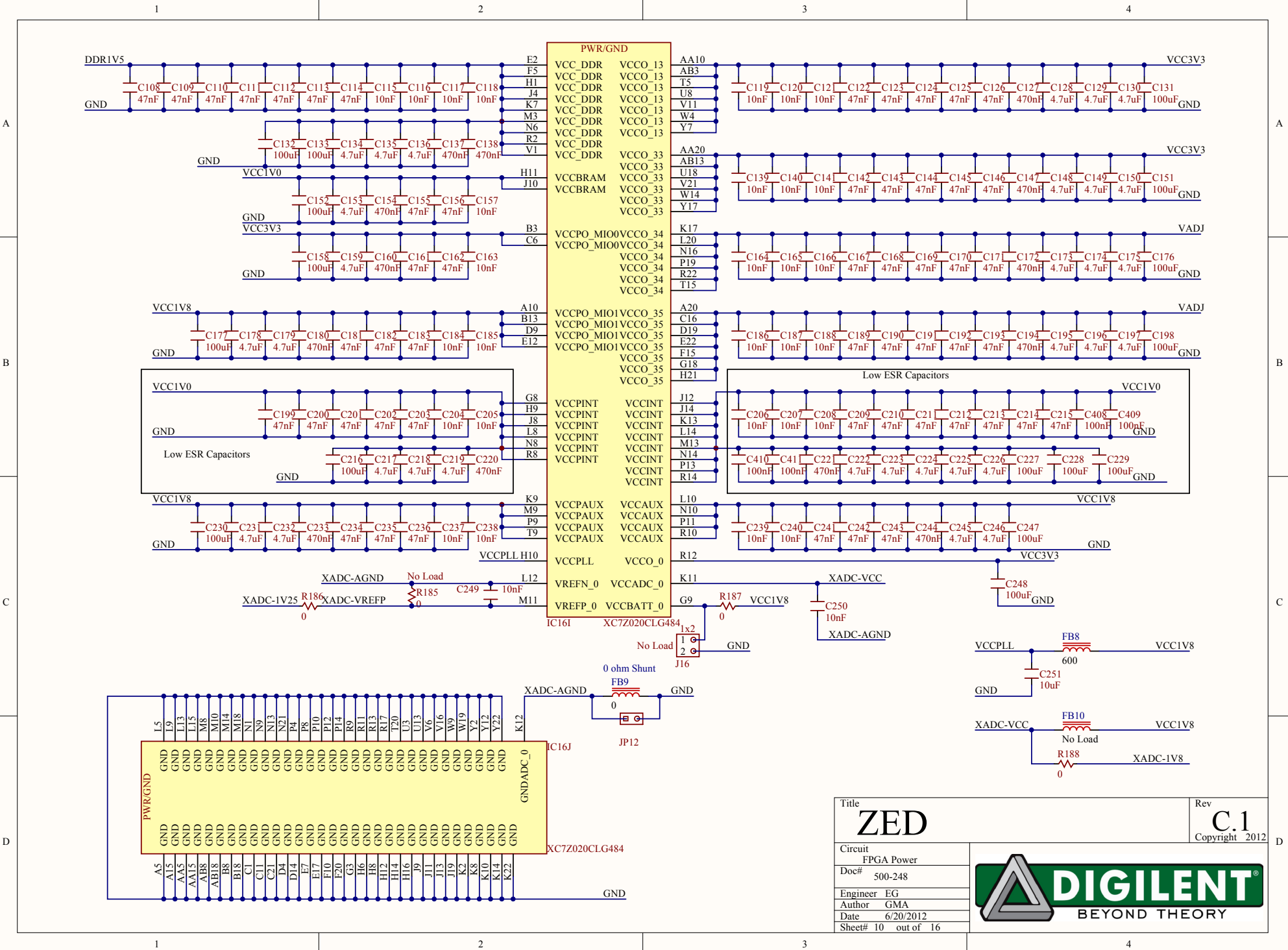


BOOT SETTING
 QSPI X001X
 JTAG 0000X

VCC3V3

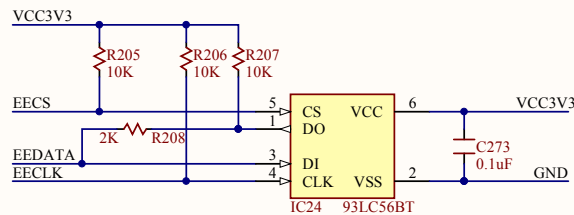
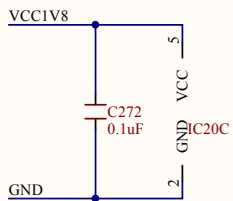
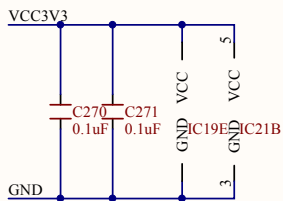
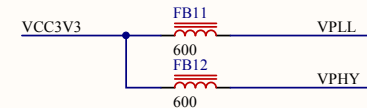
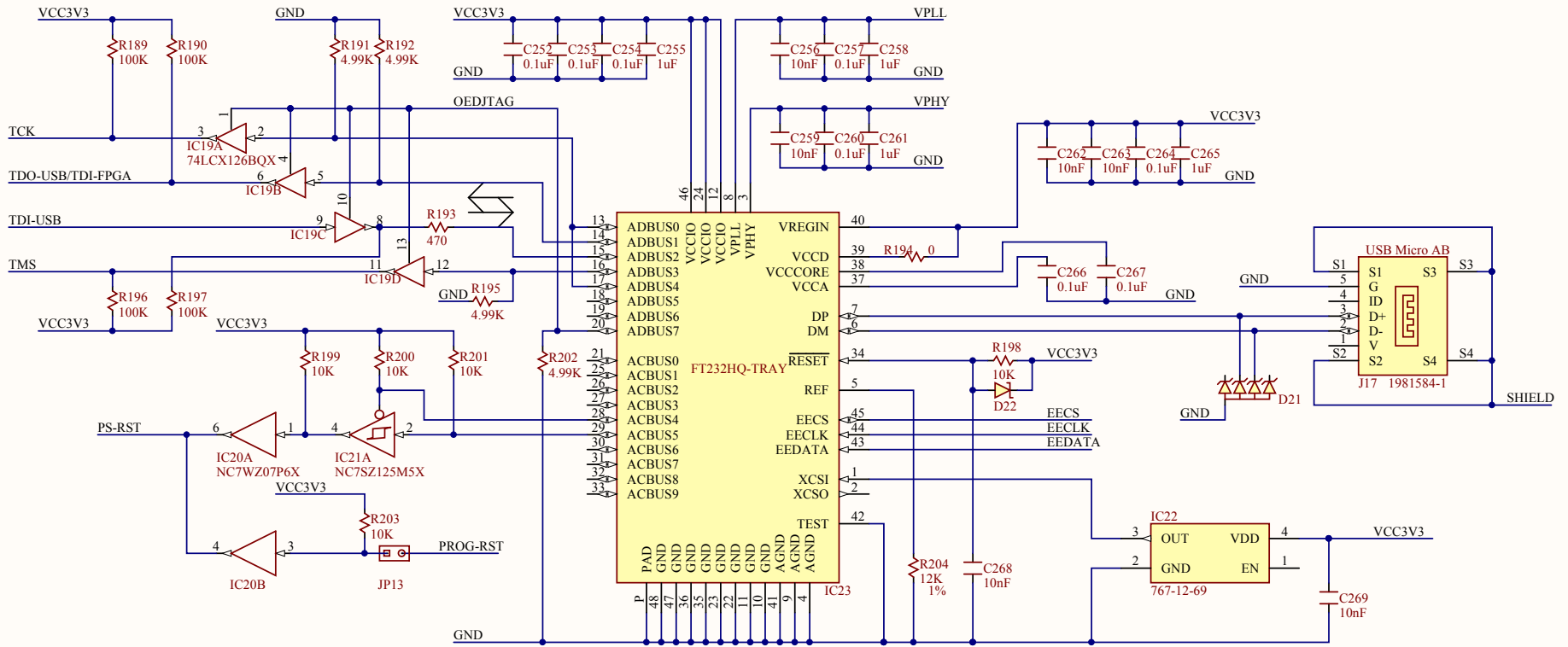


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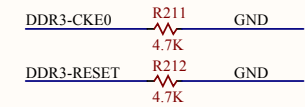
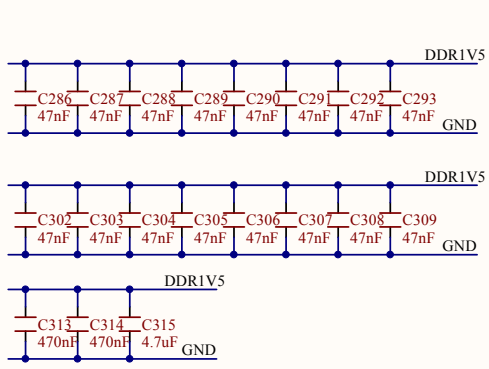
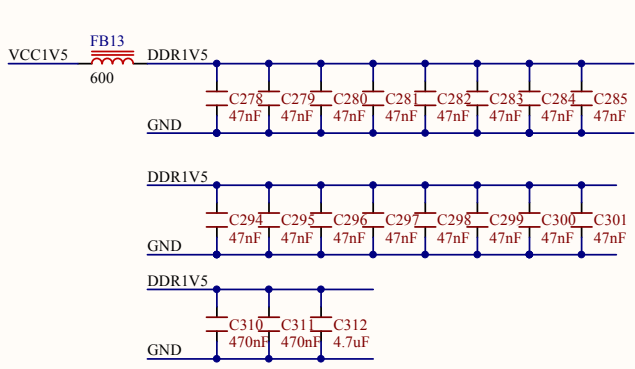
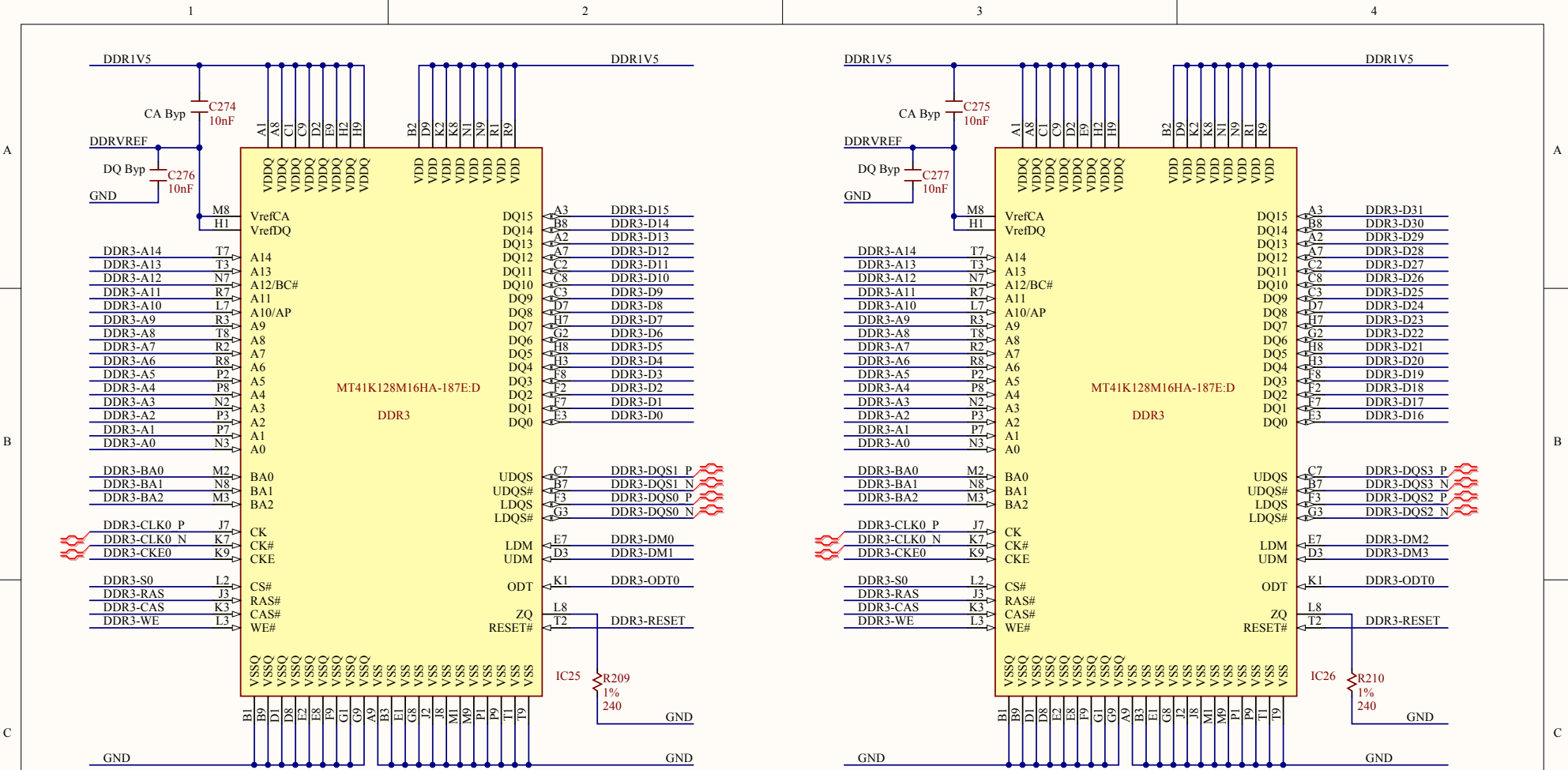
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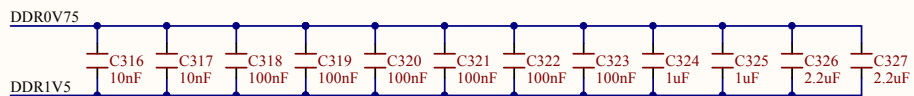
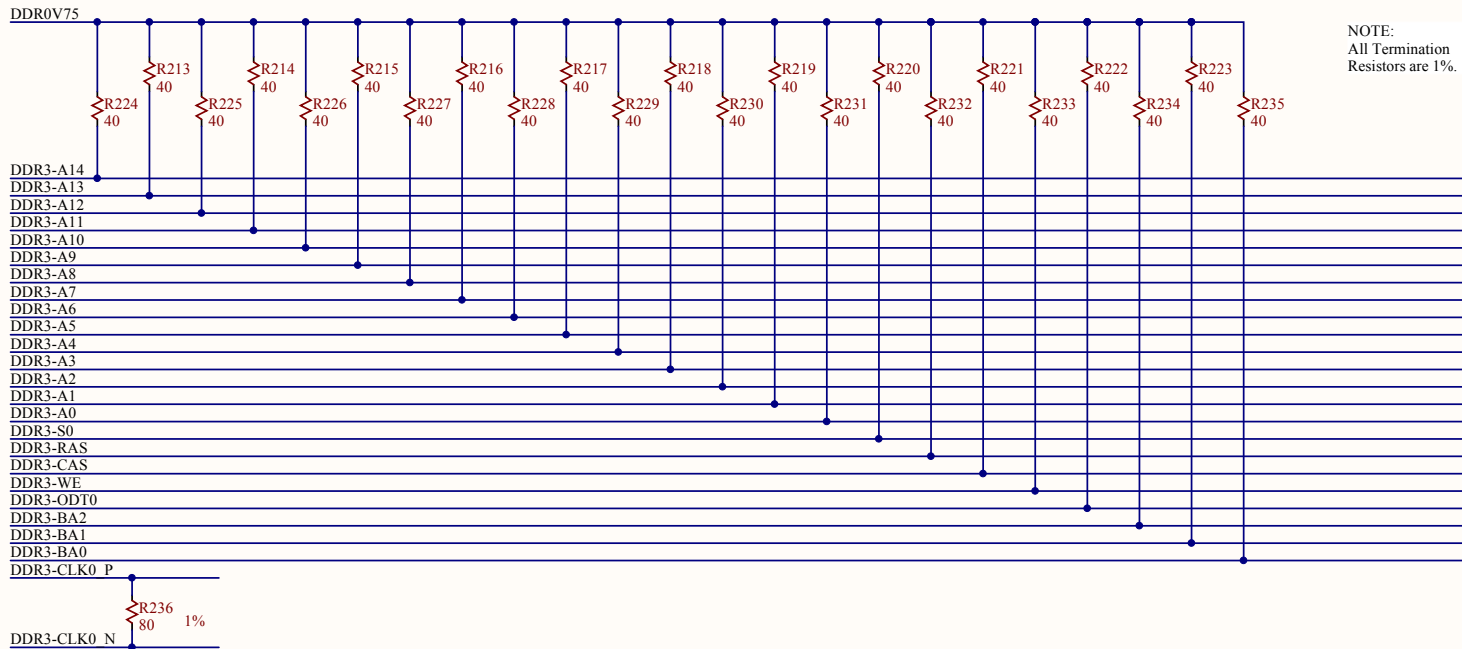
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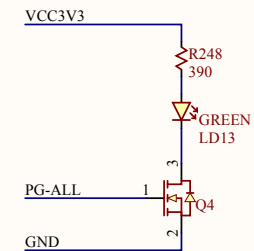
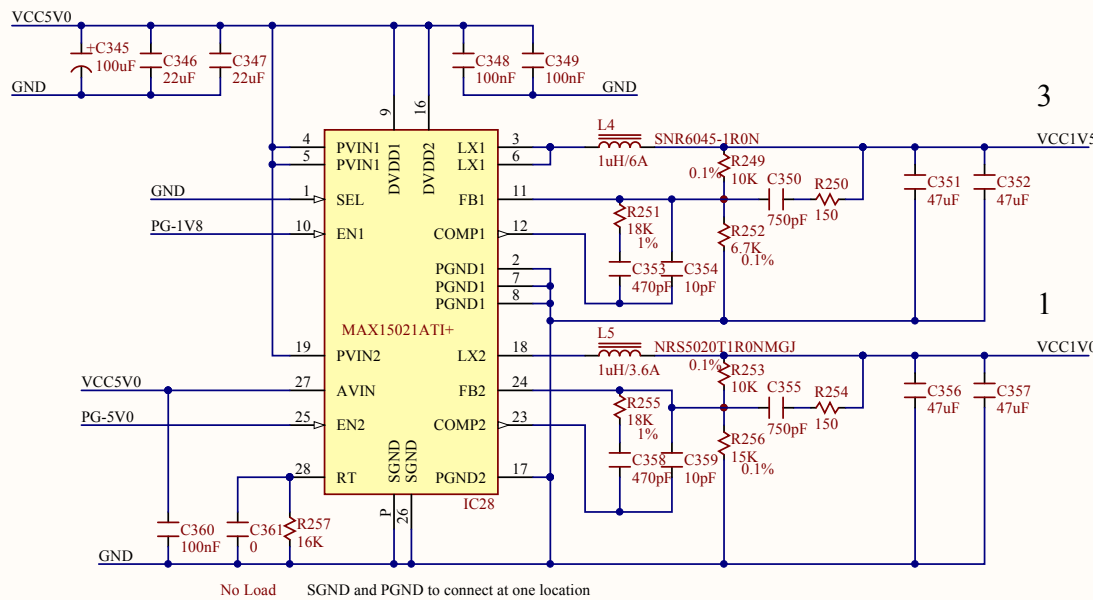
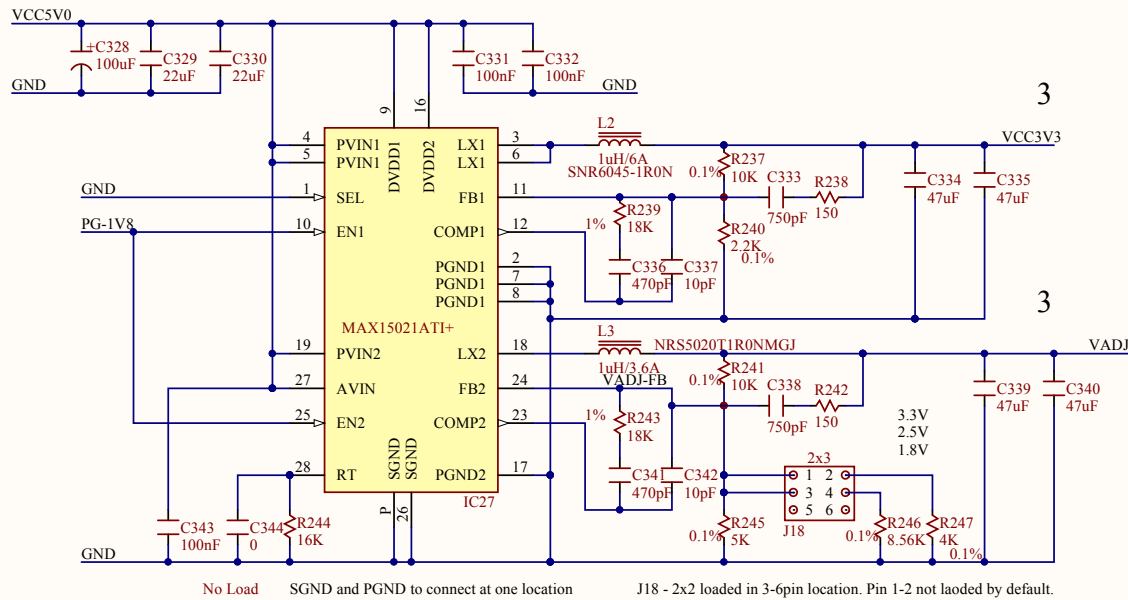


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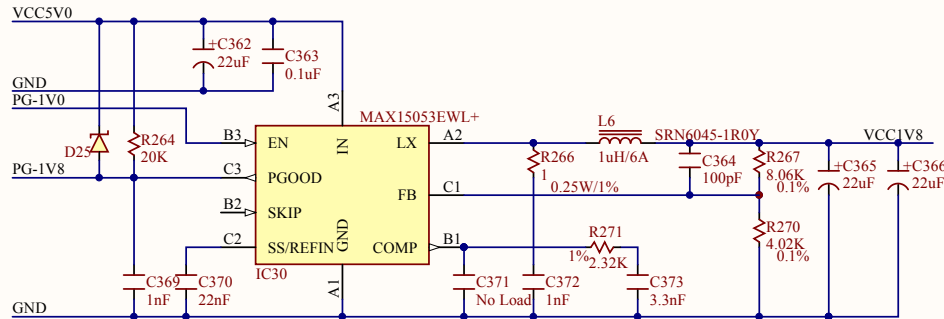
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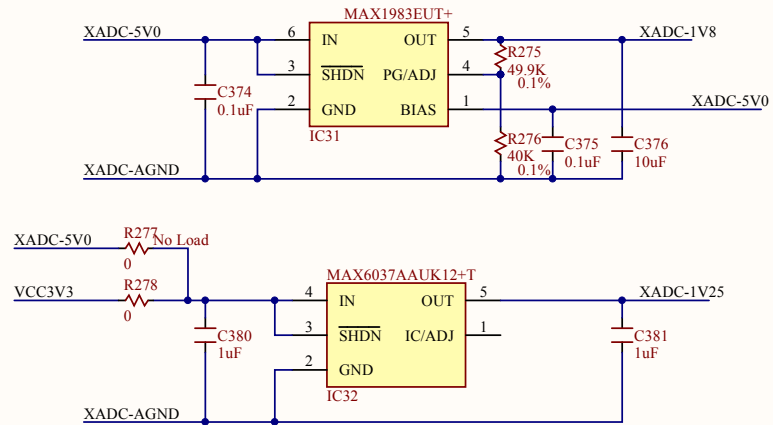
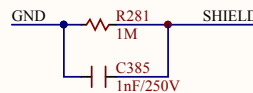
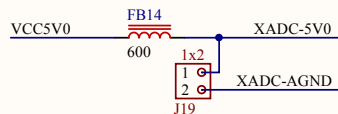
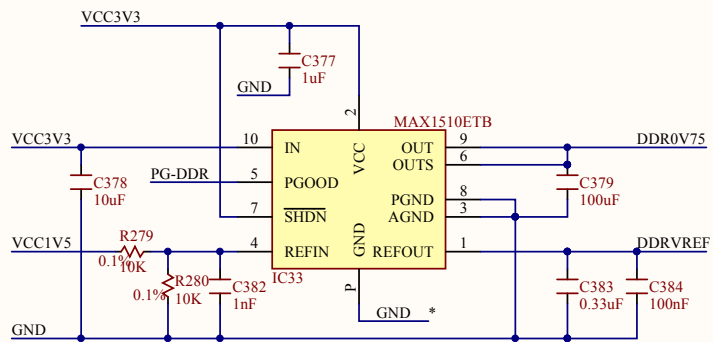
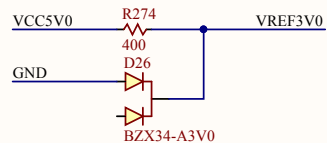
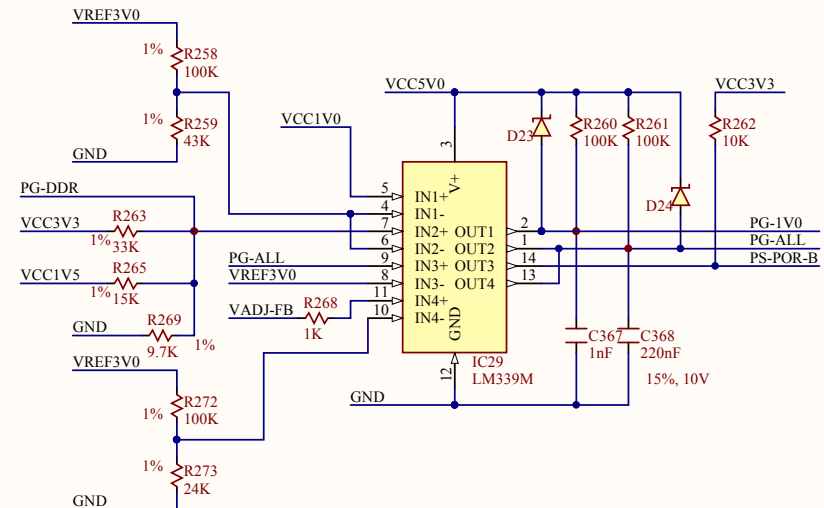
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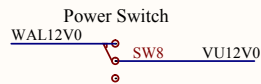
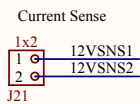
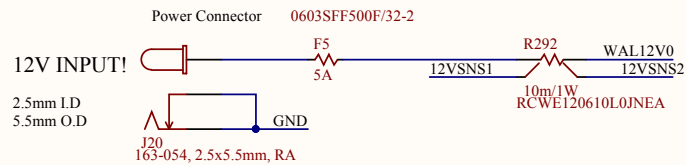
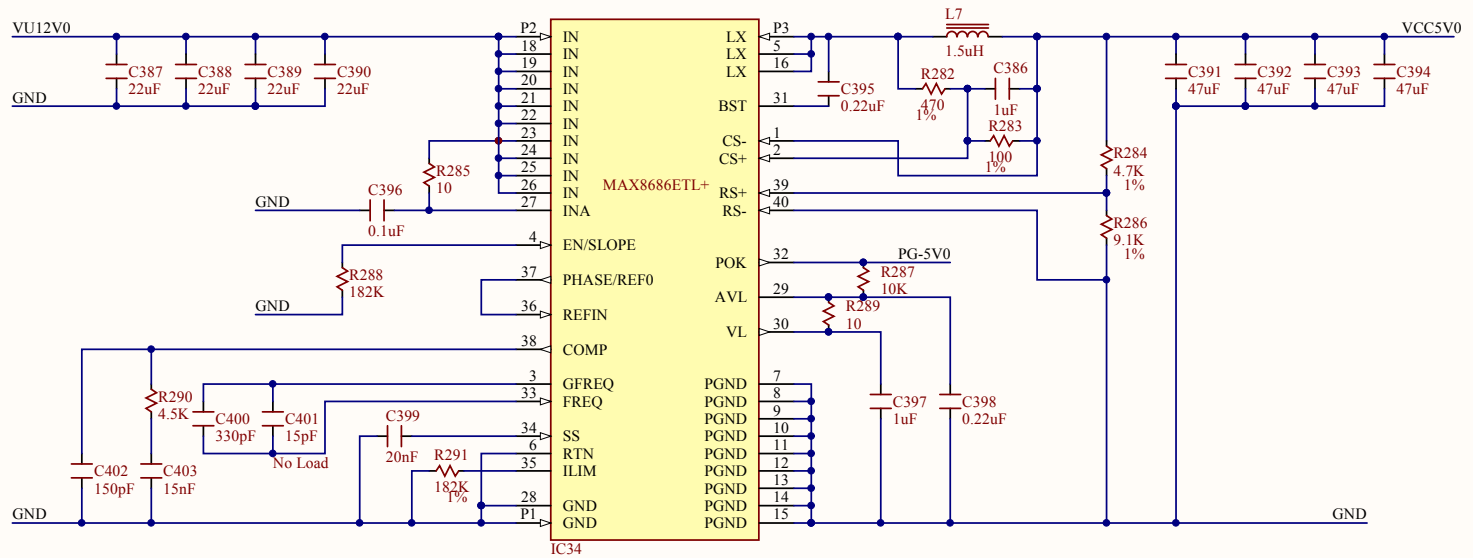
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