XUP Virtex-II Pro Quick Start

System Generator for DSP
Performing Hardware-in-the-Loop
Via JTAG Co-Simulation

Introduction

This quick start will guide you through the process of setting up the XUP Virtex-II Pro board to enable hardware-in-the-loop verification via JTAG co-simulation. This process can be extended to any board with a JTAG connection

References

- Matlab help menu → Xilinx System Generator → JTAG hardware co-simulation
- XUP Virtex-II Pro user guide (http://www.xilinx.com/univ/xupv2p.html)

Requirements

- Matlab R14.1 with Signal Processing blockset
- V7.1 ISE Foundation with latest service pack
- V7.1 System Generator for DSP
- XUP Virtex-II Pro board with Power Supply
- Xilinx Parallel-IV JTAG download cable (USB cable not supported for hardware-in-the-loop verification)

Directory Structure

- /design/user (contains the user Simulink design file)
- /design/completed (contains the completed Simulink design file)
- /digilent (contains the board support package for the XUP Virtex-II Pro)

Design Description

Simulate a digital band-pass filter with the following specifications:

- Sampling Frequency (Fs) = 1.5 MHz
- Fstop 1 = 270 kHz
- Fpass 1 = 300 kHz
- Fpass 2 = 450 khz
- Fstop 2 = 480 kHz
- Attenuation on both sides of the passband = 54 dB
- Pass band ripple = 1

Two different sources are used to simulate the filter:
- The chirp block, which sweeps between the specified frequencies of 6 KHz and 10 KHz without regard for the instantaneous output frequency
- The random source generator, which outputs a random signal of uniform distribution with a range of -1.9 to 1.9. Uniform is a better choice to drive a fixed-point filter because it is bounded.

Steps

- Generate board support package
- Simulate an FIR filter and generate the run-time hardware model
- Connect hardware model to the design and perform a hardware in the loop verification

Generate Board Support Package   Step 1

You will quickly generate the board support package for the XUP board using SBDBuilder, which is a graphical utility to automate the four board support package files. Refer to the Matlab help menu for detailed information on SBDBuilder and XUP Virtex-II Pro user manual for information on the board.
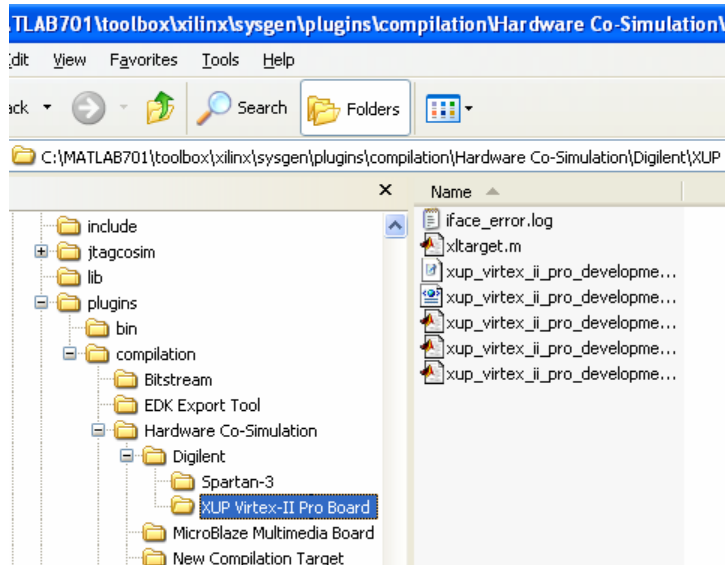
❶ Invoke SBDBuilder by typing the following at the Matlab command prompt: xlSBDBuilder

❷ Enter a the target board information and clock sections as follows:
- Board Name: XUP Virtex-II Pro
- Frequency (MHz): 100 (This is the system clock frequency on the XUP board)
- Pin Location: AJ15 (This is the pin location of the system clock)

❸ Connect the Parallel-IV cable to the JTAG port of the XUP board and turn the power on.

❹ Fill in the following for JTAG options
- Boundary Scan Position: 3 (the Virtex-II Pro xc2vp30 is the third device in the JTAG chain)
- IR Lengths: Click the Detect button (should see: 16, 8, 14)

Note: you may verify the position of the xc2vp30 in the chain by using the impact programming utility provided with the ISE Foundation software. The impact utility can be invoked as standalone via the start menu.

❺ Under the **Targetable Devices** section, add the xc2vp30-7ff896

❻ Click the Save Files button and save the files under the system generator install path as follows:

C:\MATLAB701\toolbox\xilinx\sysgen\plugins\compilation\Hardware Co-Simulation\digilent\XUP Virtex-II Pro Board

The installation of the board support package files should resemble that as follows:
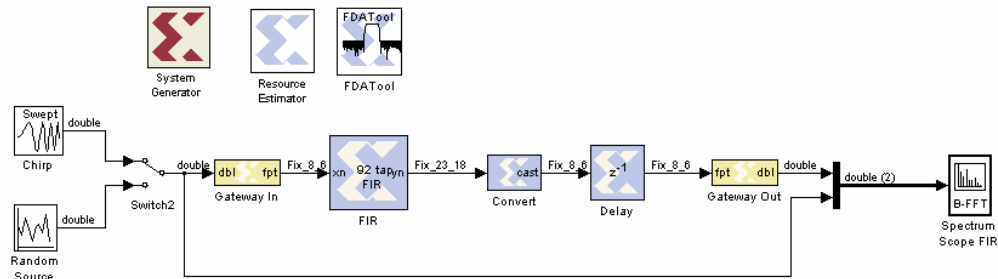

❼ Exit SBDBuilder

Simulate an FIR Filter and Generate Hardware Model   Step 2
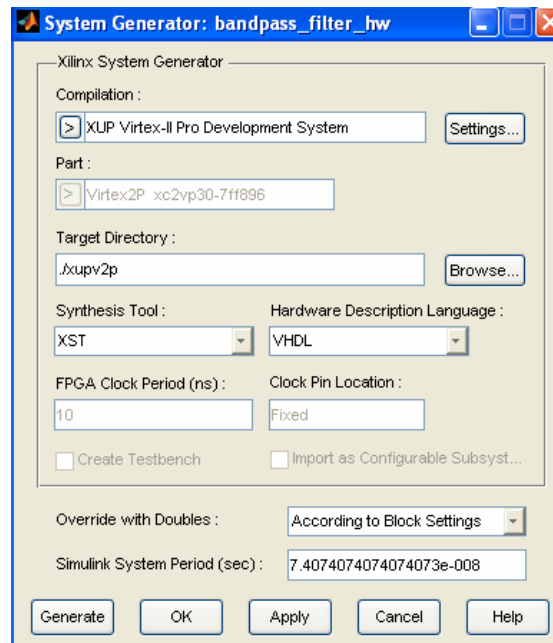
Simulate a band-pass FIR filter to verify operation and generate the run-time hardware model.

❶ Invoke Matlab and browse to the /design/user directory

❷ Open the band_pass.mdl file and simulate the design.
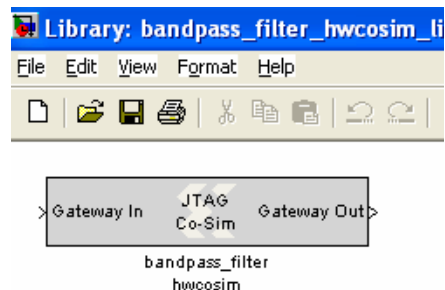
Note: Your design should look like that shown below.

❸ Double click on the system generator token to verify that the following options are selected:
- Compilation: XUP Virtex-II Pro Board
- Target Directory: ./xupv2p
- Synthesis Tool: XST
- Hardware Description Language: VHDL

Note: You may select either VHDL or Verilog

❹ Click the generate button to generate the run-time hardware model (see illustration below)

Note: System Generator will generate the HDL Code and automatically invoke the ISE Foundation software to generate the bitstream. The run-time block above represents the hardware model of the System Generator design.
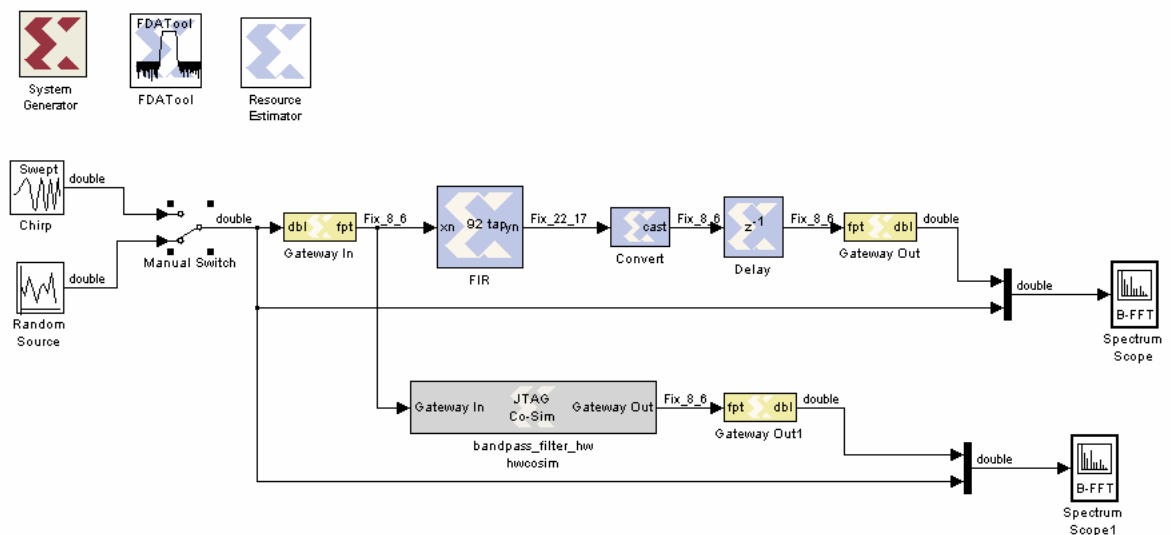
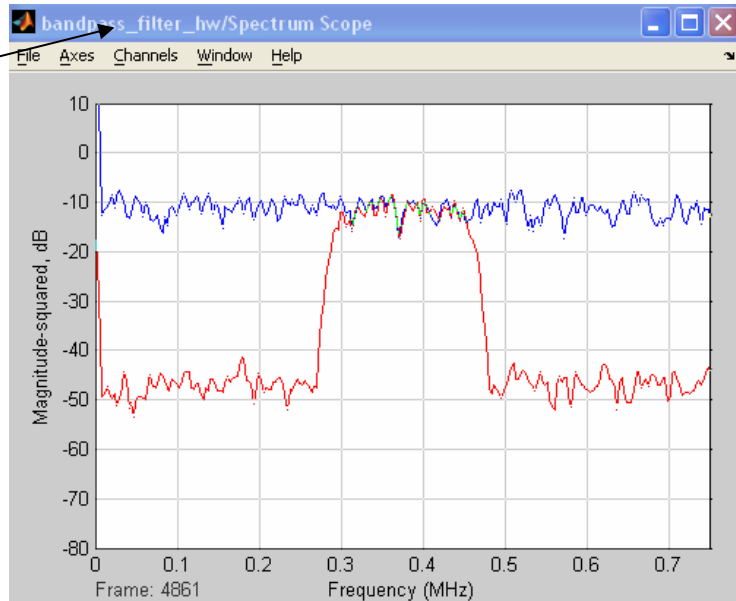Connect the hardware run-time model to the design and perform hardware-in-the-loop verification.

❶ Add the run-time block and connect it according to the figure below, noting that you may simply copy and paste the Spectrum scope and mux.

❷ Click the **Start Simulation** button to perform the hardware-in-the-loop verification.

System Generator will configure the FPGA and then simulate. You should see results as follows:

Software Simulation

Hardware Simulation