Xilinx Spartan-3 Starter Kit Master System Example (EDK)

Introduction

This system is a working example that shows how each of the peripherals on the Spartan-3 Starter Kit board can be used with the Embedded Development Kit. It is intended that a user be able to choose the hardware or software functionality they need and build onto strip out of this system. The system includes the OPB EMC, OPB GPIO and LMB BRAM as EDK IP included. The system also includes a OPB character mapped VGA controller, OPB 7-segment display interface and a FSL PS/2 keyboard interface.

Hardware Requirements:

- Xilinx Spartan-3 Starter Kit Board
- Serial cable
- Parallel 4 Download Cable or low cost JTAG3 download cable

Software Requirements:

- Embedded Development Kit (EDK) 6.2 (Version G.28) or later
- ISE 6.2i (Version G.23) or later

Design Contents

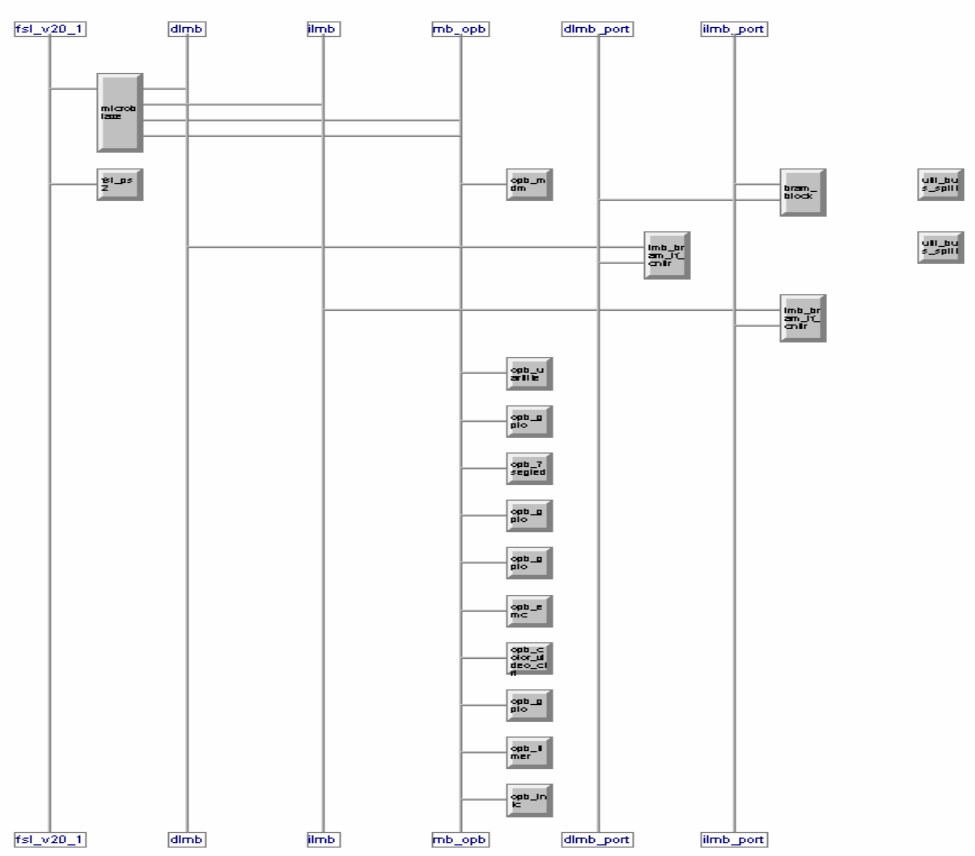

Figure 1: PBD Snapshot

Local Memory Bus (LMB)

The Local Memory Bus (LMB) is a synchronous bus used primarily to access on-chip block RAM. It uses a minimum number of control signals and a simple protocol to ensure that local block RAM is accessed in a single clock cycle.

- **LMB Masters**
  - CPU Instruction-Side LMB Interface
  - CPU Data-Side LMB Interface
- **LMB Slaves**
  - Instruction BRAM Controller
  - Data BRAM Controller

On-Chip Peripheral Bus (OPB)

The OPB connects lower-performance peripheral devices to the system. The OPB has a less complex architecture, which simplifies peripheral development. The OPB devices in the reference system include:

- **OPB Masters**
  - CPU Data-Side OPB Interface (Master ID = 0)
  - Note: The CPU Instruction-Side OPB Interface has not been connected.
- **OPB Slaves**
  - Microprocessor Debug Module (MDM)
  - UART Lite
  - GPIO (8-bit) for switches
  - GPIO (8-bit) for LEDs
  - GPIO (3-bit) for buttons
  - 7-segment display core
  - timer
  - interrupt controller
  - External Memory Controller (EMC)
  - Character mapped VGA controller

Fast Simplex Link (FSL)

The FSL is a point to point bus for high bandwidth data transfers. This is often used for hardware acceleration. The FSL devices in the reference system include:

- **FSL Master**
  - PS/2 keyboard core
- **FSL Slaves**
  - MicroBlaze FSL port 1

IP Source Version

Core Name	Version	Source
microblaze	2.10.a	EDK Installation
opb_mdm	2.00.a	EDK Installation
lmb_bram_if_cntrl	1.00.b	EDK Installation
bram_block	1.00.a	EDK Installation
opb_uartlite	1.00b	EDK Installation
opb_gpio	3.01.a	EDK Installation
opb_7segled	1.00.a	Pcores
Opb_emc	1.10.b	EDK Installation
opb_color_video_cntrl	1.00.a	Pcores
util_bus_split	1.00.a	EDK Installation

fsl_ps2	1.00.a	Pcores
opb_timer	1.00.b	EDK Installation
opb_intc	1.00.c	EDK Installation

Table 1: IP Source Version

Memory Map

Bus	IP	Base Address	High Address	Size
LMB Bus				
	lmb_bram_if_cntrl	0x0000_0000	0x0000_1FFF	8KB
	lmb_bram_if_cntrl	0x0000_0000	0x0000_1FFF	8KB
OPB Bus				
	opb_mdm	0x8010_0000	0x8010_00FF	256B
	opb_uartlite	0x8010_0100	0x8010_01FF	256B
	opb_gpio	0x8010_0200	0x0000_03FF	512B
	opb_7segled	0x8010_0400	0x8010_05ff	512B
	opb_gpio	0x8010_0600	0x8010_07ff	256B
	opb_gpio	0x8010_0800	0x8010_09ff	256B
	opb_emc	0x8010_0a00	0x8010_0a1f	32B
	opb_color_video _cntrl	0x8200_0000	0x8200_FFFF	64KB
	opb_gpio	0x8010_1200	0x8010_13FF	512B
	opb_timer	0x8010_1a00	0x8010_1aff	256B
	opb_intc	0x8010_1b00	0x8010_1bff	256B

Table 2: Memory Map

Custom Core Description

- OPB_color_video_cntrl – 8 color character mapped VGA controller for the On-Chip Peripheral (OPB)
- OPB_7segled – 7-segment four digit interface core for the On-Chip Peripheral (OPB)
- FSL_PS2 – PS/2 keyboard core for the high bandwidth Fast Simplex Link (FSL) bus.

EDK Information

Design

The EDK design is a top-level VHDL design. The design is described entirely within EDK to simplify the design flow.

Project Sub-Directory File Description

Directory	File	Description
TestApp\src	Vga.c / vga.h	OPB_controller_video_cntrl drivers
TestApp\src	Kbd.c	FSL PS/2 keyboard drivers
TestApp\src	LED_disp.c	7 segment LED core driver
TestApp\src	Testapp.c	Sample code on how to use each of the individual components.
data	system.ucf	Timing constraints and pin locations for Spartan-3 200 demonstration board
etc	bitgen.ut	Bitgen options
	download.cmd	IMPACT command file for downloading download.bit
	Fast_runtime.opt	XFLOW option file for Translate, MAP, and PAR
pcores	OPB_color_video_cntrl	Character mapped color video controller
	OPB_7segled	Four digit 7-segment display controller
	FSL_PS/2	PS/2 Keyboard core
sim	Start_simulation.bat	Starts the behavioral simulation
	System_start.do	ModelSim DO file which loads the simuation
	testbench.vhd	Testbench to drive clock and reset signals
	system.xmp	XPS project file
project	system.mhs	Microprocessor Hardware Specification
	system.mss	Microprocessor Software Specification

Table 3: Customized File Description

Implementation

1. In XPS, select the Applications tab.
2. Right click on “Project: TestApp” and deselect Mark to Initialize BRAMs.
   - **Note:** All of the other projects should also be deselected.
   - None of the projects will be selected as software will be downloaded using the debugger.
3. Press the Generate Netlist icon
   - Generates the synthesis, hdl, and implementation directories.
4. Press the Generate Bitstream icon
   - Runs translate, map, par, and bitgen
5. Press the Generate Libraries icon
   - Generates the software libraries for your system.
6. Press the Compile Program Sources icon
   - Compiles the software project and saves the executable (executable.elf) in the TestApp directory
7. Press the Update Bitstream icon
   - Runs data2mem to update the system.bit with the execuatable.elf file. A new bit file containing the BRAM initialization strings is created called download.bit

(Refer to the EDK documentation for further details)

Download using Parallel Cable IV / Debug

The following steps explain how to download the program.

1. Connect Parallel-IV cable to Xilinx Spartan-3 Starter kit board
2. Connect a serial cable to UART on the Xilinx Spartan-3 Starter Kit board and the COM port on your computer.
3. Start a hyper-terminal with the following settings:
   - Baud Rate – 9600
   - Data – 8 bits
   - Parity – none
   - Stop – 1 bit
   - Flow control - none
4. Connect the VGA port to a monitor and the keyboard port to a PS/2 if you would like to use these devices.
5. In XPS, press the Download icon within XPS, this will download the hardware system onto the FPGA.

   NOTE: The JTAG chain for the Xilinx Spartan-3 Starter kit Board has been defined by the download.cmd file included in the <edk_project>\etc directory.

6. In XPS, Run **Tools > XMD**. This will load the software application code via the MicroBlaze Debug Module (MDM) through XMD. In the XMD console, you should see ".....Software Running....."

(Refer to the EDK documentation for further details)

Software

TestApp software project – This is an interactive program that tests the PS/2 keyboard, VGA port, RS232 port, LEDs, buttons, switches and 7-segment display. The code is well commented to describe what the software is doing allowing the user to adapt it to their own application.