2017 MASTERs Conference

21037 AD2

The implementation of the OpenScope, a 1 MHz PIC32 MZ based IoT WiFi Oscilloscope, and more

MICROCHIP

MICROCHIP MASTERs 2017

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Class Objectives

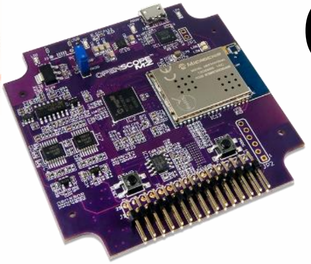
- **How to use the OpenScope and its limitations.**
- **Hardware design overview of each instrument.**
- **Interleave ADCs to obtain a higher sampling rate.**
- **Use software calibration to reduce component cost and improve accuracy.**

Class Objectives Continued

- Use DMA to off-load the CPU and improve performance.
- Trigger various Instruments
- Implement R2R Ladder DAC to create waveform generator.
- Communicate to OpenScope via WiFi HTTP or USB COM JSON interface.
- How to build OpenScope source.

Open Scope Agenda

- **Open Scope Waveforms Live Demonstration**
- **Architecture**
- **Resource Allocation**
- **DC Outputs**
- **Precision Analysis**
- **Analog Inputs**
- **DMA Parallel Processing**
- **ADC Interleaving**
- **Logic Analyzer (LA)**
- **Scope Triggering**
- **Analog Waveform Generator (AWG)**
- **Priority and Stalling Consequences**
- **USB/Serial, UART Interface**
- **Open Scope Text Based Protocol**
- **Building the Sources**

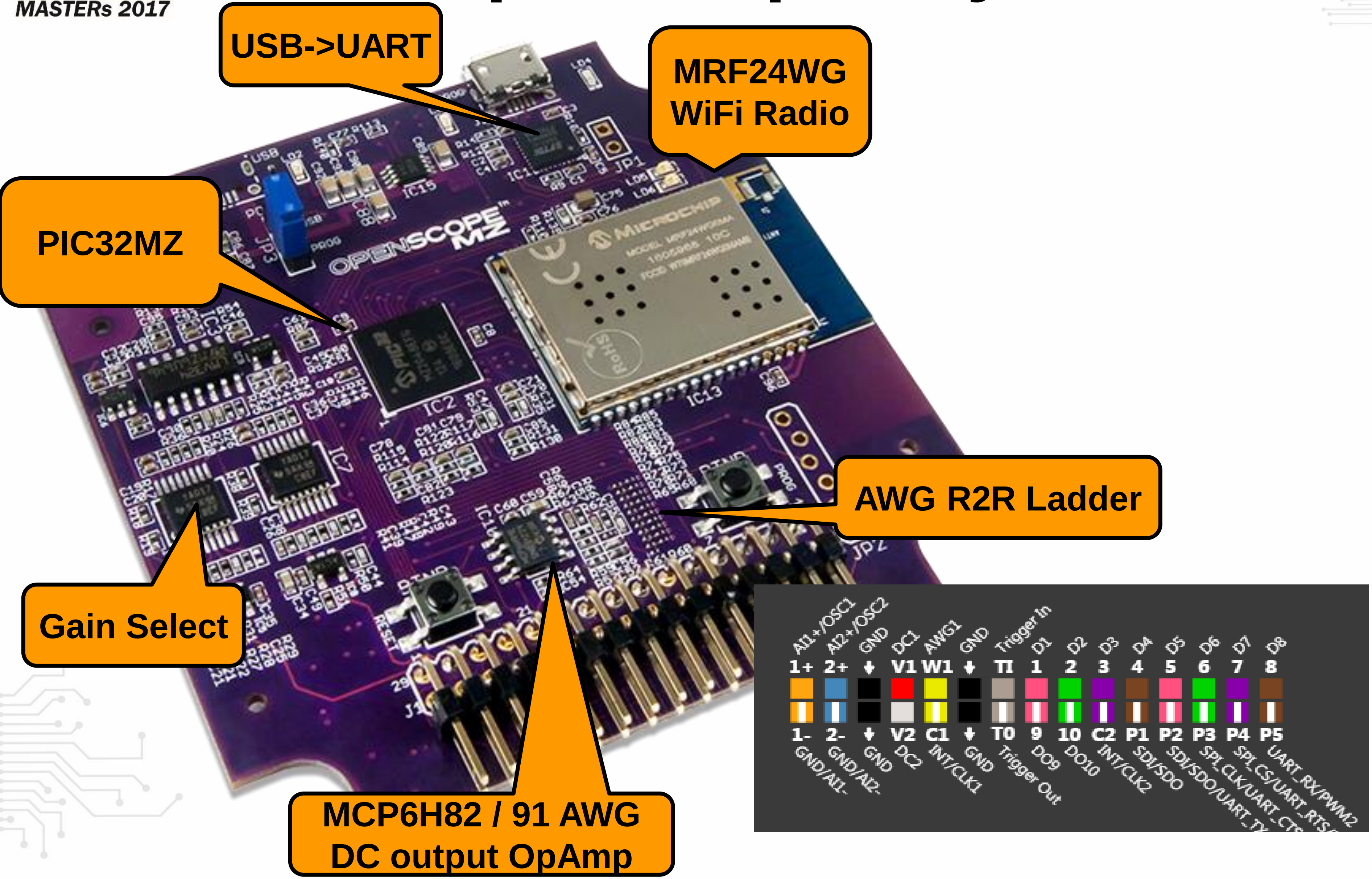


OpenScope Features

$89.00

- 2 Oscilloscope channels with 12 bits at 2MHz bandwidth and 6.25 MS/s max sampling rate
- 1 function generator - 1MHz bandwidth @ 10 MS/s update rate
- 10 Logic Analyzer inputs or user programmable pins @ 10 MS/s update rate
- 2 User programmable power supplies supplying up to 50mA and ± 4V power
- WiFi or USB interface
- Browser-based WaveForms Live multi-instrument software

OpenScope Layout



USB->UART

MRF24WG WiFi Radio

PIC32MZ

AWG R2R Ladder

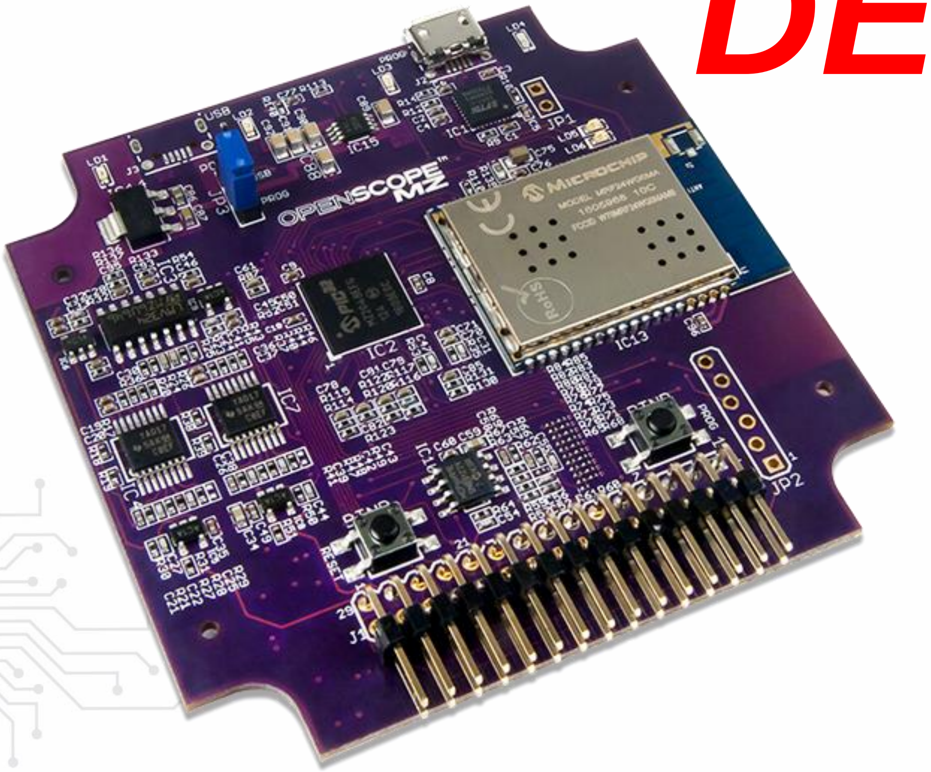
Gain Select

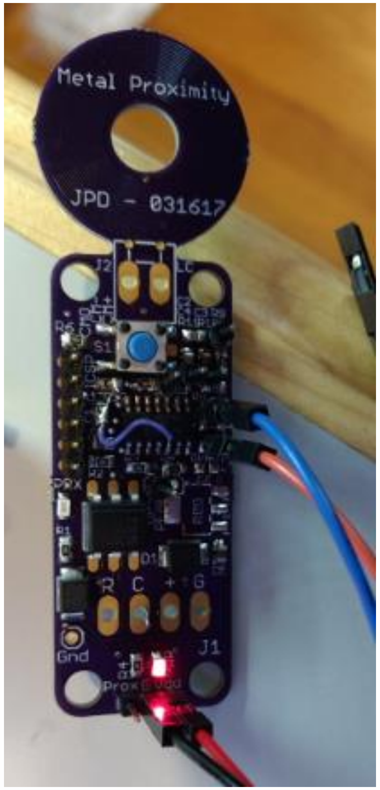
MCP6H82 / 91 AWG DC output OpAmp

Top function	Top pin	Bottom pin	Bottom function
AI1+/OSC1	1+	1-	GND/AI1-
AI2+/OSC2	2+	2-	GND/AI2-
GND	⏚	⏚	GND
DC1	V1	V2	DC2
AWG1	W1	C1	INT/CLK1
GND	⏚	⏚	GND
Trigger In	TI	T0	Trigger Out
D1	1	9	DO9
D2	2	10	DO10
D3	3	C2	INT/CLK2
D4	4	P1	SDI/SDO
D5	5	P2	SDI/SDO
D6	6	P3	SDI/SDO/UART_TX
D7	7	P4	SPI_CLK/UART_CTS
D8	8	P5	SPI_CS/UART_RTS
			UART_RX/PWM2

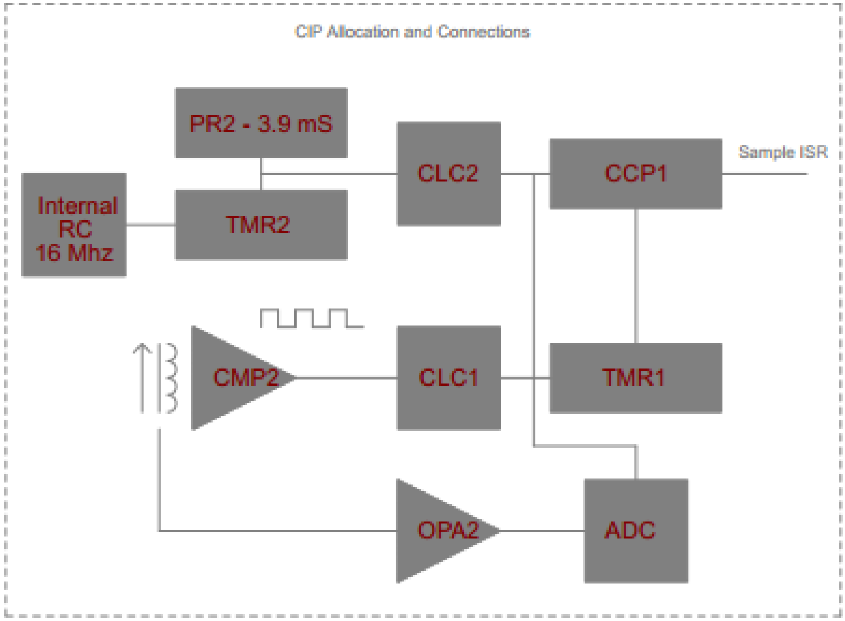
OpenScope™

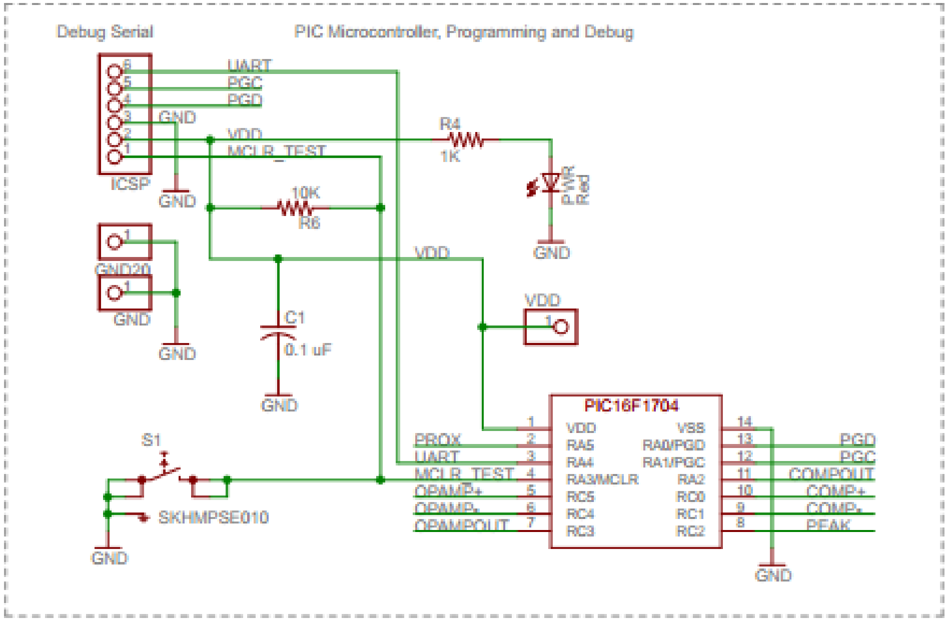
LC TANK DEMO

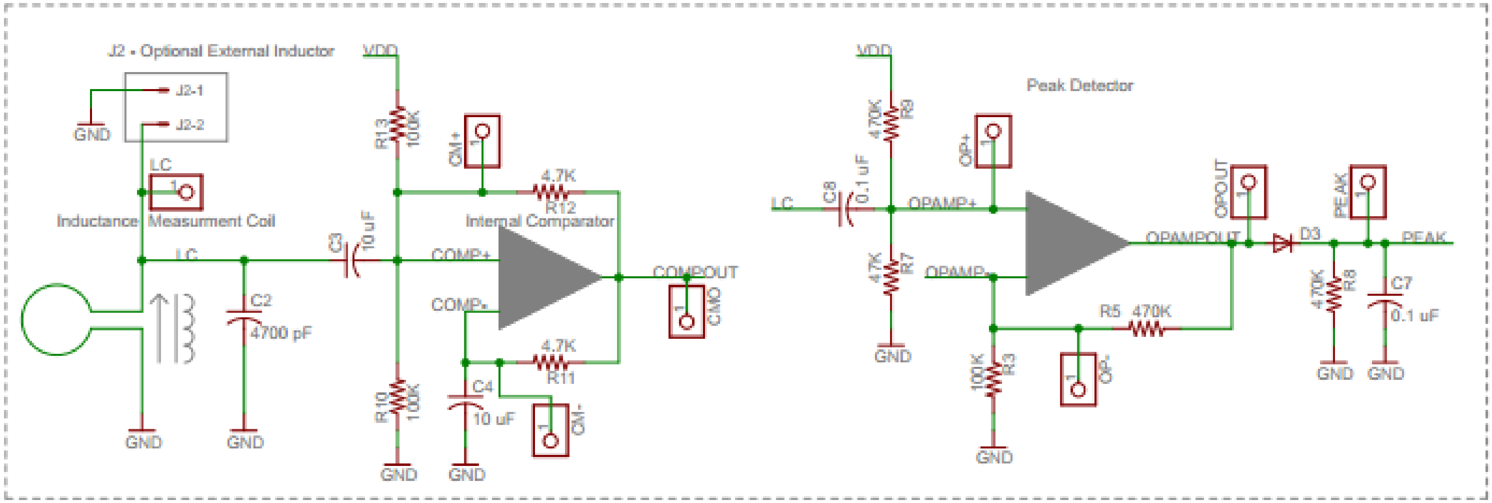




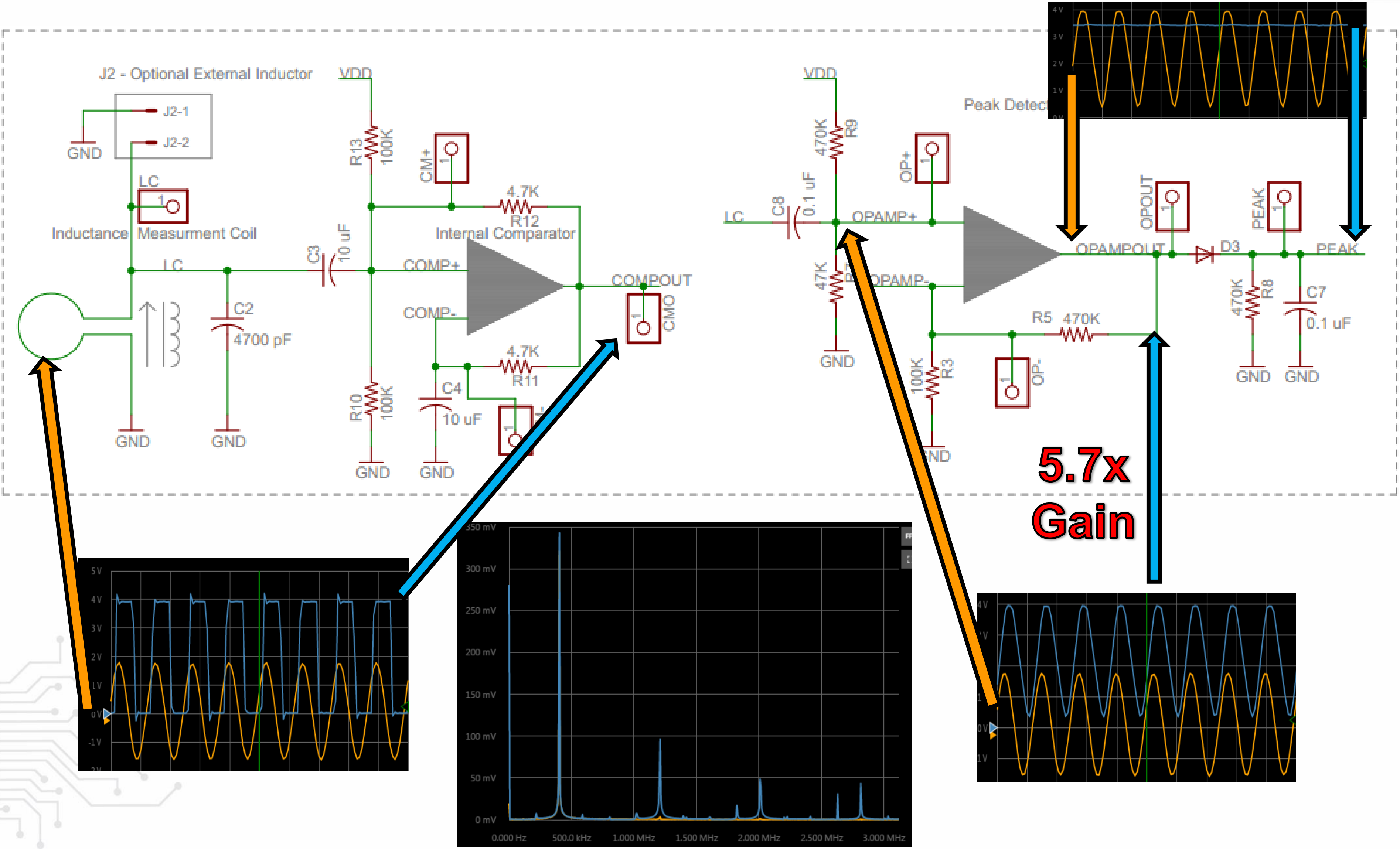
PIC® MCU based LC Tank







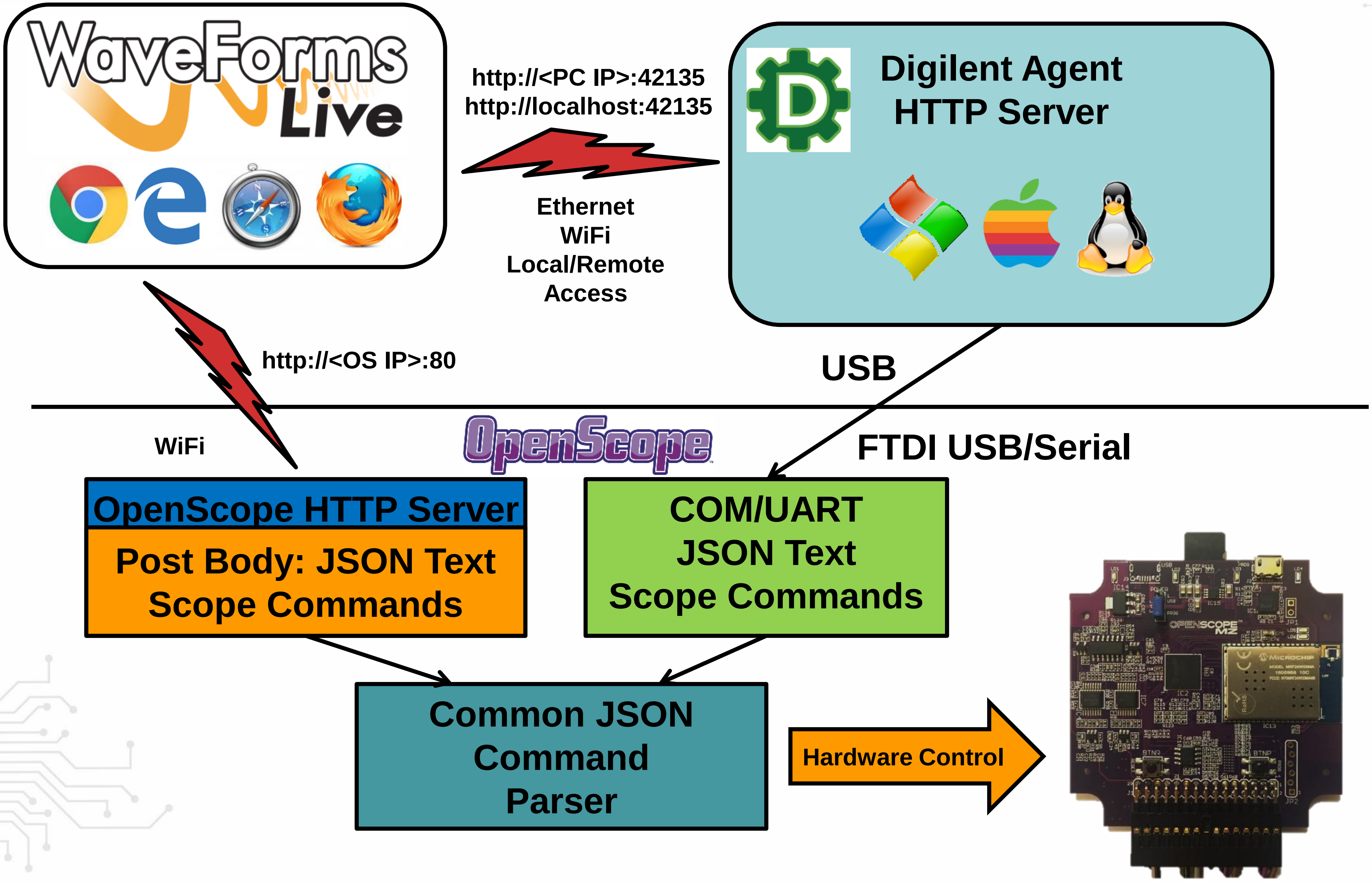
LC Tank Demo Board



5.7x Gain

Architecture

User Interface Communications



WaveForms Live

http://<PC IP>:42135
http://localhost:42135

Ethernet
WiFi
Local/Remote
Access

Digilent Agent
HTTP Server

USB

http://<OS IP>:80

WiFi

OpenScope

FTDI USB/Serial

OpenScope HTTP Server

Post Body: JSON Text
Scope Commands

COM/UART
JSON Text
Scope Commands

Common JSON
Command
Parser

Hardware Control

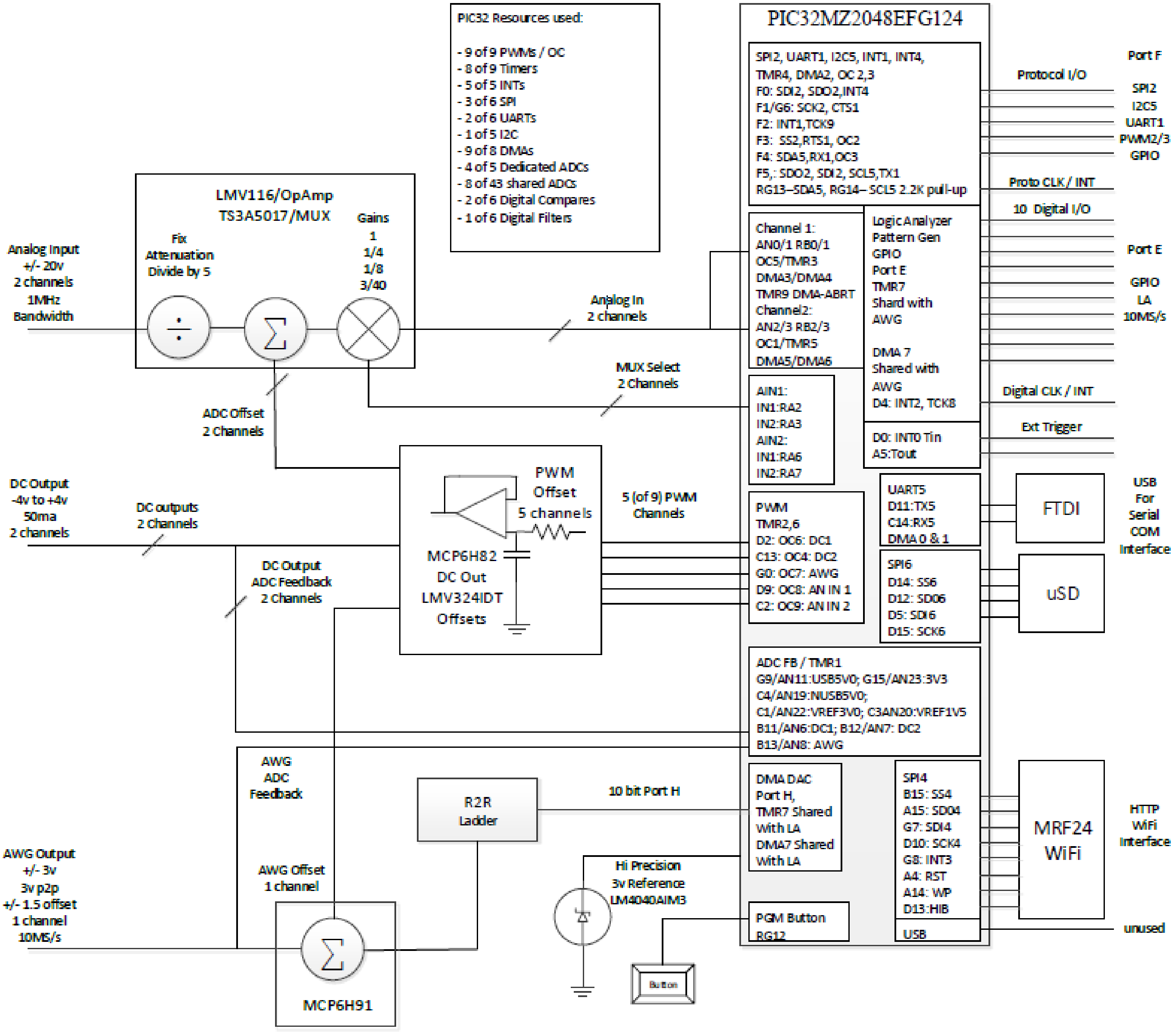
Major Components

- **Hardware**
  - PIC32MZ, MRF24 WiFi Radio, USB/Serial, uSD, Analog Circuits, Flywires
- **Firmware**
  - Instrument operation, Calibration, Communication, WiFi, Storage
- **Waveformslive (WFL)**
  - Brower Based UI (local and remote internet)
  - Native iOS and Android Apps
- **Digilent Agent (DA)**
  - USB/Serial Communication, Setup, Local/Remote Internet Connectivity

Hardware Block Diagram

PIC32 Resources used:

- 9 of 9 PWMs / OC
- 8 of 9 Timers
- 5 of 5 INTs
- 3 of 6 SPI
- 2 of 6 UARTs
- 1 of 5 I2C
- 9 of 8 DMAs
- 4 of 5 Dedicated ADCs
- 8 of 43 shared ADCs
- 2 of 6 Digital Compares
- 1 of 6 Digital Filters



PIC32MZ2048EFG124

SPI2, UART1, I2C5, INT1, INT4,
TMR4, DMA2, OC 2,3
F0: SDI2, SDO2,INT4
F1/G6: SCK2, CTS1
F2: INT1,TCK9
F3: SS2,RTS1, OC2
F4: SDA5,RX1,OC3
F5,: SDO2, SDI2, SCL5,TX1
RG13–SDA5, RG14– SCL5 2.2K pull-up

Channel 1:
AN0/1 RB0/1
OC5/TMR3
DMA3/DMA4
TMR9 DMA-ABRT
Channel2:
AN2/3 RB2/3
OC1/TMR5
DMA5/DMA6

Logic Analyzer
Pattern Gen
GPIO
Port E
TMR7
Shard with
AWG

DMA 7
Shared with
AWG
D4: INT2, TCK8

D0: INT0 Tin
A5:Tout

AIN1:
IN1:RA2
IN2:RA3
AIN2:
IN1:RA6
IN2:RA7

PWM
TMR2,6
D2: OC6: DC1
C13: OC4: DC2
G0: OC7: AWG
D9: OC8: AN IN 1
C2: OC9: AN IN 2

UART5
D11:TX5
C14:RX5
DMA 0 & 1

SPI6
D14: SS6
D12: SDO6
D5: SDI6
D15: SCK6

ADC FB / TMR1
G9/AN11:USB5V0; G15/AN23:3V3
C4/AN19:NUSB5V0;
C1/AN22:VREF3V0; C3AN20:VREF1V5
B11/AN6:DC1; B12/AN7: DC2
B13/AN8: AWG

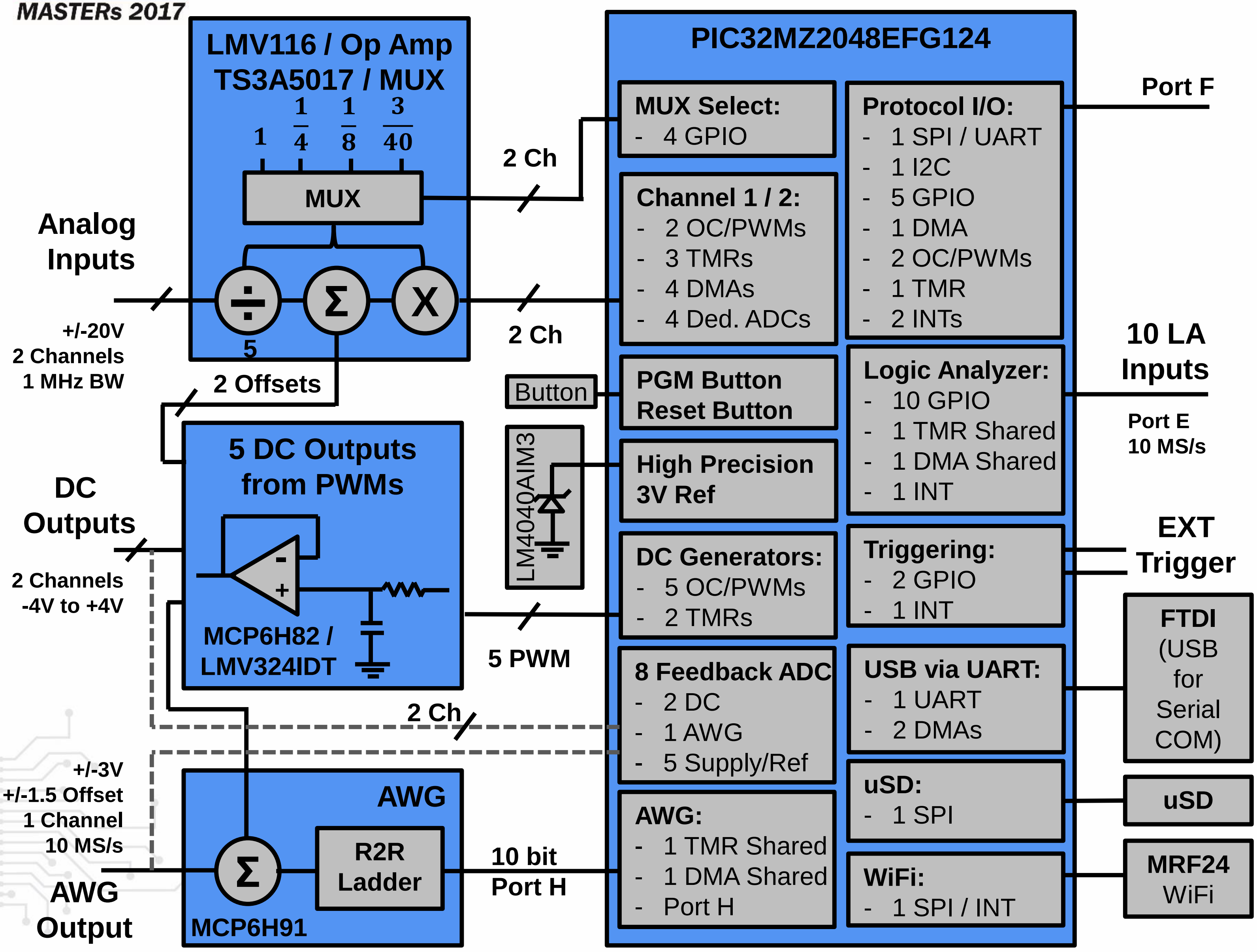
DMA DAC
Port H,
TMR7 Shared
With LA
DMA7 Shared
With LA

SPI4
B15: SS4
A15: SDO4
G7: SDI4
D10: SCK4
G8: INT3
A4: RST
A14: WP
D13:HIB

PGM Button
RG12

USB

Hardware Block Diagram

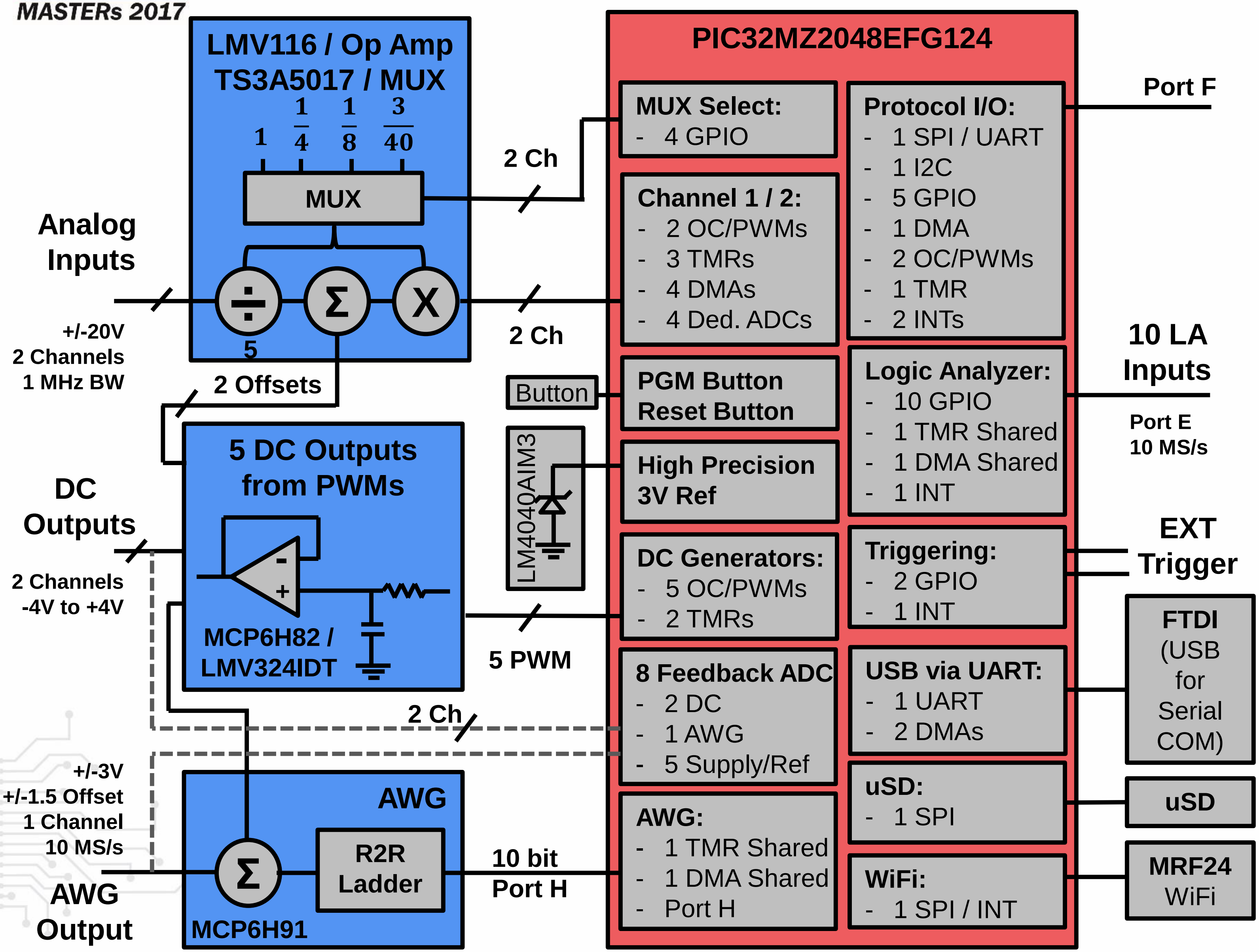


PIC32 Resource Usage Summary Table

PWM / OC	9 of 9
Timers	7 of 9
INTs	5 of 5
SPI	3 of 6
UART	2 of 6
I2C	1 of 5
DMAs	9 of 8
Dedicated ADCs	4 of 5
Shared ADCs	8 of 43
Digital Compare	2 of 6
Digital Filters	1 of 6

Resource Allocation

Resource Allocation



LMV116 / Op Amp
TS3A5017 / MUX

$1 \quad \frac{1}{4} \quad \frac{1}{8} \quad \frac{3}{40}$

MUX

÷ Σ X

5

Analog Inputs

+/-20V
2 Channels
1 MHz BW

2 Ch

2 Ch

2 Offsets

5 DC Outputs from PWMs

MCP6H82 /
LMV324IDT

DC Outputs

2 Channels
-4V to +4V

Button

LM4040AIM3

5 PWM

2 Ch

+/-3V
+/-1.5 Offset
1 Channel
10 MS/s

AWG

R2R Ladder

Σ

MCP6H91

AWG Output

10 bit
Port H

PIC32MZ2048EFG124

MUX Select:
- 4 GPIO

Channel 1 / 2:
- 2 OC/PWMs
- 3 TMRs
- 4 DMAs
- 4 Ded. ADCs

PGM Button
Reset Button

High Precision 3V Ref

DC Generators:
- 5 OC/PWMs
- 2 TMRs

8 Feedback ADC
- 2 DC
- 1 AWG
- 5 Supply/Ref

AWG:
- 1 TMR Shared
- 1 DMA Shared
- Port H

Protocol I/O:
- 1 SPI / UART
- 1 I2C
- 5 GPIO
- 1 DMA
- 2 OC/PWMs
- 1 TMR
- 2 INTs

Logic Analyzer:
- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

Triggering:
- 2 GPIO
- 1 INT

USB via UART:
- 1 UART
- 2 DMAs

uSD:
- 1 SPI

WiFi:
- 1 SPI / INT

Port F

10 LA Inputs

Port E
10 MS/s

EXT Trigger

FTDI
(USB for Serial COM)

uSD

MRF24
WiFi

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PIC32 Peripheral Resources

- PWM are used to drive offset voltages for the DCout, Analog In, and AWG. Also used for interleave ADC triggers.
- Timers are used to trigger ADCs, DMA transfers, PWMs, and Trigger delays
- DMA used to transfer ADC/AWG/LA and Serial Data without CPU utilization.

Resources

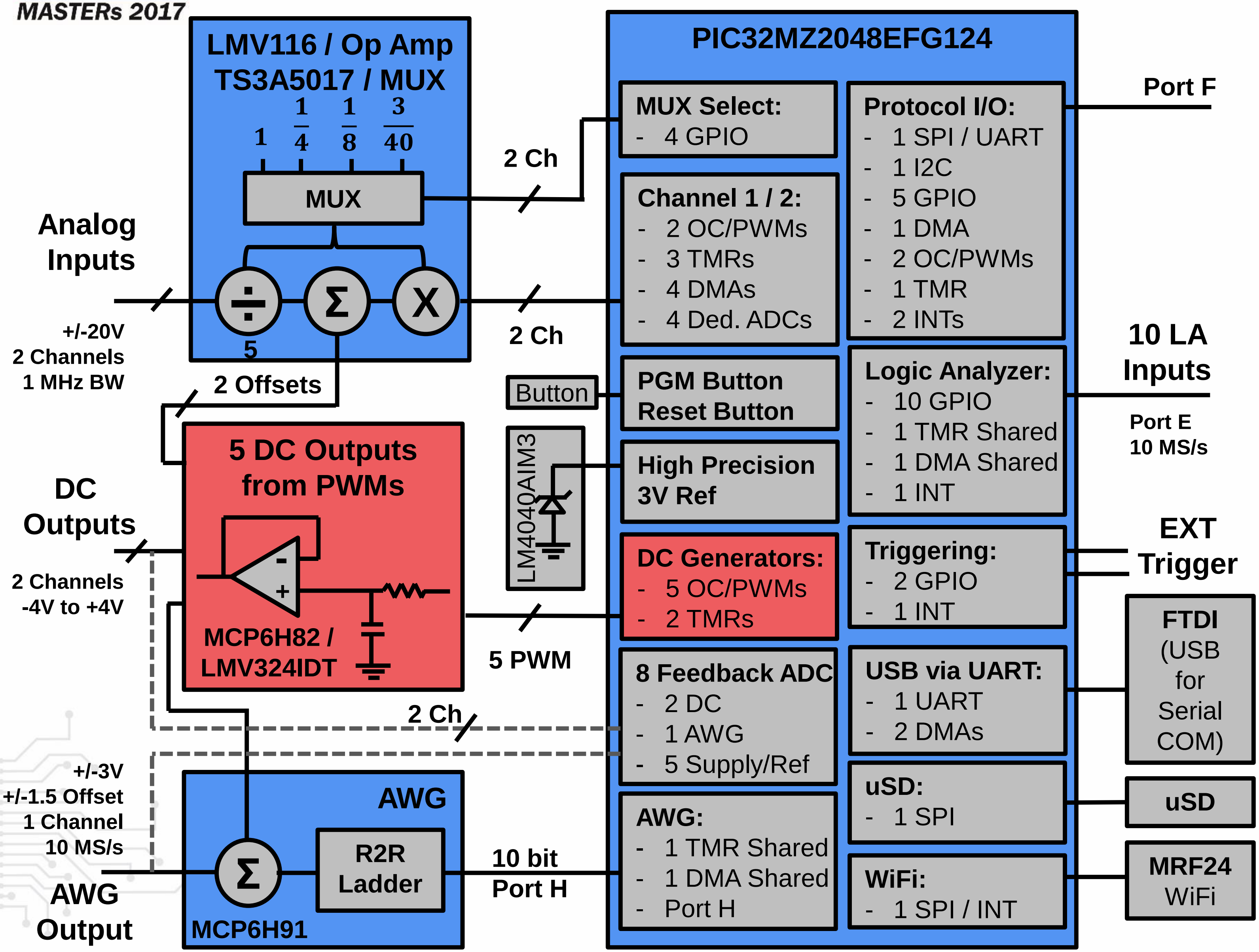
- **ADCs**
  - 4 Dedicated (Scope 1, 2), 8 Shared Calibration Feedback
- **ADC Digital Compares**
  - 2 ADC (Scope 1,2 High/Low Triggers), 4 Spares
- **PWMs**
  - 3 Offset, 2 ADC Interleave, 2 DC, 2 User
- **Timers**
  - 2 ADC, 1 DC/OC, 1 Offset/OC, 1 AWG/LA, 1 Trigger, 1 protocol, 2 spare

Resource Continued

- **DMAs**
  - 2 UART, 4 ADC (Scope 1,2), 1 AWG / LA, 1 Protocol
- **UARTs**
  - 1 COM (Digilent Agent), 1 Protocol, 4 spares
- **SPI**
  - 1 MRF24WG WiFi Radio, 1 µSD, 1 protocol, 1 unavailable, 2 spares.
- **External Interrupts**
  - 1 MRF24WG WiFi Radio, 3 External Triggers, 1 Protocol

DC Outputs

DC Outputs



LMV116 / Op Amp
TS3A5017 / MUX

1   $\frac{1}{4}$ $\frac{1}{8}$ $\frac{3}{40}$

MUX

÷   Σ   X

5

Analog Inputs

+/-20V
2 Channels
1 MHz BW

2 Offsets

2 Ch

2 Ch

5 DC Outputs from PWMs

MCP6H82 /
LMV324IDT

DC Outputs

2 Channels
-4V to +4V

Button

LM4040AIM3

5 PWM

2 Ch

AWG

R2R Ladder

Σ

MCP6H91

+/-3V
+/-1.5 Offset
1 Channel
10 MS/s

AWG Output

10 bit
Port H

PIC32MZ2048EFG124

MUX Select:
- 4 GPIO

Channel 1 / 2:
- 2 OC/PWMs
- 3 TMRs
- 4 DMAs
- 4 Ded. ADCs

PGM Button
Reset Button

High Precision
3V Ref

DC Generators:
- 5 OC/PWMs
- 2 TMRs

8 Feedback ADC
- 2 DC
- 1 AWG
- 5 Supply/Ref

AWG:
- 1 TMR Shared
- 1 DMA Shared
- Port H

Protocol I/O:
- 1 SPI / UART
- 1 I2C
- 5 GPIO
- 1 DMA
- 2 OC/PWMs
- 1 TMR
- 2 INTs

Logic Analyzer:
- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

Triggering:
- 2 GPIO
- 1 INT

USB via UART:
- 1 UART
- 2 DMAs

uSD:
- 1 SPI

WiFi:
- 1 SPI / INT

Port F

10 LA Inputs

Port E
10 MS/s

EXT Trigger

FTDI
(USB for Serial COM)

uSD

MRF24
WiFi

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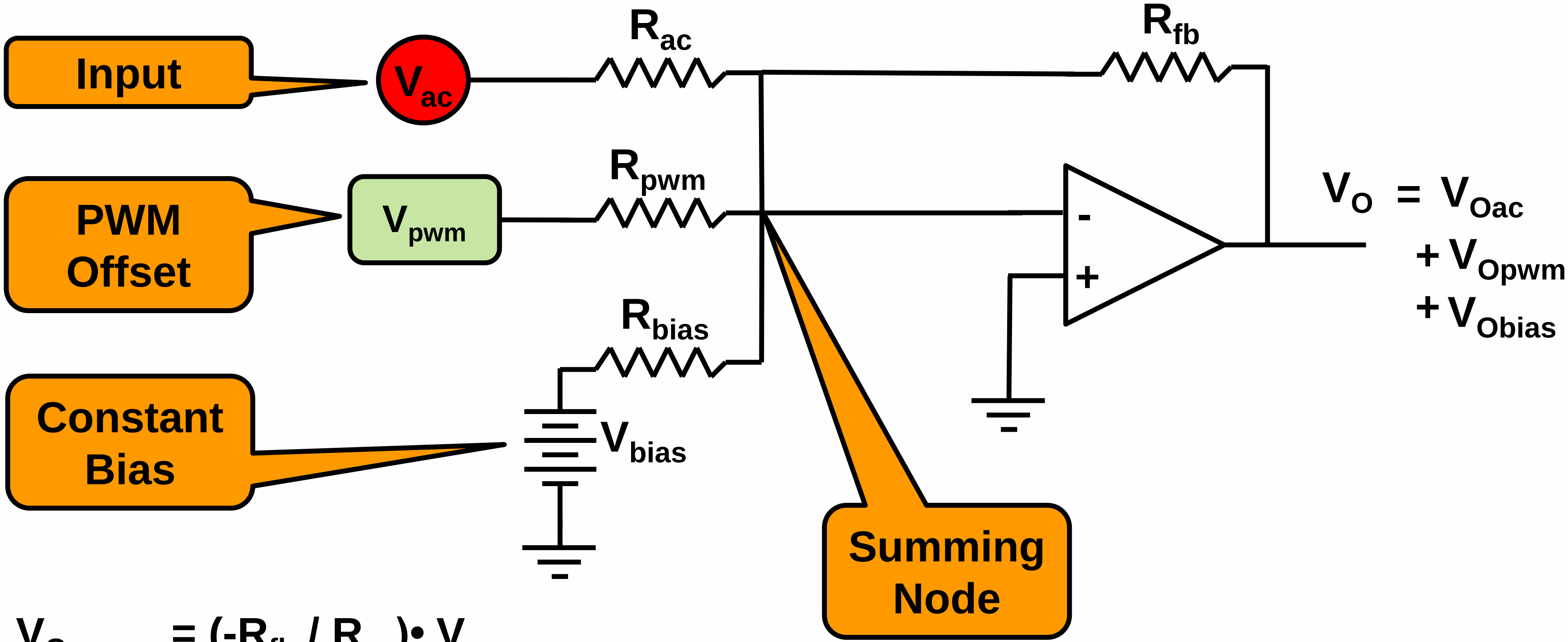
OpAmps 101 a Refresher


Input

PWM Offset

Constant Bias

Summing Node

$V_O = V_{Oac} + V_{Opwm} + V_{Obias}$

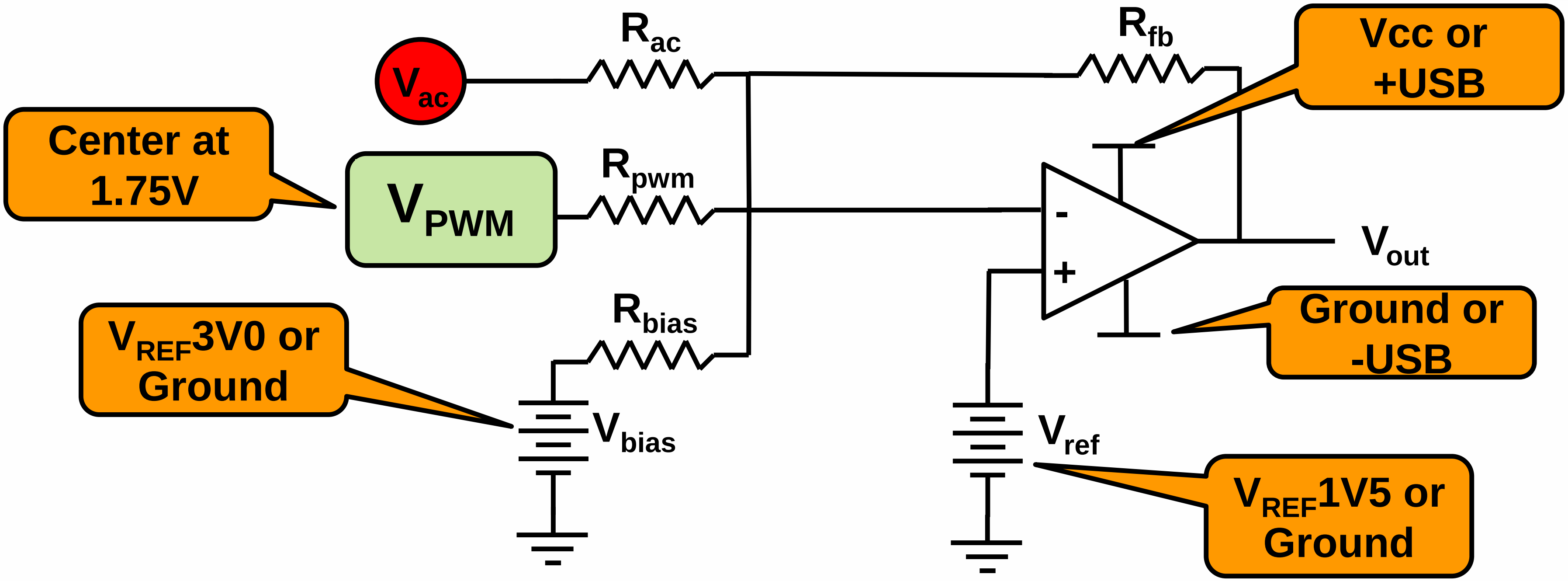
$V_{Oac} = (-R_{fb} / R_{ac}) \bullet V_{ac}$

$V_{Opwm} = (-R_{fb} / R_{pwm}) \bullet V_{pwm}$

$V_{Obias} = (-R_{fb} / R_{bias}) \bullet V_{bias}$

$V_O = (-R_{fb} / R_{ac}) \bullet V_{ac} + (-R_{fb} / R_{pwm}) \bullet V_{pwm} + (-R_{fb} / R_{bias}) \bullet V_{bias}$

OpAmp Gain and Offset Math



Vcc or +USB

Center at 1.75V

Ground or -USB

V_{REF}3V0 or Ground

V_{REF}1V5 or Ground

$V_O = (-R_{fb} / R_{ac})\bullet(V_{ac}-V_{ref})+(-R_{fb} / R_{pwm})\bullet(V_{pwm}-V_{ref})+(-R_{fb} / R_{bias})\bullet(V_{bias}-V_{ref})+V_{ref}$

Let $A = (-R_{fb} / R_{ac})$; $B = (-R_{fb} / R_{pwm})$; $C' = (-R_{fb} / R_{bias})$

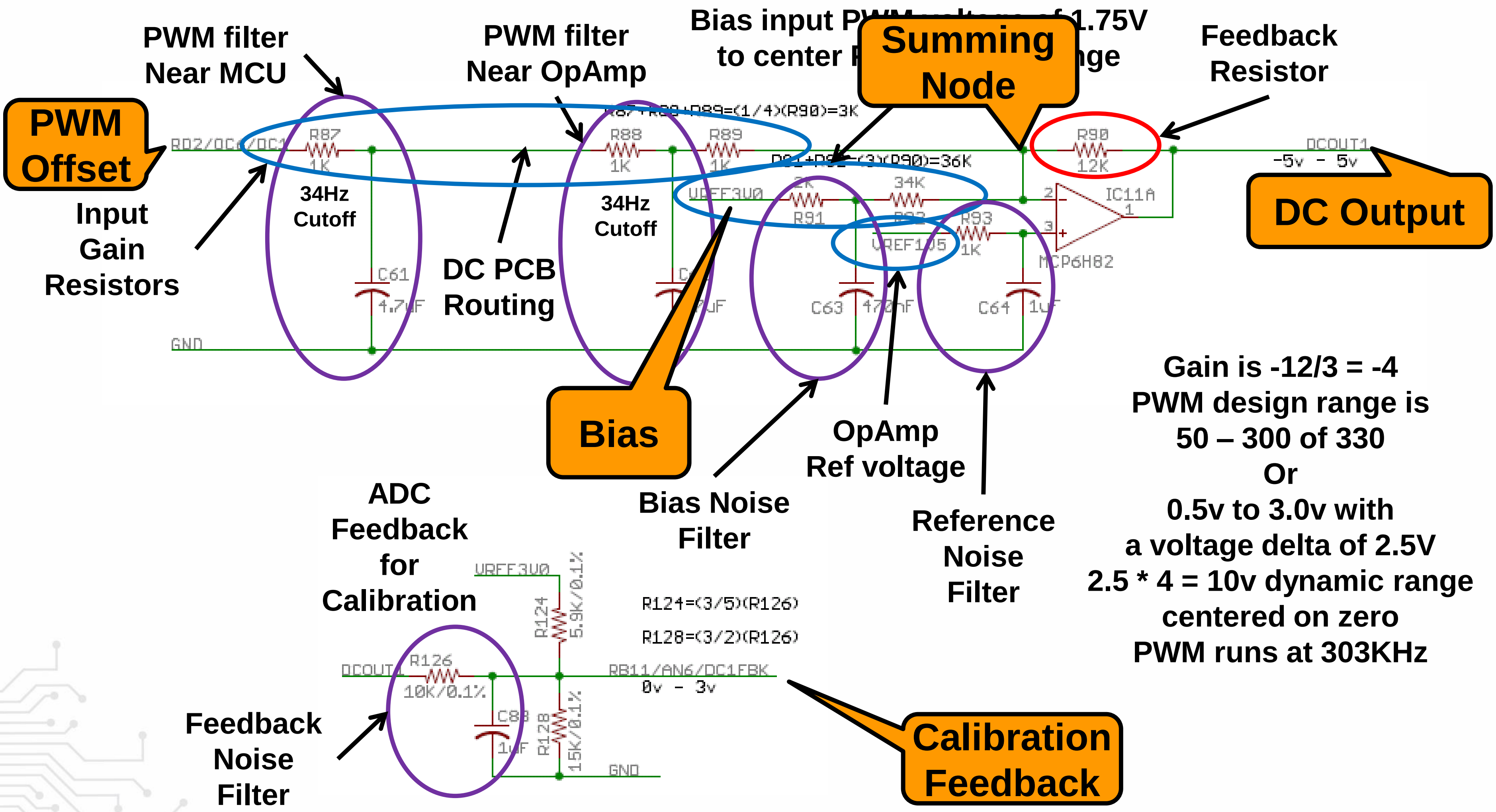
$V_O = A\bullet V_{ac}+B\bullet V_{pwm}+C'\bullet V_{bias}-(A+B+C'-1)\bullet V_{ref}$

$V_O = (-R_{fb} / R_{ac})\bullet V_{ac} +(-R_{fb} / R_{pwm})\bullet V_{pwm} +(-R_{fb} / R_{bias})\bullet V_{bias}$
$+ (R_{fb} / R_{ac})\bullet V_{ref} +(R_{fb} / R_{pwm})\bullet V_{ref} +(R_{fb} / R_{bias})\bullet V_{ref} +V_{ref}$

Let $C = C'\bullet V_{bias}-(A+B+C'-1)\bullet V_{ref} = (-R_{fb} / R_{bias})\bullet(V_{bias}- V_{ref}) - (A+B-1)\bullet V_{ref}$

$V_O = A\bullet V_{ac}+B\bullet V_{pwm}+C$

PWM, DC Outputs and Offsets



PWM Offset

PWM filter Near MCU

Input Gain Resistors

34Hz Cutoff

DC PCB Routing

PWM filter Near OpAmp

34Hz Cutoff

Bias input P 1.75V to center P nge

Summing Node

Feedback Resistor

DC Output

Bias

Bias Noise Filter

OpAmp Ref voltage

Reference Noise Filter

ADC Feedback for Calibration

Feedback Noise Filter

Calibration Feedback

Gain is -12/3 = -4
PWM design range is
50 – 300 of 330
Or
0.5v to 3.0v with
a voltage delta of 2.5V
2.5 * 4 = 10v dynamic range
centered on zero
PWM runs at 303KHz

PWM Design Limits

- PWM has 330 unique values.
- The PWM output will be from 0 to Vcc (3.3v), so each PWM value corresponds to 10mV.
- The PWM internal clock runs at 100MHz, so the frequency of the PWM is 100MHz/330 = 303KHz
- All PWM analog design ranges are from 50 to 300 to allow for headroom calibration; center around 175

PWM Usage and Considerations

- **5 PWMs provide DC outputs and offsets.**
  - 2 DC output circuits
  - 3 offset circuits
    - 2 Analog-in offsets
    - 1 AWG offset
- **There are at least 2 filters, one close to the MCU so DC is routed about the board, one near its final usage to filter out crosstalk noise**
- **There is a setup time of approx 30 - 100ms; The software uses 500ms, about 500 time constants**

Most Circuits are described as Polynomials

- **$\mu V = A \bullet D_{adc} + B \bullet D_{pwm} + C$**
- **DC Feedback**
  - $\mu VDC_{out} = (595000000 \bullet D_{adc} - 409600000000 \bullet V_{Ref3.0}) / 241664$
- **DC Output**
  - $\mu VDC_{out} = -40{,}000 \bullet D_{pwm} + 7{,}000{,}000$
- **Analog Input**
  - $\mu V_{in} = (13{,}183{,}593.75 / R_{1Sx}) \bullet D_{adc} + (154{,}338{,}032 / R_{2Sx}) \bullet D_{pwm} - (27{,}000{,}000{,}000 / R_{2Sx})$
- **Waveform Generator (AWG)**
  - $\mu Vawg \approx -2987 \bullet D_{dac} - 11995 \bullet D_{pwm} + 3630161$
  - $\mu V_{PWM}Offset = -11995 \bullet D_{pwm} + 2099125$
    - Table Lookup – Best Fit for D_{dac}

DC Feedback: $V = A \bullet D_{adc} - B$

$$V_{adc} = (3/4096) \bullet D_{adc}$$
$$= (R_{124})(R_{128})/((R_{124})(R_{126})+(R_{126})(R_{128})+(R_{124})(R_{128}))) \bullet DC_{out}$$
$$+ V_{Ref3.0} \bullet (R_{126})(R_{128})/((R_{124})(R_{126})+(R_{126})(R_{128})+(R_{124})(R_{128})))$$

$$D_{adc} = (4096/3)V_{adc} = (241664/595) \bullet DC_{out} + (81920/119) \bullet V_{Ref3.0}$$

OR

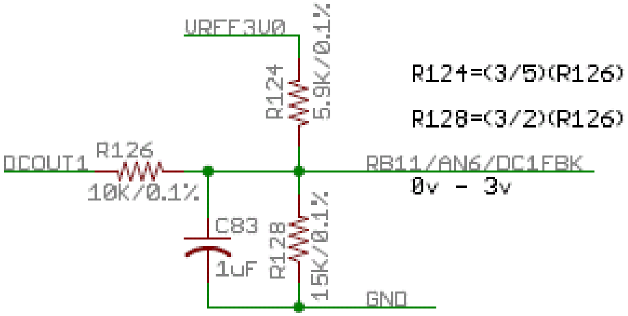
$$\mu VDC_{out} = (595000000 \bullet D_{adc} - 409600000000 \bullet V_{Ref3.0}) / 241664$$

For:

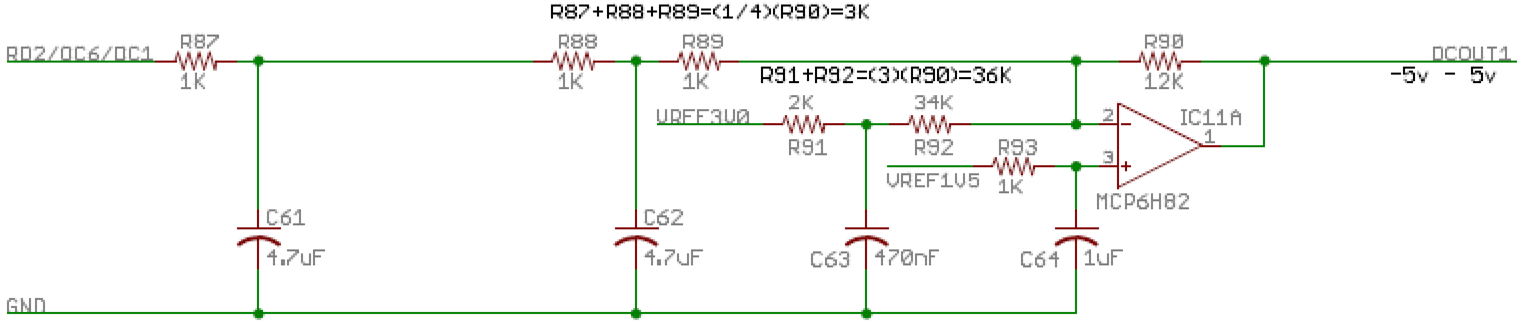
$DC_{out} = -5$; $D_{adc} = 34$; $V_{adc} = 0.02521V$;

$DC_{out} = 0$; $D_{adc} = 2065$; $V_{adc} = 1.5126V$;

$DC_{out} = 5$; $D_{adc} = 4096$; $V_{adc} = 3.0V$;



DC_{out}: $V = -A \bullet D_{pwm} + B$



$$DC_{out} = -R_{90} / (R_{87}+R_{88}+R_{87}) \bullet V_{CC3.3} / 330 \bullet D_{pwm}$$
$$+ V_{Ref1.5} \bullet R_{90} / (R_{87}+R_{88}+R_{87}) + (V_{Ref1.5} - V_{Ref3.0}) \bullet R_{90} / (R_{91}+R_{92}) + V_{Ref1.5}$$

$$DC_{out} = -0.04 \bullet D_{pwm} + 7$$

OR

$$qVDC_{out} = -40000 \bullet D_{pwm} + 7000000$$

$A = 40000$; $B = 7000000$

For:

$D_{pwm} = 50;$	$DC_{out} = 5.0V$
$D_{pwm} = 175;$	$DC_{out} = 0.0V$
$D_{pwm} = 300;$	$DC_{out} = -5.0V$

DC_{out} Calibration

$$\mu\,\text{VDC}_{1\text{out}} = -A \cdot D_{1\text{pwm}} + B$$

$$-\,\mu\,\text{VDC}_{2\text{out}} = A \cdot D_{2\text{pwm}} - B$$

$$(\mu\text{VDC}_{1\text{out}} - \mu\text{VDC}_{2\text{out}}) = A \cdot (D_{2\text{pwm}} - D_{1\text{pwm}})$$

$$A = (\mu\text{VDC}_{1\text{out}} - \mu\text{VDC}_{2\text{out}}) / (D_{2\text{pwm}} - D_{1\text{pwm}})$$

$$B = \mu\text{VDC}_{1\text{out}} + A \cdot D_{1\text{pwm}}$$

$A \approx 40000$

$B \approx 7000000$

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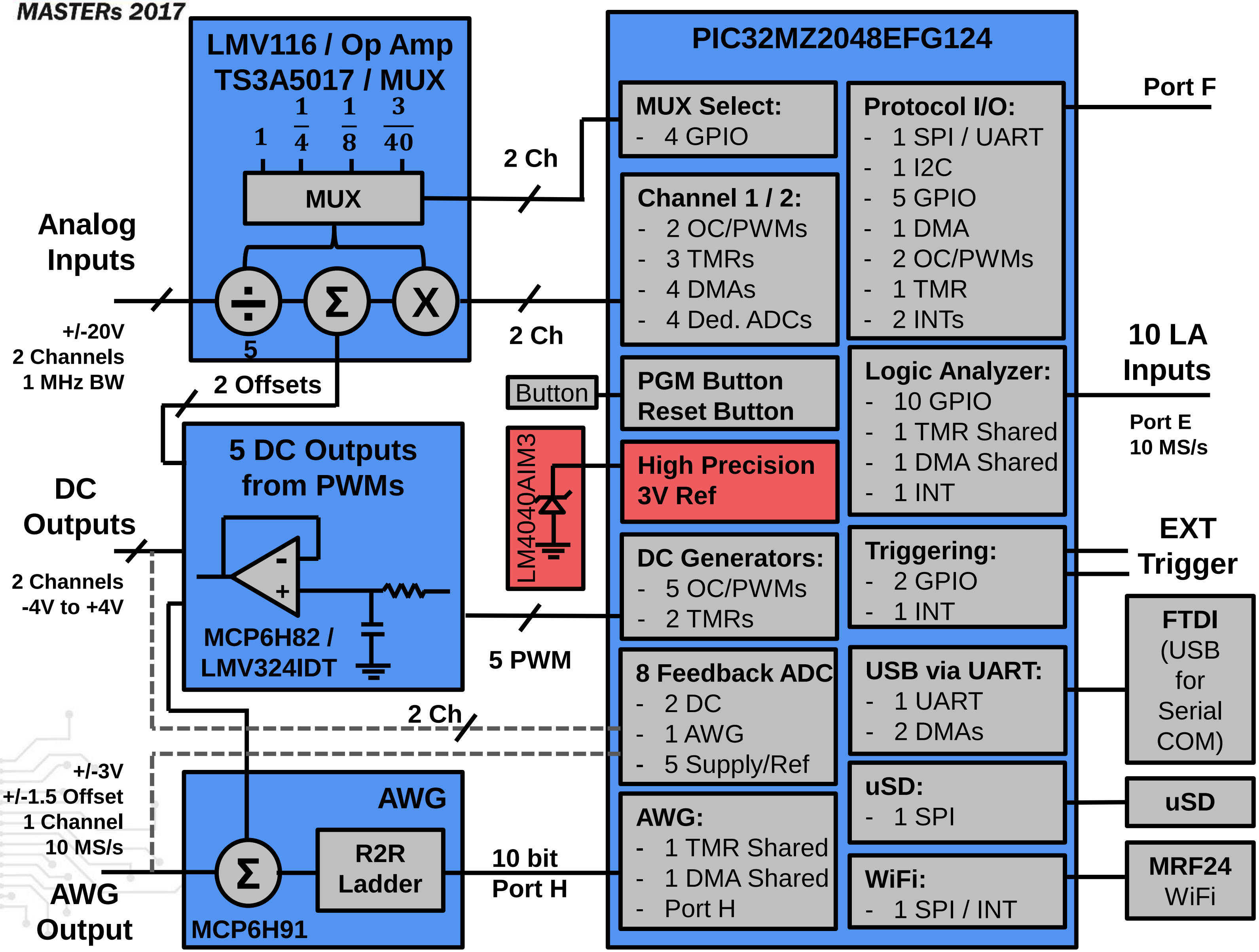
Precision Analysis

Precision Analysis



LMV116 / Op Amp TS3A5017 / MUX

PIC32MZ2048EFG124

MUX Select:
- 4 GPIO

Channel 1 / 2:
- 2 OC/PWMs
- 3 TMRs
- 4 DMAs
- 4 Ded. ADCs

PGM Button Reset Button

High Precision 3V Ref

DC Generators:
- 5 OC/PWMs
- 2 TMRs

8 Feedback ADC
- 2 DC
- 1 AWG
- 5 Supply/Ref

AWG:
- 1 TMR Shared
- 1 DMA Shared
- Port H

Protocol I/O:
- 1 SPI / UART
- 1 I2C
- 5 GPIO
- 1 DMA
- 2 OC/PWMs
- 1 TMR
- 2 INTs

Logic Analyzer:
- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

Triggering:
- 2 GPIO
- 1 INT

USB via UART:
- 1 UART
- 2 DMAs

uSD:
- 1 SPI

WiFi:
- 1 SPI / INT

5 DC Outputs from PWMs

MCP6H82 / LMV324IDT

AWG

R2R Ladder

MCP6H91

FTDI (USB for Serial COM)

uSD

MRF24 WiFi

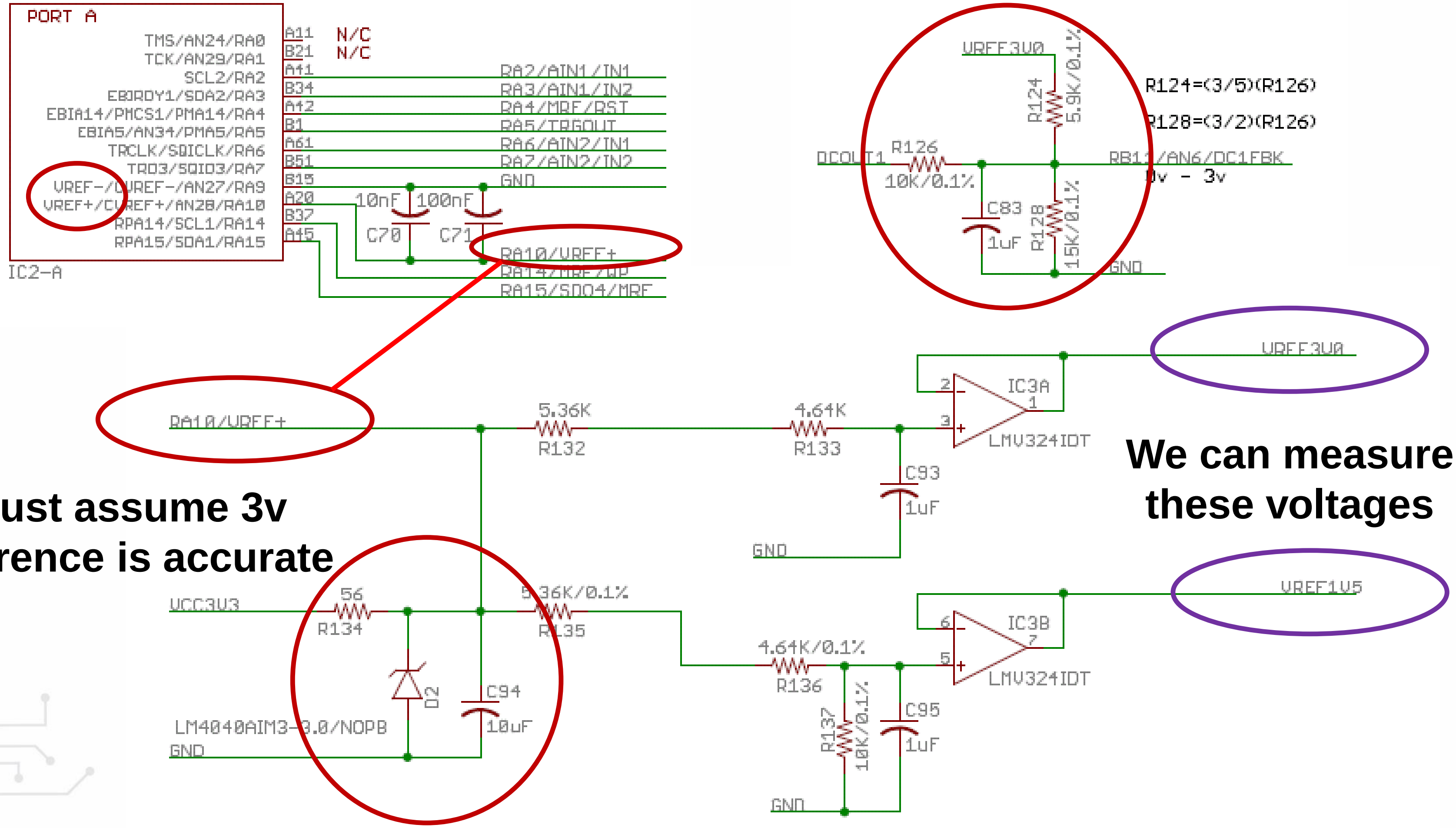
PIC32 Resource Usage Summary Table

PWM / OC	9 of 9
Timers	7 of 9
INTs	5 of 5
SPI	3 of 6
UART	2 of 6
I2C	1 of 5
DMAs	9 of 8
Dedicated ADCs	4 of 5
Shared ADCs	8 of 43
Digital Compare	2 of 6
Digital Filters	1 of 6

Where Precision and Accuracy is Needed

- **The 3 volt reference is the most critical component.**
- **The MZ ADC must be accurate, the 3 volt reference must go directly and cleanly into the MZ ADC reference.**
- **Feedback circuits used to calibrate must be accurate and assumed to be true.**

Where is Precision Needed



Must assume feedback resistors are accurate

Must assume 3v reference is accurate

We can measure these voltages

Where Accuracy is Not Needed

- **Resistor only need to be 5% and Capacitors 20%.**
  - We use 1% Resistors and 10% Capacitors
- **Voltages, including distributed voltage references are all measured and accounted for mathematically.**
- **Opamps only need to behave linearly.**

OpAmp Considerations

- **Use inexpensive OpAmps <50¢**
  - Common Mode Input Considerations
    - High input capacitance.
    - Not rail to rail, often as low as Vcc – 1.3v.
    - High input bias currents.
    - Non-linear input bias currents.
    - Non-linear as you approach input limits.
  - Output Considerations
    - Not rail to rail outputs.
    - Headroom drop-off; V_{out} = Vcc – HR(mA_{out}).

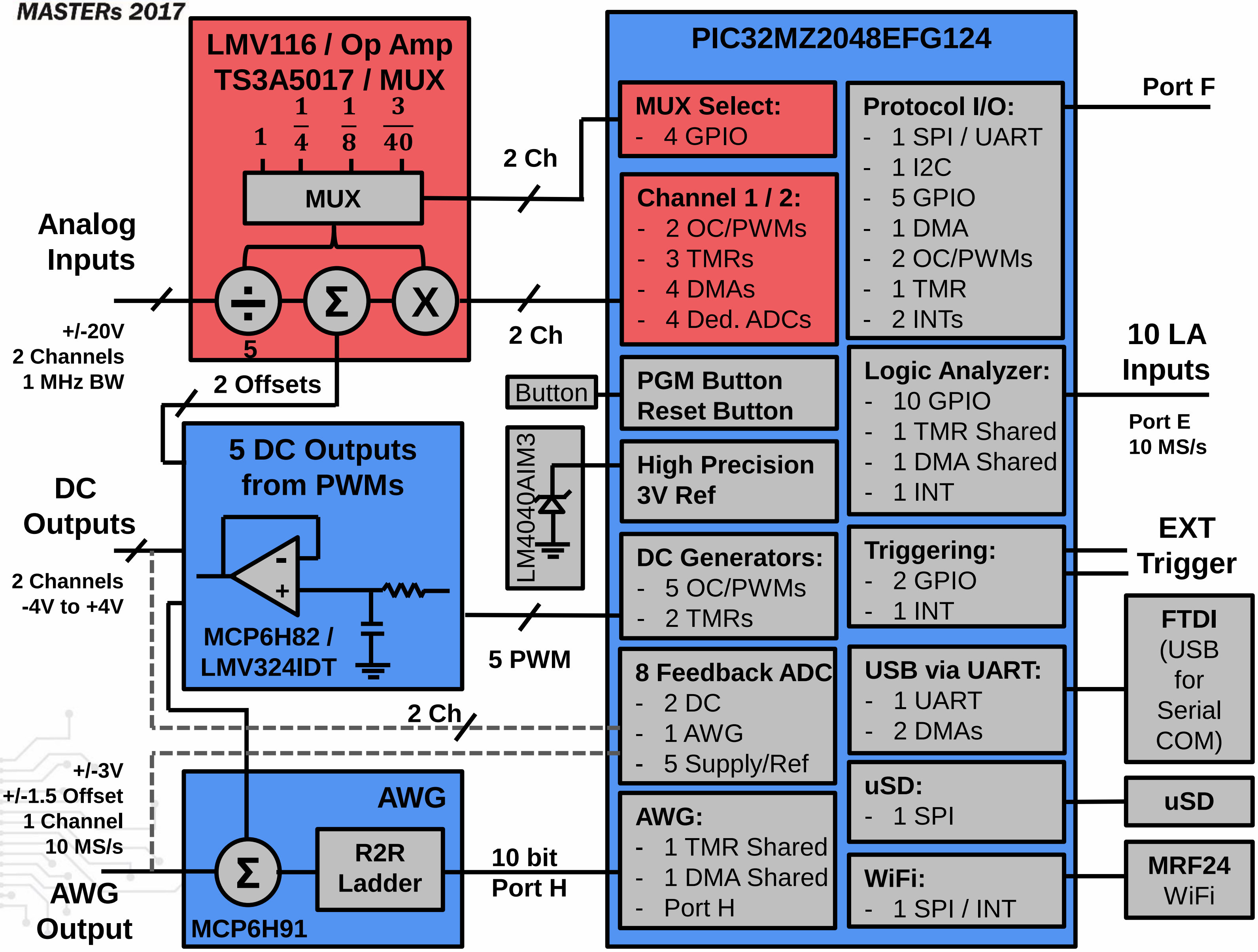
OpAmp Usage

- **Use inverting mode for AC signals**
  - Common Mode Input
    - Fixed operating input voltage, the reference voltage.
    - Constant input bias current.
    - Will not approach input limits.
    - Operate at ideal voltage, at or near Vcc /2
      - Most linear operation
- **May use non-inverting mode for DC**
  - Select an OpAmp with good Headroom/rail-to-rail characteristics, vs bandwidth: LMV324IDT.

2017 MASTERs Conference

Analog Inputs

Analog Inputs



LMV116 / Op Amp
TS3A5017 / MUX

1 $\frac{1}{4}$ $\frac{1}{8}$ $\frac{3}{40}$

MUX

÷ Σ X

5

Analog Inputs

+/-20V
2 Channels
1 MHz BW

2 Ch

2 Ch

2 Offsets

Button

LM4040AIM3

5 DC Outputs from PWMs

MCP6H82 / LMV324IDT

DC Outputs

2 Channels
-4V to +4V

5 PWM

2 Ch

AWG

R2R Ladder

Σ

MCP6H91

+/-3V
+/-1.5 Offset
1 Channel
10 MS/s

AWG Output

10 bit
Port H

PIC32MZ2048EFG124

MUX Select:
- 4 GPIO

Channel 1 / 2:
- 2 OC/PWMs
- 3 TMRs
- 4 DMAs
- 4 Ded. ADCs

PGM Button
Reset Button

High Precision 3V Ref

DC Generators:
- 5 OC/PWMs
- 2 TMRs

8 Feedback ADC
- 2 DC
- 1 AWG
- 5 Supply/Ref

AWG:
- 1 TMR Shared
- 1 DMA Shared
- Port H

Protocol I/O:
- 1 SPI / UART
- 1 I2C
- 5 GPIO
- 1 DMA
- 2 OC/PWMs
- 1 TMR
- 2 INTs

Logic Analyzer:
- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

Triggering:
- 2 GPIO
- 1 INT

USB via UART:
- 1 UART
- 2 DMAs

uSD:
- 1 SPI

WiFi:
- 1 SPI / INT

Port F

10 LA Inputs

Port E
10 MS/s

EXT Trigger

FTDI
(USB for Serial COM)

uSD

MRF24
WiFi

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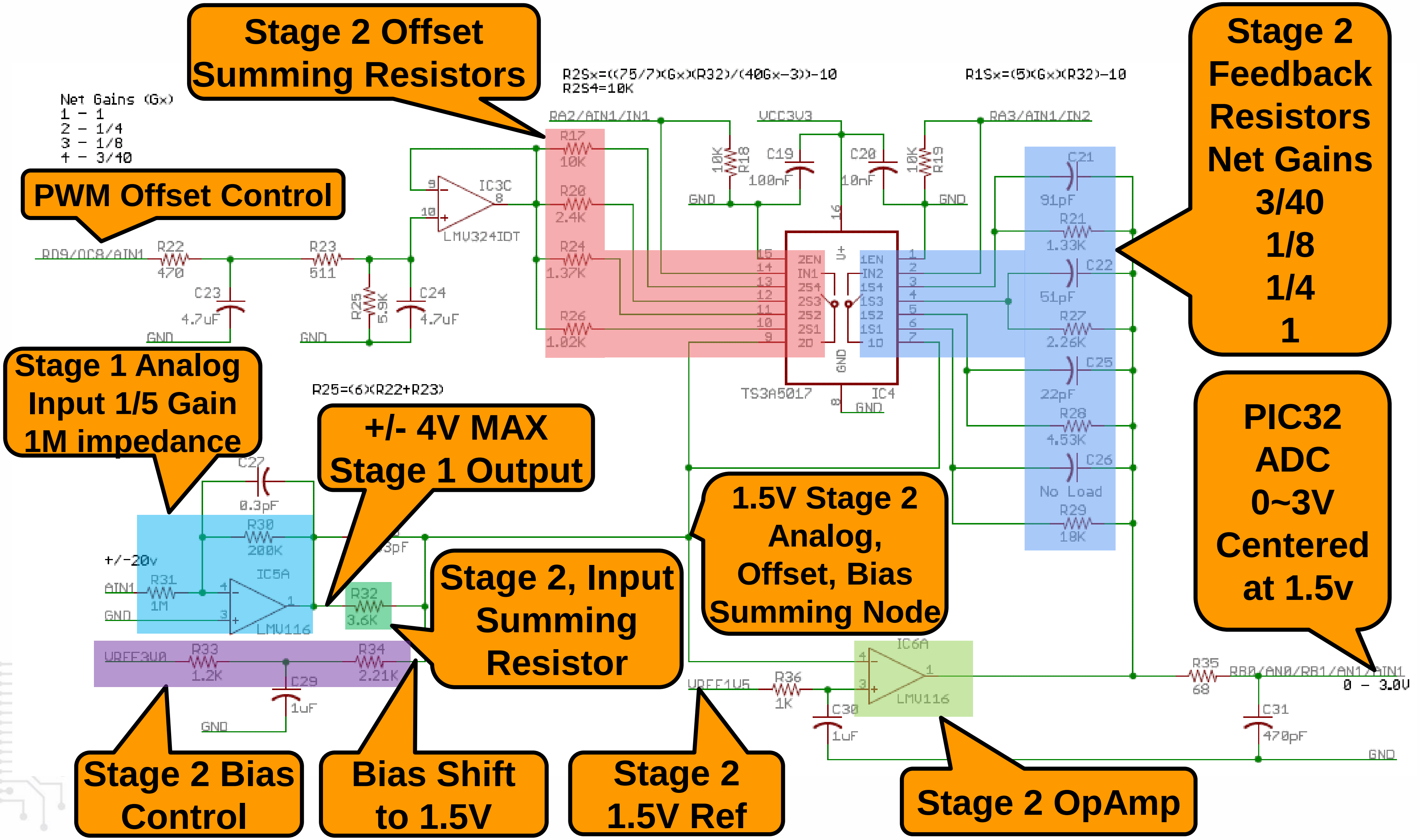
Analog Input



Stage 2 Offset Summing Resistors

Stage 2 Feedback Resistors Net Gains 3/40 1/8 1/4 1

PWM Offset Control

Stage 1 Analog Input 1/5 Gain 1M impedance

+/- 4V MAX Stage 1 Output

1.5V Stage 2 Analog, Offset, Bias Summing Node

PIC32 ADC 0~3V Centered at 1.5v

Stage 2, Input Summing Resistor

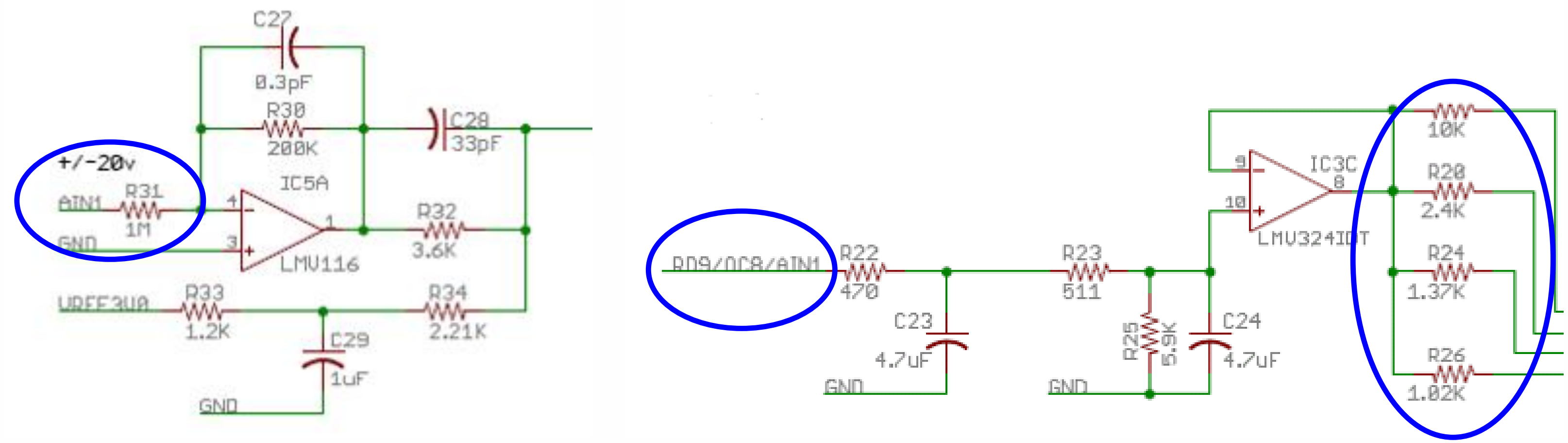
Stage 2 Bias Control

Bias Shift to 1.5V

Stage 2 1.5V Ref

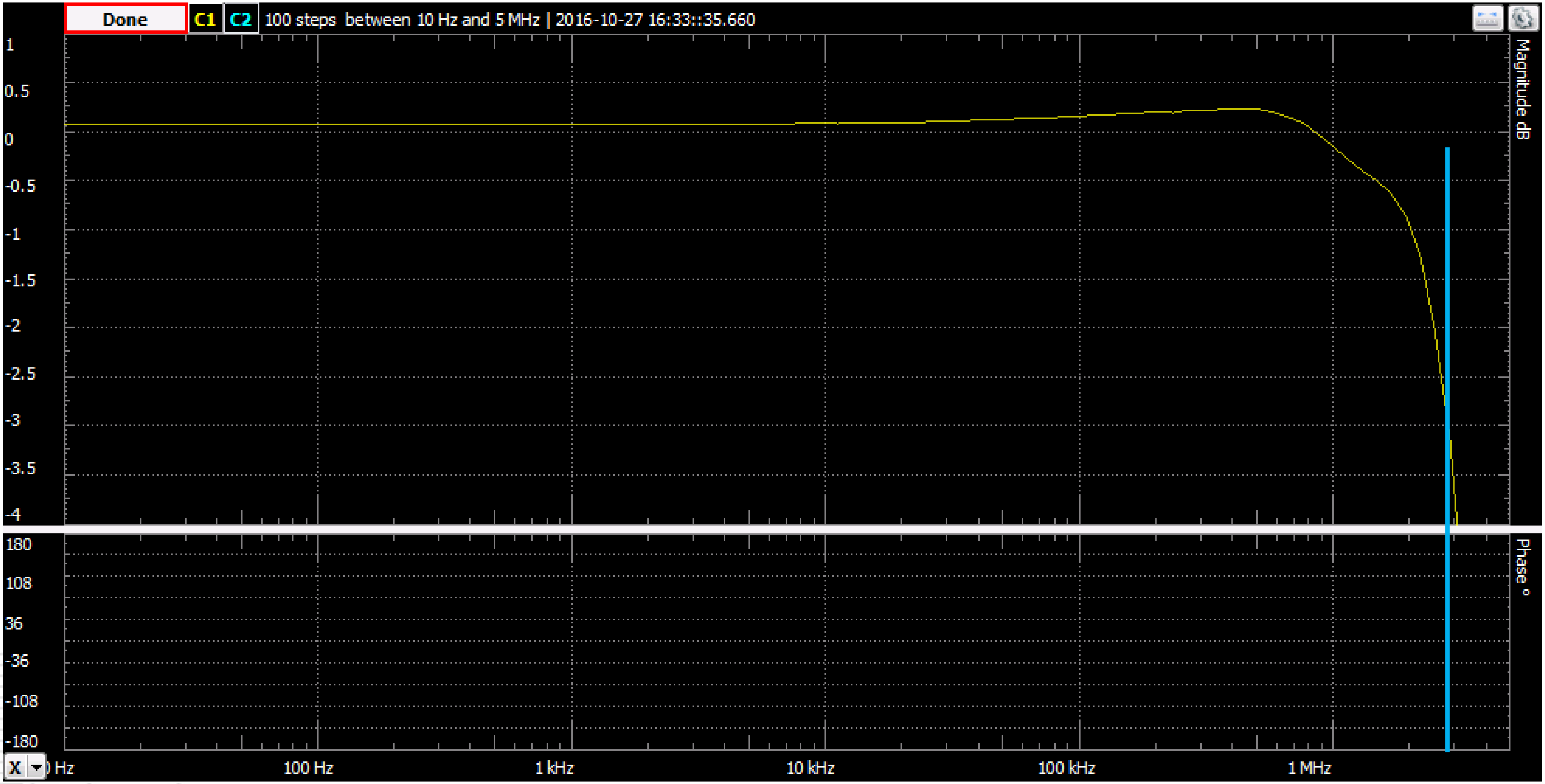
Stage 2 OpAmp

Pseudo AC Coupling



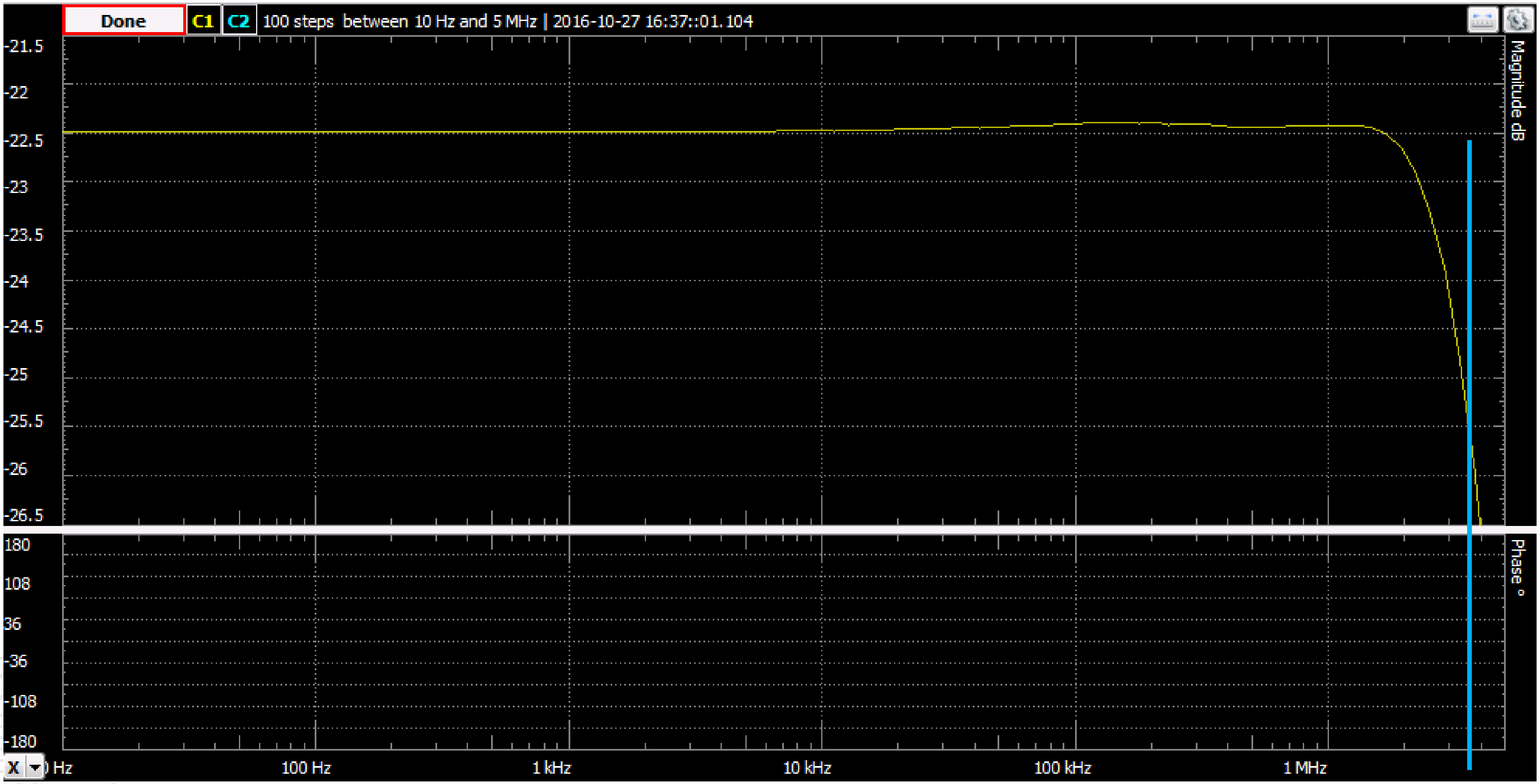
- No AC coupling, direct DC coupling.
- Input offset bias via PWM8 allows for pseudo AC coupling.
- Small P2P offset signals can be centered on the MZs ADC input.

Typical Unity Gain Response



-3db ~2.9MHz

3/40 Gain



Done C1 C2 100 steps between 10 Hz and 5 MHz | 2016-10-27 16:37::01.104

-3db ~3.5MHz

Analog In

$V = A \cdot D_{adc} + B \cdot D_{pwm} - C$

$$\mu V_{in} = (1000000)(3/4096)(R_{31}/R_{30})(R_{32}/R_{1Sx})D_{adc}$$
$$+(1000000)\ (3.3/330)(R_{25}/(R_{22}+R_{23}+R_{25}))(R_{31}/R_{30})(R_{32}/R_{2Sx})D_{pwm}$$
$$-(1000000)(R_{31}/R_{30})(R_{32}/R_{2Sx})VRef_{1.5}$$

$$\mu V_{in} = (13{,}183{,}593.75\ /R_{1Sx})D_{adc}$$
$$+\ (154{,}338{,}032.2627525069030664147653/R_{2Sx})D_{pwm}$$
$$-\ (27{,}000{,}000{,}000/R_{2Sx})$$

Gain 1; A = 732.4, B = 151,311.8, C = 26,470,588.2
Gain 1/4: A = 2,910.3, B = 112,655.5, C = 19,708,029.2
Gain 1/8: A = 5,833.4, B = 64,307.5, C = 11,250,000
Gain 3/40: A = 9,912.5, B = 15,433.8, C = 2,700,000

Calibration

Connect a DC_{out} to the analog input (V_{in})

Hold D_{pwm} constant, vary V_{in} via the DC_{out}

$$\mu V_{in1} = A \cdot D_{adc1} + B \cdot D_{pwm1} – C$$
$$-\mu V_{in2} = -A \cdot D_{adc2} - B \cdot D_{pwm1} + C$$

$$(\mu V_{in1} - \mu V_{in2}) = A \cdot (D_{adc1} - D_{adc2})$$

$$A = (\mu V_{in1} - \mu V_{in2}) / (D_{adc1} - D_{adc2})$$

Hold V_{in} constant, vary D_{pwm} :

$$\mu V_{in1} = A \cdot D_{adc1} + B \cdot D_{pwm1} – C$$
$$-\mu V_{in1} = -A \cdot D_{adc2} - B \cdot D_{pwm2} + C$$

$$0 = A \cdot (D_{adc1} - D_{adc2}) + B \cdot (D_{pwm1} - D_{pwm2})$$

$$B = A \cdot (D_{adc2} – D_{adc1}) / (D_{pwm1} - D_{pwm2})$$
$$C = A \cdot D_{adc1} + B \cdot D_{pwm1} – \mu V_{in1}$$

Question:
How Good is the Uncalibrated Hardware?

a) Within 1%

b) Within 3%

c) Within 5%

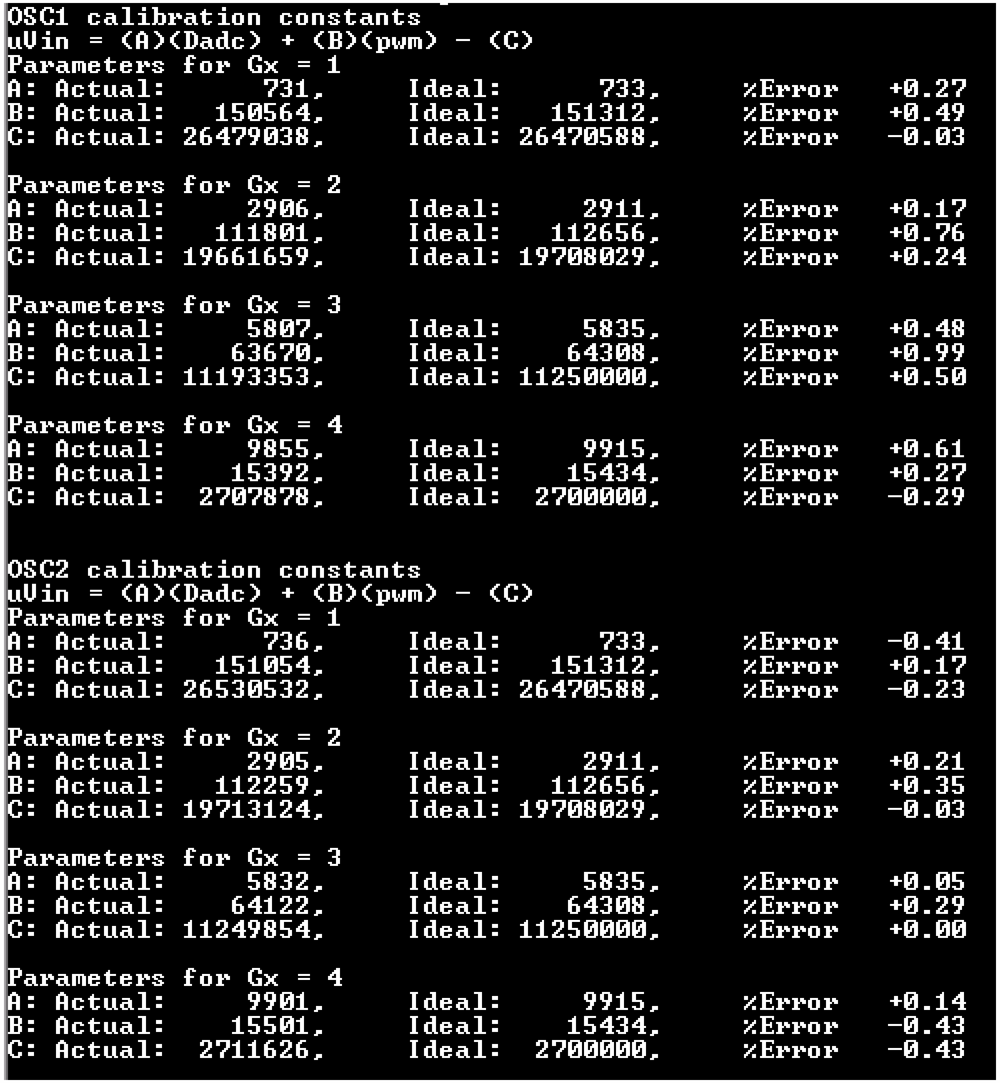
d) Within 10%

e) Within 20%

f) Within 50%

g) Worse than 50%

Actual Instrument Results



```
OSC1 calibration constants
uVin = (A)(Dadc) + (B)(pwm) - (C)
Parameters for Gx = 1
A: Actual:      731,     Ideal:      733,     %Error   +0.27
B: Actual:   150564,     Ideal:   151312,     %Error   +0.49
C: Actual: 26479038,     Ideal: 26470588,     %Error   -0.03

Parameters for Gx = 2
A: Actual:     2906,     Ideal:     2911,     %Error   +0.17
B: Actual:   111801,     Ideal:   112656,     %Error   +0.76
C: Actual: 19661659,     Ideal: 19708029,     %Error   +0.24

Parameters for Gx = 3
A: Actual:     5807,     Ideal:     5835,     %Error   +0.48
B: Actual:    63670,     Ideal:    64308,     %Error   +0.99
C: Actual: 11193353,     Ideal: 11250000,     %Error   +0.50

Parameters for Gx = 4
A: Actual:     9855,     Ideal:     9915,     %Error   +0.61
B: Actual:    15392,     Ideal:    15434,     %Error   +0.27
C: Actual:  2707878,     Ideal:  2700000,     %Error   -0.29


OSC2 calibration constants
uVin = (A)(Dadc) + (B)(pwm) - (C)
Parameters for Gx = 1
A: Actual:      736,     Ideal:      733,     %Error   -0.41
B: Actual:   151054,     Ideal:   151312,     %Error   +0.17
C: Actual: 26530532,     Ideal: 26470588,     %Error   -0.23

Parameters for Gx = 2
A: Actual:     2905,     Ideal:     2911,     %Error   +0.21
B: Actual:   112259,     Ideal:   112656,     %Error   +0.35
C: Actual: 19713124,     Ideal: 19708029,     %Error   -0.03

Parameters for Gx = 3
A: Actual:     5832,     Ideal:     5835,     %Error   +0.05
B: Actual:    64122,     Ideal:    64308,     %Error   +0.29
C: Actual: 11249854,     Ideal: 11250000,     %Error   +0.00

Parameters for Gx = 4
A: Actual:     9901,     Ideal:     9915,     %Error   +0.14
B: Actual:    15501,     Ideal:    15434,     %Error   -0.43
C: Actual:  2711626,     Ideal:  2700000,     %Error   -0.43
```

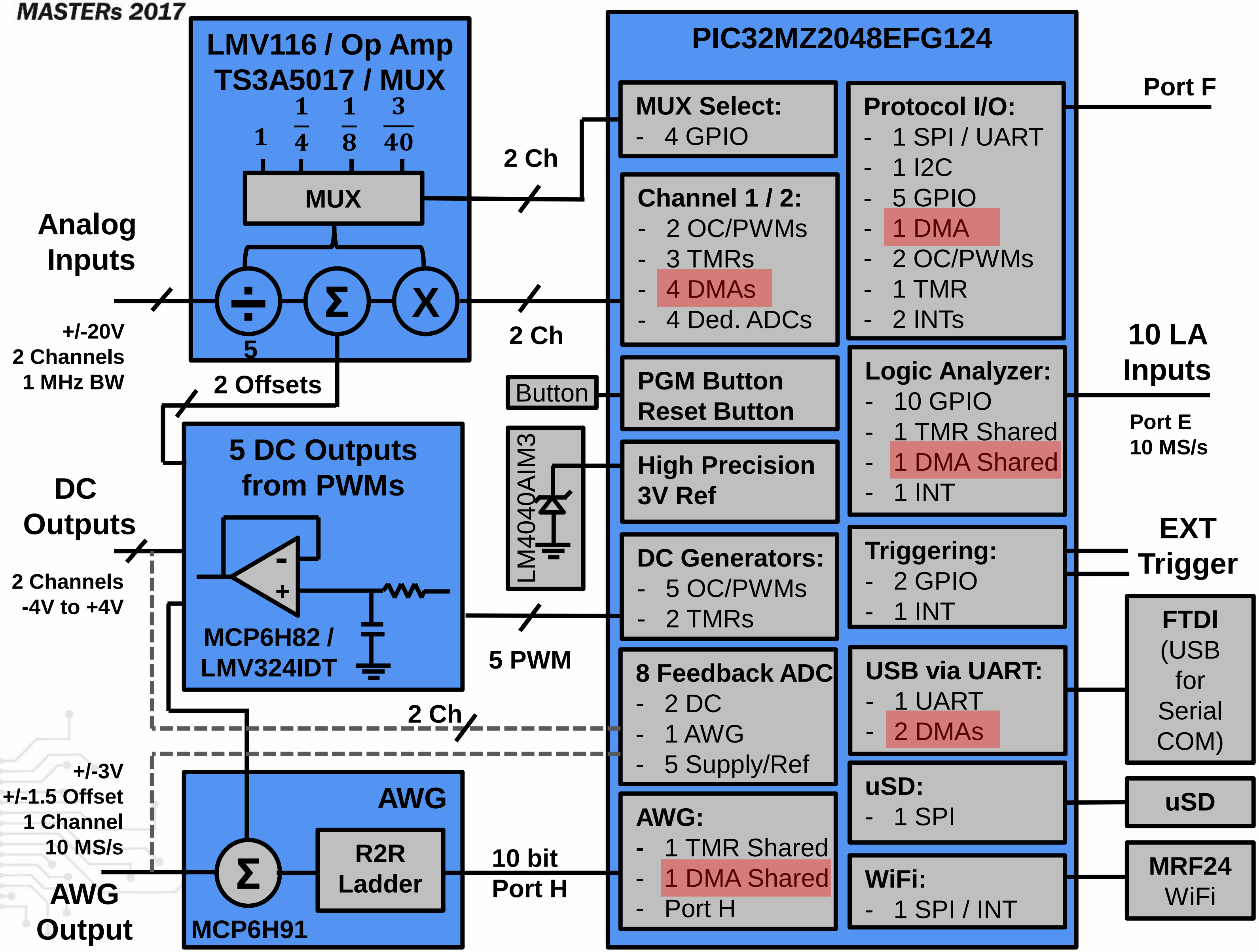
Open Scope Agenda

- Open Scope Waveforms Live Demonstration
- Architecture
- Resource Allocation
- DC Outputs
- Precision Analysis
- Analog Inputs
- **DMA Parallel Processing**
- ADC Interleaving
- Logic Analyzer (LA)
- Scope Triggering
- Analog Waveform Generator (AWG)
- Priority and Stalling Consequences
- USB/Serial, UART Interface
- Open Scope Text Based Protocol
- Building the Sources

DMA Parallel Processing

15 Minute Break

DMA Usage



LMV116 / Op Amp
TS3A5017 / MUX

Analog Inputs

+/-20V
2 Channels
1 MHz BW

2 Ch

2 Ch

2 Offsets

5 DC Outputs from PWMs

MCP6H82 /
LMV324IDT

DC Outputs

2 Channels
-4V to +4V

Button

LM4040AIM3

5 PWM

2 Ch

AWG

R2R Ladder

MCP6H91

+/-3V
+/-1.5 Offset
1 Channel
10 MS/s

AWG Output

10 bit
Port H

PIC32MZ2048EFG124

MUX Select:
- 4 GPIO

Channel 1 / 2:
- 2 OC/PWMs
- 3 TMRs
- 4 DMAs
- 4 Ded. ADCs

PGM Button
Reset Button

High Precision
3V Ref

DC Generators:
- 5 OC/PWMs
- 2 TMRs

8 Feedback ADC
- 2 DC
- 1 AWG
- 5 Supply/Ref

AWG:
- 1 TMR Shared
- 1 DMA Shared
- Port H

Protocol I/O:
- 1 SPI / UART
- 1 I2C
- 5 GPIO
- 1 DMA
- 2 OC/PWMs
- 1 TMR
- 2 INTs

Logic Analyzer:
- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

Triggering:
- 2 GPIO
- 1 INT

USB via UART:
- 1 UART
- 2 DMAs

uSD:
- 1 SPI

WiFi:
- 1 SPI / INT

Port F

10 LA Inputs

Port E
10 MS/s

EXT Trigger

FTDI
(USB for Serial COM)

uSD

MRF24
WiFi

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DMA Usage

- DMA allows for background processing freeing the CPU to do other things.
- DMA works in parallel with the CPU
- DMA can be triggered on any interrupt (event) and doesn’t require interrupt routines (ISRs).
- DMA can access peripherals and memory at speeds well surpassing the CPU or ISRs.

PIC32 Cache Considerations

- **Default memory allocation is in memory section KSEG0 whose data can be stored in the cache.**
- **The CPU cache is not updated when data is transferred via DMA.**
- **DMA Buffers must be allocated in the KSEG1 region whose data will NOT be stored in the cache.**
- **Cache coherency must be considered.**

DMA Observations

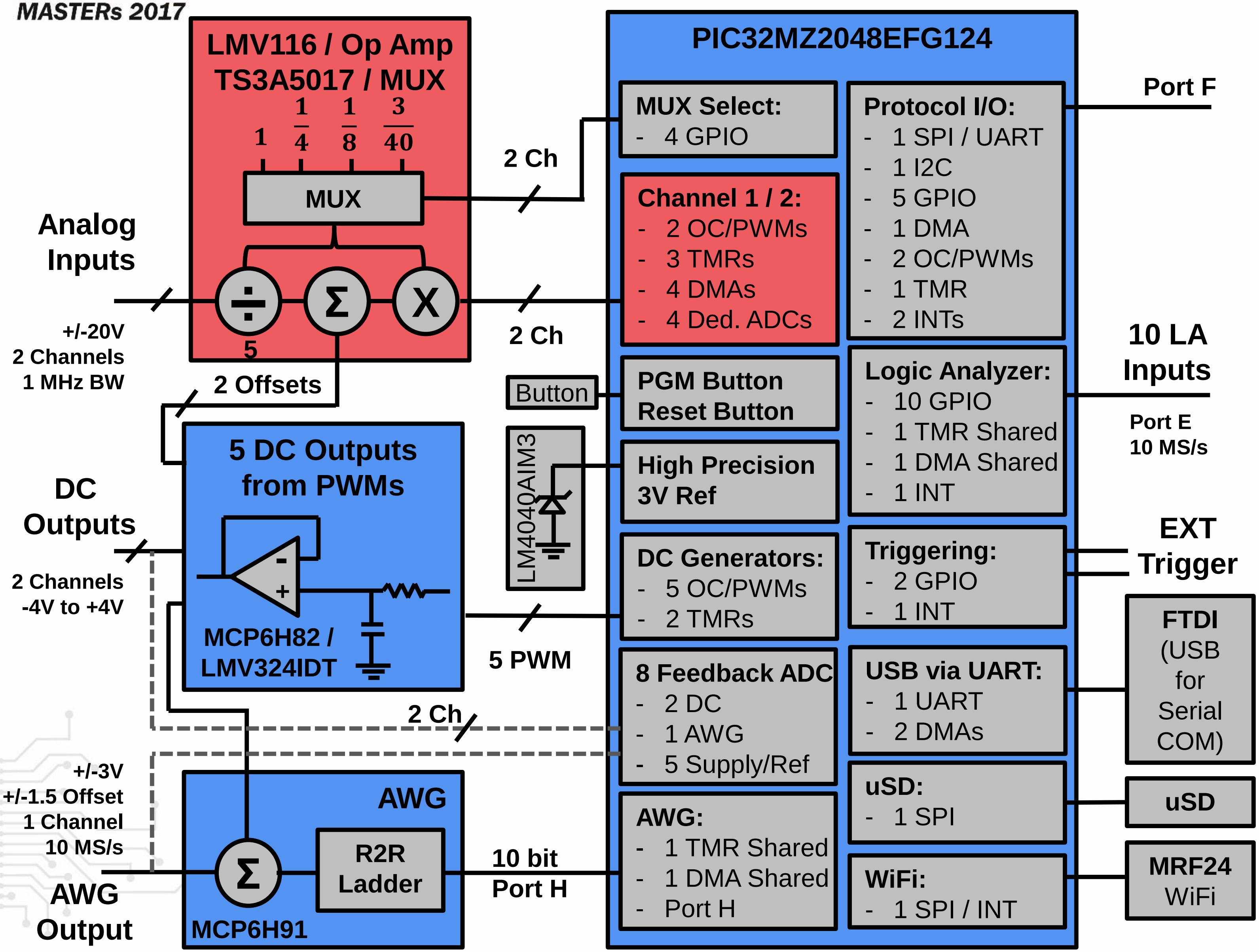
- **DMA Transfers To/From Non-Cached Memory**
  - Declare buffers as __attribute__((coherent)) to ensure the compiler creates KSEG1 (non-cached) references to the Memory.
  - If reading from cached memory (normal addressing) you may not get the correct values.
  - A trick is to memcpy() to/from KSEG0/KSEG1 to ensure both cached and non-cached memory is the same; however this will slow down your code.
  - MPLAB® X IDE only sees cached memory, irrespective of the addressing mode you select.

DMA Observations (continued)

- **Max Cell Triggering <15MT/s**
  - Reduces to about 10MT/s when using multiple DMA channels
  - Triggers are missed if triggered too fast
- **Max DMA Block Size <64K**
  - Destination/Source size of 64K (set to a value of 0) degrades DMA performance substantially and interferes with other channels.
- **All Cell Transfers are Serialized**
  - The highest priority DMA stalls all other channels during the cell transfer time.
  - Irrespective of the buses in use.

ADC Interleaving

ADC Interleaving



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1 $\frac{1}{4}$ $\frac{1}{8}$ $\frac{3}{40}$

MUX

÷ Σ X

5

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+/-20V
2 Channels
1 MHz BW

2 Ch

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2 Offsets

5 DC Outputs from PWMs

MCP6H82 /
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DC Outputs

2 Channels
-4V to +4V

Button

LM4040AIM3

5 PWM

2 Ch

+/-3V
+/-1.5 Offset
1 Channel
10 MS/s

AWG

R2R Ladder

MCP6H91

AWG Output

10 bit
Port H

PIC32MZ2048EFG124

MUX Select:
- 4 GPIO

Channel 1 / 2:
- 2 OC/PWMs
- 3 TMRs
- 4 DMAs
- 4 Ded. ADCs

PGM Button
Reset Button

High Precision
3V Ref

DC Generators:
- 5 OC/PWMs
- 2 TMRs

8 Feedback ADC
- 2 DC
- 1 AWG
- 5 Supply/Ref

AWG:
- 1 TMR Shared
- 1 DMA Shared
- Port H

Protocol I/O:
- 1 SPI / UART
- 1 I2C
- 5 GPIO
- 1 DMA
- 2 OC/PWMs
- 1 TMR
- 2 INTs

Logic Analyzer:
- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

Triggering:
- 2 GPIO
- 1 INT

USB via UART:
- 1 UART
- 2 DMAs

uSD:
- 1 SPI

WiFi:
- 1 SPI / INT

Port F

10 LA Inputs

Port E
10 MS/s

EXT Trigger

FTDI
(USB for Serial COM)

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MRF24
WiFi

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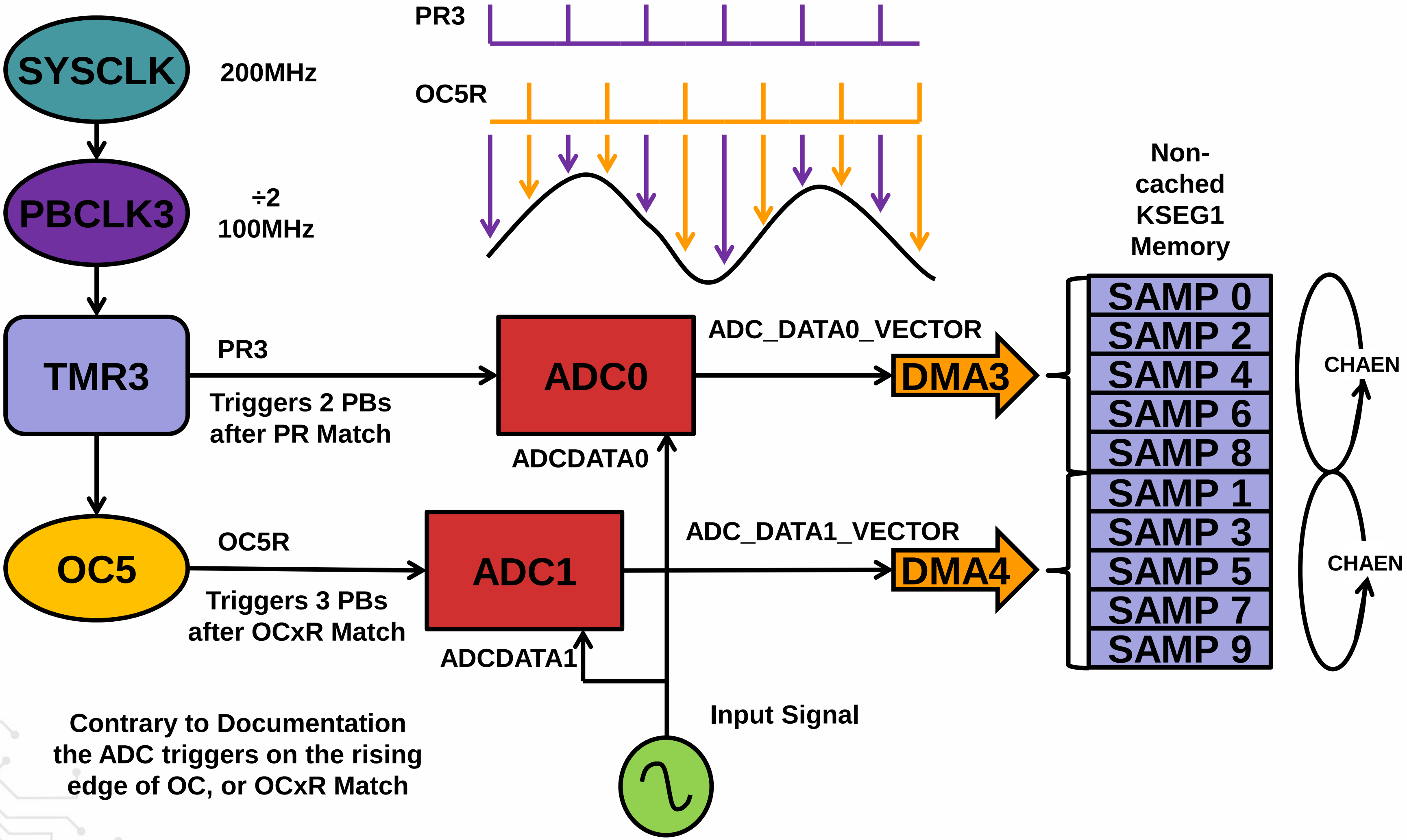
Interleaving ADCs



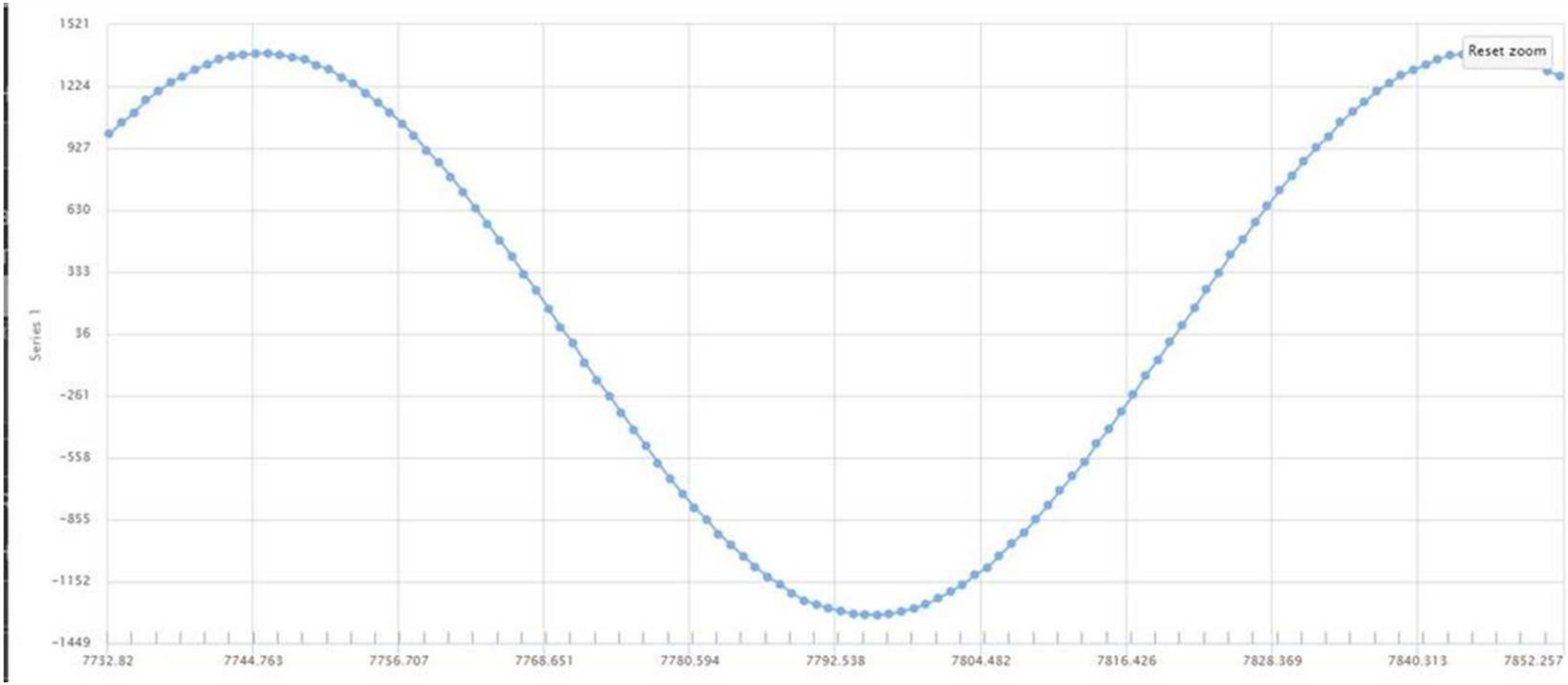
SYSCLK
200MHz
PBCLK3
÷2
100MHz
TMR3
PR3
Triggers 2 PBs after PR Match
OC5
OC5R
Triggers 3 PBs after OCxR Match
PR3
OC5R
ADC0
ADCDATA0
ADC1
ADCDATA1
ADC_DATA0_VECTOR
DMA3
ADC_DATA1_VECTOR
DMA4
Input Signal
Non-cached KSEG1 Memory
SAMP 0
SAMP 2
SAMP 4
SAMP 6
SAMP 8
SAMP 1
SAMP 3
SAMP 5
SAMP 7
SAMP 9
CHAEN
CHAEN

Contrary to Documentation the ADC triggers on the rising edge of OC, or OCxR Match

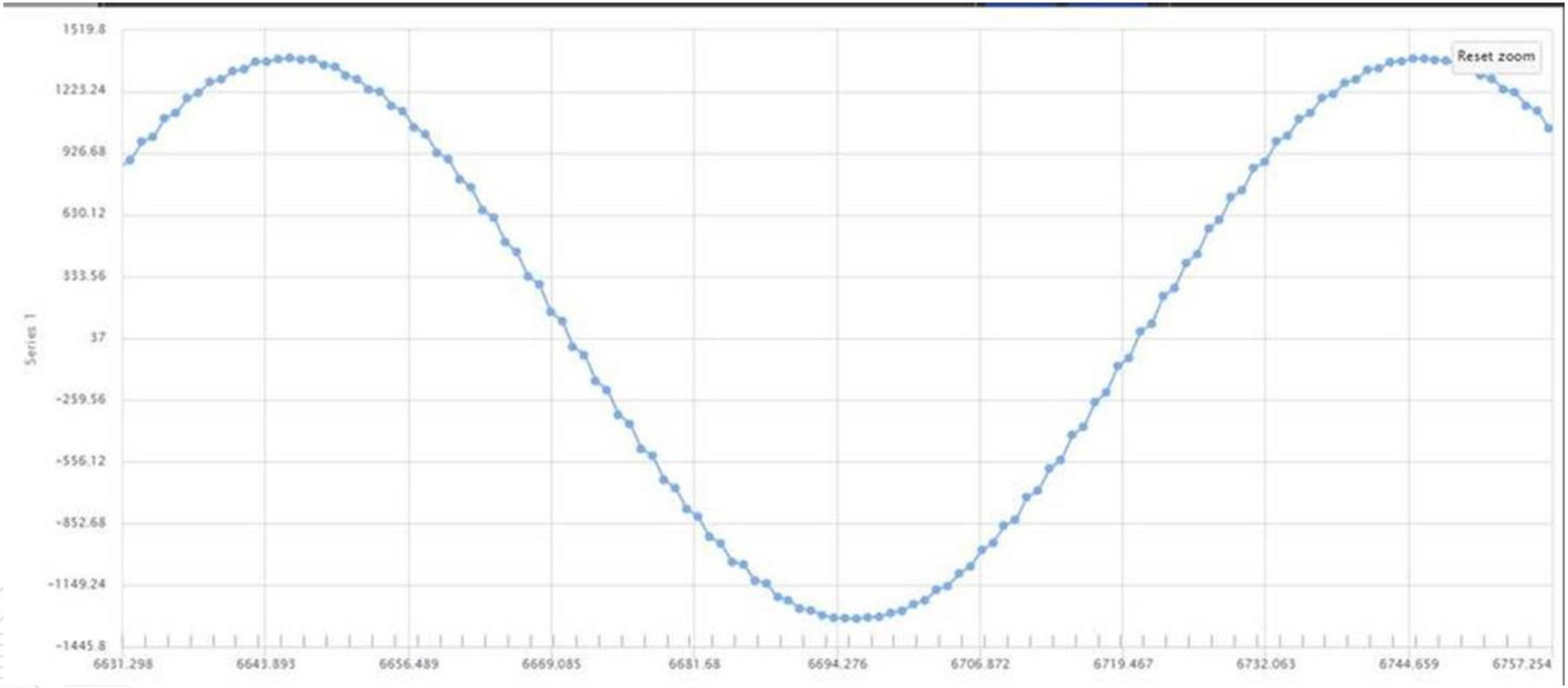
ADC Observations

- **Toss the First Conversion**
  - For an unknown reason, whenever the ADC sit unused for a few milliseconds, the first conversion will be off. The solution is to run the ADC and toss one or more conversions.
- **ADCs OC event is on OCxR Match**
  - The OC documentation says the interrupt is on the failing edge of the OC, or on OCxRS Match; but the ADC is connected directly to the rising edge of the OC.

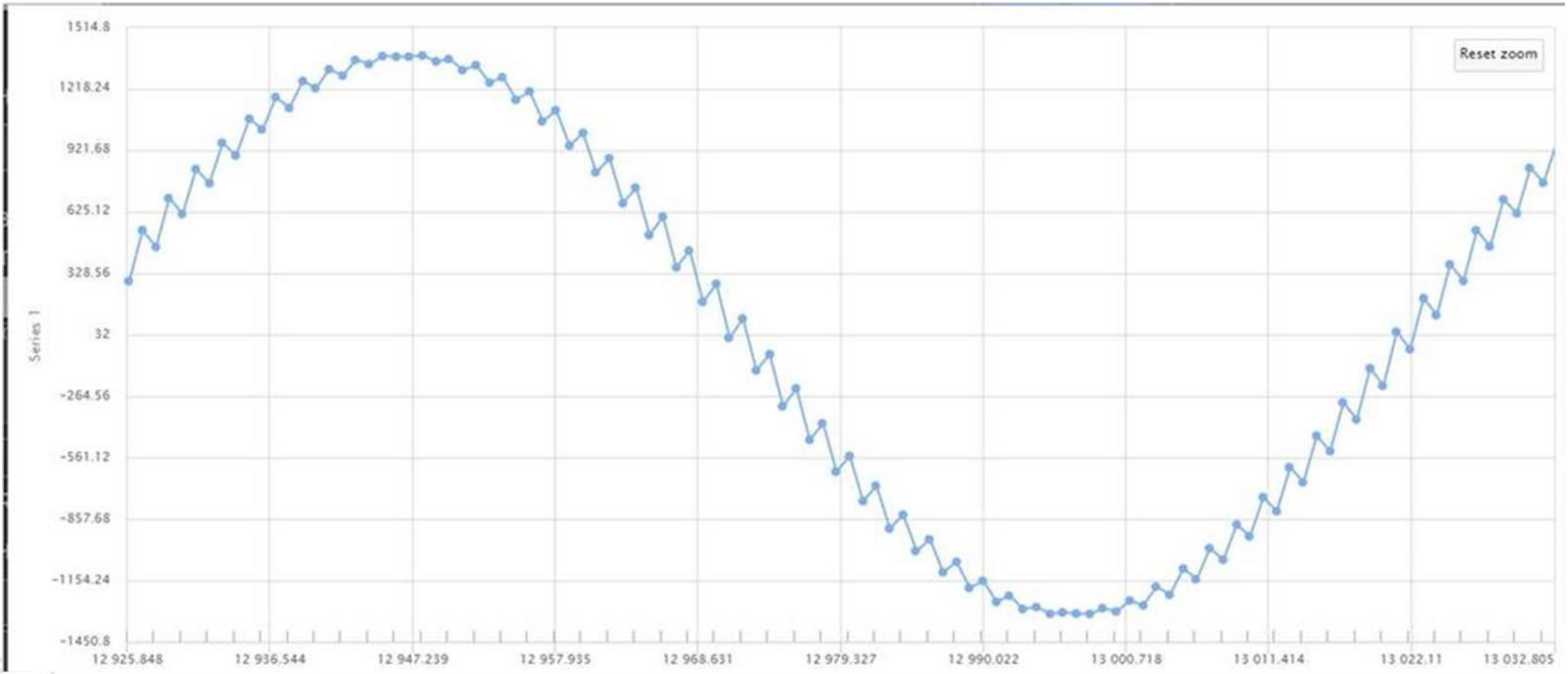
Correct Interleaving



Improper Interleaving timing

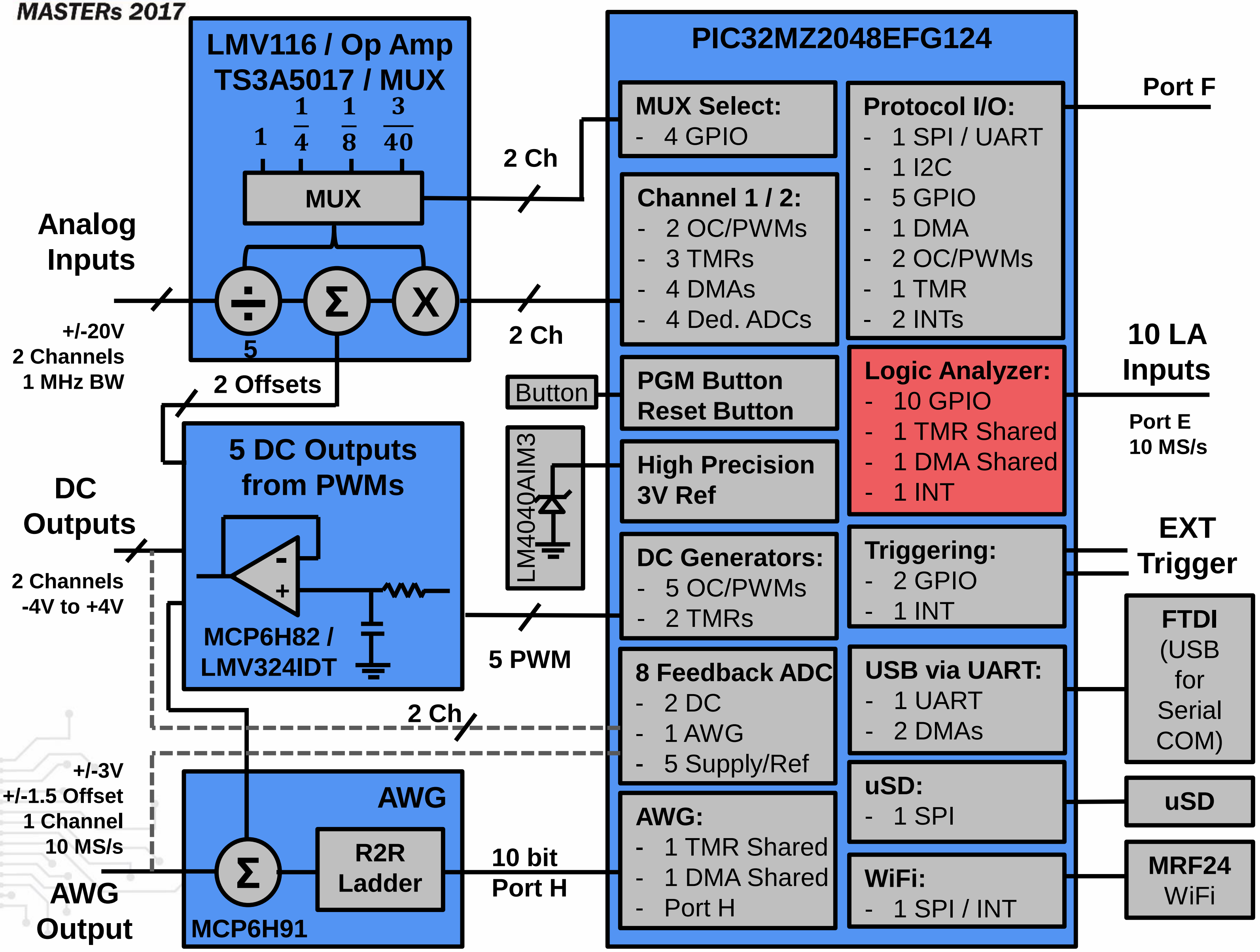


Interleaving out of Sync



Logic Analyzer

Logic Analyzer



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+/-3V
+/-1.5 Offset
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10 MS/s

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10 bit
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Reset Button

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AWG:
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- 1 DMA Shared
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Protocol I/O:
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- 1 I2C
- 5 GPIO
- 1 DMA
- 2 OC/PWMs
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- 2 DMAs

uSD:
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Port F

10 LA Inputs

Port E
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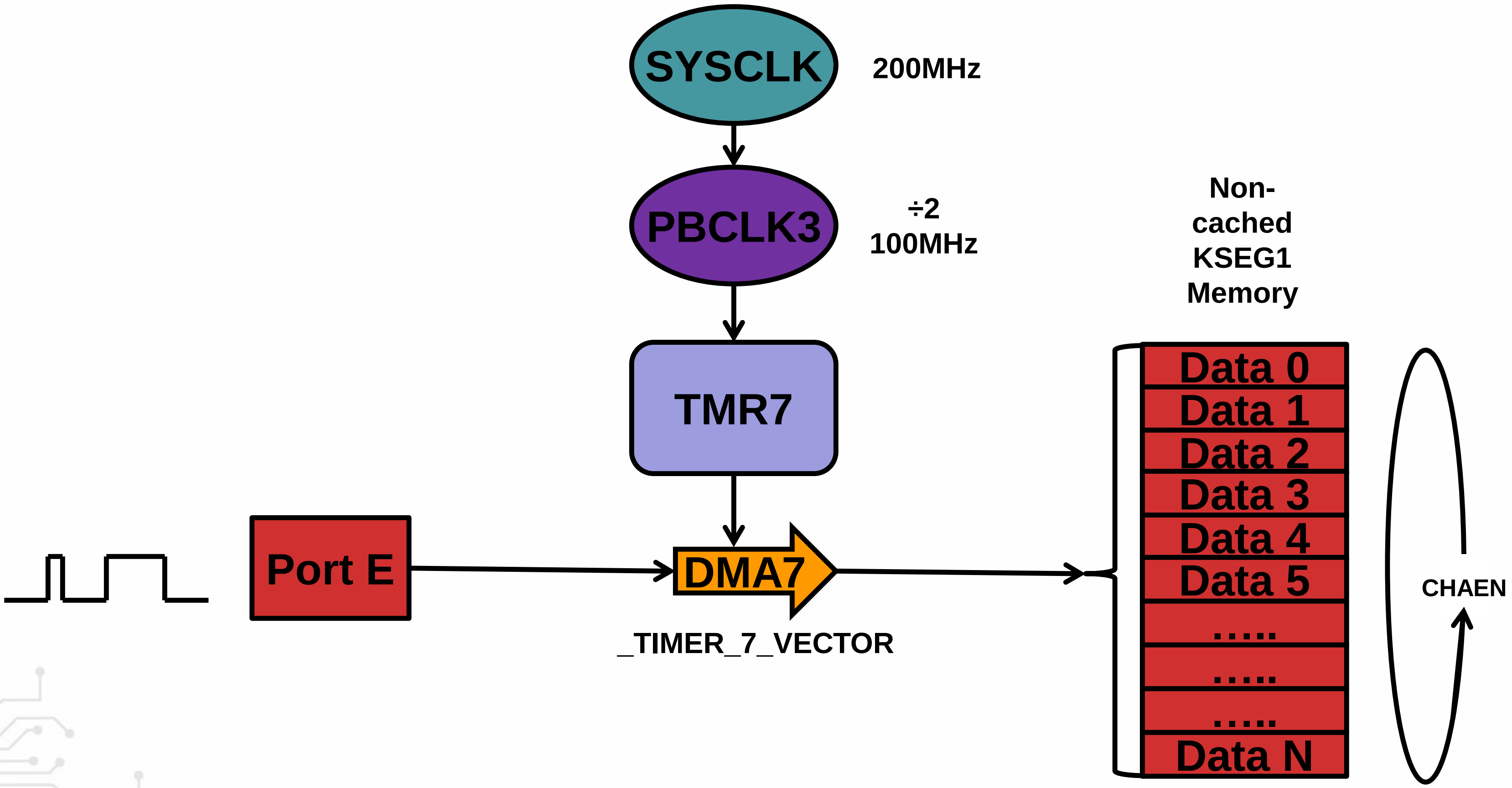
Logic Analyzer



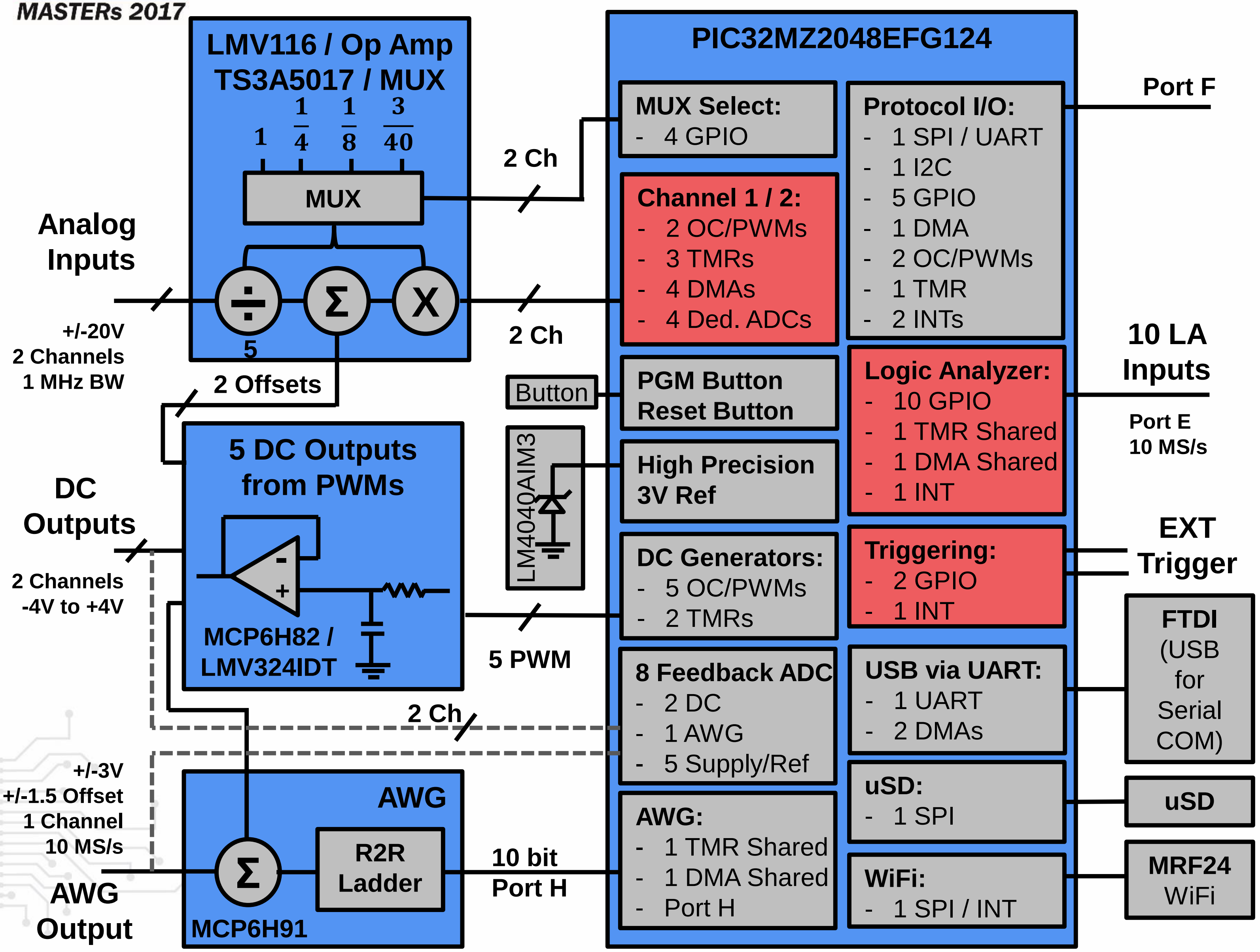
Timer 7 and DMA 7 are shared with the AWG

LA Limitations

- **Maximum Sample rate is 10MS/s**
  - The max speed we can trigger a DMA off of a timer is 10MS/s before saturating the DMA trigger.
  - IO Bus is capable of running at 50MS/s. However, only 1 DMA cell transfer can run at a time and running the LA at 50MS/s would stall all other DMAs, including the UART DMA which would stop all communication.
- **Must run at highest DMA priority**
  - To ensure that transfers are not stalled by other DMAs or skew sample timing.

Scope Triggering

Scope Triggering



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MCP6H91

+/-3V
+/-1.5 Offset
1 Channel
10 MS/s

AWG Output

10 bit Port H

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- 5 GPIO
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- 2 OC/PWMs
- 1 TMR
- 2 INTs

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- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

Triggering:
- 2 GPIO
- 1 INT

USB via UART:
- 1 UART
- 2 DMAs

uSD:
- 1 SPI

WiFi:
- 1 SPI / INT

Port F

10 LA Inputs

Port E
10 MS/s

EXT Trigger

FTDI
(USB for Serial COM)

uSD

MRF24
WiFi

PIC32 Resource Usage Summary Table

PWM / OC	9 of 9
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Shared ADCs	8 of 43
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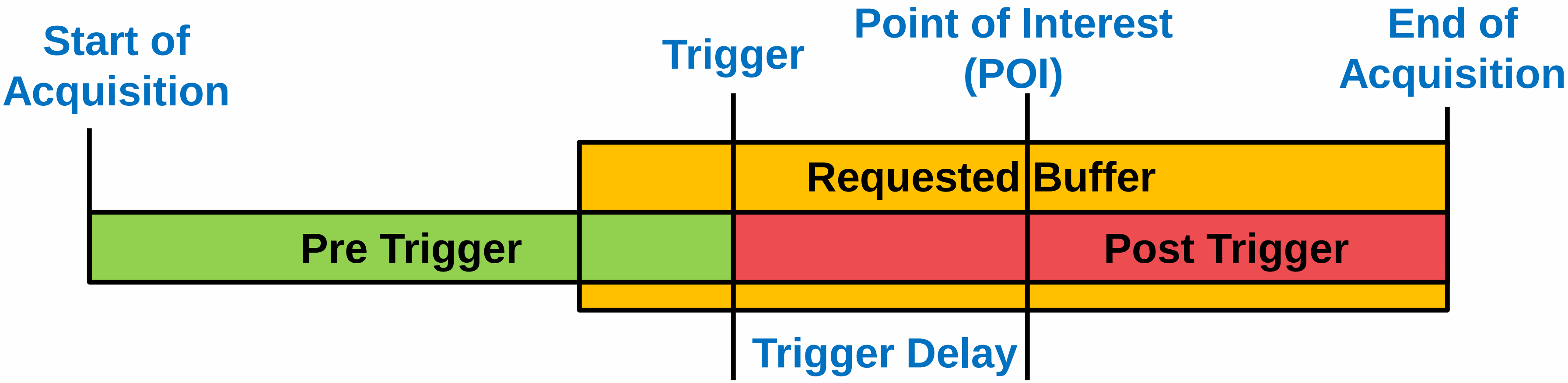
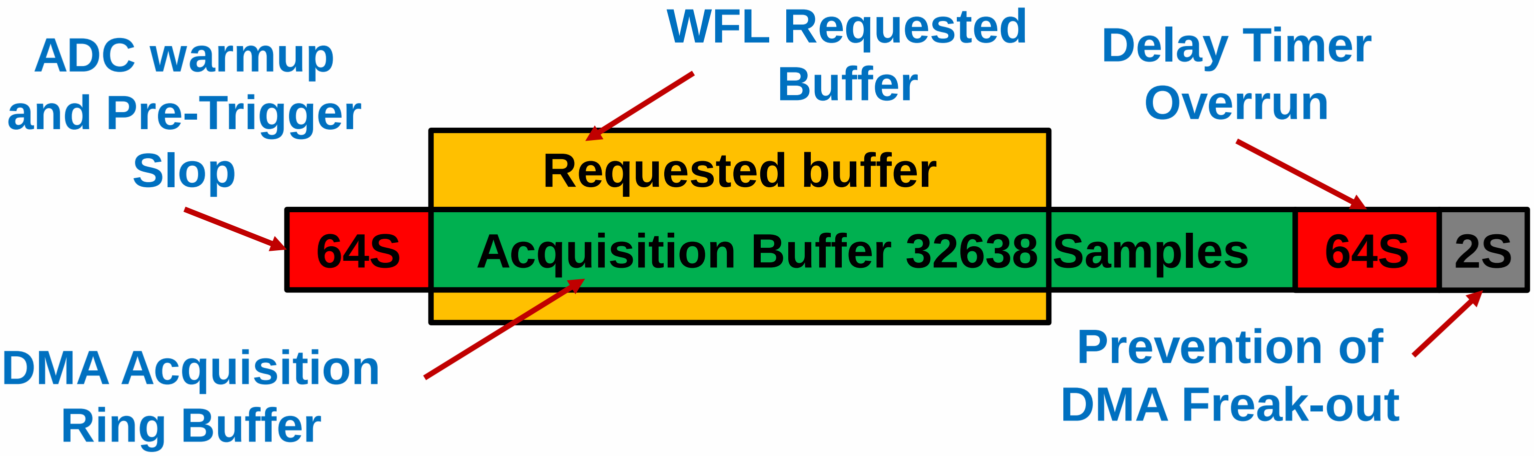
Digital Filters	1 of 6

Trigger Components



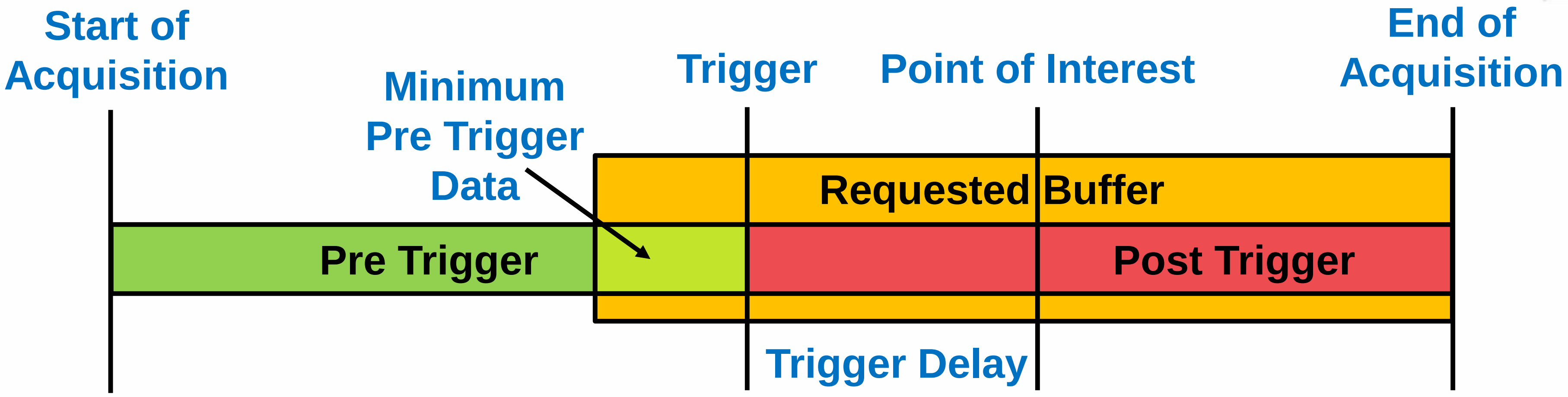
- Trigger: Where the trigger conditions are met. This is also the time reference to all acquired data.
- Point of Interest (POI): The users focal point within the data. Usually the center of the scope trace. This is where the user wants to see the signal.
- Trigger Delay: The Positive or Negative time between POI and the trigger.
- Requested Buffer: The data requested for display. The POI is “usually” scrolled to the center of this buffer.
- Time synchronization is always referenced to the trigger, the display buffer is referenced/scrolled to the POI.

Acquisition Buffer


ADC warmup and Pre-Trigger Slop
WFL Requested Buffer
Delay Timer Overrun
Requested buffer
64S
Acquisition Buffer 32638 Samples
64S
2S
DMA Acquisition Ring Buffer
Prevention of DMA Freak-out

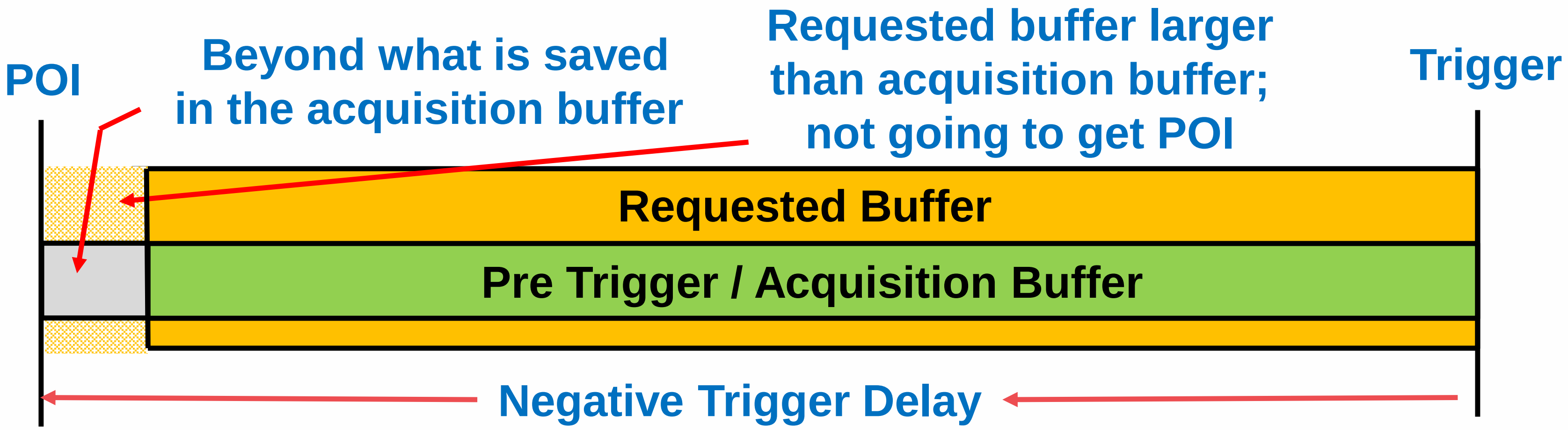
- DMA destination size is 65532 bytes, or 32766 samples (32638+64+64) of 16bit ADC data.
- DMA has a maximum destination size of 65536 bytes, but when a full 65536 is specified the DMA “freaks-out” and causes massive DMA stalls. We reduce by 4 bytes to “back-off” the maximum.
- 64 samples (128 bytes) are used as additional pre-trigger samples to warm-up the ADC and to ensure good data is in the buffer.
- 64 samples (128 bytes) are used as overrun slop to allow for additional DMA transfers between when the termination timer fires and the interrupt routines stops DMA transfers.
- The WFL request buffer overlays the start of the Acquisition Buffer.

Trigger Implications

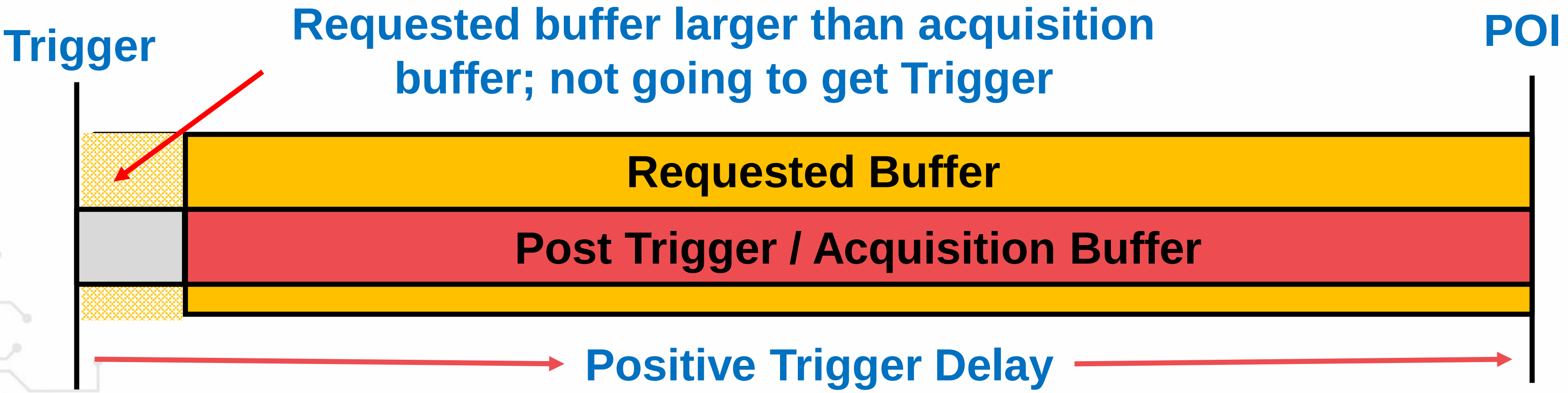


- Because it is not know when the Trigger will occur, acquisition must run continuously before the trigger.
- Acquisition must run without the trigger enabled to ensure the minimum pre-trigger data is collected.
- Acquisition must continue to run until all post trigger data is collected.

Trigger/POI Implications

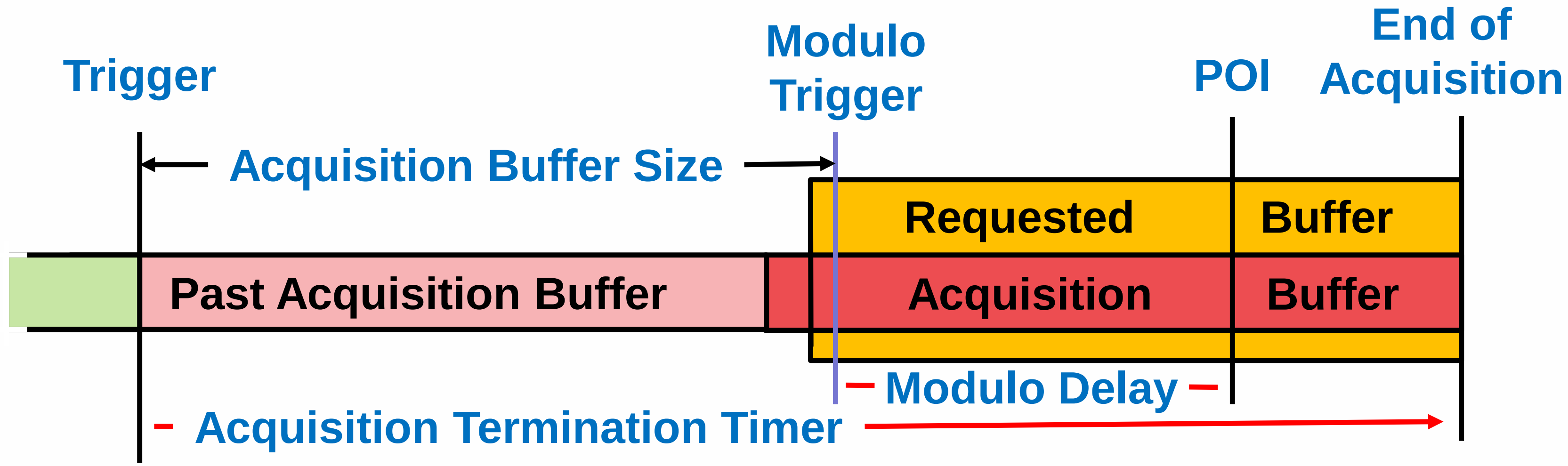

POI
Beyond what is saved in the acquisition buffer
Requested buffer larger than acquisition buffer; not going to get POI
Trigger
Requested Buffer
Pre Trigger / Acquisition Buffer
Negative Trigger Delay

- Cannot have POI any further back than your acquisition buffer size.


Trigger
Requested buffer larger than acquisition buffer; not going to get Trigger
POI
Requested Buffer
Post Trigger / Acquisition Buffer
Positive Trigger Delay

- If POI is delayed more than your acquisition buffer size, the Trigger will not be retained.

Timing, Acquisition Termination



- If the positive delay is larger than the acquisition buffer, timing between the trigger to the POI must be maintained. Modulo math is used to maintain timing of the trigger and POI. All timing is based off of the trigger.
- End of Acquisition is usually after the POI to fill out the display. The termination timer determines when acquisition stops.
- Trigger and POI indexes in the requested buffer are pre calculated. The actual modulo trigger (and data) is scrolled to the pre calculated trigger index in the buffer at the end of acquisition.

Oscilloscope Threshold Triggers

- **Uses ADC hardware Digital Comparator and Interrupts**
- **Rising Edge,** (falling Edge, Thresholds switched)
  - Interrupt 1, below lower threshold.
  - Interrupt 2, above upper threshold.
    - This is the trigger, DMA pointers saved.
    - Delay Timer9 is started.
    - Search back in buffer for actual trigger.
  - Interrupt 3, Timer9 expires.
    - Acquisition has ended.
    - All DMA transfers are stopped.

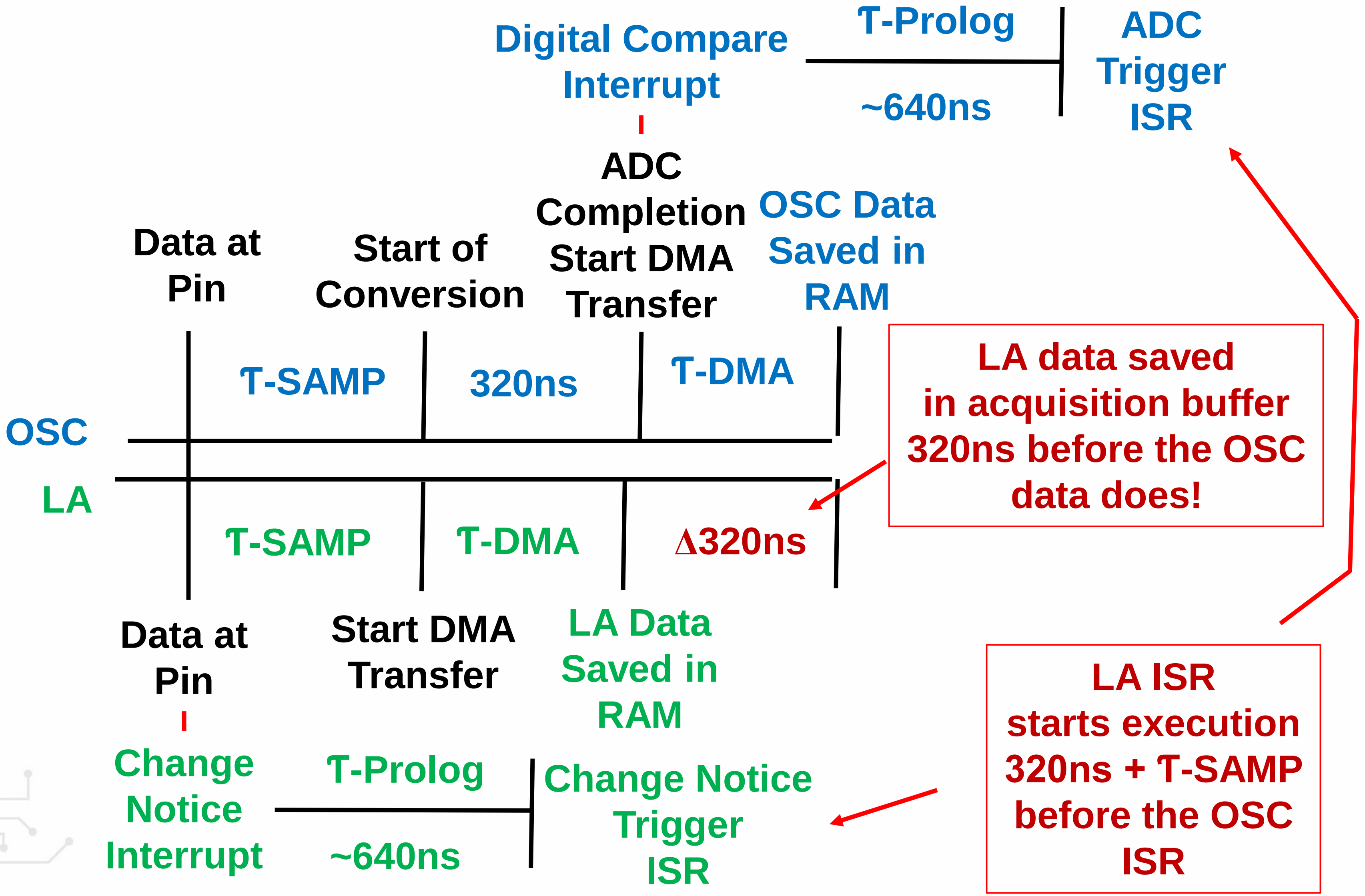
Logic Analyzer Change Notice Triggers

- **Uses I/O Port Change Notice and Interrupts**
- **Rising/Falling/Either Edge**
  - Interrupt 1, does not exist.
  - Interrupt 2, Change Notice Event.
    - This is the trigger, DMA pointers saved.
    - Delay Timer9 is started.
    - Search back in buffer for actual trigger.
  - Interrupt 3, Timer9 expires.
    - Acquisition has ended.
    - All DMA transfers are stopped.

Supported Triggers

- **Oscilloscope**
  - Rising or Falling Edge Triggers.
  - Rise / Fall Time with lower and upper threshold.
  - By default WFL sets the lower threshold 30mV below the upper threshold.
- **Logic Analyzer**
  - Rising, Falling, or Either Edge Triggers.
  - 10 LA signal channels.
  - Any combination of LA pins can be Triggers.
  - Pattern matching is not supported.

Multi-Instrument Timing



Digital Compare Interrupt

T-Prolog

~640ns

ADC Trigger ISR

ADC Completion Start DMA Transfer

Data at Pin

Start of Conversion

OSC Data Saved in RAM

OSC

T-SAMP

320ns

T-DMA

LA

T-SAMP

T-DMA

Δ320ns

LA data saved in acquisition buffer 320ns before the OSC data does!

Data at Pin

Start DMA Transfer

LA Data Saved in RAM

Change Notice Interrupt

T-Prolog

~640ns

Change Notice Trigger ISR

LA ISR starts execution 320ns + T-SAMP before the OSC ISR

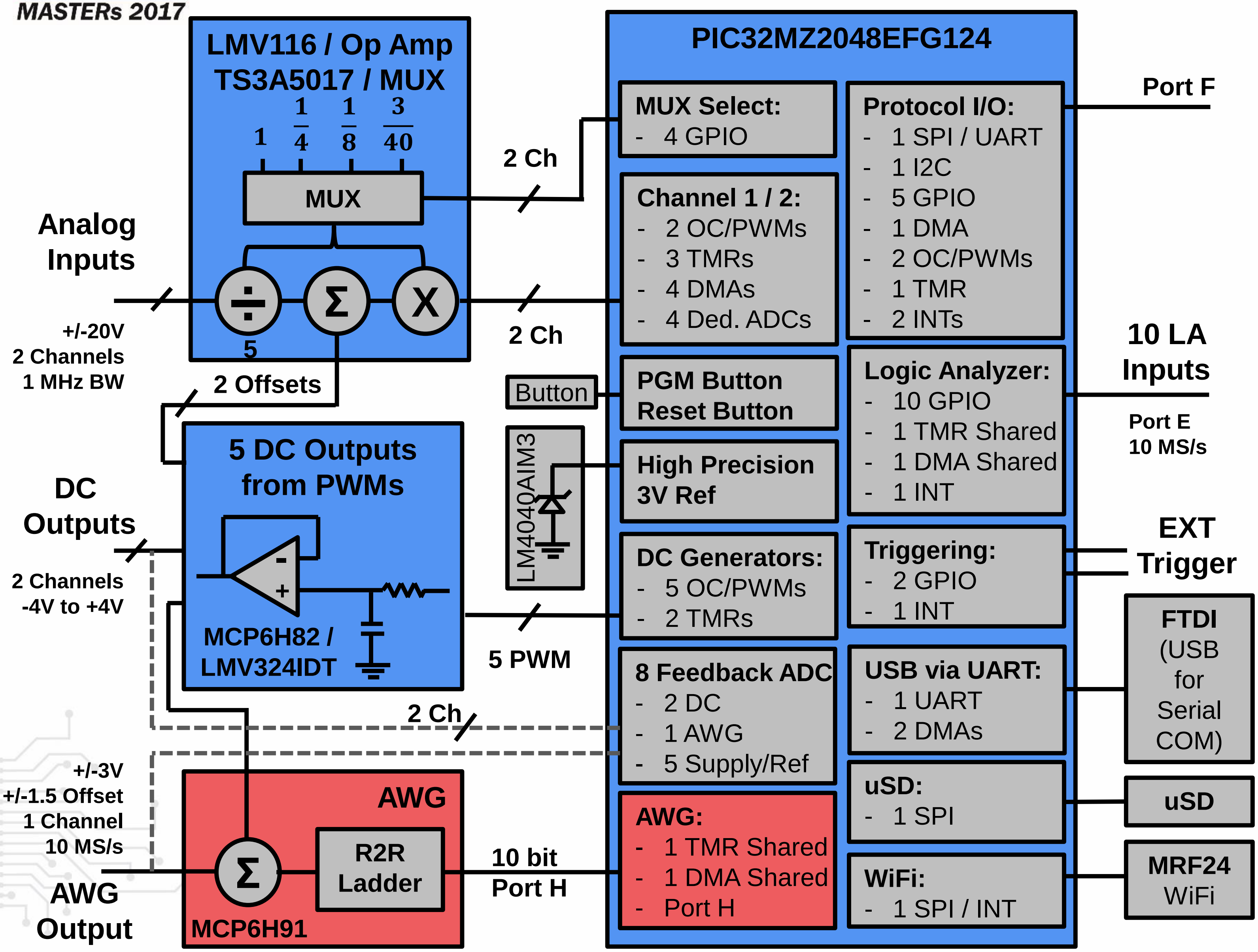
Multi-Instrument Compensation

- **All OSC data in the acquisition buffer is 320ns later than data in the LA buffer.**
  - The conversion time of the ADC, 1/3,125,000
  - To sync the data, we must move the OSC back 320ns, or the LA forward 320ns when comparing the 2 buffers.
- **The ISR synchronizes the DMA pointers.**
  - All DMA pointers for all instrument acquisition buffers are snapshot. Then time adjusted for the OSC/LA.
  - The ISR must look back in the buffer to find the actual trigger. All other instrument pointers must be adjusted.
  - At very low sample rates (T-SAMP >> T-Prolog) it is possible that the LA ISR can execute before the DMA transfers the data to RAM. The PORT register must be considered when finding the actual trigger.

Analog Waveform Generator (AWG)

Analog Waveform Generator (AWG)

MICROCHIP MASTERs 2017



Analog Inputs

+/-20V
2 Channels
1 MHz BW

LMV116 / Op Amp
TS3A5017 / MUX

$1 \quad \frac{1}{4} \quad \frac{1}{8} \quad \frac{3}{40}$

MUX

÷ Σ X

5

2 Offsets

2 Ch

2 Ch

DC Outputs

2 Channels
-4V to +4V

5 DC Outputs from PWMs

MCP6H82 /
LMV324IDT

Button

LM4040AIM3

5 PWM

2 Ch

+/-3V
+/-1.5 Offset
1 Channel
10 MS/s

AWG Output

AWG

Σ

R2R Ladder

MCP6H91

10 bit
Port H

PIC32MZ2048EFG124

MUX Select:
- 4 GPIO

Channel 1 / 2:
- 2 OC/PWMs
- 3 TMRs
- 4 DMAs
- 4 Ded. ADCs

PGM Button
Reset Button

High Precision 3V Ref

DC Generators:
- 5 OC/PWMs
- 2 TMRs

8 Feedback ADC
- 2 DC
- 1 AWG
- 5 Supply/Ref

AWG:
- 1 TMR Shared
- 1 DMA Shared
- Port H

Protocol I/O:
- 1 SPI / UART
- 1 I2C
- 5 GPIO
- 1 DMA
- 2 OC/PWMs
- 1 TMR
- 2 INTs

Logic Analyzer:
- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

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- 1 UART
- 2 DMAs

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(USB for Serial COM)

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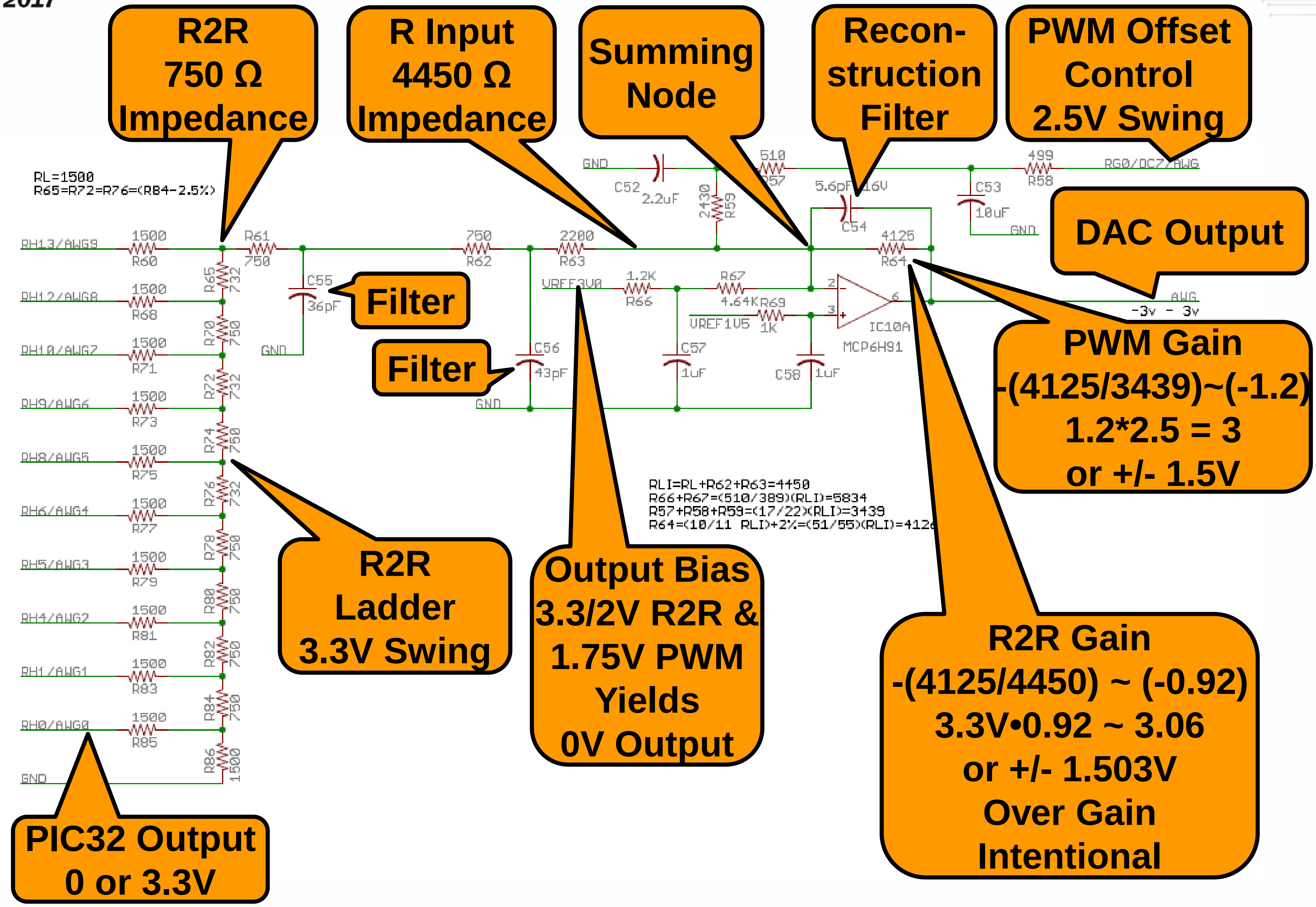
Function Generator



R2R 750 Ω Impedance

R Input 4450 Ω Impedance

Summing Node

Recon-struction Filter

PWM Offset Control 2.5V Swing

DAC Output

Filter

Filter

PWM Gain -(4125/3439)~(-1.2) 1.2*2.5 = 3 or +/- 1.5V

R2R Ladder 3.3V Swing

Output Bias 3.3/2V R2R & 1.75V PWM Yields 0V Output

R2R Gain -(4125/4450) ~ (-0.92) 3.3V•0.92 ~ 3.06 or +/- 1.503V Over Gain Intentional

PIC32 Output 0 or 3.3V

RL=1500
R65=R72=R76=(R84-2.5%)

RLI=RL+R62+R63=4450
R66+R67=(510/389)(RLI)=5834
R57+R58+R59=(17/22)(RLI)=3439
R64=(10/11 RLI)+2%=(51/55)(RLI)=412

AWG: $V = -A \cdot D_{dac} - B \cdot D_{pwm} + C$

$$Vout = -R_{64}/(R_{60}+R_{62}+R_{63}) \cdot V_{cc} \cdot D_{dac}/1024 - R_{64}/(R_{57}+R_{58}+R_{59}) \cdot V_{cc} \cdot D_{pwm}/330$$
$$+ R_{64}/(R_{60}+R_{62}+R_{63}) \cdot VRef_{1.5} + R_{64}/(R_{57}+R_{58}+R_{59}) \cdot VRef_{1.5}$$
$$+ (VRef_{1.5} - VRef_{3.0}) \cdot R_{64}/(R_{66}+R_{67}) + VRef_{1.5}$$

$$Vout = -4125/4450/1024 \cdot V_{cc} \cdot D_{dac} - 4125/3439/330 \cdot V_{cc} \cdot D_{pwm} + 2.130161 + 1.5$$

$A \approx 0.002987$; $B \approx 0.011995$; $C \approx 3.630161$

$$\mu Vout \approx -2987 \cdot D_{dac} - 11995 \cdot D_{pwm} + 3630161$$

$-2987 \cdot D_{dac}$ Implemented via best fit table lookup

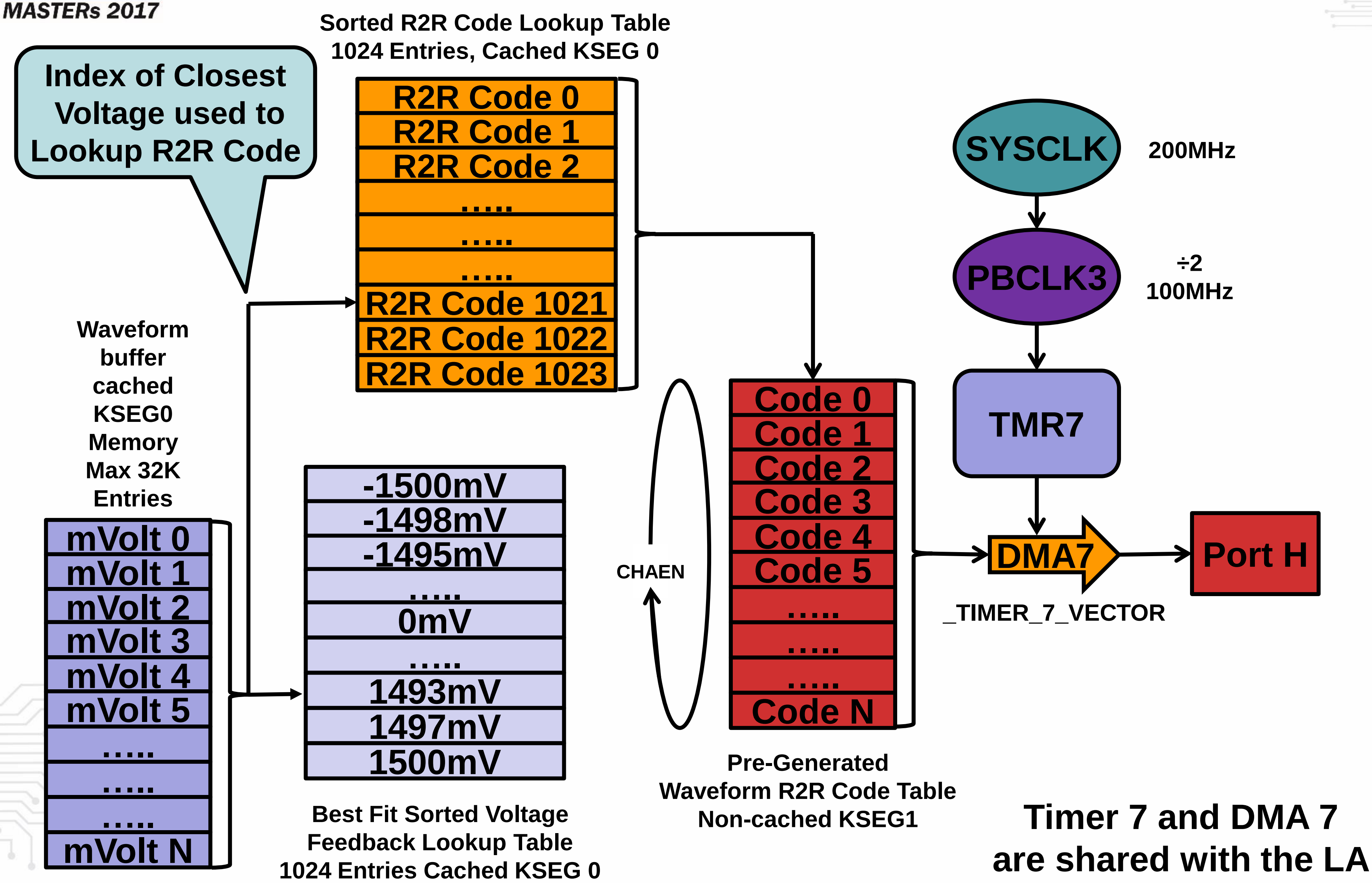
$\mu V_{PWM}Offset = 0$; When $D_{pwm} = 175$;

$$\mu V_{PWM}Offset = -11995 \cdot D_{pwm} + 2099125$$

AWG Calibration

- Only the PWM Offset Coefficients are calibrated.
- Coefficient for the R2R ladder is NOT calibrated.
- Each voltage code is applied and then read via the feedback network.
- The read codes are sorted.
- A best fit sorted lookup table is used to determine which code to use for a specific voltage.

Waveform Generator



Index of Closest Voltage used to Lookup R2R Code

Sorted R2R Code Lookup Table
1024 Entries, Cached KSEG 0

R2R Code 0
R2R Code 1
R2R Code 2
.....
.....
.....
R2R Code 1021
R2R Code 1022
R2R Code 1023

Waveform buffer cached KSEG0 Memory Max 32K Entries

mVolt 0
mVolt 1
mVolt 2
mVolt 3
mVolt 4
mVolt 5
.....
.....
.....
mVolt N

-1500mV
-1498mV
-1495mV
.....
0mV
.....
1493mV
1497mV
1500mV

Best Fit Sorted Voltage
Feedback Lookup Table
1024 Entries Cached KSEG 0

CHAEN

Code 0
Code 1
Code 2
Code 3
Code 4
Code 5
.....
.....
.....
Code N

Pre-Generated
Waveform R2R Code Table
Non-cached KSEG1

SYSCLK 200MHz

PBCLK3 ÷2 100MHz

TMR7

DMA7

Port H

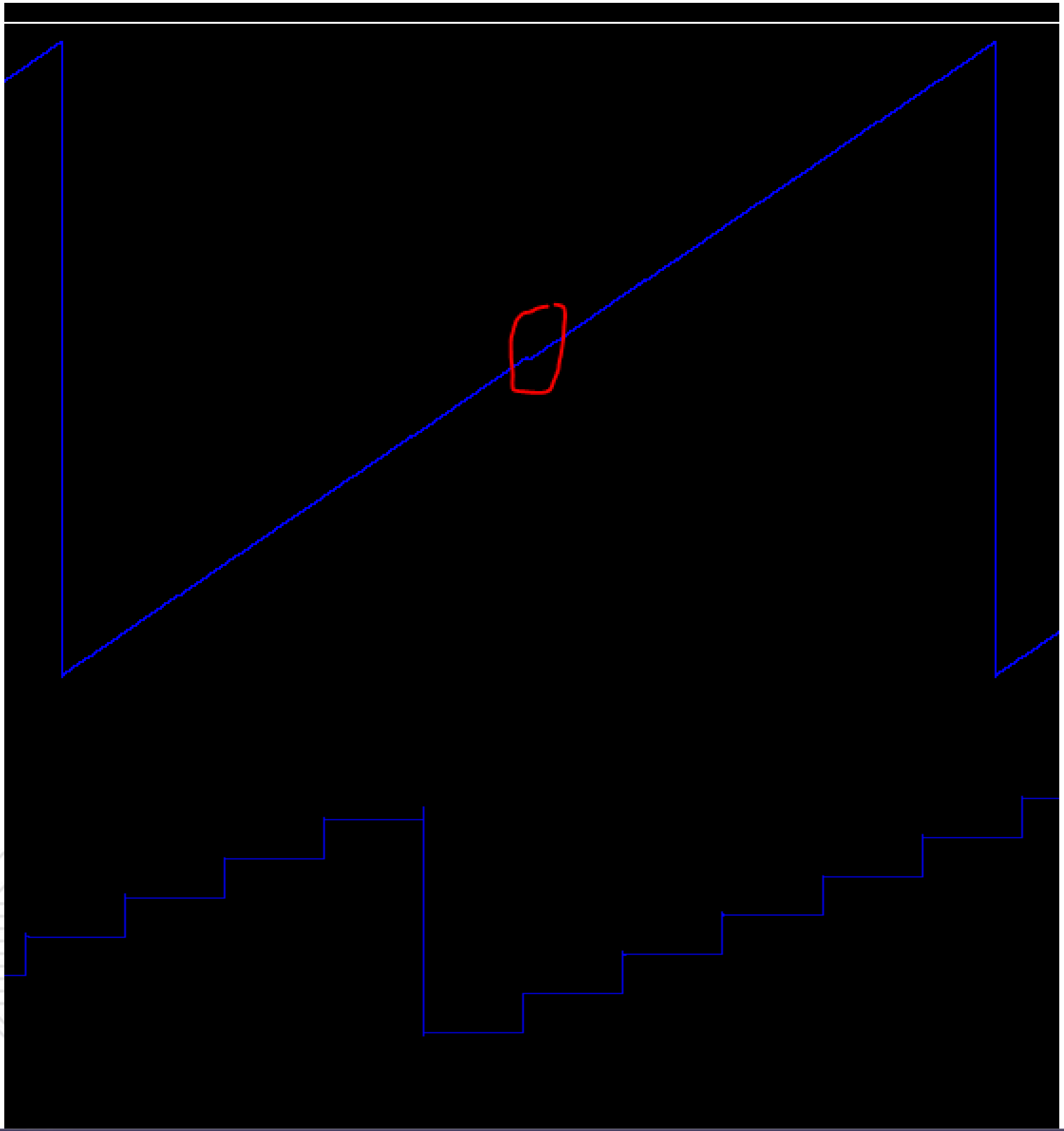
_TIMER_7_VECTOR

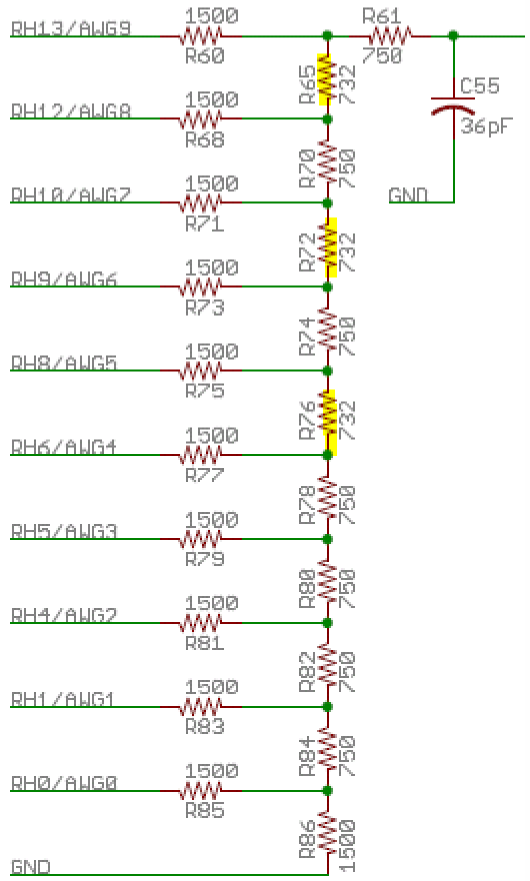
Timer 7 and DMA 7 are shared with the LA

R2R Ladder is not Precise

- **Only 1% resistors are used.**
- **It is possible to have missing codes.**
  - For example if when switching from 0x1FF to 0x200 if that step is greater than 3mv, there is no way to pick up the missing LSB.
- **There is a propagation delay through the ladder that causes switching spikes.**
  - Most noticeable when switching from/to 0x1FF <-> 0x200

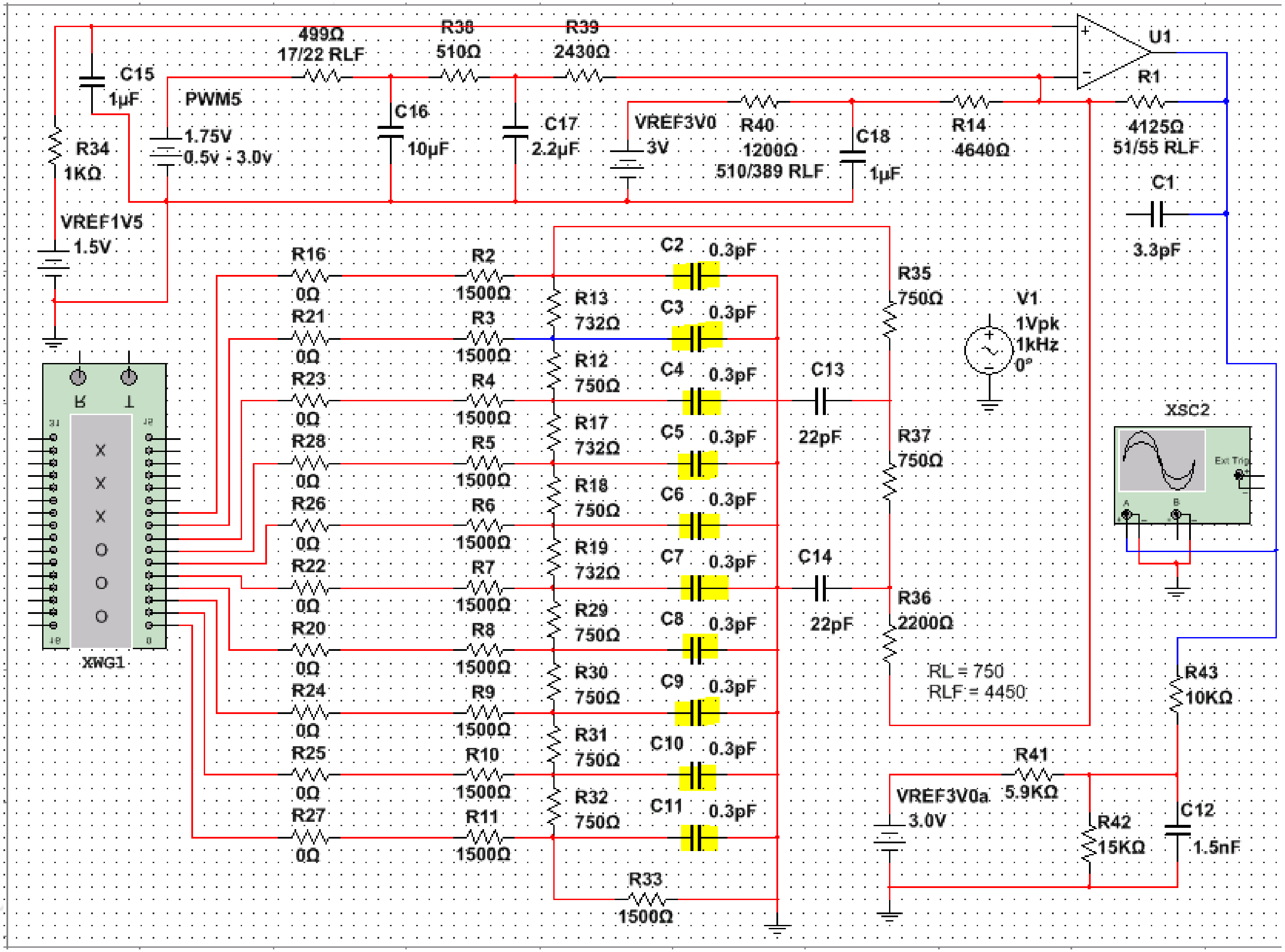
Accommodate Missing Codes



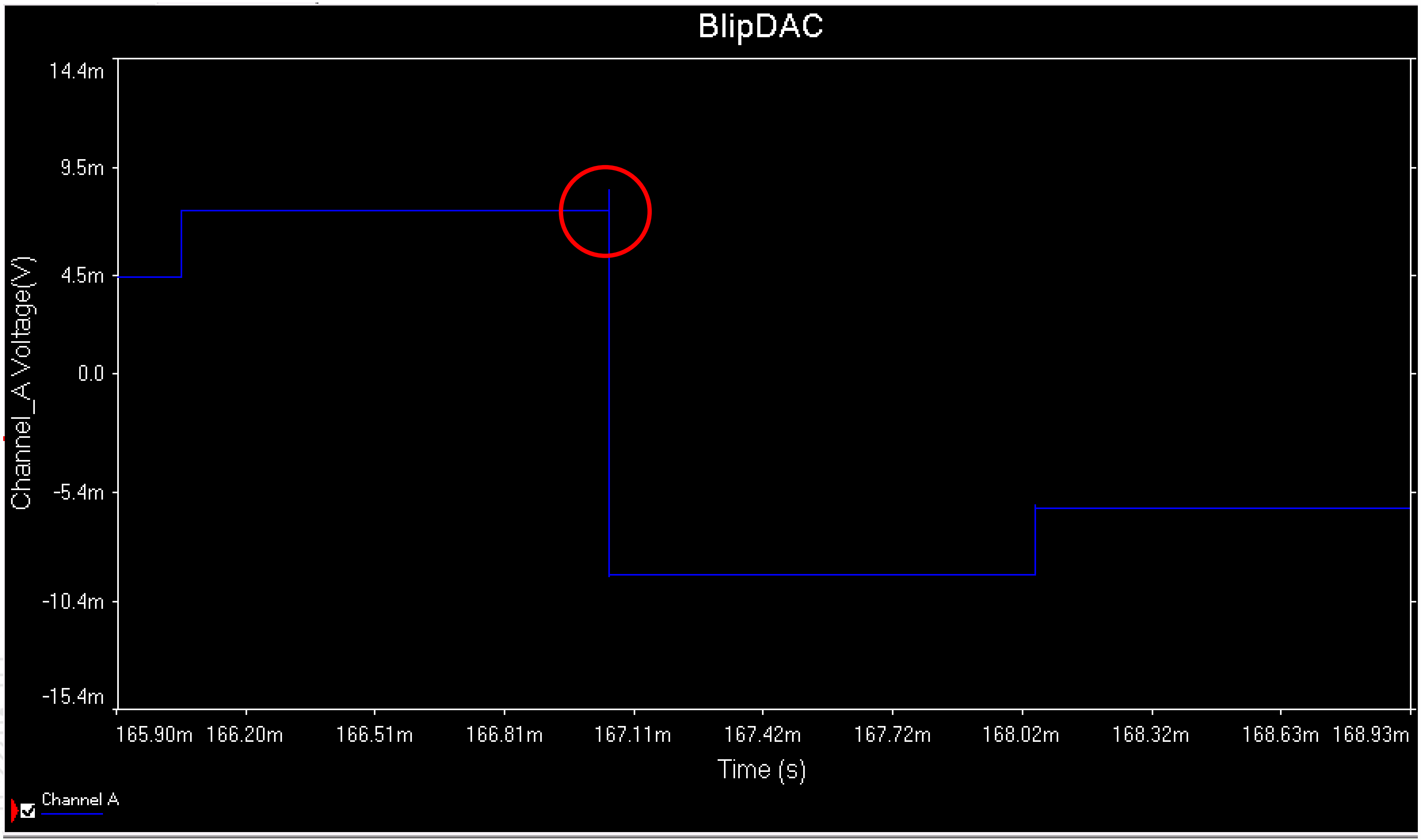


RLI=RL+R62+R63=4450
R66+R67=(510/389)(RLI)=5834
R57+R58+R59=(17/22)(RLI)=3439
R64=(10/11 RLI)+2%=(51/55)(RLI)=4126

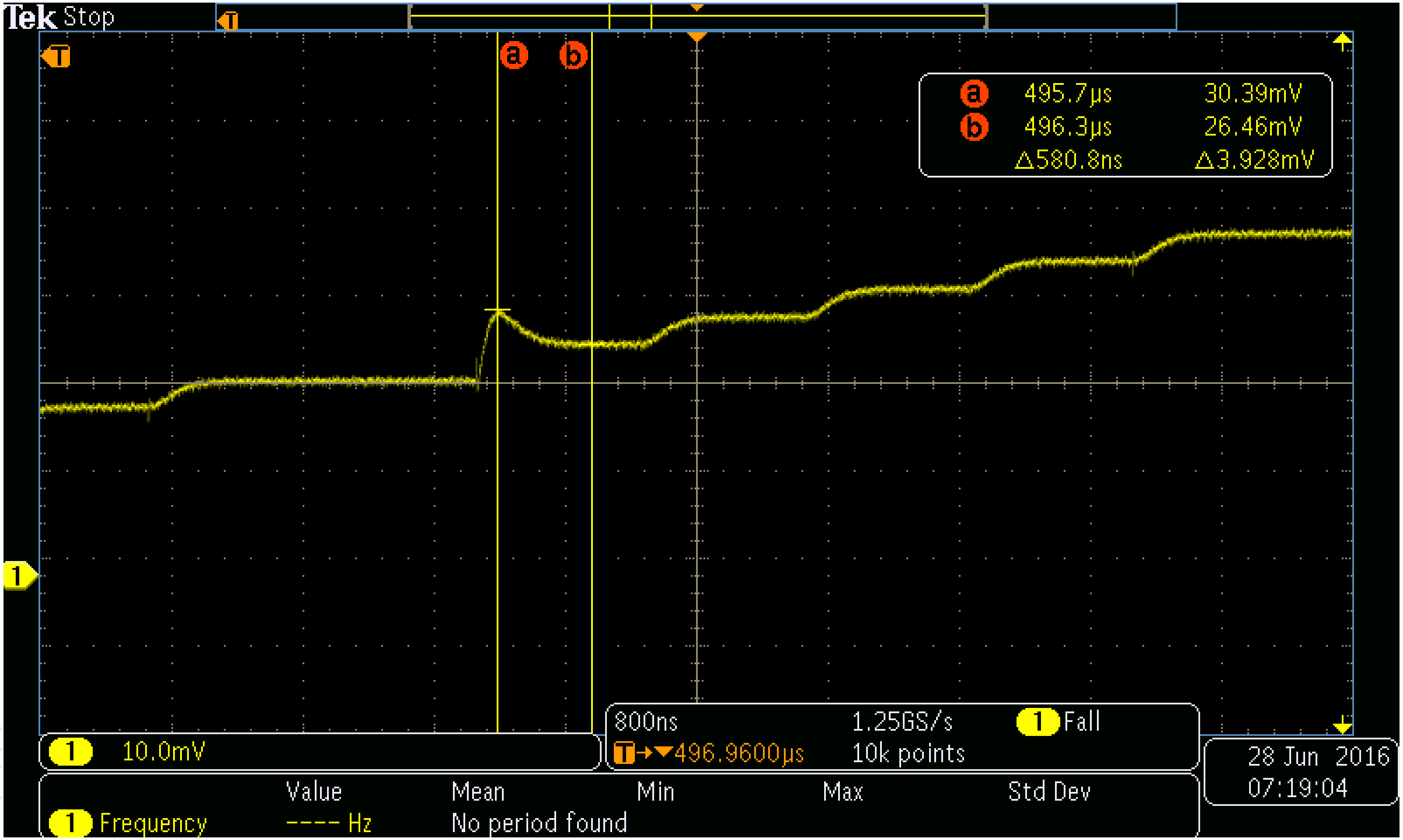
Transmission Delay in the R2R Ladder



Simulated Transmission Delay



Actual Transmission Delay

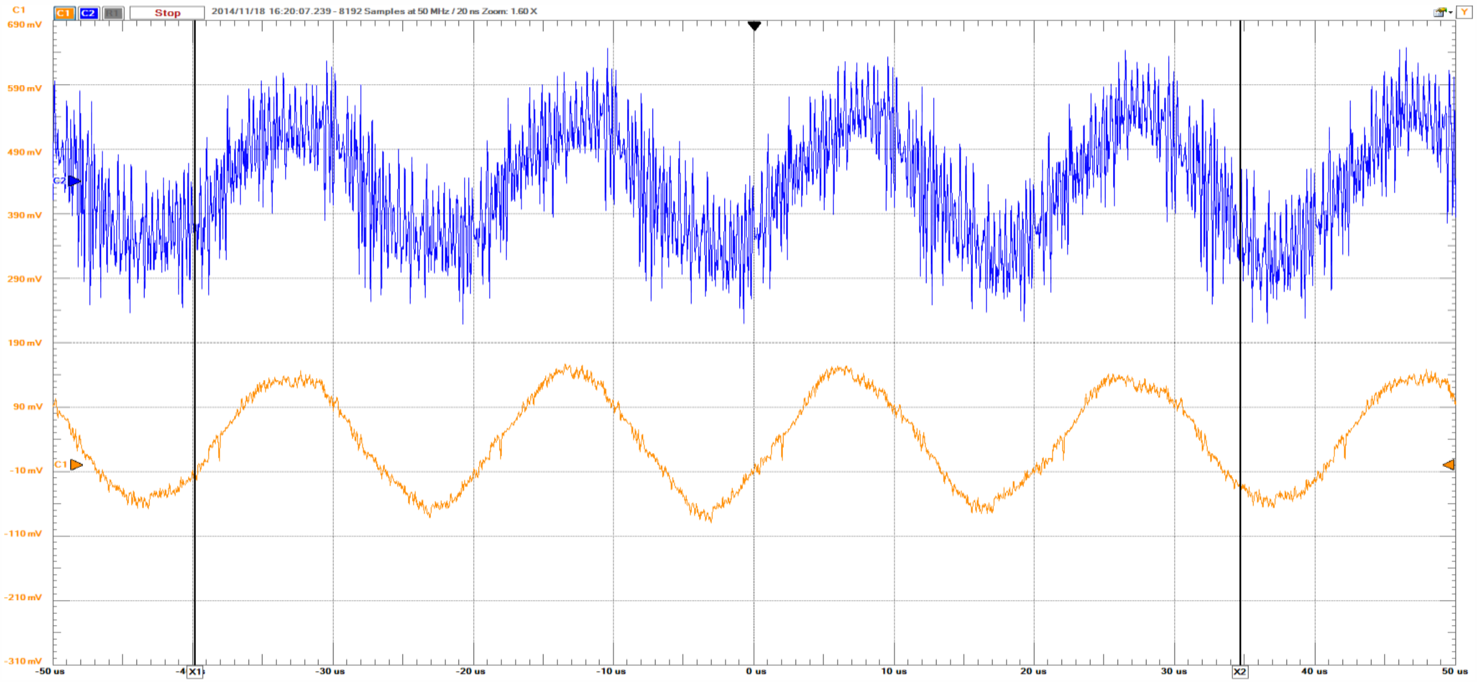


```
a   495.7µs    30.39mV
b   496.3µs    26.46mV
    Δ580.8ns   Δ3.928mV
```

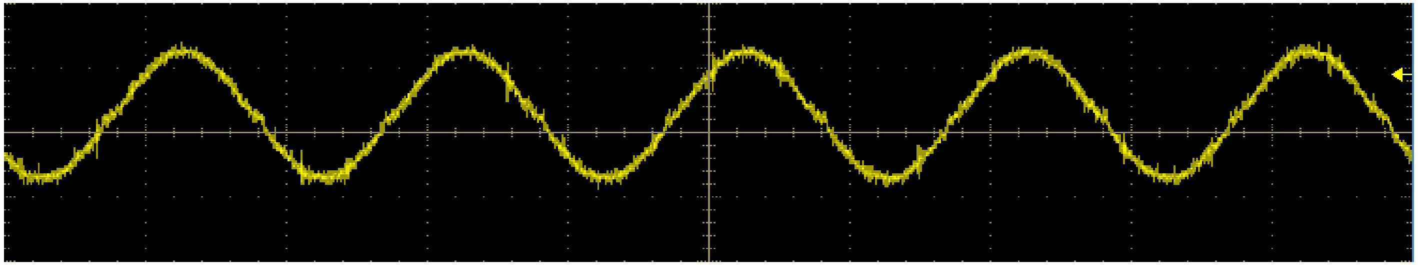
```
1  10.0mV      800ns                1.25GS/s     1 Fall
               T→▼496.9600µs        10k points
                                                         28 Jun 2016
                                                         07:19:04
                Value    Mean               Min    Max    Std Dev
1 Frequency     ---- Hz  No period found
```

Or you can buy a DAC

50kHz Sine, 200mVpk-pk, 100mV/div, (1000 unit pricing)
blue – DAC7822 ($4.28)
yellow – AD5405 ($6.62)



OpenScope R2R Ladder/MCP6H91 ($1.06)



Open Scope Agenda

- Open Scope Waveforms Live Demonstration
- Architecture
- Resource Allocation
- DC Outputs
- Precision Analysis
- Analog Inputs
- DMA Parallel Processing
- ADC Interleaving
- Logic Analyzer (LA)
- Scope Triggering
- Analog Waveform Generator (AWG)
- **Priority and Stalling Consequences**
- USB/Serial, UART Interface
- Open Scope Text Based Protocol
- Building the Sources

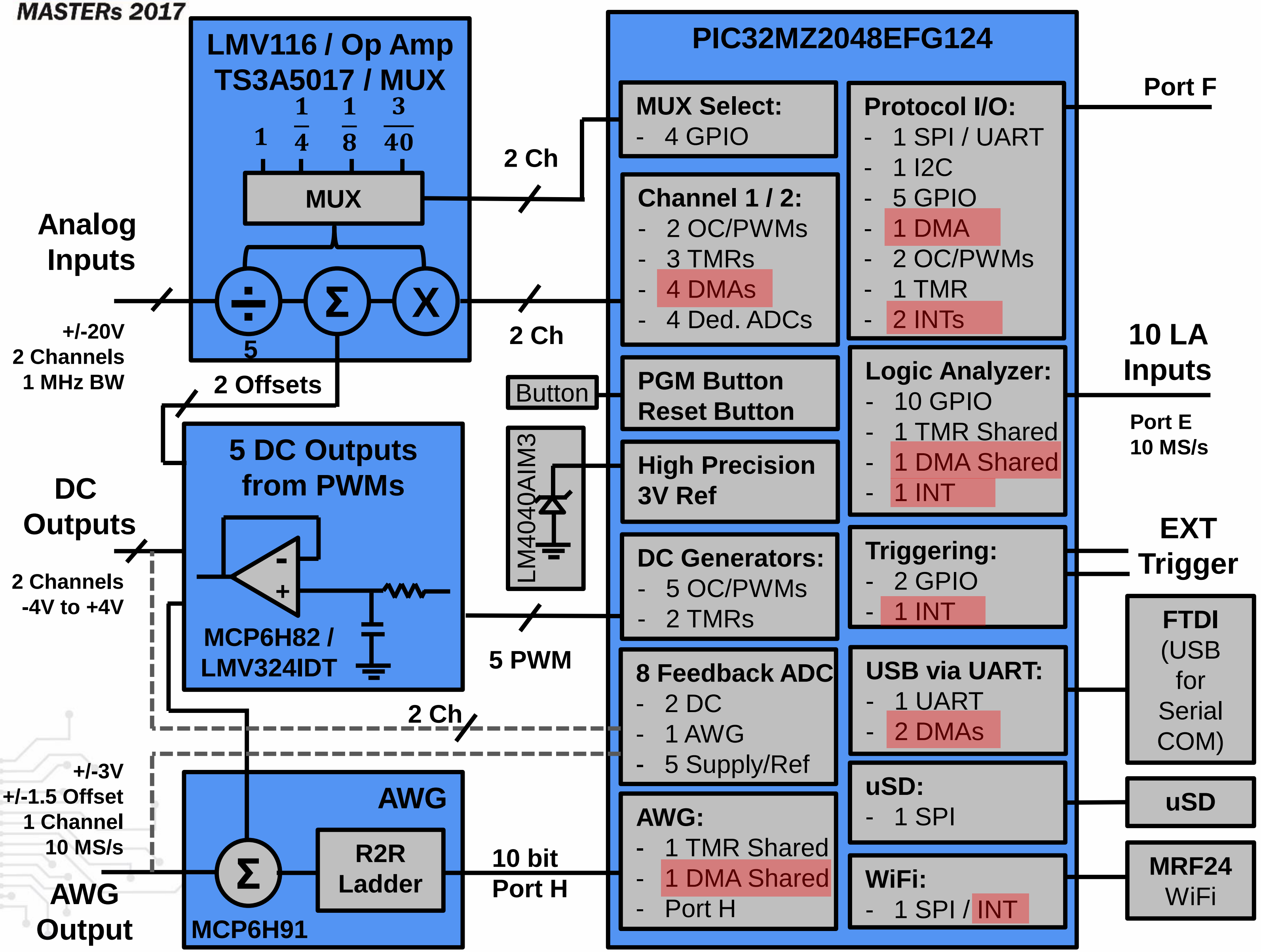
2017 MASTERs Conference

Priority and Stalling Consequences

15 Minute Break

MICROCHIP

Priority and Stalling



LMV116 / Op Amp
TS3A5017 / MUX

$1 \quad \frac{1}{4} \quad \frac{1}{8} \quad \frac{3}{40}$

MUX

÷ Σ X

5

Analog Inputs

+/-20V
2 Channels
1 MHz BW

2 Ch

2 Ch

2 Offsets

5 DC Outputs from PWMs

MCP6H82 /
LMV324IDT

DC Outputs

2 Channels
-4V to +4V

5 PWM

2 Ch

Button

LM4040AIM3

AWG

R2R Ladder

Σ

MCP6H91

+/-3V
+/-1.5 Offset
1 Channel
10 MS/s

AWG Output

10 bit
Port H

PIC32MZ2048EFG124

MUX Select:
- 4 GPIO

Channel 1 / 2:
- 2 OC/PWMs
- 3 TMRs
- 4 DMAs
- 4 Ded. ADCs

PGM Button
Reset Button

High Precision 3V Ref

DC Generators:
- 5 OC/PWMs
- 2 TMRs

8 Feedback ADC
- 2 DC
- 1 AWG
- 5 Supply/Ref

AWG:
- 1 TMR Shared
- 1 DMA Shared
- Port H

Protocol I/O:
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- 1 I2C
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10 LA Inputs

Port E
10 MS/s

EXT Trigger

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(USB for Serial COM)

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DMA Stalling

- Experimentally, maximum cell transfer top out at <15MTrig/s, and more like 10MTrig/s if multiple DMAs are in use. Cell transfer triggers are missed (not queued) if the trigger rate is exceeded.
- Only the highest priority DMA cell transfer will run at a time regardless of busses in use; all other DMAs will stall.
- Various system busses have different DMA speeds. IO Bus at 50MTran/s, RAM to RAM at 100MTran/s.
- A transfer is the cell size or 32bits, whichever is smaller.
- The current transfer will complete before a higher priority DMA will be allowed to run.

DMA Priority

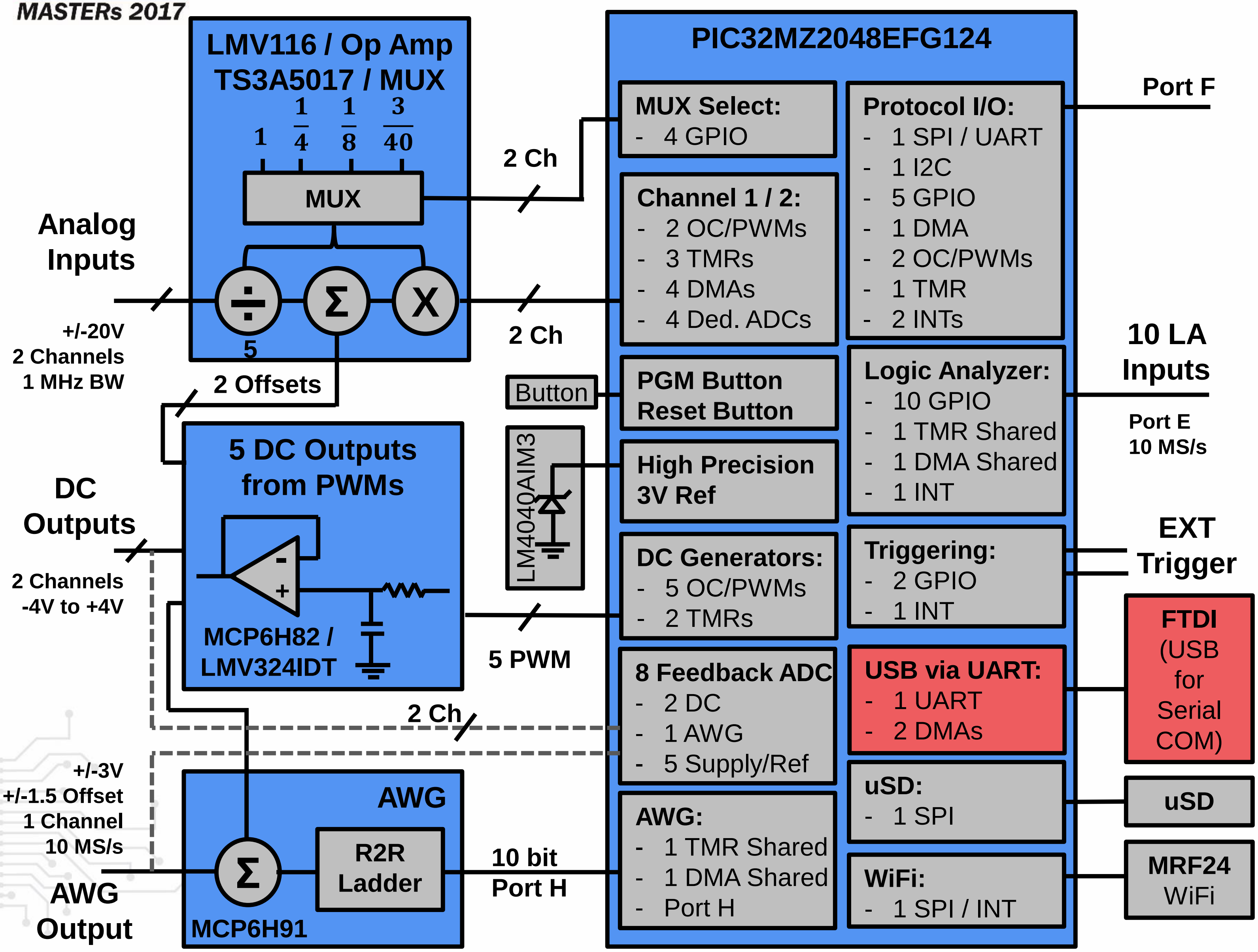
- **Top priority to the AWG & LA (10MT/s)**
  - In order to read (LA) or write (AWG) samples at extremely regular rates, the AWG/LA must not be stalled. Stalls cause distortions in the waveform.
  - Both the AWG and LA use the IO bus and have top priority, so they can not run at the same time, or one would stall the other.
- **Next priority to Analog-In (3.125MT/s)**
  - We have up to the conversion time, 320ns, for the DMA to transfer the ADC result to RAM.
- **UART has lowest priority (139kT/s)**
  - The UART has an 8 byte FIFO and runs at 139kTran/s. There is lots of time to keep up.

Interrupt Priorities

- **Minimal interrupts in the system**
  - Trigger Interrupts
    - Priority 7, Trace competition interrupt on TMR9.
    - Priority 6, Trigger detection interrupt
      - OSC, Digital Compare threshold INT.
      - LA, Change Notice INT.
    - Priority 5, OSC pre-threshold INT.
  - WiFi Interrupt
    - Priority 3, MRF24 WiFi Data Ready INT.

USB/Seral, UART Interface

USB / Serial Interface



LMV116 / Op Amp
TS3A5017 / MUX

$1 \quad \frac{1}{4} \quad \frac{1}{8} \quad \frac{3}{40}$

MUX

÷ Σ X

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Analog Inputs

+/-20V
2 Channels
1 MHz BW

2 Ch

2 Ch

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MCP6H82 /
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-4V to +4V

Button

LM4040AIM3

5 PWM

2 Ch

AWG

R2R Ladder

Σ

MCP6H91

+/-3V
+/-1.5 Offset
1 Channel
10 MS/s

AWG Output

10 bit
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PIC32MZ2048EFG124

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3V Ref

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Port E
10 MS/s

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(USB for Serial COM)

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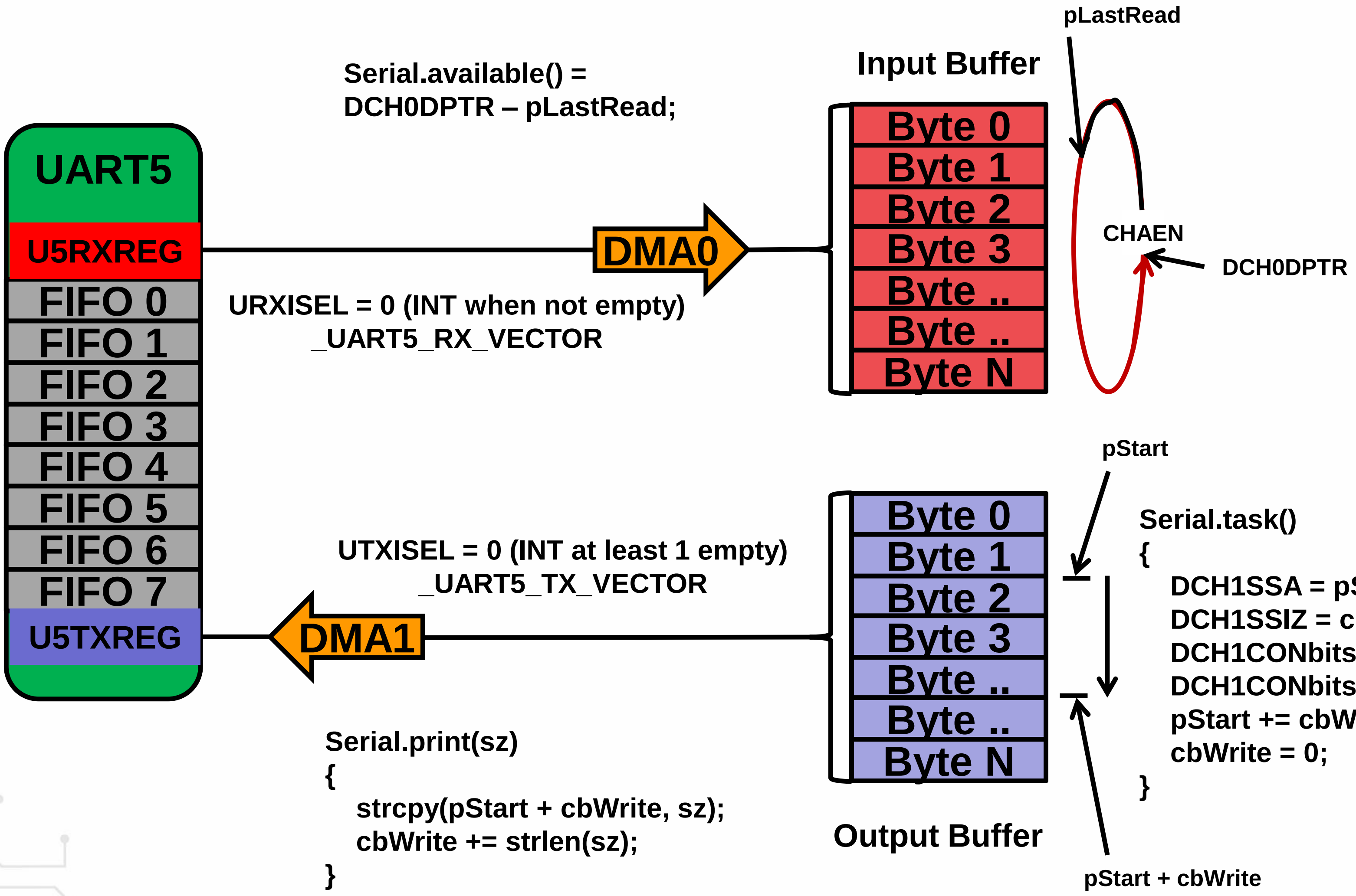
USB/Serial, UART Interface

- **FTDI FT232RQ USB/Serial Converter.**
  - Offloads the USB stack to the FTDI chip.
  - Runs at 1.25MBaud, 139kB/s.
  - Requires USB 2.0 High Speed or better.
  - Provides text communication via Terminal.
    - Menu Mode
    - JSON Mode
  - Negotiates 500mA on the USB bus.
  - Provides the board Serial Number during enumeration in Device Instance Path / Parent

DMA and the UART



```
Serial.available() =
DCH0DPTR – pLastRead;
```

URXISEL = 0 (INT when not empty)
_UART5_RX_VECTOR

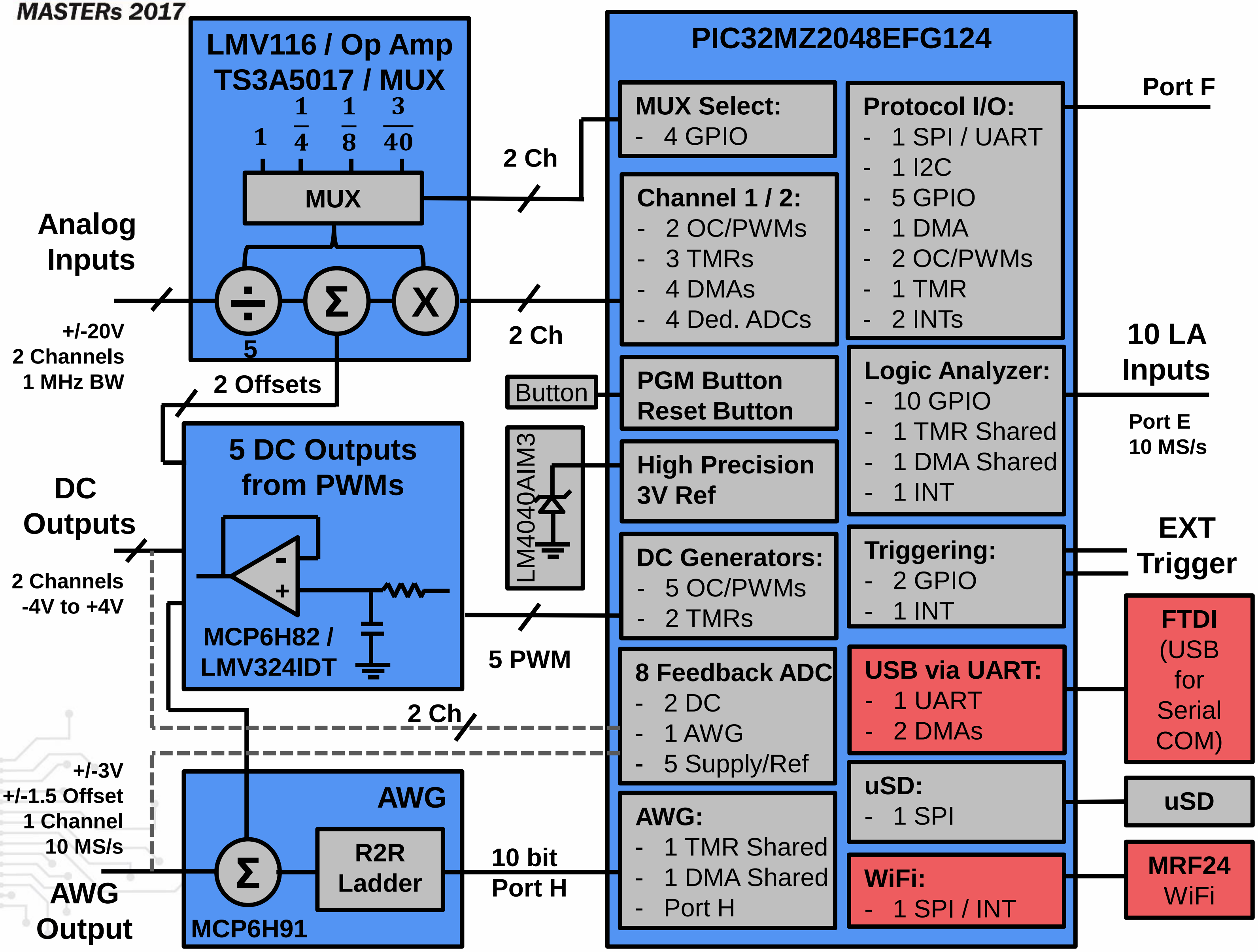
UTXISEL = 0 (INT at least 1 empty)
_UART5_TX_VECTOR

```
Serial.print(sz)
{
    strcpy(pStart + cbWrite, sz);
    cbWrite += strlen(sz);
}
```

```
Serial.task()
{
    DCH1SSA = pStart;
    DCH1SSIZ = cbWrite;
    DCH1CONbitsCHAEN = 0;
    DCH1CONbits.CHEN = 1;
    pStart += cbWrite;
    cbWrite = 0;
}
```

OpenScope Text Based Protocol

Text Based Protocol



Analog Inputs

+/-20V
2 Channels
1 MHz BW

LMV116 / Op Amp
TS3A5017 / MUX

1 $\frac{1}{4}$ $\frac{1}{8}$ $\frac{3}{40}$

MUX

÷ Σ X

5

2 Offsets

2 Ch

2 Ch

DC Outputs

2 Channels
-4V to +4V

5 DC Outputs from PWMs

MCP6H82 /
LMV324IDT

Button

LM4040AIM3

5 PWM

2 Ch

+/-3V
+/-1.5 Offset
1 Channel
10 MS/s

AWG Output

AWG

R2R Ladder

MCP6H91

10 bit
Port H

PIC32MZ2048EFG124

MUX Select:
- 4 GPIO

Channel 1 / 2:
- 2 OC/PWMs
- 3 TMRs
- 4 DMAs
- 4 Ded. ADCs

PGM Button
Reset Button

High Precision 3V Ref

DC Generators:
- 5 OC/PWMs
- 2 TMRs

8 Feedback ADC
- 2 DC
- 1 AWG
- 5 Supply/Ref

AWG:
- 1 TMR Shared
- 1 DMA Shared
- Port H

Protocol I/O:
- 1 SPI / UART
- 1 I2C
- 5 GPIO
- 1 DMA
- 2 OC/PWMs
- 1 TMR
- 2 INTs

Logic Analyzer:
- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

Triggering:
- 2 GPIO
- 1 INT

USB via UART:
- 1 UART
- 2 DMAs

uSD:
- 1 SPI

WiFi:
- 1 SPI / INT

Port F

10 LA Inputs

Port E
10 MS/s

EXT Trigger

FTDI
(USB for Serial COM)

uSD

MRF24
WiFi

PIC32 Resource Usage Summary Table

PWM / OC	9 of 9
Timers	7 of 9
INTs	5 of 5
SPI	3 of 6
UART	2 of 6
I2C	1 of 5
DMAs	9 of 8
Dedicated ADCs	4 of 5
Shared ADCs	8 of 43
Digital Compare	2 of 6
Digital Filters	1 of 6

Text Based Protocol

- **Serial and Web Based JSON Commands**
  - Comprehensive JSON/text command set
  - HTTP/HTML Post interface
    - JSON command set in body of Post
  - Serial/COM interface
    - Identical JSON command set sent as serial text.
- **Serial based Debug Prints**
  - Informative debug prints for manual observation of operation.
- **Serial based Menus**
  - Primarily used for early development; later replaced by the JSON commands.

Example JSON Command

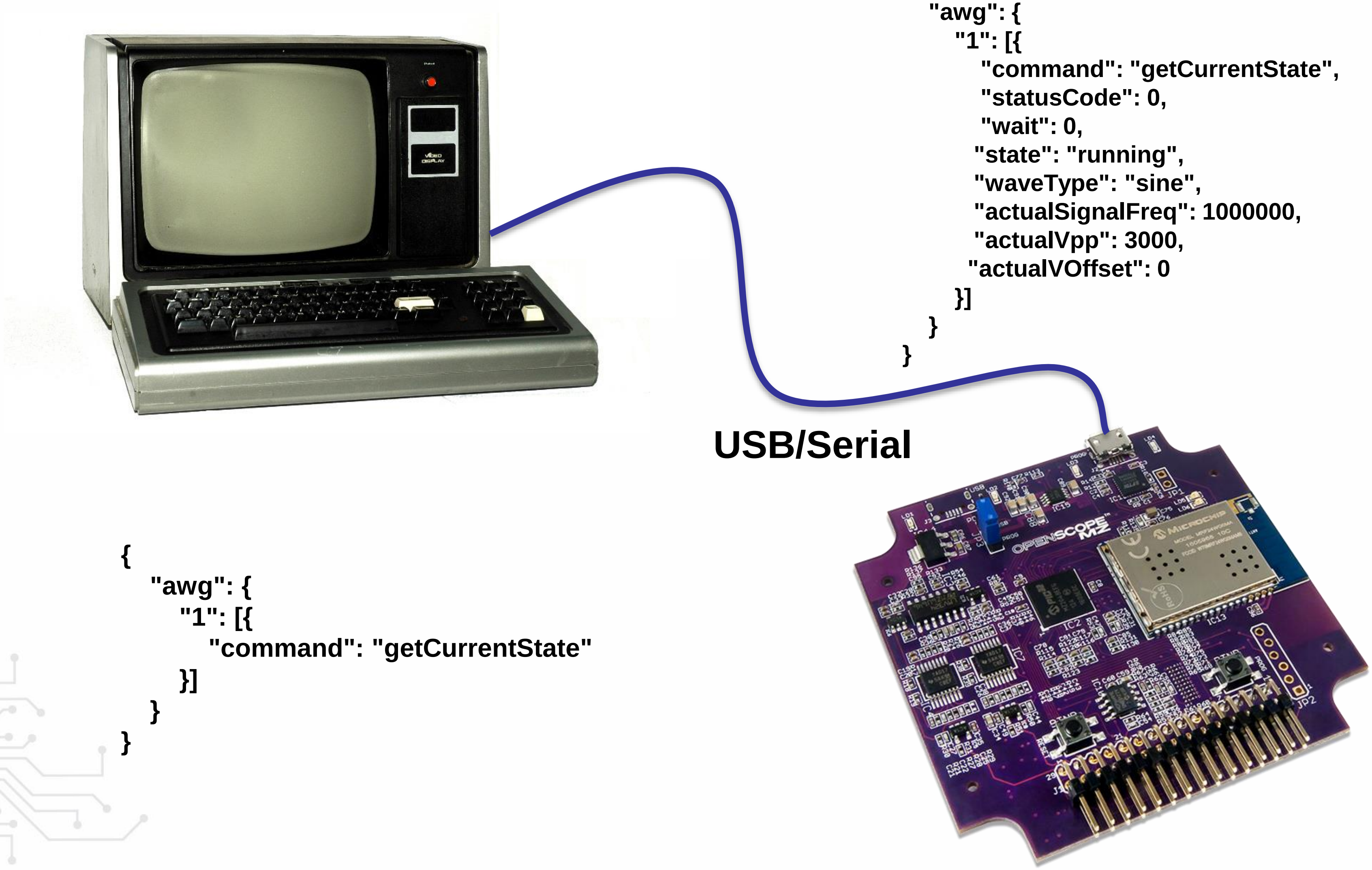
Command:

```
{"awg": {"1": [{"command": "getCurrentState"}]}}
```

Response:

```
{
        "awg": {
                "1": [{
                        "command": "getCurrentState",
                        "statusCode": 0,
                        "wait": 0,
                        "state": "running",
                        "waveType": "sine",
                        "actualSignalFreq": 1000000,
                        "actualVpp": 3000,
                        "actualVOffset": 0
                }]
        }
}
```

Terminal/JSON/Command Demo



```
{
    "awg": {
        "1": [{
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            "statusCode": 0,
            "wait": 0,
          "state": "running",
          "waveType": "sine",
          "actualSignalFreq": 1000000,
          "actualVpp": 3000,
        "actualVOffset": 0
        }]
    }
}
```
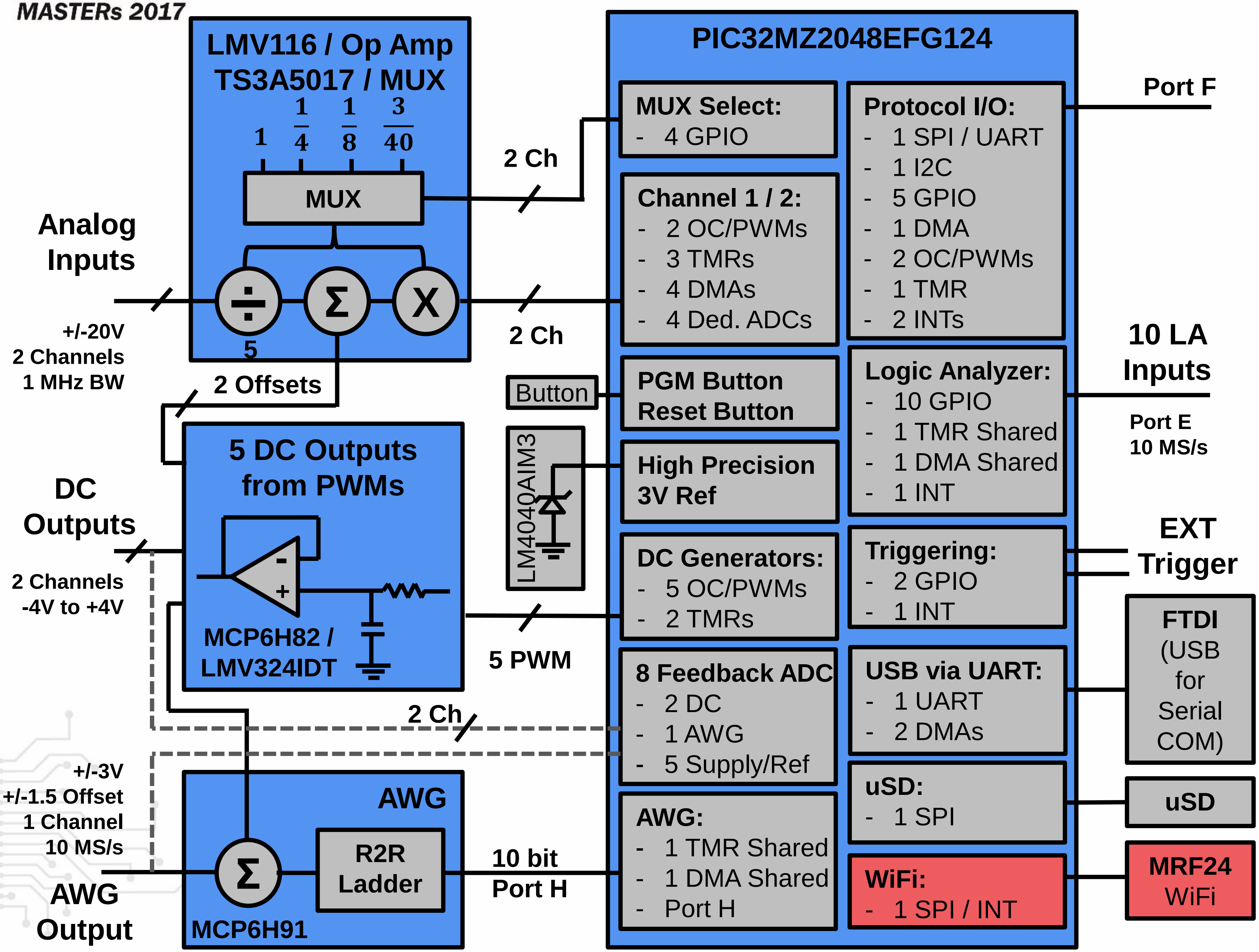

USB/Serial

```
{
    "awg": {
        "1": [{
            "command": "getCurrentState"
        }]
    }
}
```

OpenScope HTTP Interface

HTTP Interface



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- 10 GPIO
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- 1 DMA Shared
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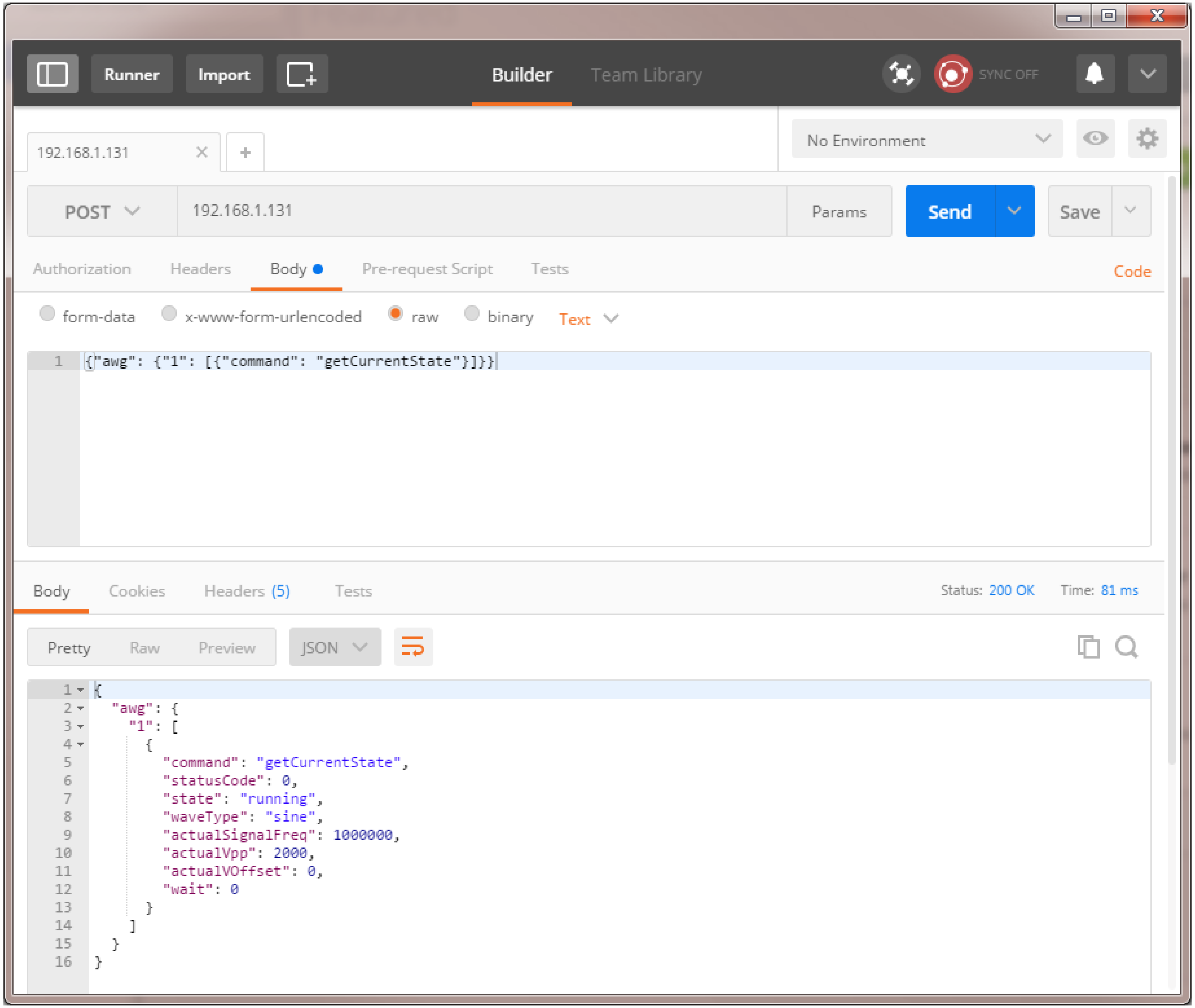
HTTP Server and Network Stack

- **The OpenScope implements a simple HTTP Server.**
  - Presented in the 2014 18020 EWN MASTERs class.
  - Supports static web content stored on the uSD card.
  - Supports dynamic content implemented in code.
  - Runs on the Digilent deIP™ Network Stack.
  - Provides the web based interface to the OpenScope.

Postman Web Demo



POST 192.168.1.131

Body: ○ form-data ○ x-www-form-urlencoded ● raw ○ binary Text

```
{"awg": {"1": [{"command": "getCurrentState"}]}}
```

Body | Cookies | Headers (5) | Tests — Status: 200 OK Time: 81 ms

Pretty | JSON

```
{
  "awg": {
    "1": [
      {
        "command": "getCurrentState",
        "statusCode": 0,
        "state": "running",
        "waveType": "sine",
        "actualSignalFreq": 1000000,
        "actualVpp": 2000,
        "actualVOffset": 0,
        "wait": 0
      }
    ]
  }
}
```

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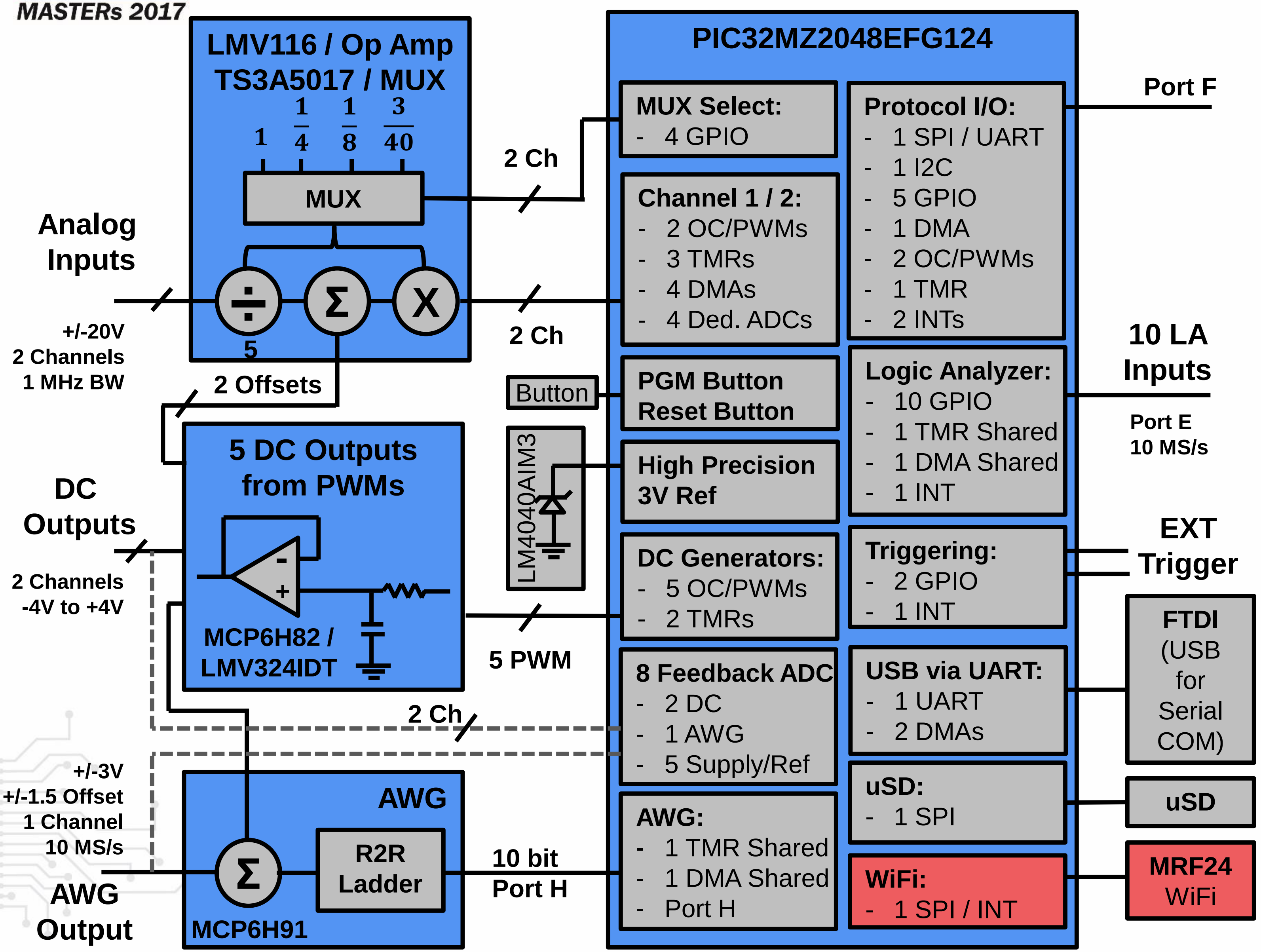
Connectivity, WiFi, Hotspots, and Isolation

MICROCHIP

WiFi, Hotspots, and Isolation



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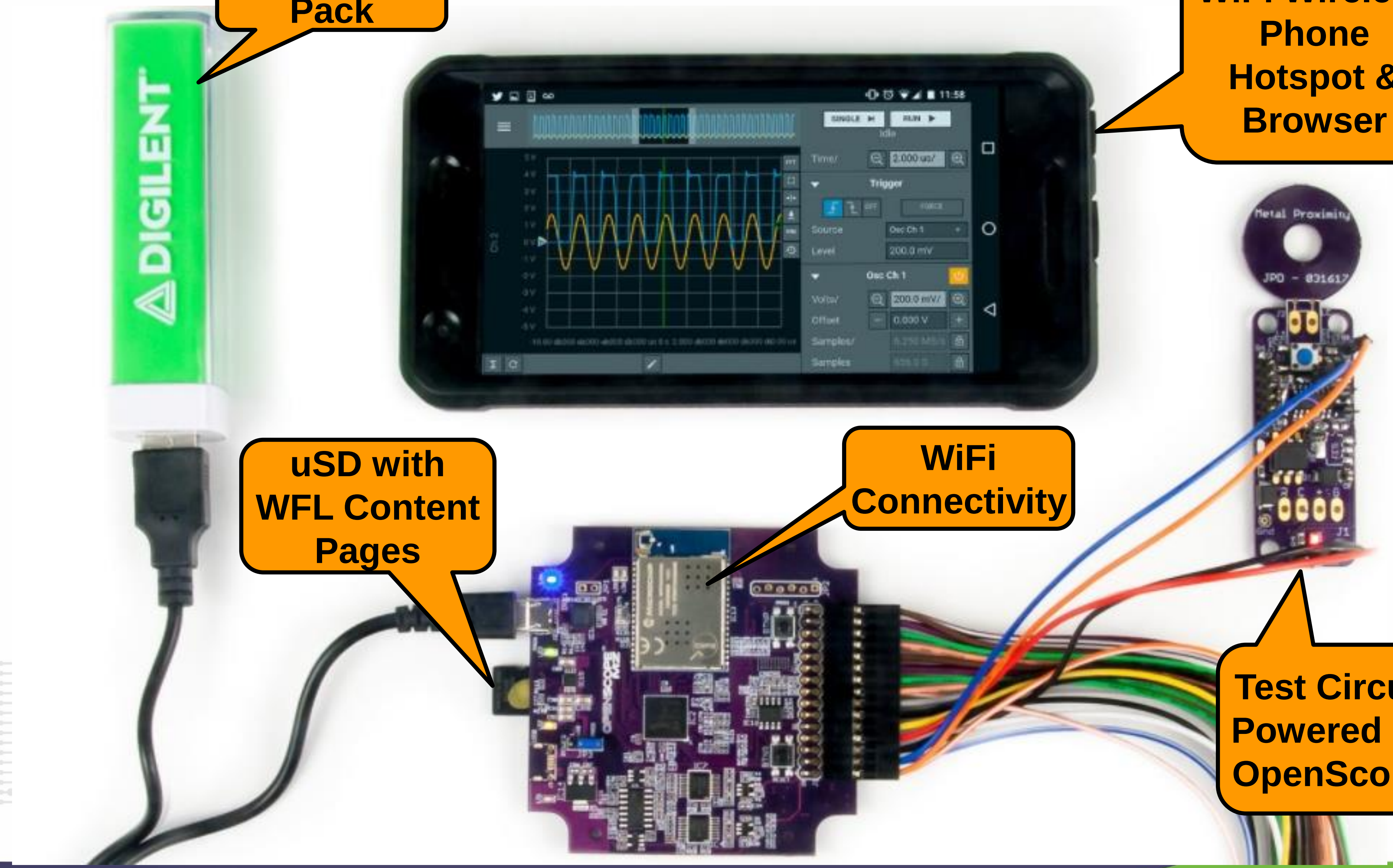
Connecting to WFL

- **http://waveformslive.com**
  - Downloads WFL off of the Digilent Servers
- **http://<OpenScope IP>**
  - Directs to the OpenScope for content.
  - Returns a redirect to http://waveformslive.com
    - The redirect page is stored in flash, there is no need for an uSD card to be present.
    - If the redirect fails, WFL will be served up from the OpenScope uSD, if present.
- **http://<OpenScope IP>/index.html**
  - Forces downloading WFL from the OpenScopes uSD card, if present.

WiFi, Hotspot, and Isolation

- **The OpenScope can serve-up WFL.**
  - If WFL is stored on the OpenScope's uSD card.
- **WFL works on most Phone Browsers.**
  - Your phone can be WFL's UI.
- **The OpenScope can connect to your phone's Hot Spot for local connectivity.**
  - World Wide Internet access is not needed.
- **Complete electrical isolation when powering the OpenScope off of a USB battery.**
  - Use your OpenScope on a deserted island.

Stand-a-lone Operation



USB Battery Pack

WiFi Wireless Phone Hotspot & Browser

uSD with WFL Content Pages

WiFi Connectivity

Test Circuit Powered by OpenScope

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Open Source Hardware and Software

MICROCHIP

The OpenScope is Open Source

- **Firmware is fully open source.**
  - Source is free and available on request.
  - All firmware is under MIT or BSD2.
  - There is no GPL/LGPL or other infectious licenses in the firmware.
  - Code can be used for commercial applications without the requirement to source 3rd party proprietary code. Attribution is required.
- **Complete Schematics are available.**
  - Schematics are posted on our product page.
  - Hardware design is under creative commons.
  - Project/Gerber files are not available.

MPLAB® X IDE Build Environment

MPLAB® X IDE project

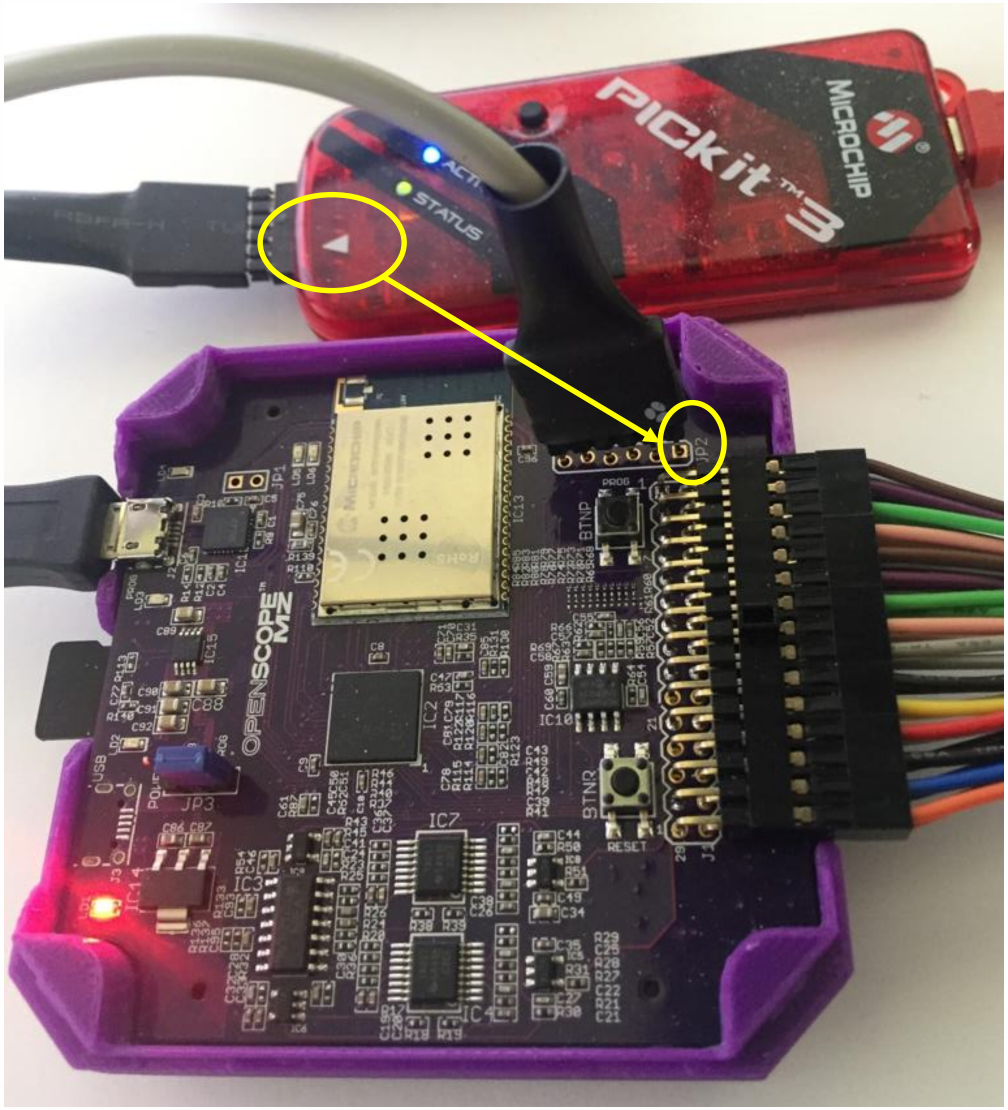
- **The OpenScope builds as a Native MPLAB® X IDE Project.**
  - In MPLAB® X IDE, Open the OpenScope.X project in the OpenScope directory.
  - If you added the OpenScope directory to your Arduino IDE Sketchbook, you can open the X project directly from the OpenScope directory.
- **Install MPLAB® XC32 1.43 compiler.**
  - Install MPLAB® XC32 1.43 or newer (free) compiler and assign that compiler to the project.
  - Or use the MPLAB® XC32 1.43 compiler that installed with the Digilent Arduino Core.

MPLAB® X IDE Considerations

- **When you program from MPLAB® X IDE, all flash is erased.**
  - You will lose calibration and WiFi information stored in flash. You will have to recalibrate and re-add WiFi information.
    - If you use a uSD card, you can save your calibration and WiFi data to the uSD card and you will not have to restore these each time you program. However, your WiFi passphrase will be easily accessible/readable on the uSD card.
  - The project programs the OpenScope's bootloader so you will not lose the bootloader.

Hardware Programmer

When plugging in the hardware programmer, make sure pin 1 of the programmer, lines up with the square pin on the ICSP connector, JP2.



Arduino IDE
Build Environment

Building with the Arduino IDE

- **Install the Arduino IDE 1.6.9**
  - Newer versions of the IDE may not work.
    - When Arduino.cc and Arduino.org remerged their IDEs, the IDE regressed and does not build subdirectories properly.
- **Install the Digilent Arduino Core**
  - In the Arduino IDE Preferences->Additional Board Managers URLs add:
    - https://s3-us-west-2.amazonaws.com/digilent/Software/Digilent_Core/package_digilent_index.json
  - In the Arduino IDE Tools->Board->Boards Manager
    - Install the Digilent Core

Arduino IDE Considerations

- **The OpenScope uses nothing from the Digilent core, almost!**
  - The OpenScope sketch is stand-a-lone, nothing from the core is brought in, except, crti.S.
    - When building from MPLAB® X IDE, X provides this file. The Digilent Core, and X provided crti.S are functionally equivalent.
    - Unfortunately, the core is still compiled.
  - OpenScope.ino has no code in it.
    - However, Arduino always compiles the sketch's .ino file; it still must compile for the OpenScope.
    - The .ino file implicitly includes Arduino.h; however, this contributes nothing to the code.

MPLAB® XC32 Considerations

- **Both the Digilent Arduino toolchain and MPLAB® X IDE toolchain use the official Microchip MPLAB® XC32 compiler.**
  - Unlike the chipKIT core that uses a special chipKIT compiler, the Digilent core uses the same MPLAB® XC32 compiler as MPLAB® X IDE native builds.
  - The MPLAB® XC32 compiler is used with the –mnewlib-libc option to force the usage of the open source newlib runtime libraries.
  - By default the OpenScope is compiled without optimizations, so the “free” MPLAB® XC32 is used.
  - Both X/Arduino builds generate substantially the same code. (build order and placement may vary).

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Resource Links

OpenScope Resource Links

- Digilent: www.digilent.com
- Microchip: www.microchip.com
- Arduino: www.Arduino.cc
- General OpenScope Documentation: https://reference.digilentinc.com/reference/instrumentation/openscope-mz/start

- **OpenScope Firmware:** https://reference.digilentinc.com/reference/instrumentation/openscope-mz/previous-versions

OpenScope Resource Links

- Firmware Source: https://github.com/Digilent/openscope-mz
- Waveformslive Browser Page: https://www.waveformslive.com
- Waveformslive Documentation: https://reference.digilentinc.com/reference/software/waveforms-live/start
- Digilent Agent: https://reference.digilentinc.com/reference/software/digilent-agent/start
- PIC32MZ: http://www.microchip.com/wwwproducts/en/PIC32MZ2048EFG124

OpenScope Resource Links

- MPLAB® X IDE (3.60 or newer): http://www.microchip.com/mplab/mplab-x-ide
- XC32 Compiler (1.43 or newer): http://www.microchip.com/mplab/compilers
- Arduino IDEs (1.6.9) https://www.arduino.cc/en/Main/OldSoftwareReleases#previous
- Digilent Arduino Core https://s3-us-west-2.amazonaws.com/digilent/Software/Digilent_Core/package_digilent_index.json

Open Scope Summary

- Open Scope Waveforms Live Demonstration
- Architecture
- Resource Allocation
- DC Outputs
- Precision Analysis
- Analog Inputs
- DMA Parallel Processing
- ADC Interleaving
- Logic Analyzer (LA)
- Scope Triggering
- Analog Waveform Generator (AWG)
- Priority and Stalling Consequences
- USB/Serial, UART Interface
- Open Scope Text Based Protocol
- Building the Sources

Hope you enjoyed our class..

OPENSCOPE
MZ

OpenScope™

Appendix

Waveformslive Brower Based User Interface

Waveformslive (WFL) Browser Based UI

- **Written using:**
  - TypeScript, strict superset of JavaScript.
  - Uses the Flot Graphics Package.
  - Ionic 2, built on Angular 2 and utilizes Apache Cordova.
  - Cordova supports the creation of native applications to Android, iOS, Windows, and more.
- **Targets PCs, Tablets, and Phones.**
- **Runs on most Browsers**
  - Chrome, Edge, Firefox, Safari

WFL Communications

- **HTTP Posts with an HTML body containing OpenScope JSON commands.**
- **Binary data is transferred using the HTTP Chunked Transfer Encoding.**
- **Communicates to the Digilent Agent in an identical manner as the OpenScope; with HTTP Post messages.**
  - The Digilent Agent supports a config URL where HTTP Posts with Digilent Agent specific JSON commands can be interpreted.

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Digilent Agent

Digilent Agent (DA)

- **A local HTTP server forwarding OpenScope commands over the USB/Serial/COM interface.**
  - Same HTTP protocol as the OpenScope.
  - Written in QT for cross-platform support.
    - Runs on Windows, MAC, and Linux
- **Started out as the OpenScope Configuration Utility to configure WiFi and calibration.**
  - Configuration commands were designed as OpenScope JSON commands.
  - The DA can forward on any and all WFL commands enabling USB/Serial connectivity to the OpenScope.

Digilent Agent, Not Just for the OpenScope; Looking Forward

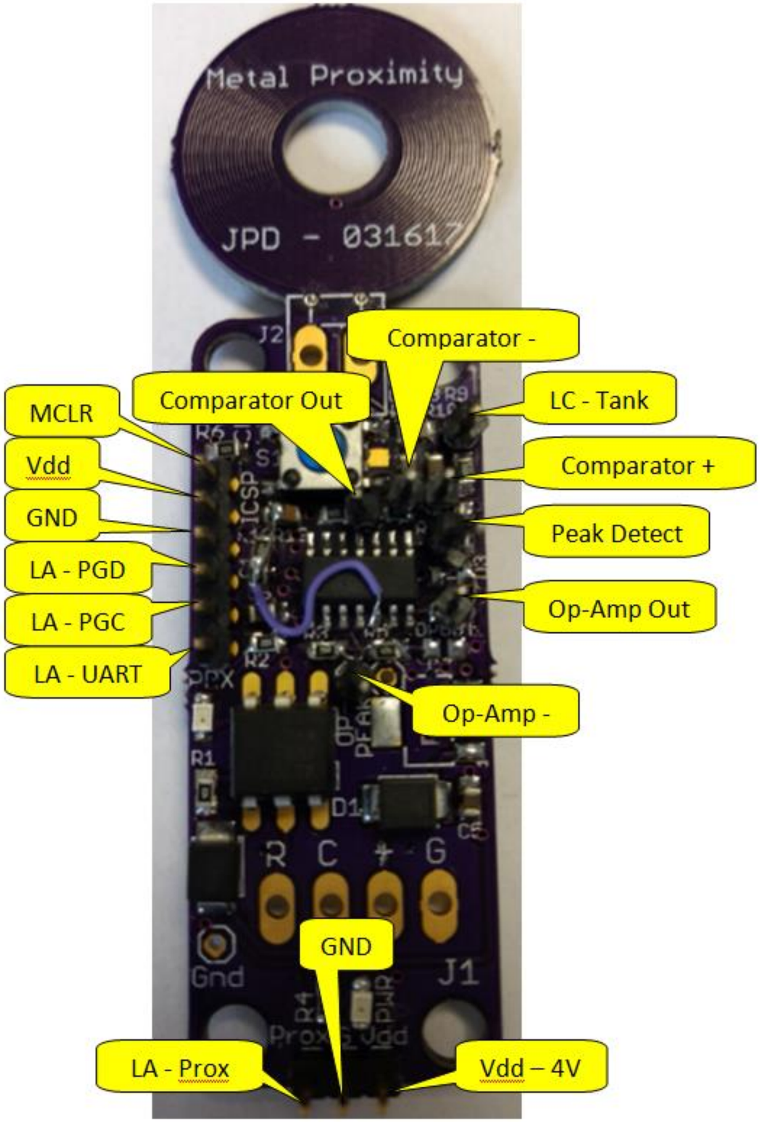
- **The DA can convert to other interfaces and protocols.**
  - The JSON command set is generic to instrumentation, not specific to the OpenScope
  - The JSON commands can be translated into Analog Discovery commands and connected to the Analog Descovery via its native Adept protocol.
- **WFL can be developed as a generic instrumentation Browser Based UI for many instruments**
- **LabVIEW can connect to the DA and communication easily to the AD2 and/or OpenScope.**

Enabling WiFi/Internet Connectivity with the DA

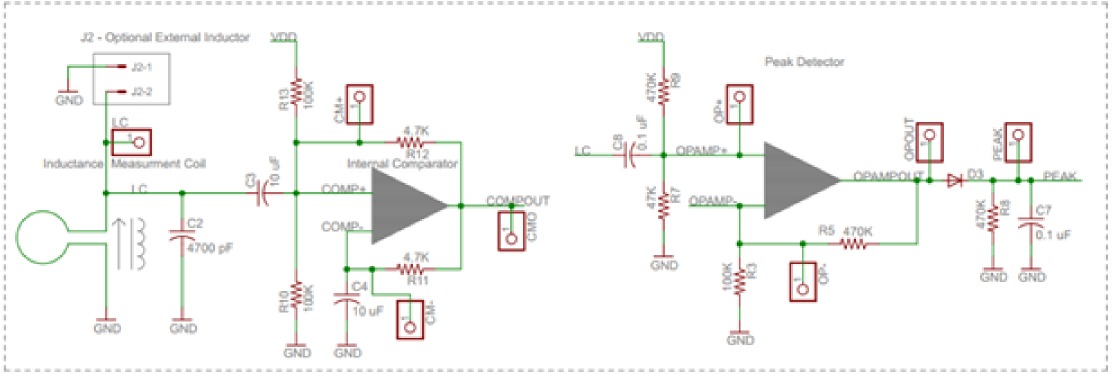
- **The DA runs as an HTTP server on the PC.**
  - The PC is connected to the internet.
  - Anything that is connected to the internet can communicate to the DA.
  - Could make a less expensive OpenScope with no WiFi module and still talk WiFi to it through a DA. Also could enable WiFi access to the AD2.
- **WFL is a Web Based Application**
  - It is connected to the internet and can communicate with any or many DAs on the internet.
  - Could support multiple instruments over a range of PCs. This could be useful for data collection over a widely distributed instrumentation network.

LC Tank Examples

LC Tank Board Test Points

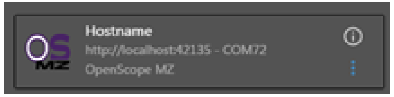


LC Tank Schematic and Setup



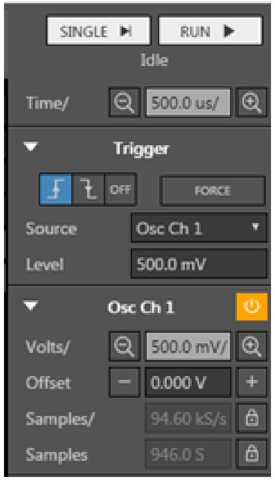
Demo Procedure:

- Type www.waveformslive.com and connect to OpenScope via Digilent Agent to start GUI:

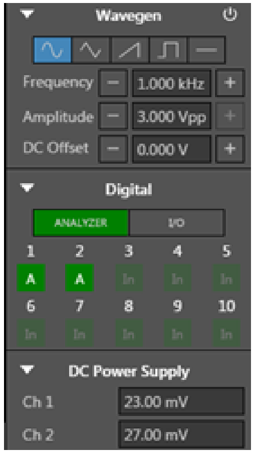


Hostname
http://localhost:42135 - COM72
OpenScope MZ

- Review instruments (time base, trigger, OSC1/2, Wavegen, Digital Logic Analyzer, DC Power)



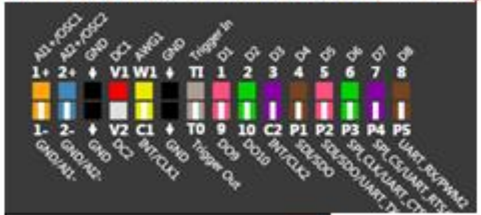
SINGLE RUN
Idle
Time/ 500.0 us/
Trigger
FORCE
Source Osc Ch 1
Level 500.0 mV
Osc Ch 1
Volts/ 500.0 mV/
Offset 0.000 V
Samples/ 94.60 kS/s
Samples 946.0 S

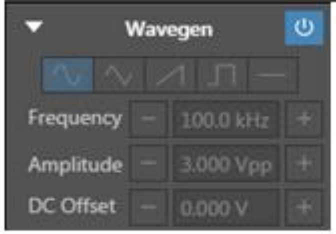


Wavegen
Frequency 1.000 kHz
Amplitude 3.000 Vpp
DC Offset 0.000 V
Digital
ANALYZER I/O
1 2 3 4 5
A A In In In
6 7 8 9 10
In In In In In
DC Power Supply
Ch 1 23.00 mV
Ch 2 27.00 mV

Waveform Generator Demo

- Connect AWG to OSC1, set AWG to 100 Khz, 3V P-P, sine Wave





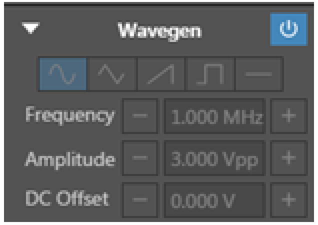
Wavegen

Frequency 100.0 kHz

Amplitude 3.000 Vpp

DC Offset 0.000 V

- Increase frequency to 1 Mhz



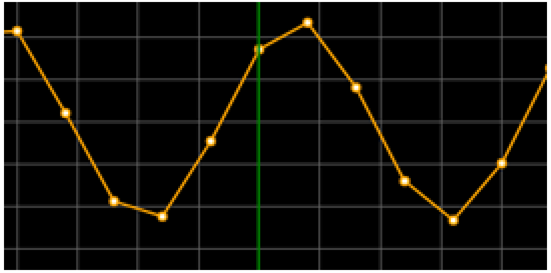
Wavegen

Frequency 1.000 MHz

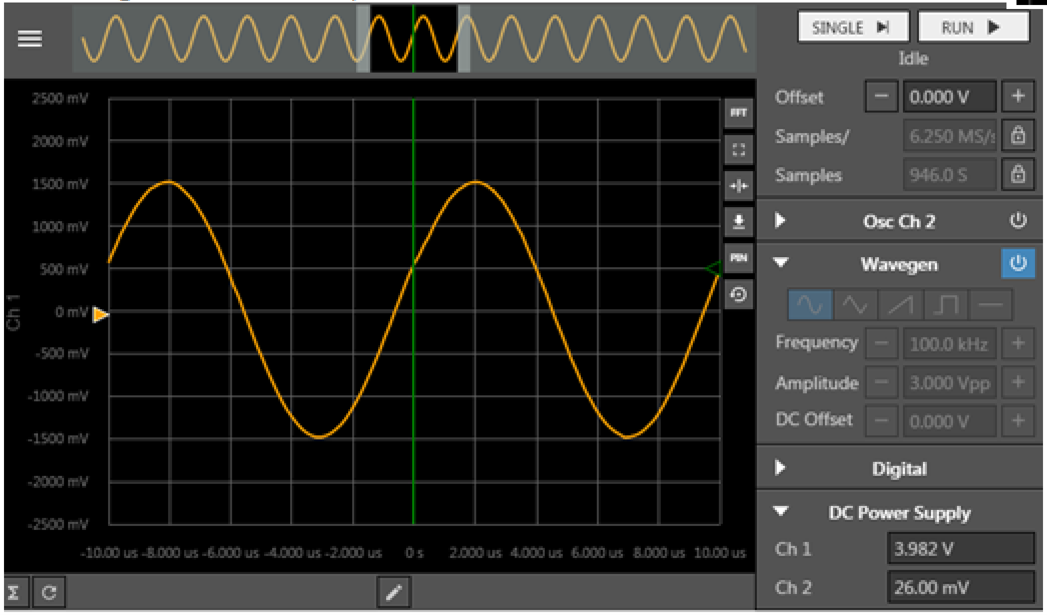
Amplitude 3.000 Vpp

DC Offset 0.000 V

- Observe ~6 sample points per cycle (1 Mhz input, 6.25 Ms/S)



- Press "Single" and observe captured waveforms on OSC1



Offset 0.000 V

Samples/ 6.250 MS/s

Samples 946.0 S

Osc Ch 2

Wavegen

Frequency 100.0 kHz

Amplitude 3.000 Vpp

DC Offset 0.000 V

Digital

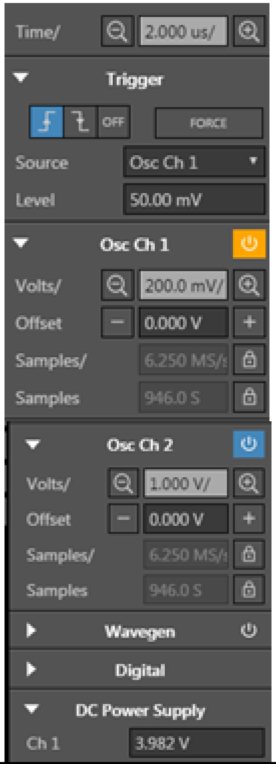
DC Power Supply

Ch 1 3.982 V

Ch 2 26.00 mV

Oscilloscope and FFT Demo

- Connect Power, Ground and OSC1 to LC, OSC2 to Comparator output
- Disable waveform generator
- Set OSC1 to 200 mV
- Set OSC2 to 1V
- Set time base to 2 uS/Division



Time/ 2.000 us/

Trigger

FORCE

Source: Osc Ch 1

Level: 50.00 mV

Osc Ch 1

Volts/ 200.0 mV/

Offset: 0.000 V

Samples/ 6.250 MS/s

Samples: 946.0 S

Osc Ch 2

Volts/ 1.000 V/

Offset: 0.000 V

Samples/ 6.250 MS/s

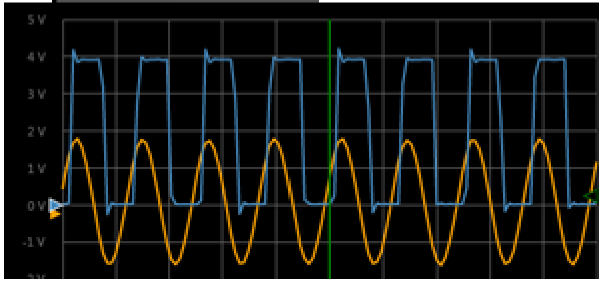
Samples: 946.0 S

Wavegen

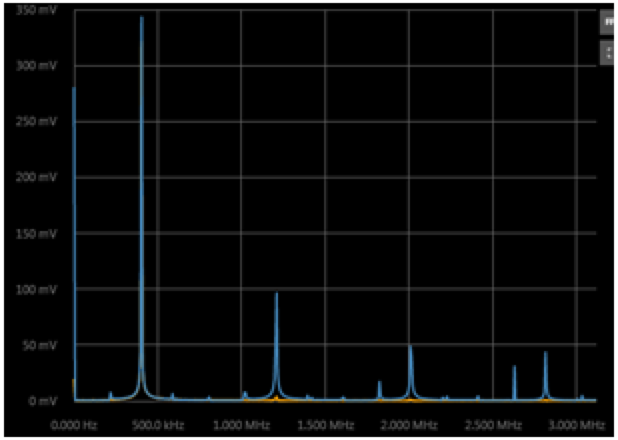
Digital

DC Power Supply

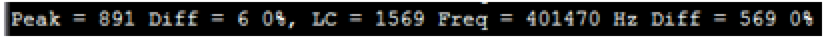
Ch 1: 3.982 V



- Observe FFT:



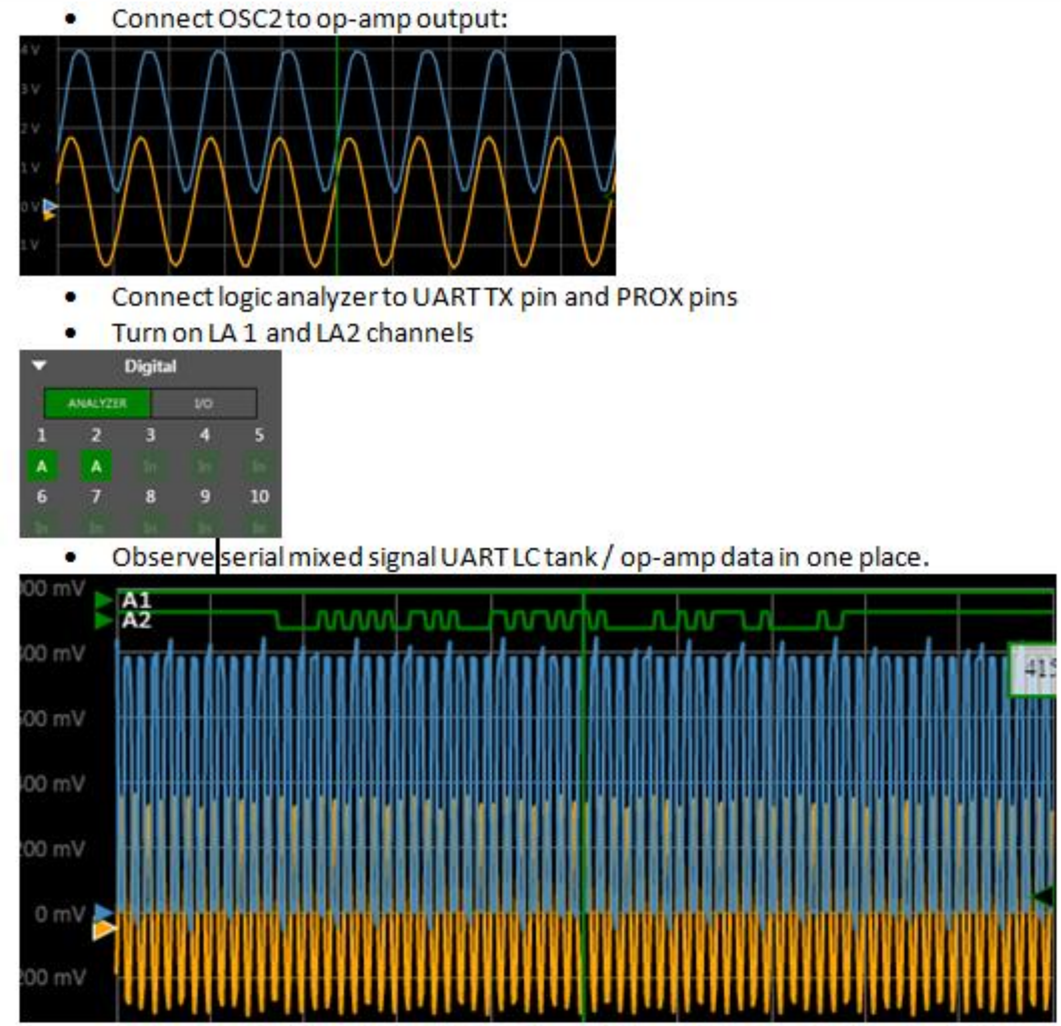
- Compare to board measured frequency in terminal program



```
Peak = 891 Diff = 6 0%, LC = 1569 Freq = 401470 Hz Diff = 569 0%
```

- Add metal and show frequency change.

Logic Analyzer Demo



- Connect OSC2 to op-amp output:
- Connect logic analyzer to UART TX pin and PROX pins
- Turn on LA 1 and LA2 channels
- Observe serial mixed signal UART LC tank / op-amp data in one place.

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