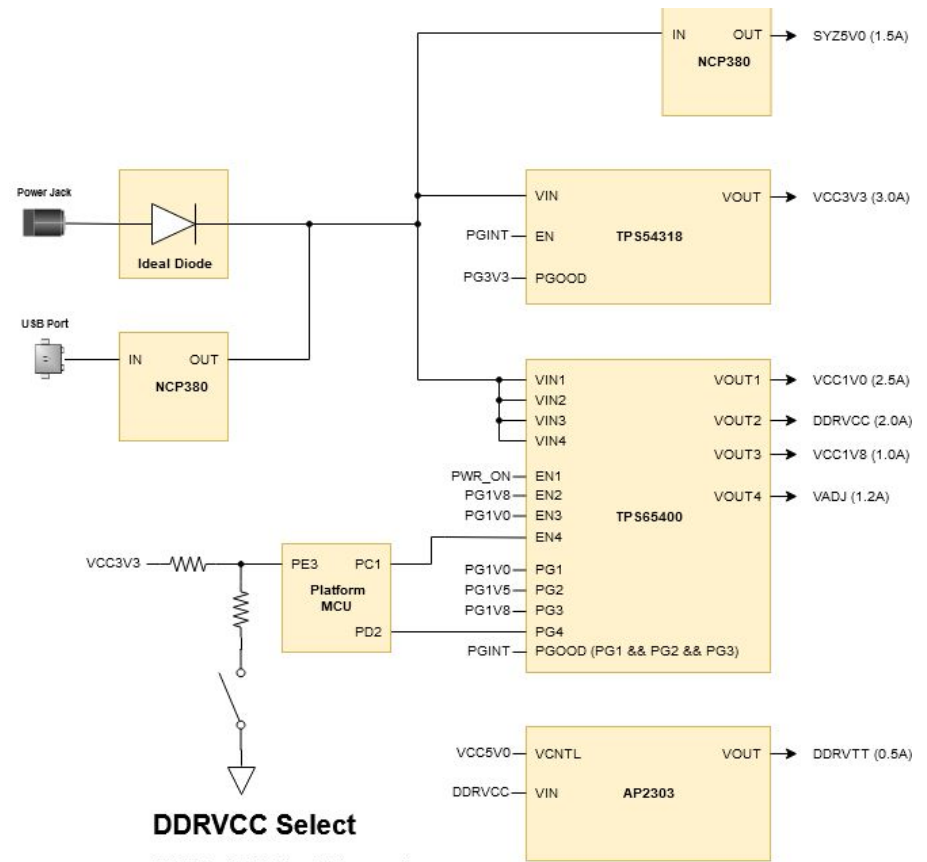


# Sheet Index

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- 2 IO, Pmods and Zmods
- 3 USB Hub
- 4 USB FIFO/SPI
- 5 Configuration
- 6 FPGA Banks
- 7 FPGA Banks
- 8 FPGA Power
- 9 DDR3 Memory
- 10 Platform MCU
- 11 Power Regulation
- 12 Power regulation
- 13 USB JTAG/UART

## Power Tree



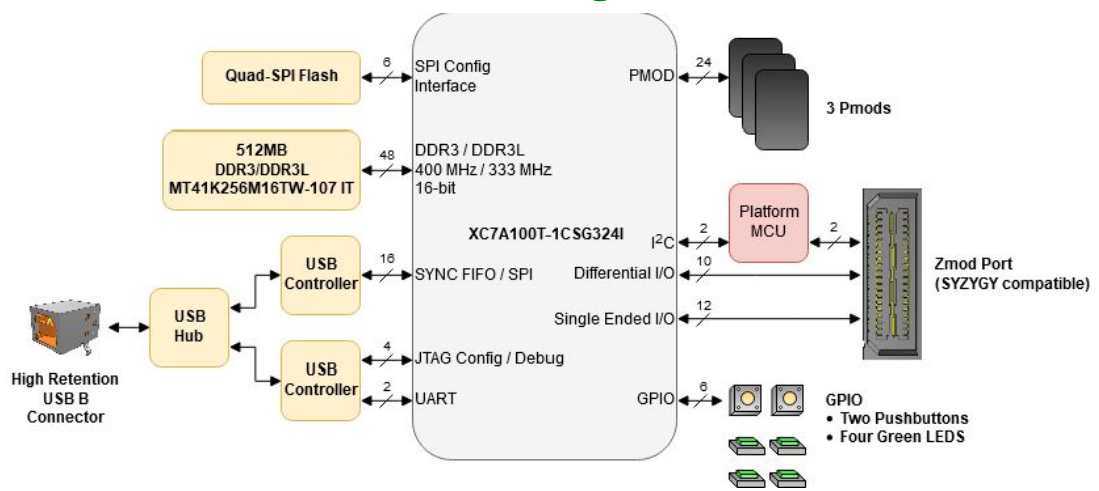
### DDRVC Select

DDRVC = 1.35V with switch in on position  
 DDRVC = 1.5V with switch in off position  
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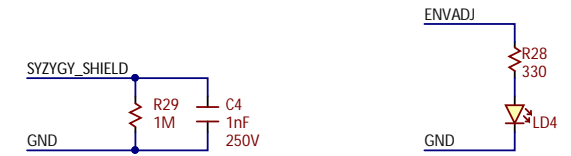
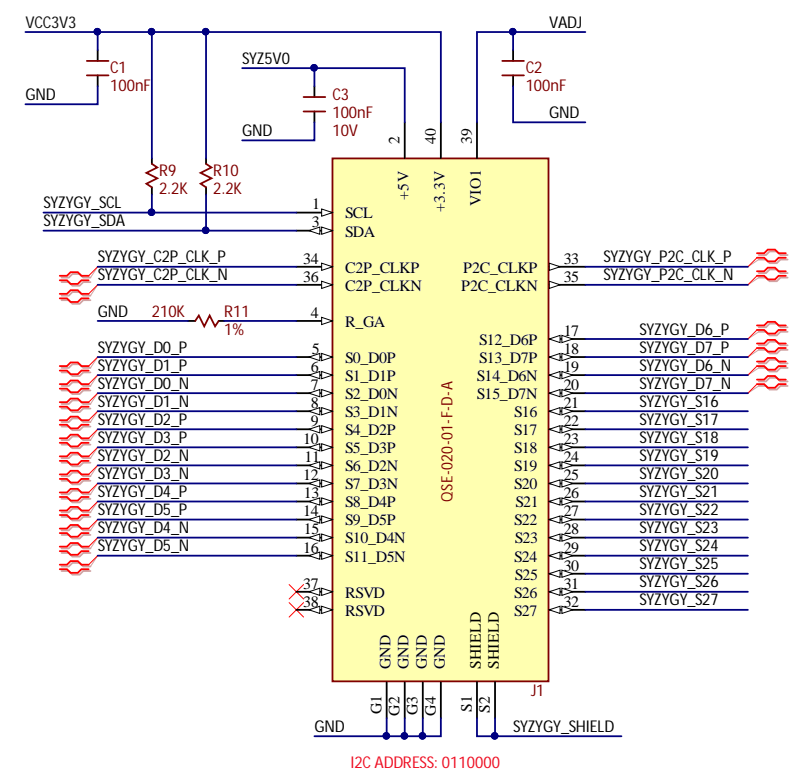
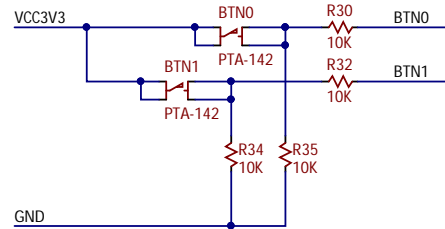
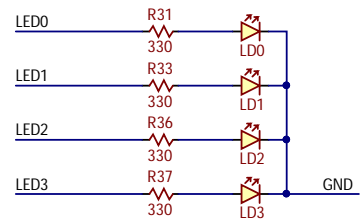
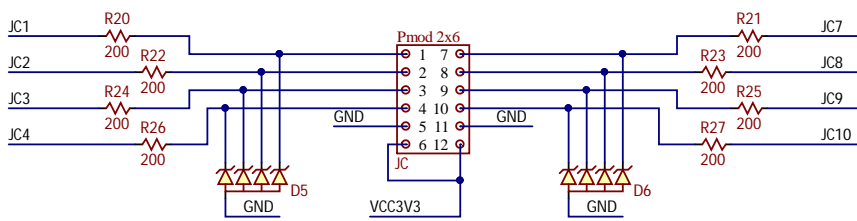
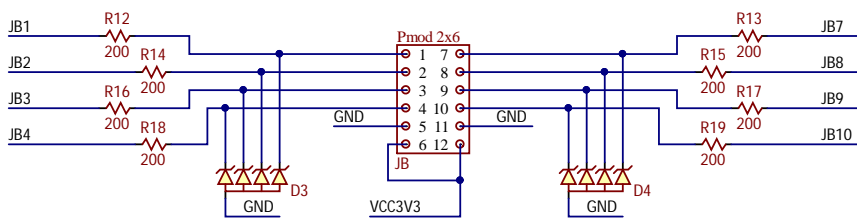
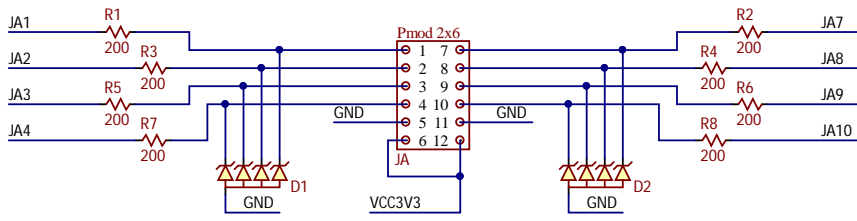
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## Block Diagram



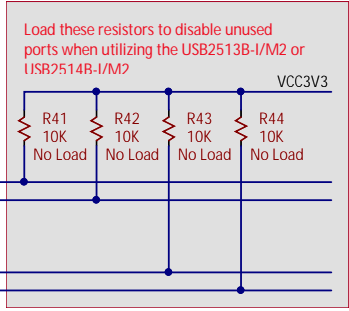
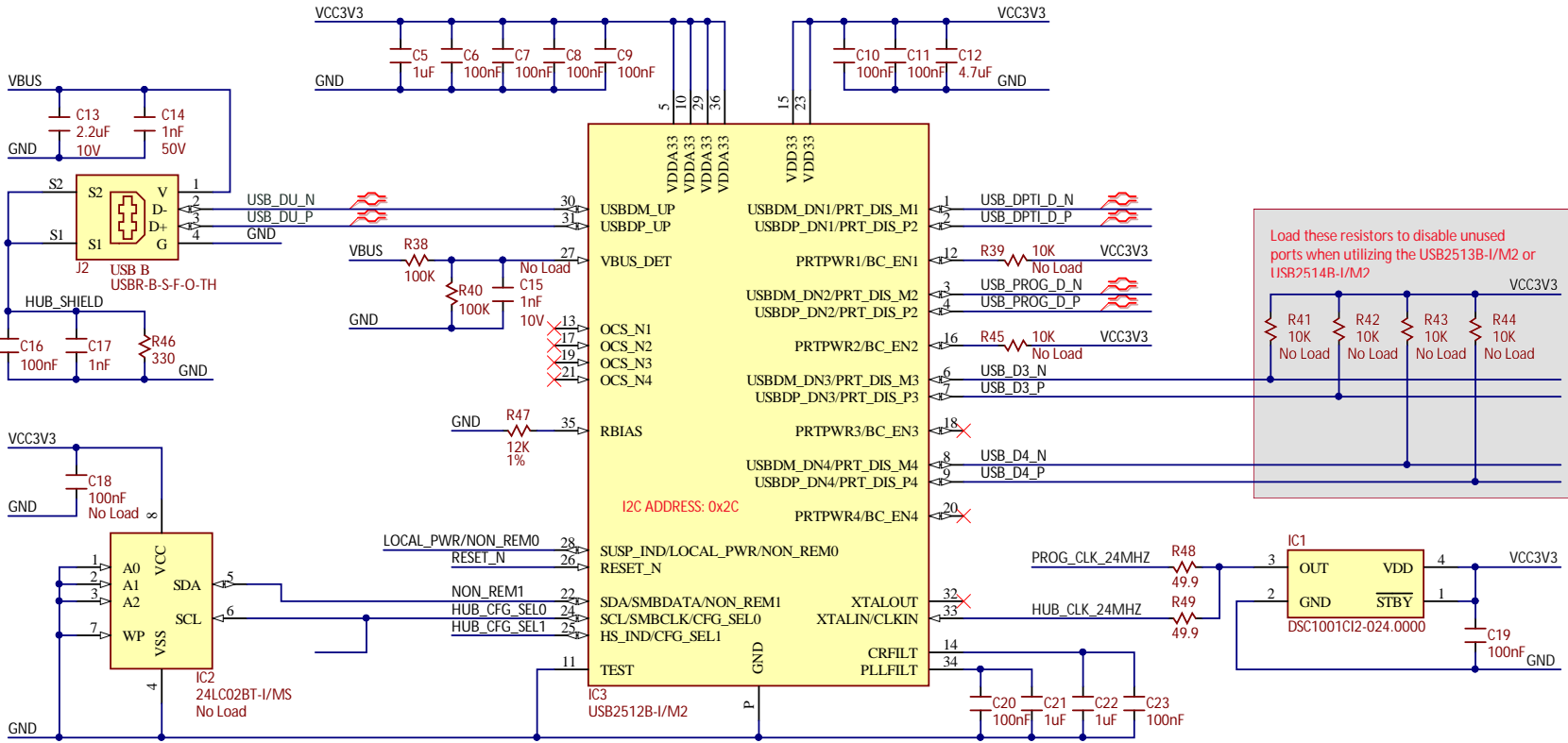
Title <b>USB104 A7</b>		Rev <b>B.1</b> Copyright 2019
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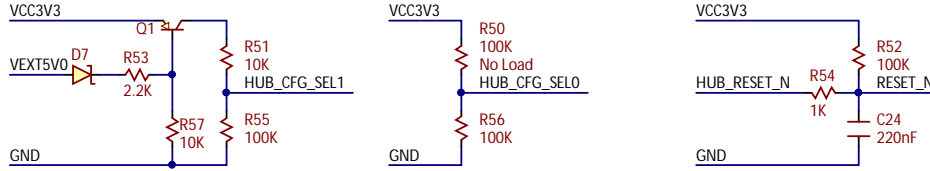


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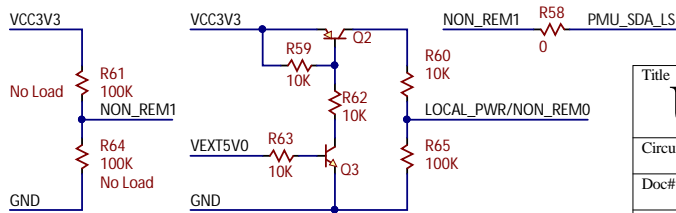


CFG_SEL1	CFG_SELO	Hub Configuration
0	0	Default Configuration, Strapping Enabled, Self Powered
0	1	Configured via SMBus, Strapping disabled
1	0	Default Configuration, Strapping Enabled, Bus Powered
1	1	Configured via I2C EEPROM, Strapping disabled



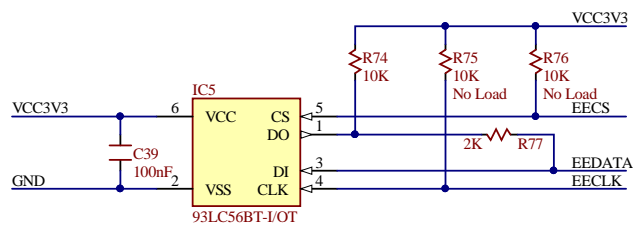
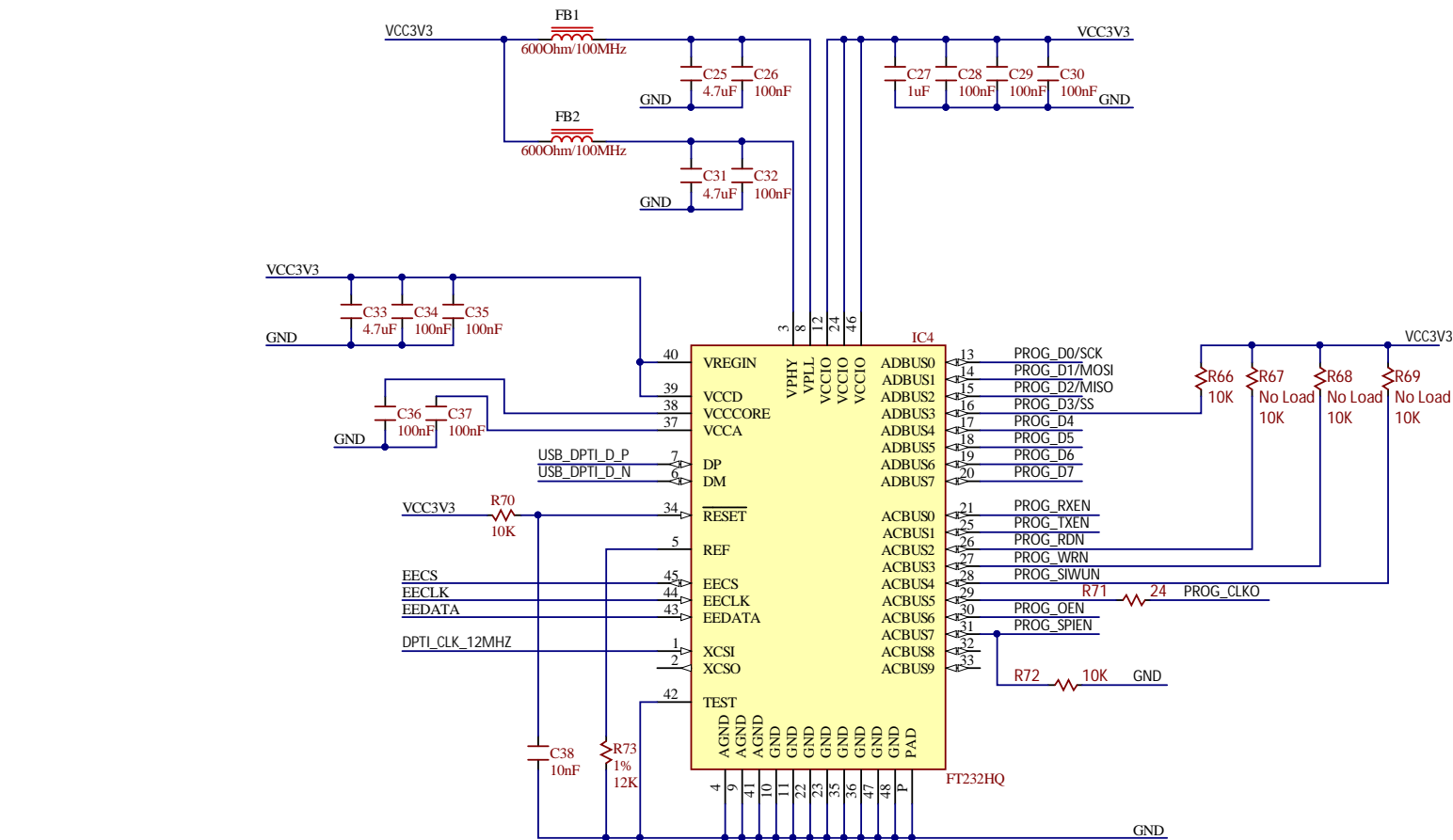
Note: CFG\_SELx and NON\_REMx are sampled on the rising edge of RESET\_N

NOM_REM1	NOM_REM0	Port Configuration
0	0	All ports are removable
0	1	Port 1 is non-removable
1	0	Ports 1 and 2 are non-removable
1	1	When available, ports 1, 2, and 3 are non-removable



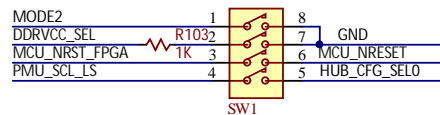
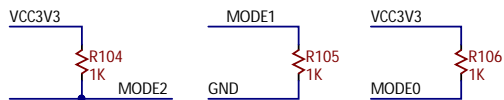
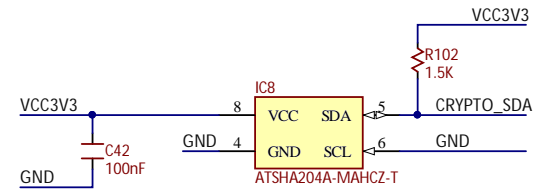
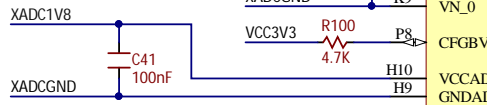
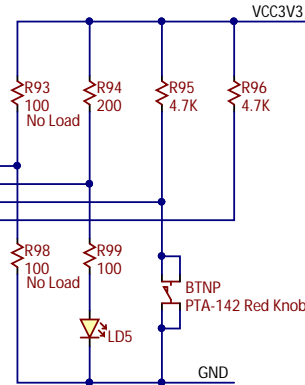
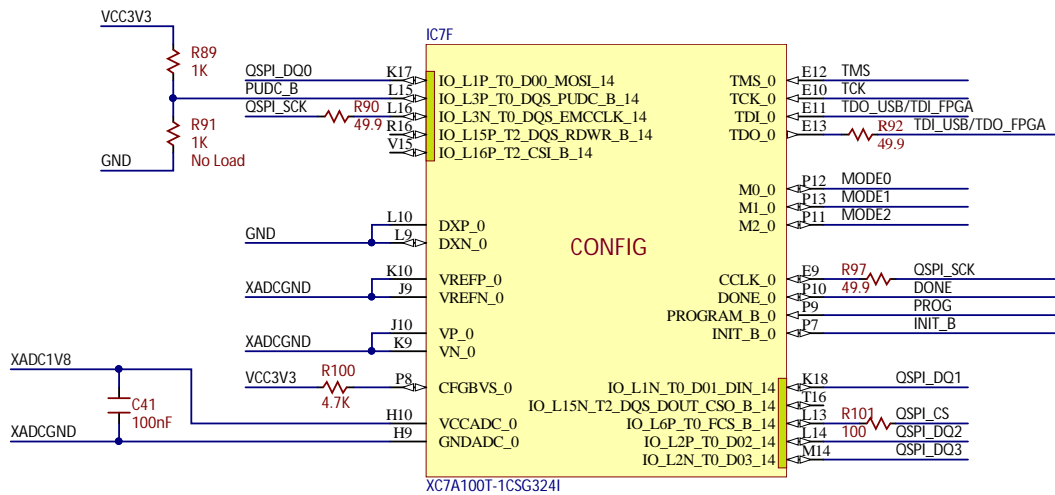
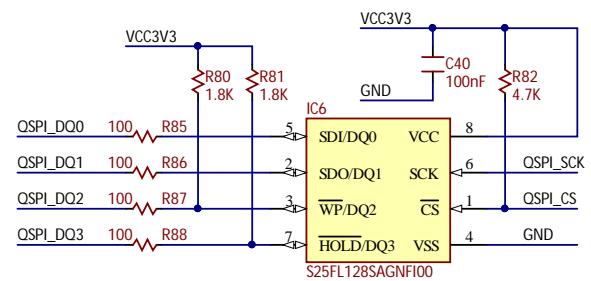
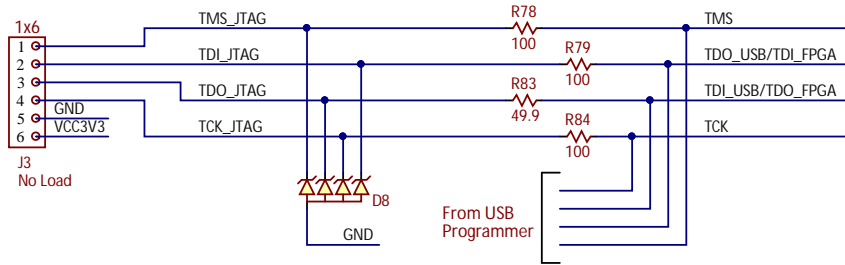
Note: Use of LOCAL\_PWR requires the hub to be configured via SMBus or EEPROM.

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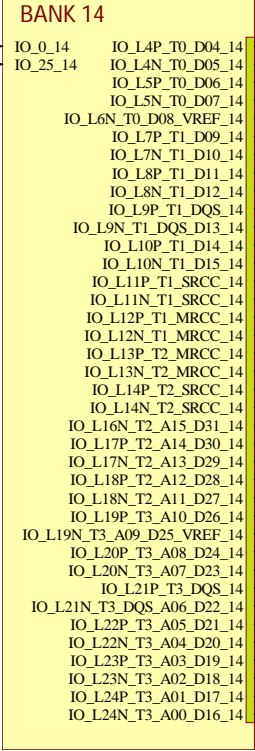




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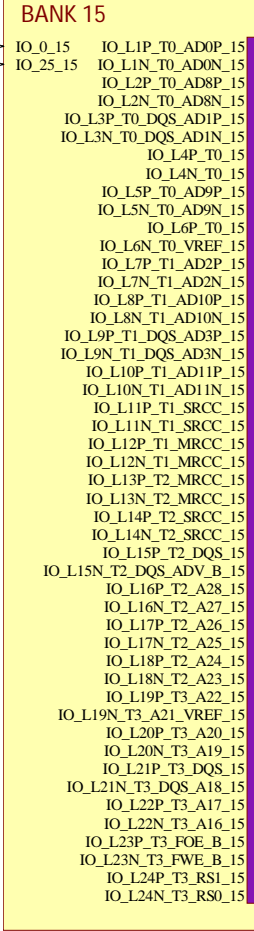
IC7A



XC7A100T-1CSG324I



IC7B

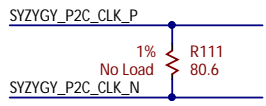


XC7A100T-1CSG324I

IC7C



XC7A100T-1CSG324I

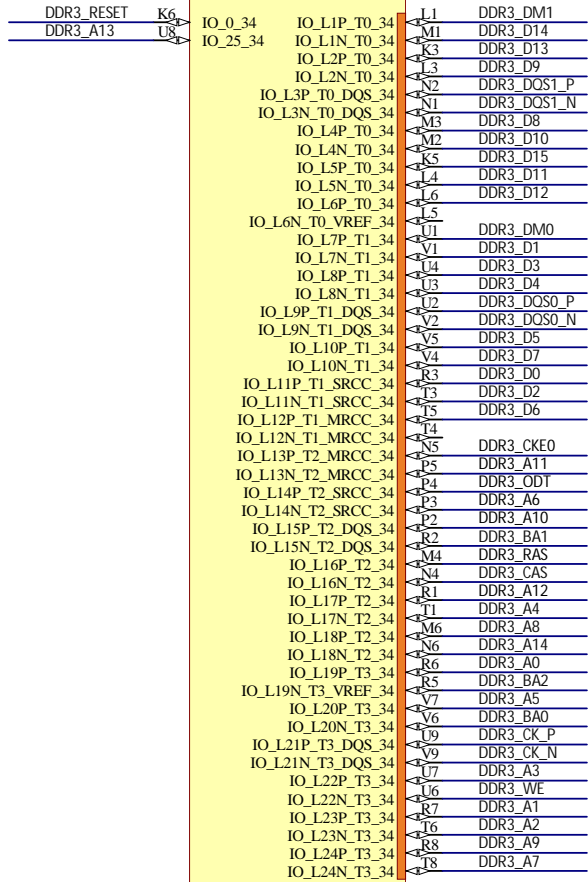


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IC7D

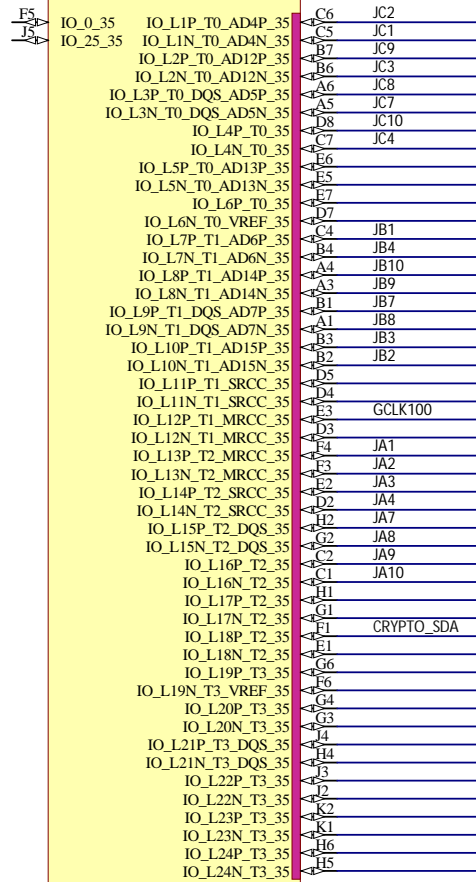
**BANK 34**



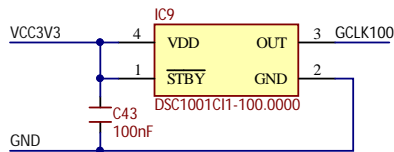
XC7A100T-1CSG324I

IC7E

**BANK 35**

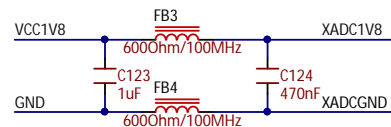
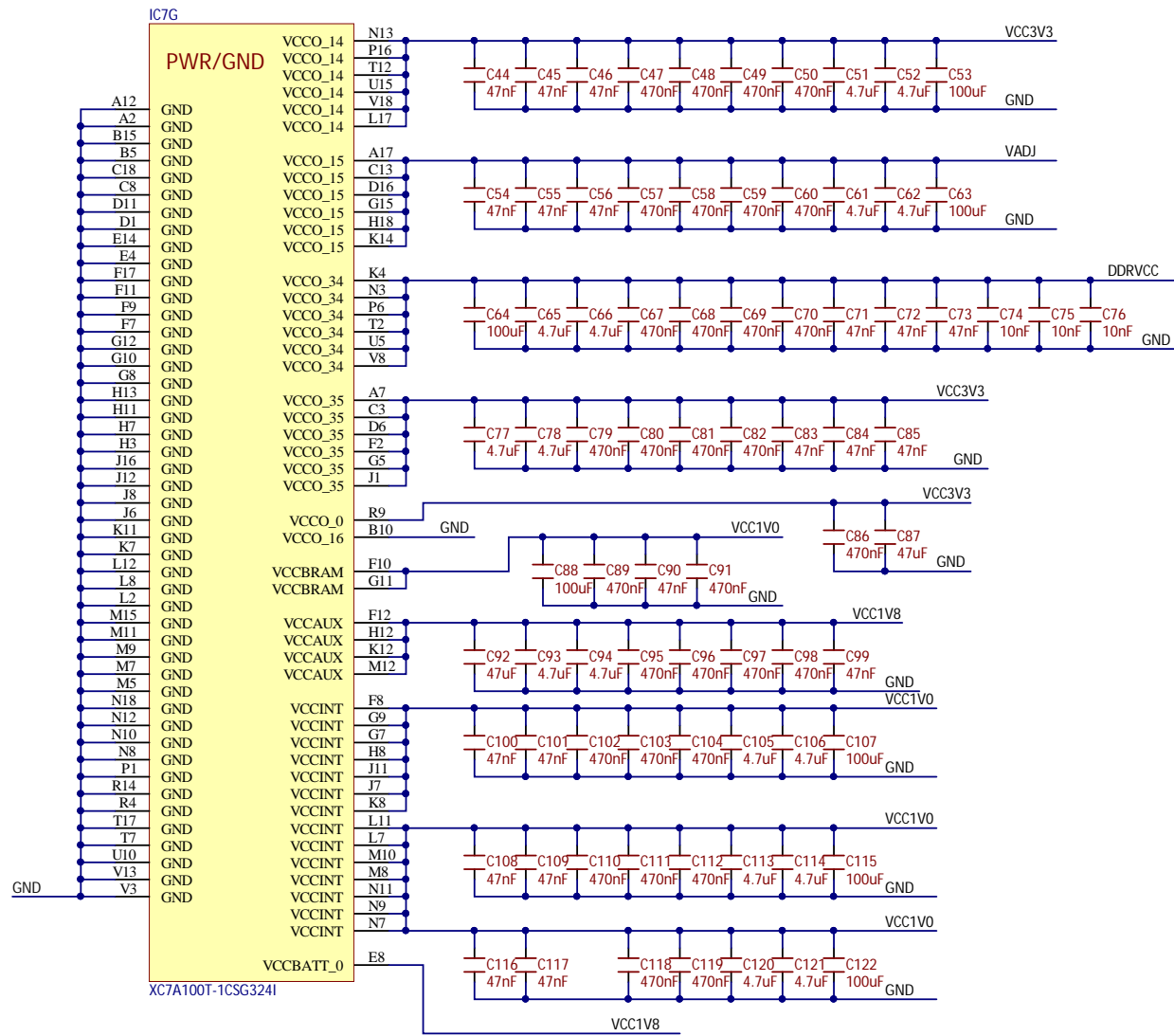


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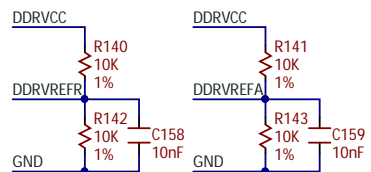
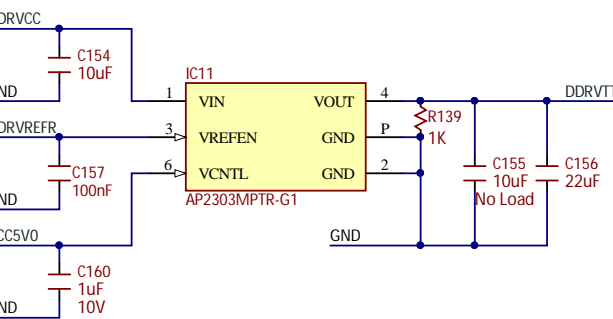
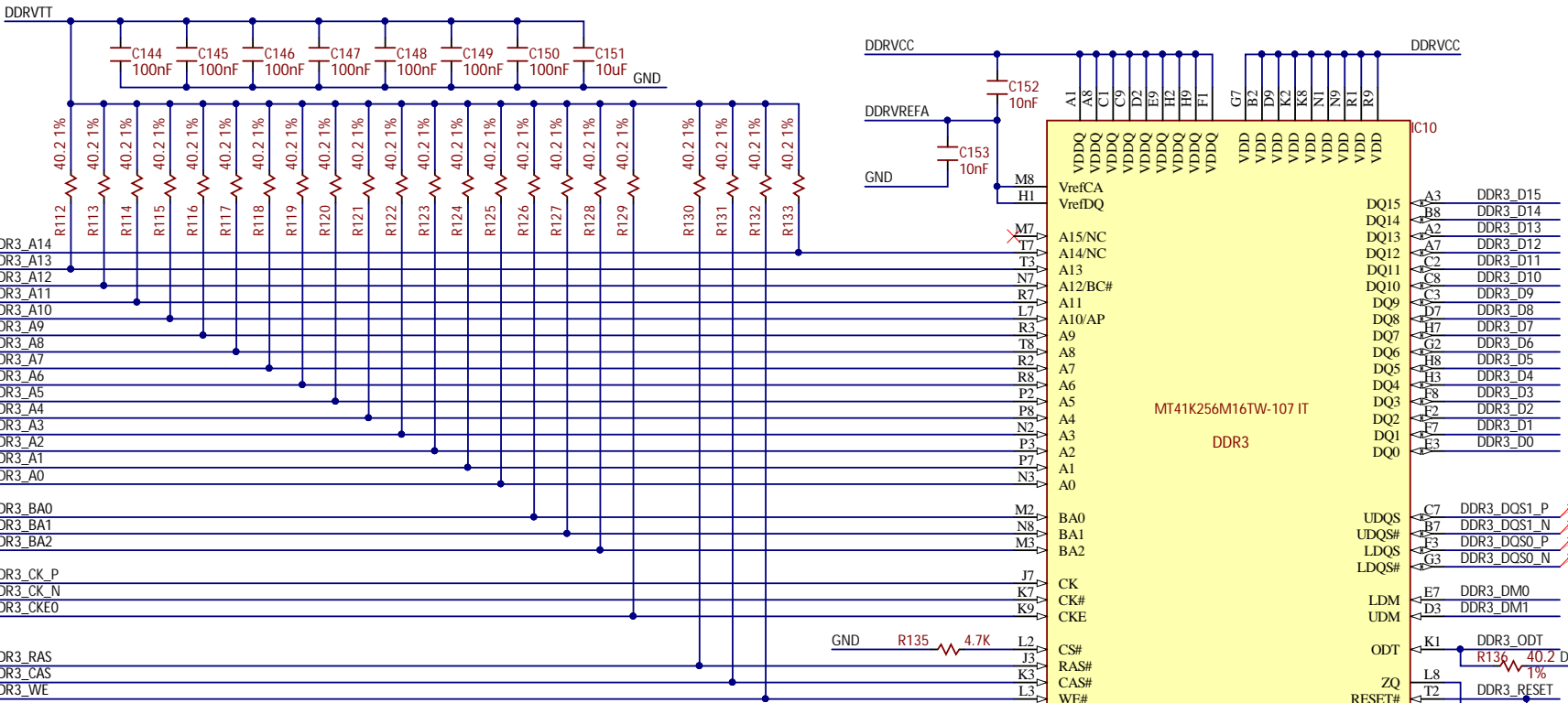
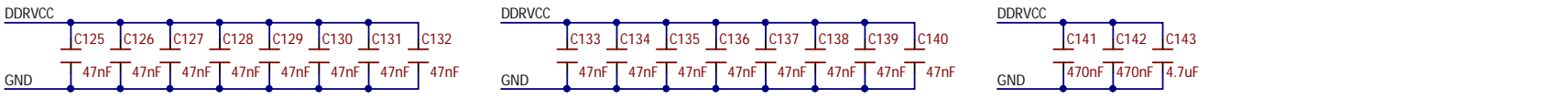




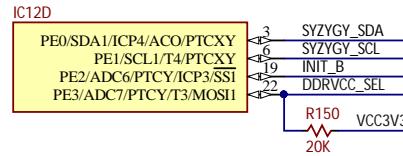
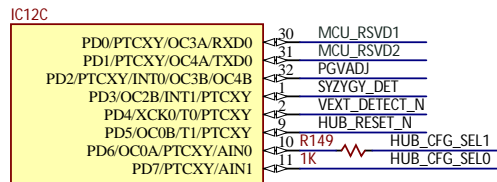
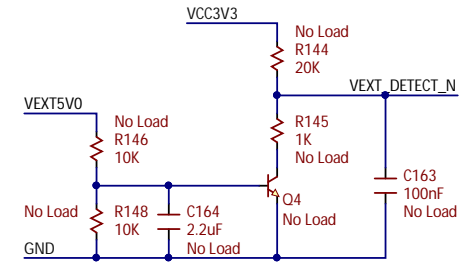
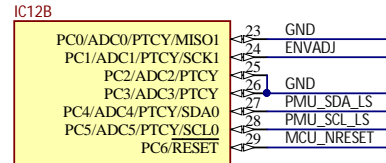
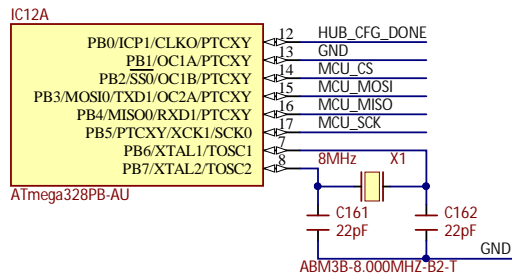
Title		Rev
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Circuit	FPGA Power	
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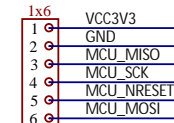
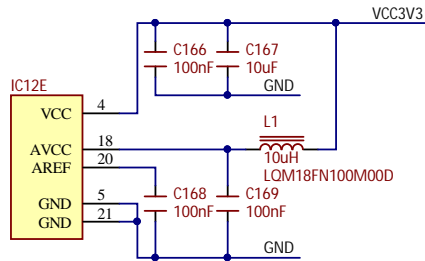


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Circuit		DDR3
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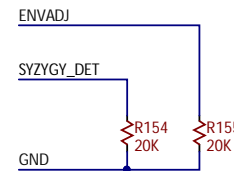
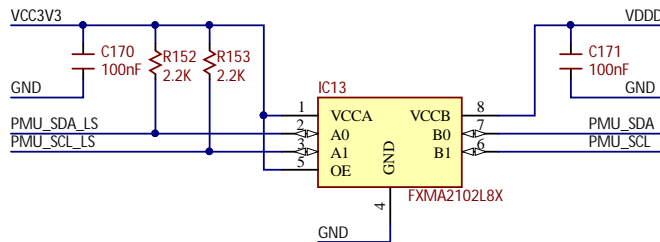
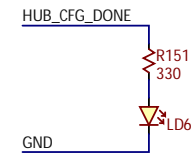


DDRVC_SEL	DDRVC Voltage
0	1.35 Volts
1	1.50 Volts

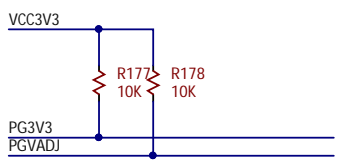
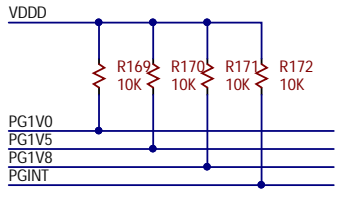
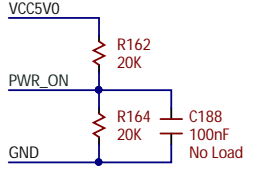
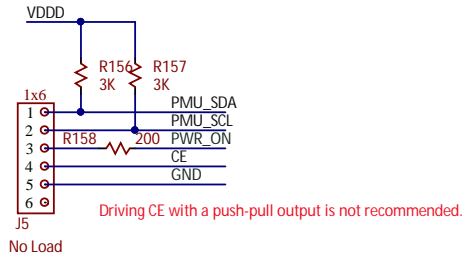
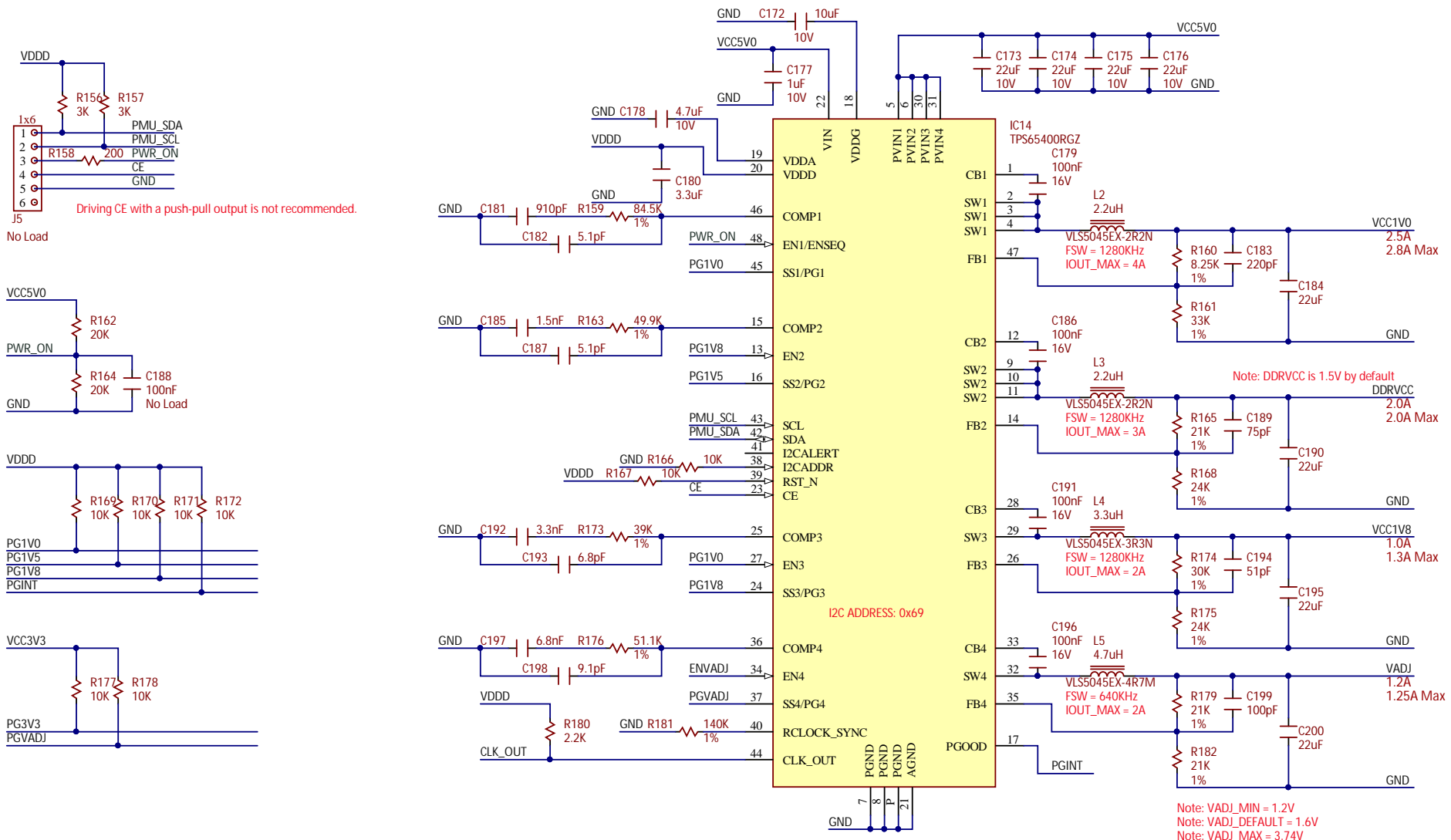
Note: DDRVC\_SEL is only sampled one time during each boot sequence.



J4  
No Load  
Program/Debug using MPLAB SNAP Debugger  
Pin 2 of the SNAP connects to pin 1 on the board  
SNAP Pinout: <http://microchipdeveloper.com/pickit4:interface-pinouts>



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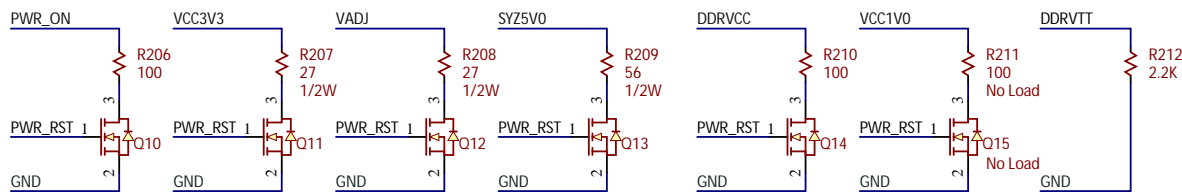
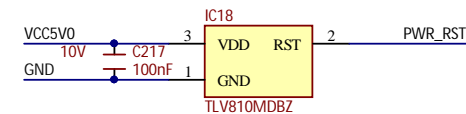
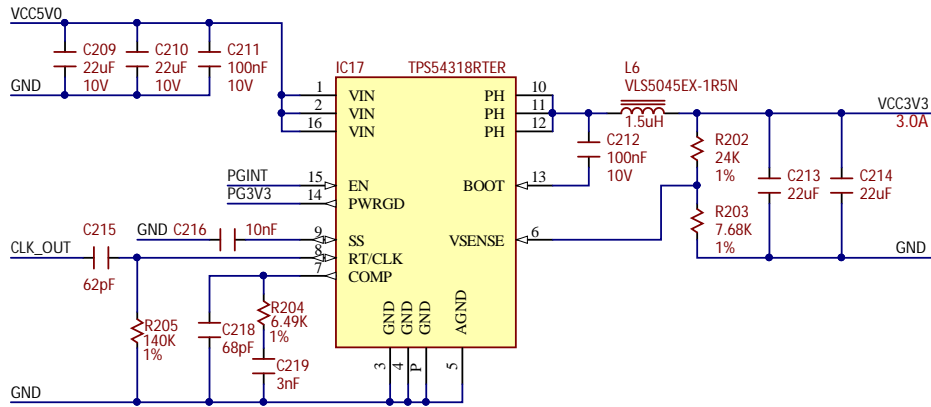
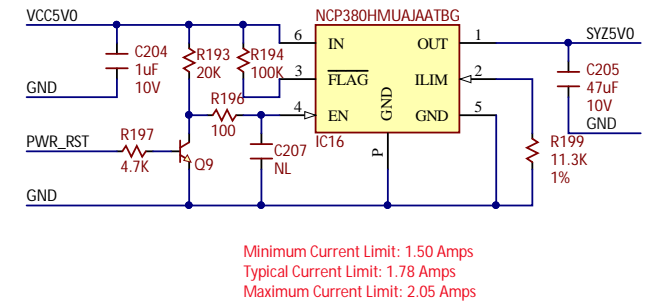
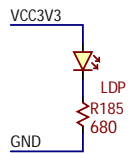
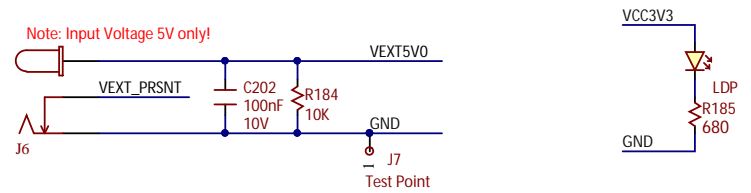
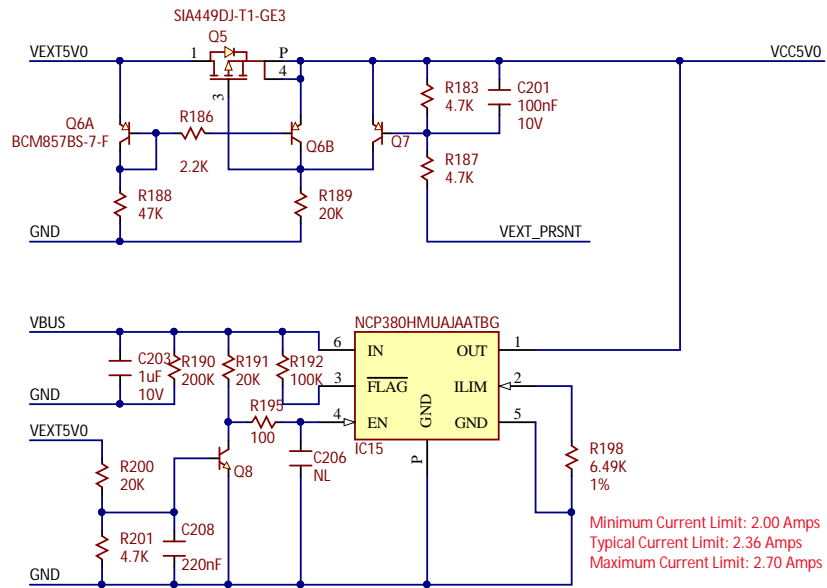


ISENSE\_GAIN = 10A/V for all channels  
 TON\_RAMP\_RATE = 0.25V/ms for all channels

Note: VADJ\_MIN = 1.2V  
 Note: VADJ\_DEFAULT = 1.6V  
 Note: VADJ\_MAX = 3.74V

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A

A

B

B

C

C

D

D

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