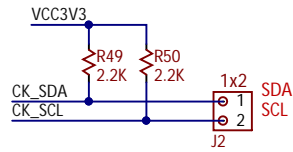
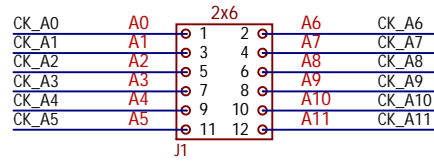


Foot
F1
Foot
F2
Foot
F3
Foot
F4

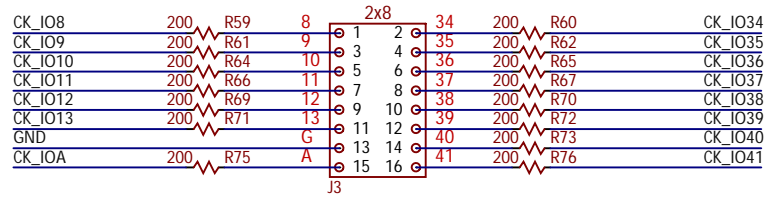
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<p>Title: PYNQ-Z1</p>	
<p>Rev: C.0 Copyright 2016</p>	
<p>Circuit: PMODs, User I/O</p>	
<p>Doc#: 6003-500-017</p>	
<p>Engineer: GTM</p>	
<p>Author: DL</p>	
<p>Date: 8/9/16</p>	
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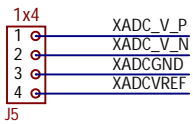
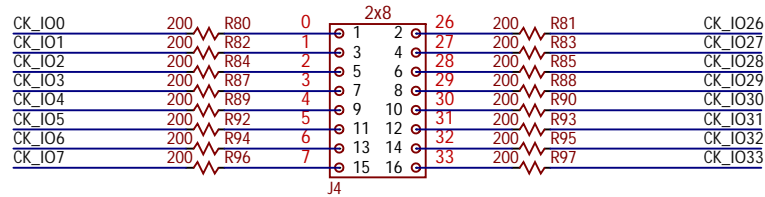
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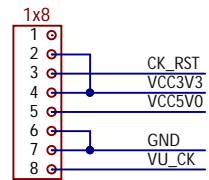
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IOL

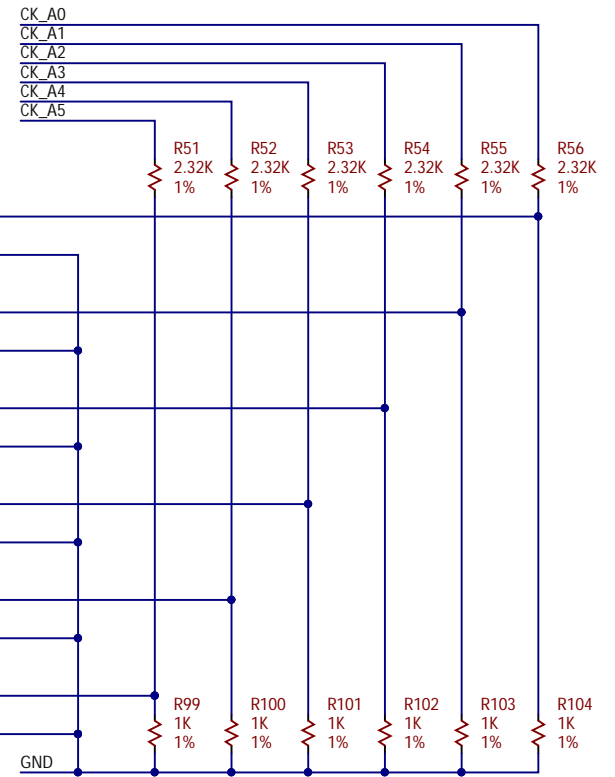
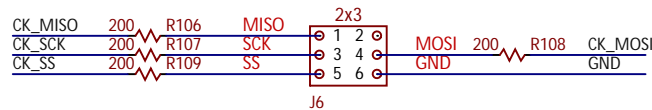


POWER



J7 EFS140GB1L10

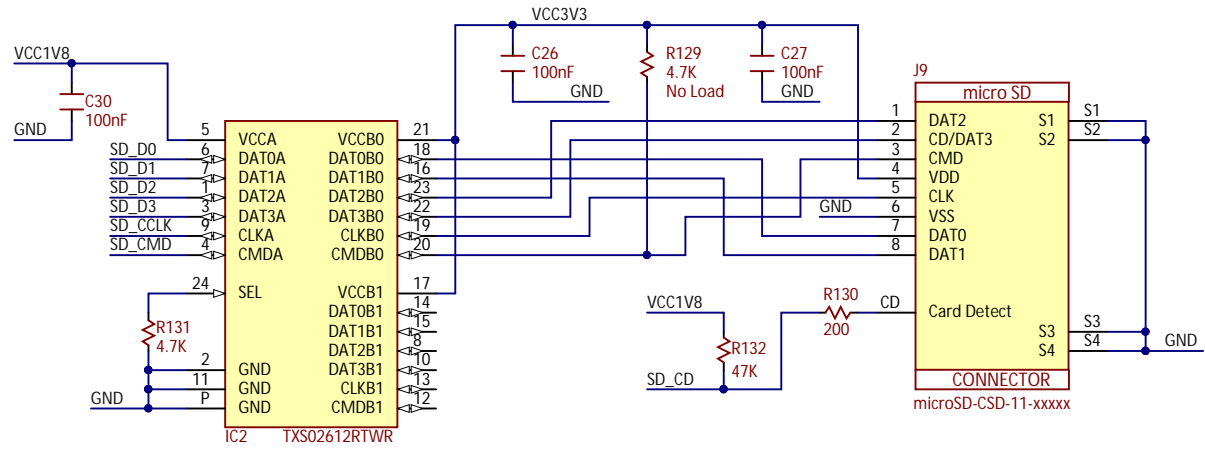
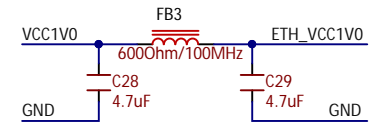
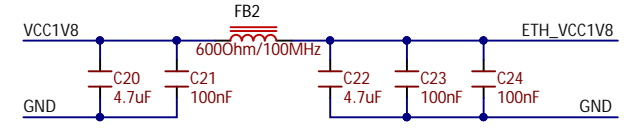
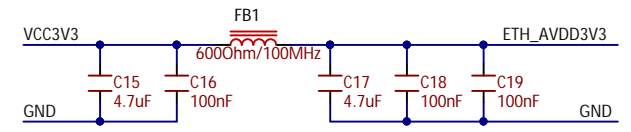
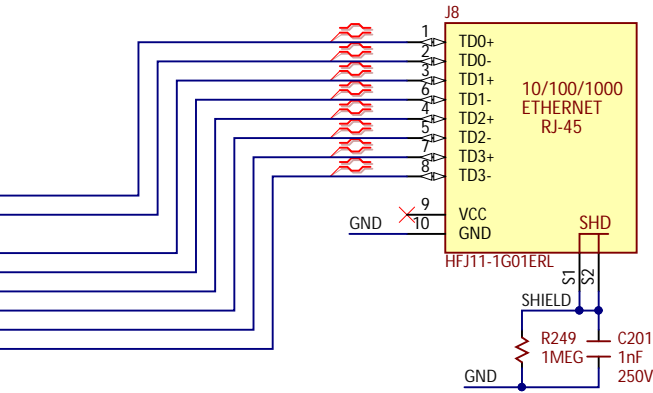
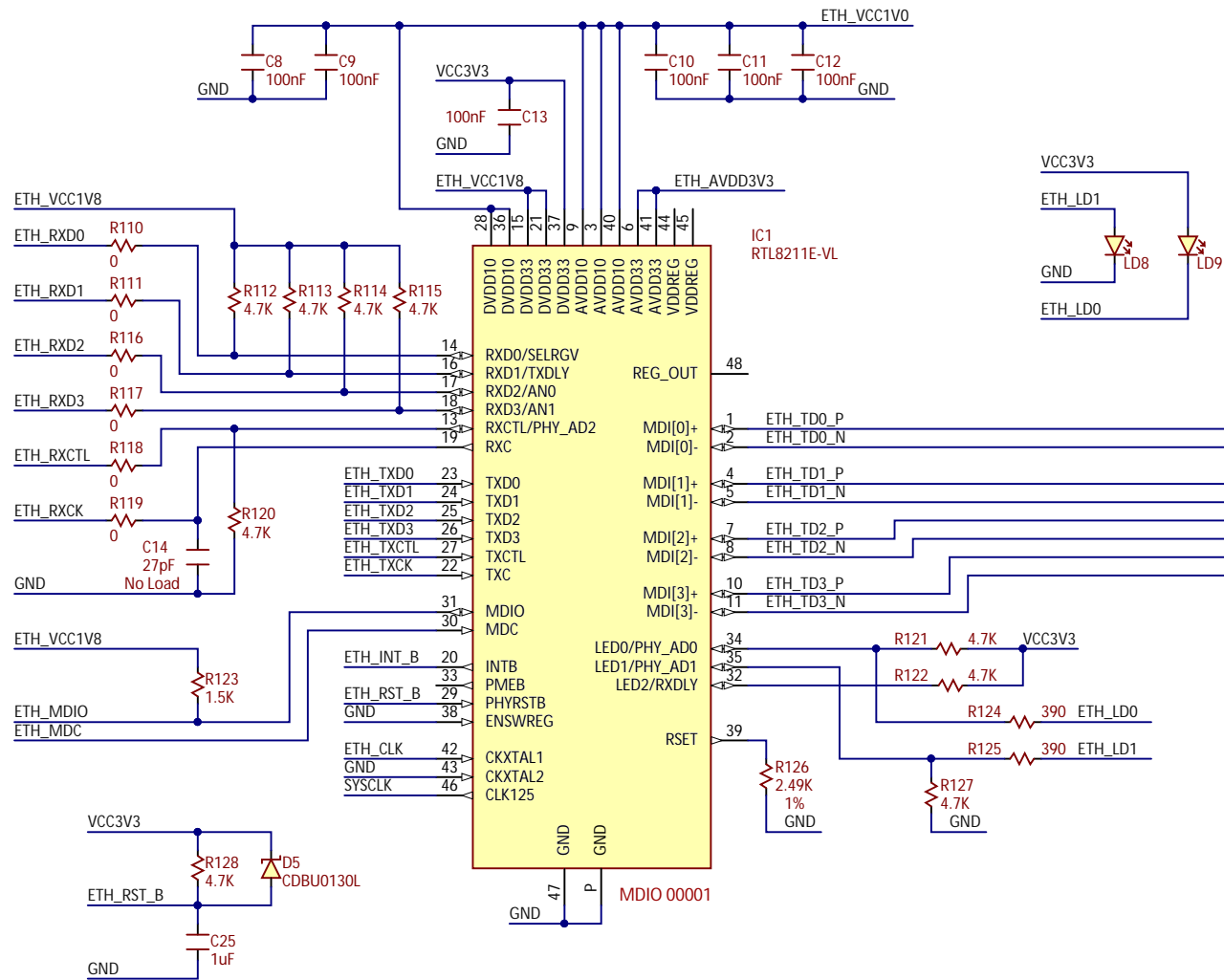
SPI



Note: Terminate N signals next to Analog Header

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Circuit Ethernet and SD Card		
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A

A

B

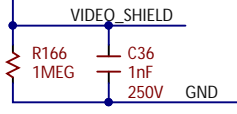
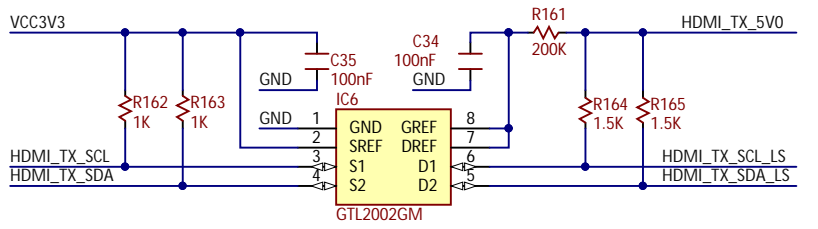
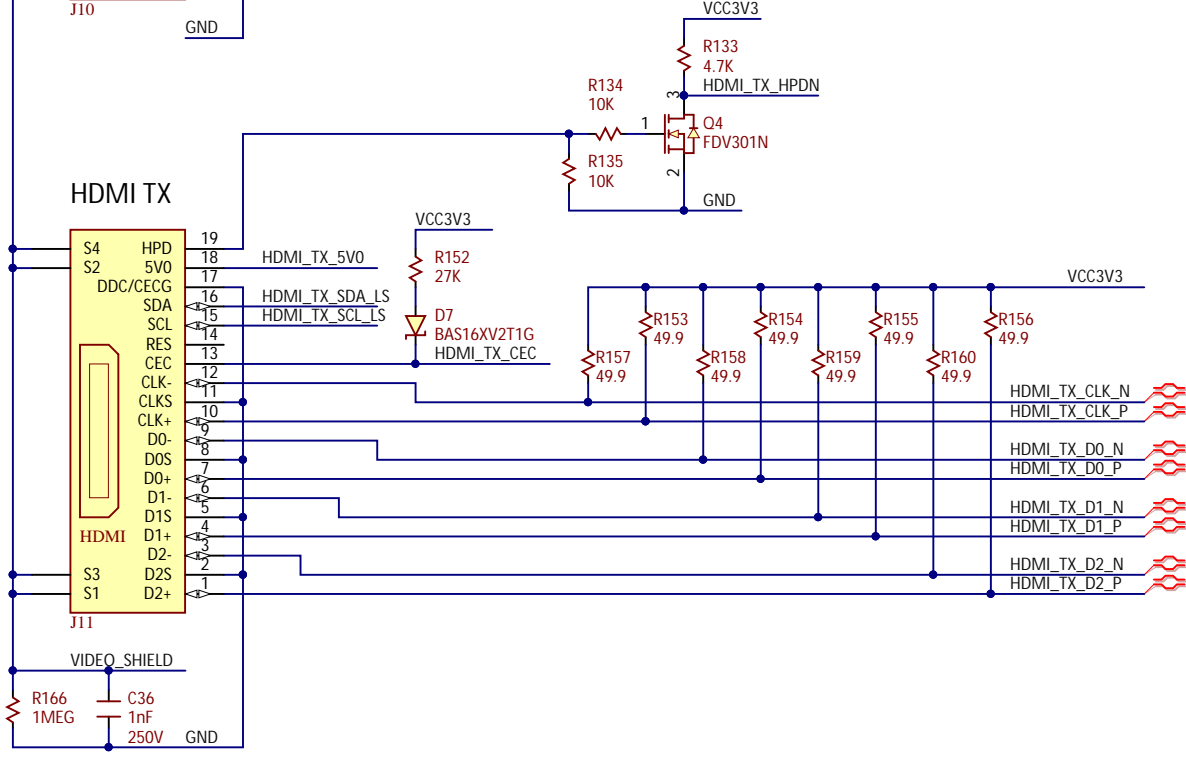
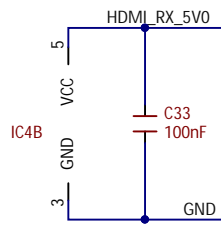
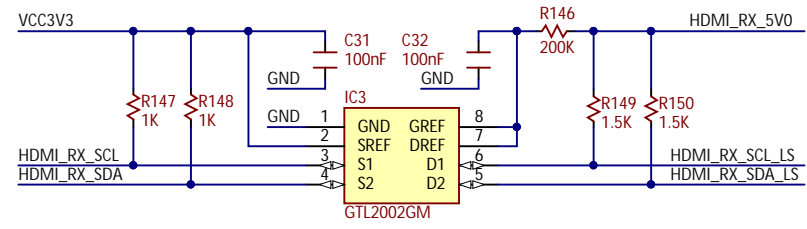
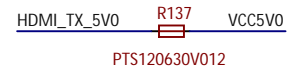
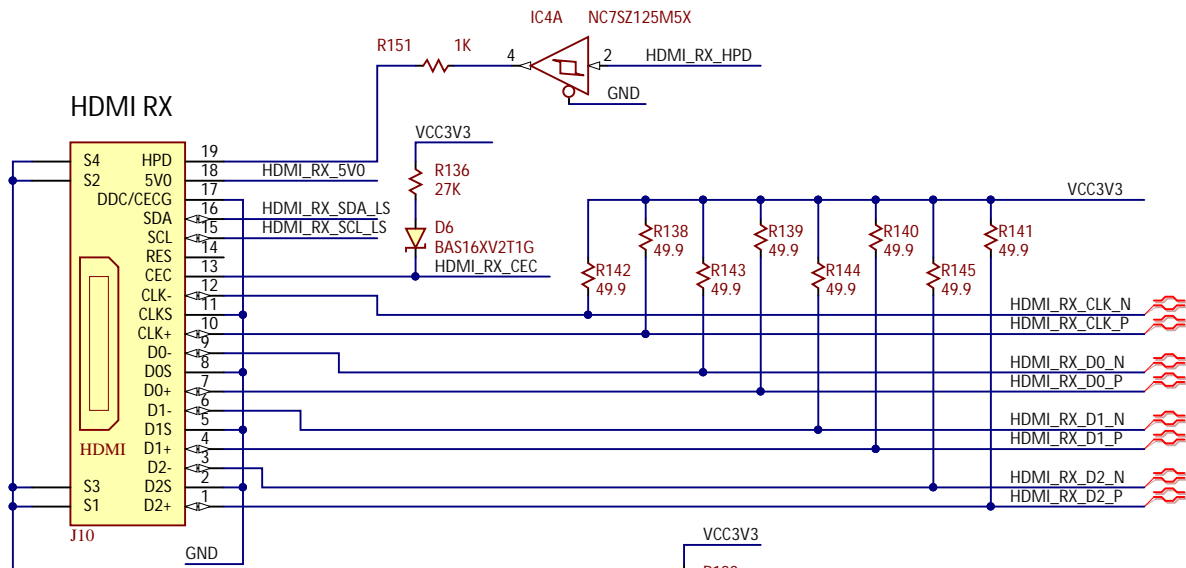
B

C

C

D

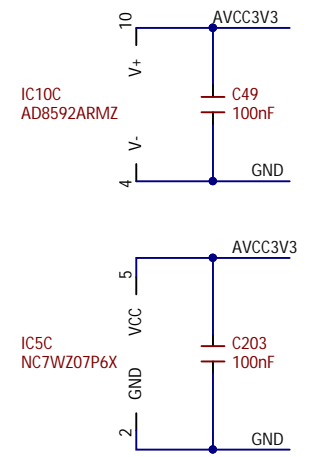
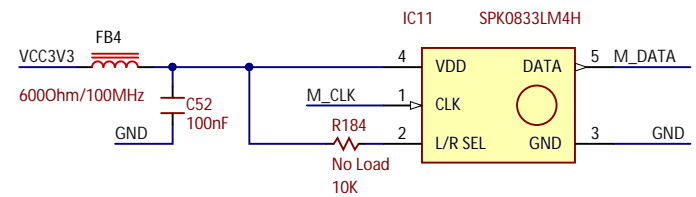
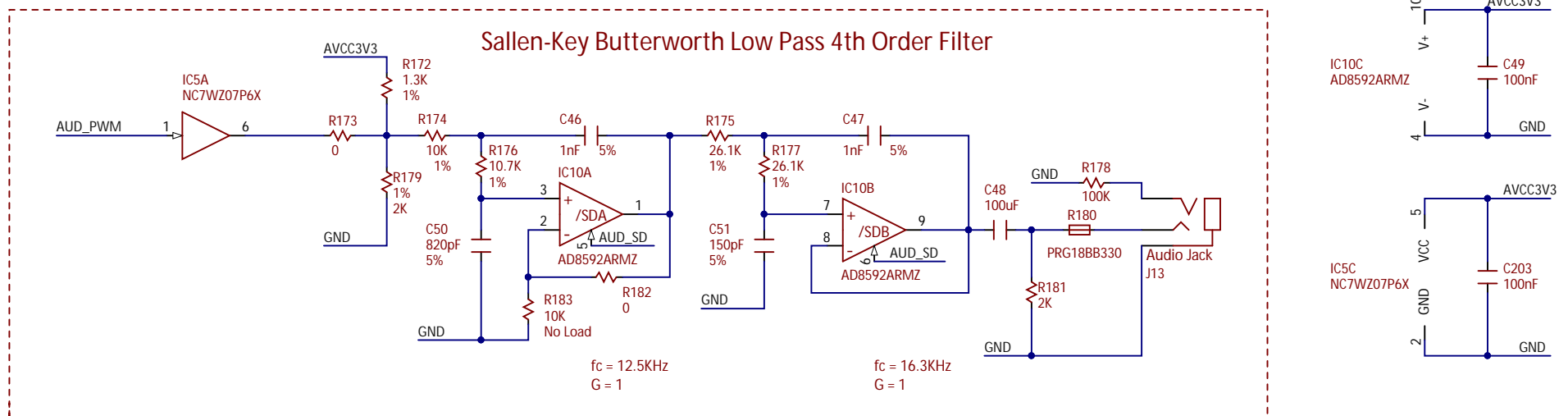
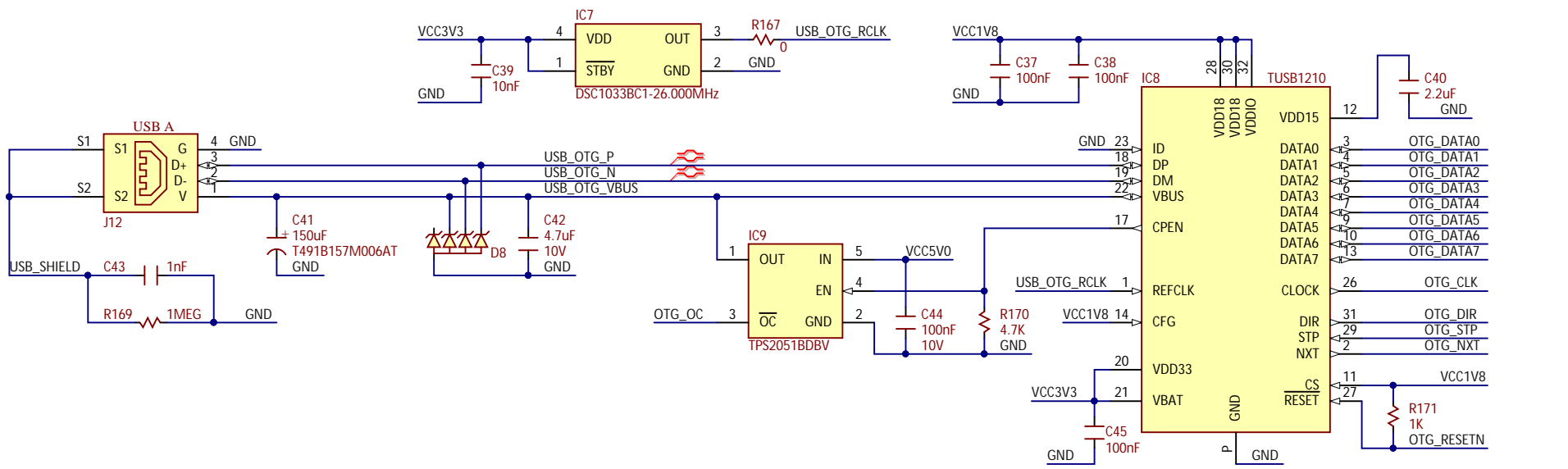
D



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Circuit	HDMI	
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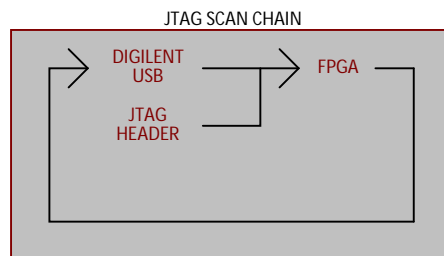
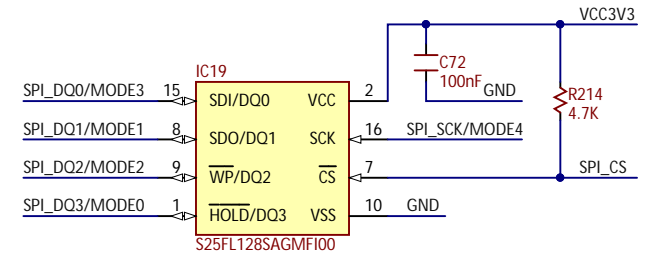
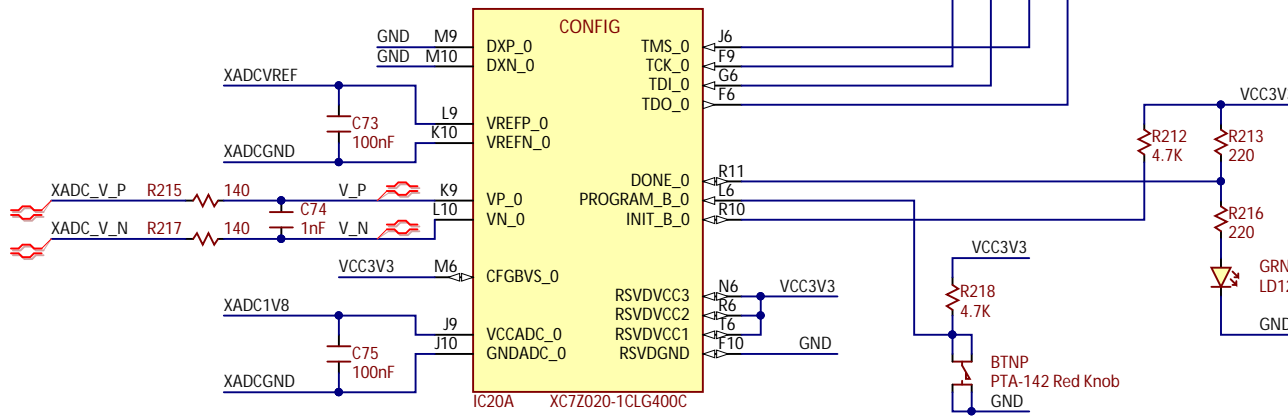
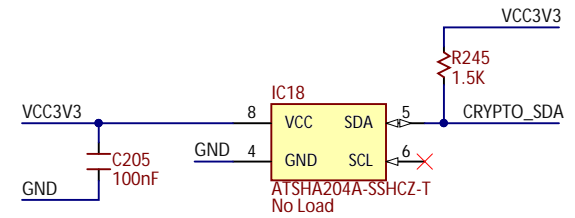
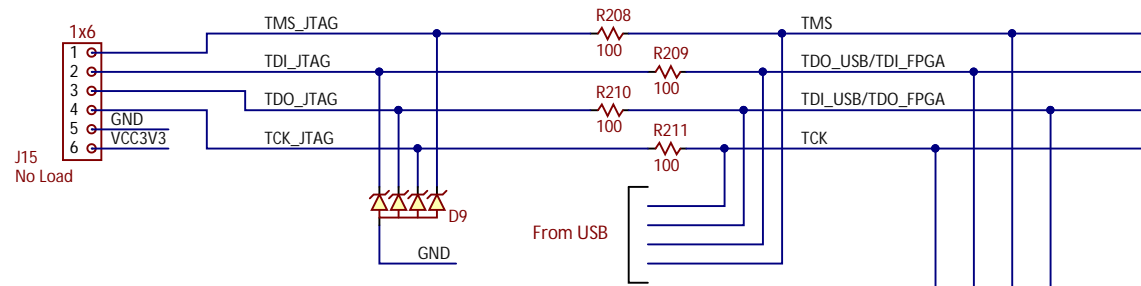


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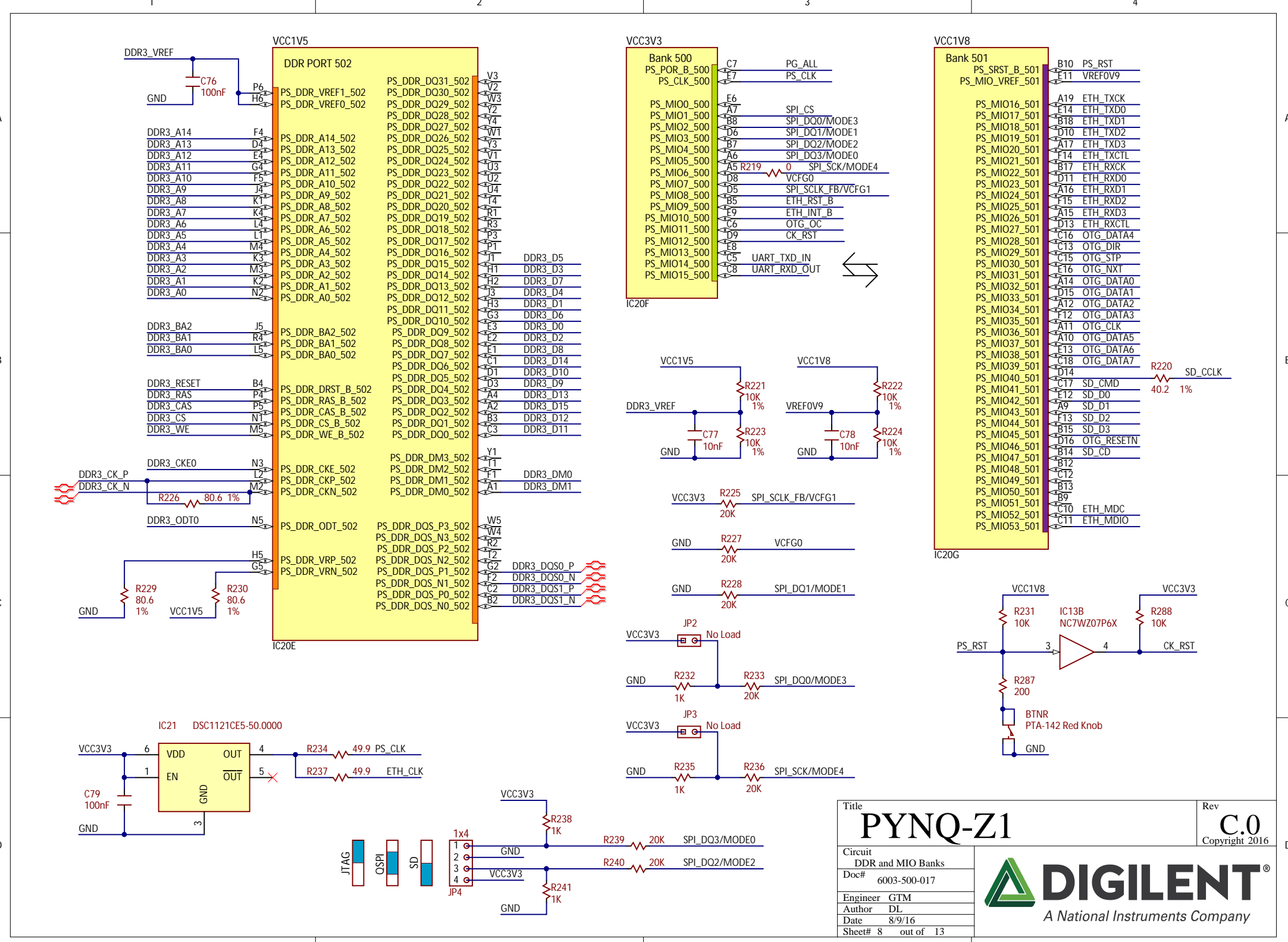
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Circuit FPGA Configuration, Flash		
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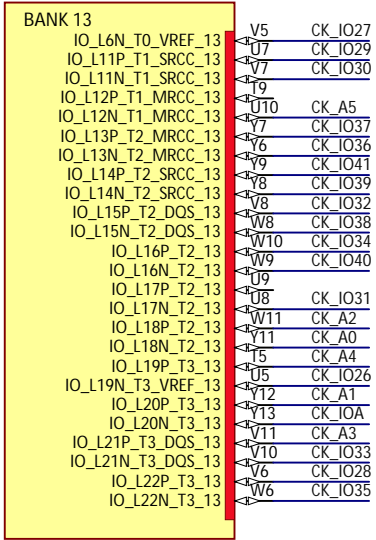




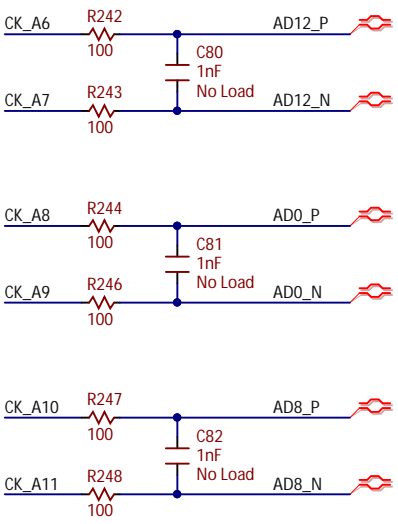
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Circuit DDR and MIO Banks		
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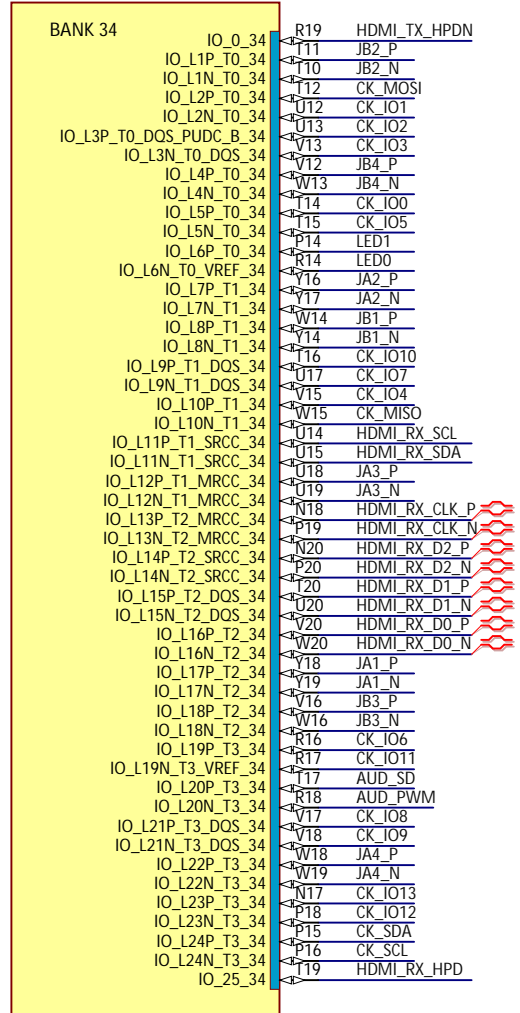
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IC20B

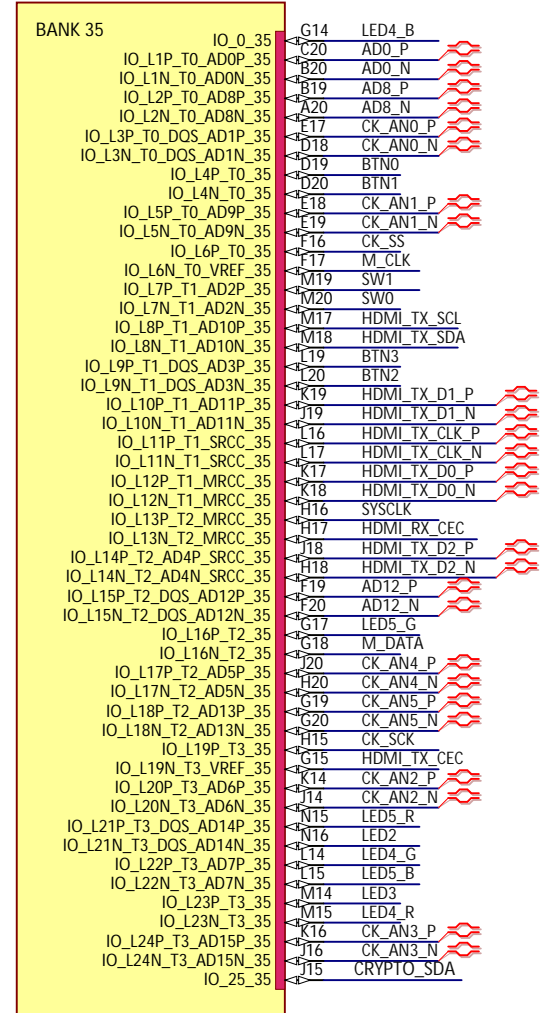


VCC3V3



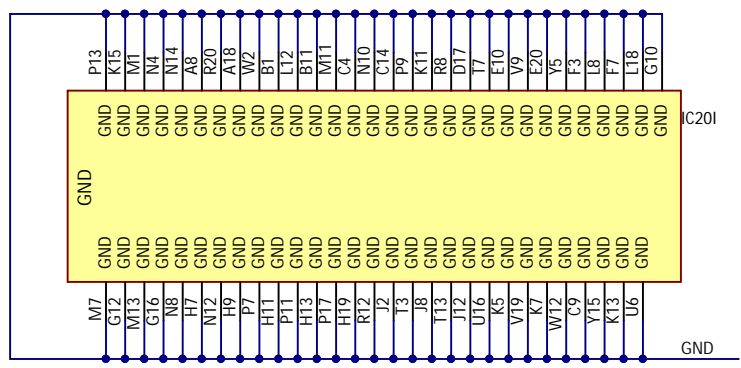
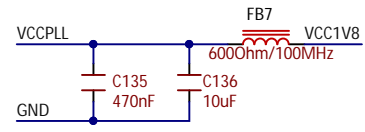
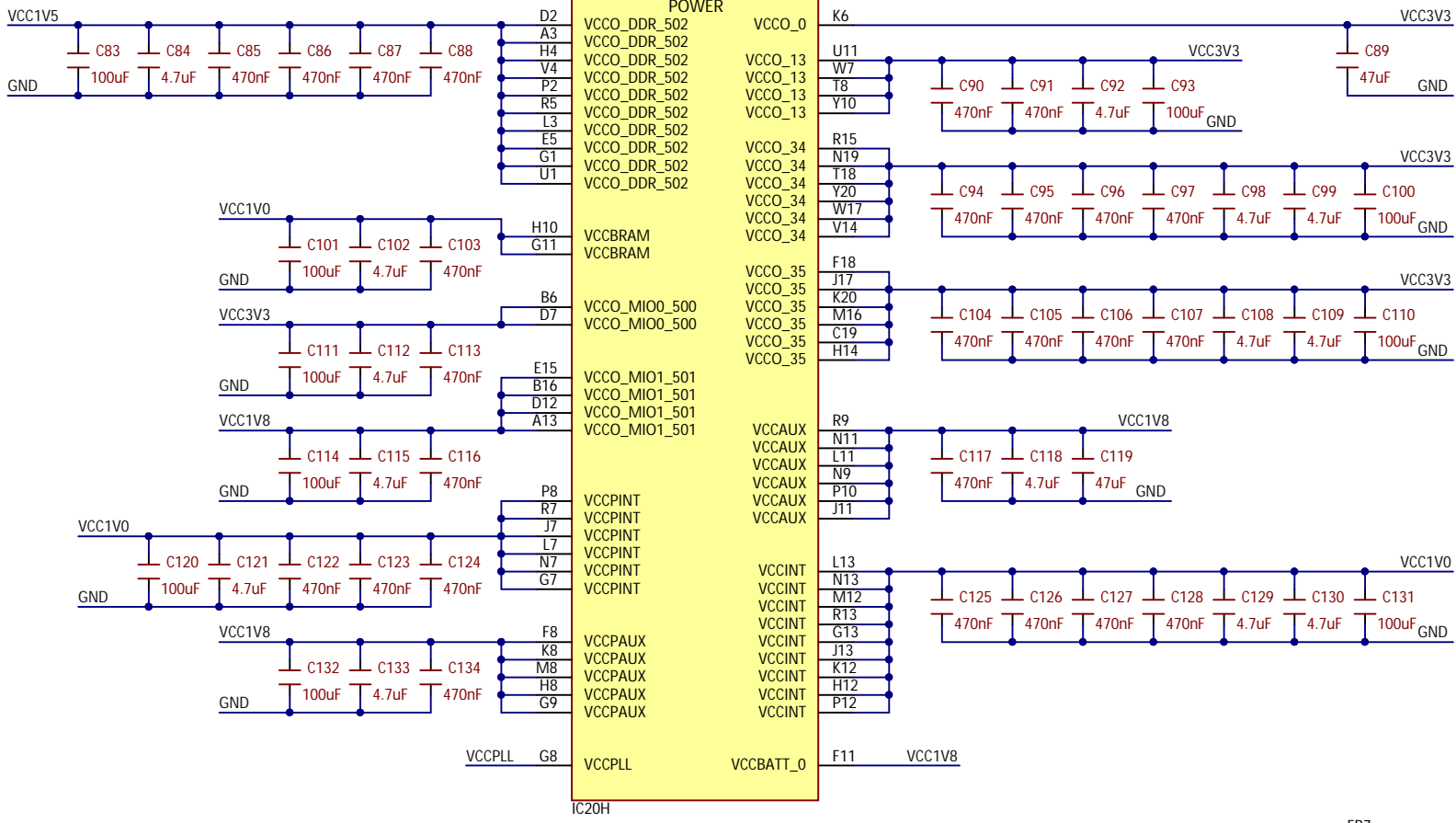
IC20C

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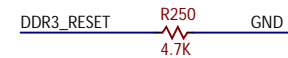
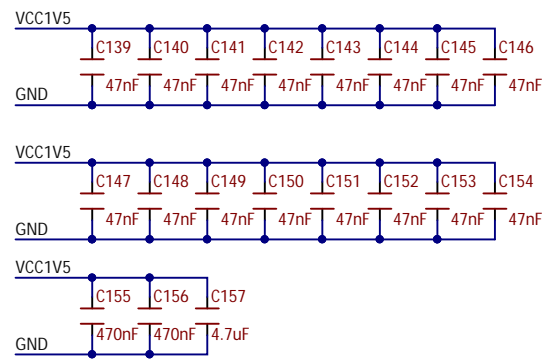
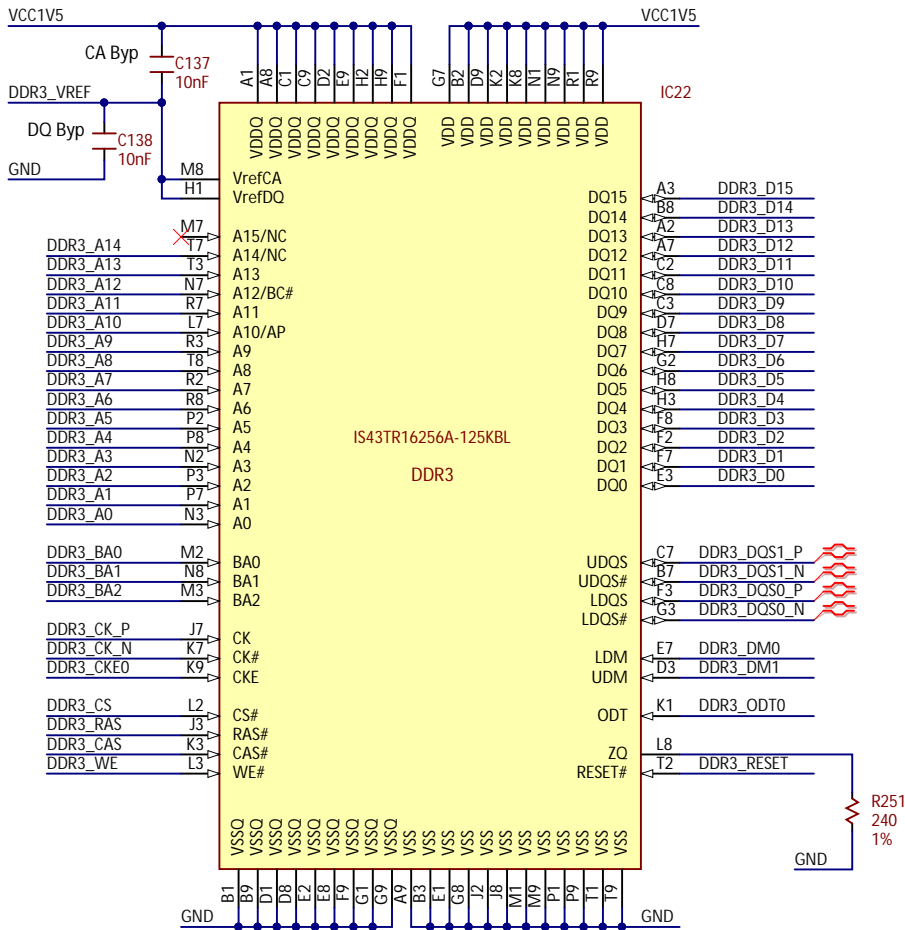


IC20D

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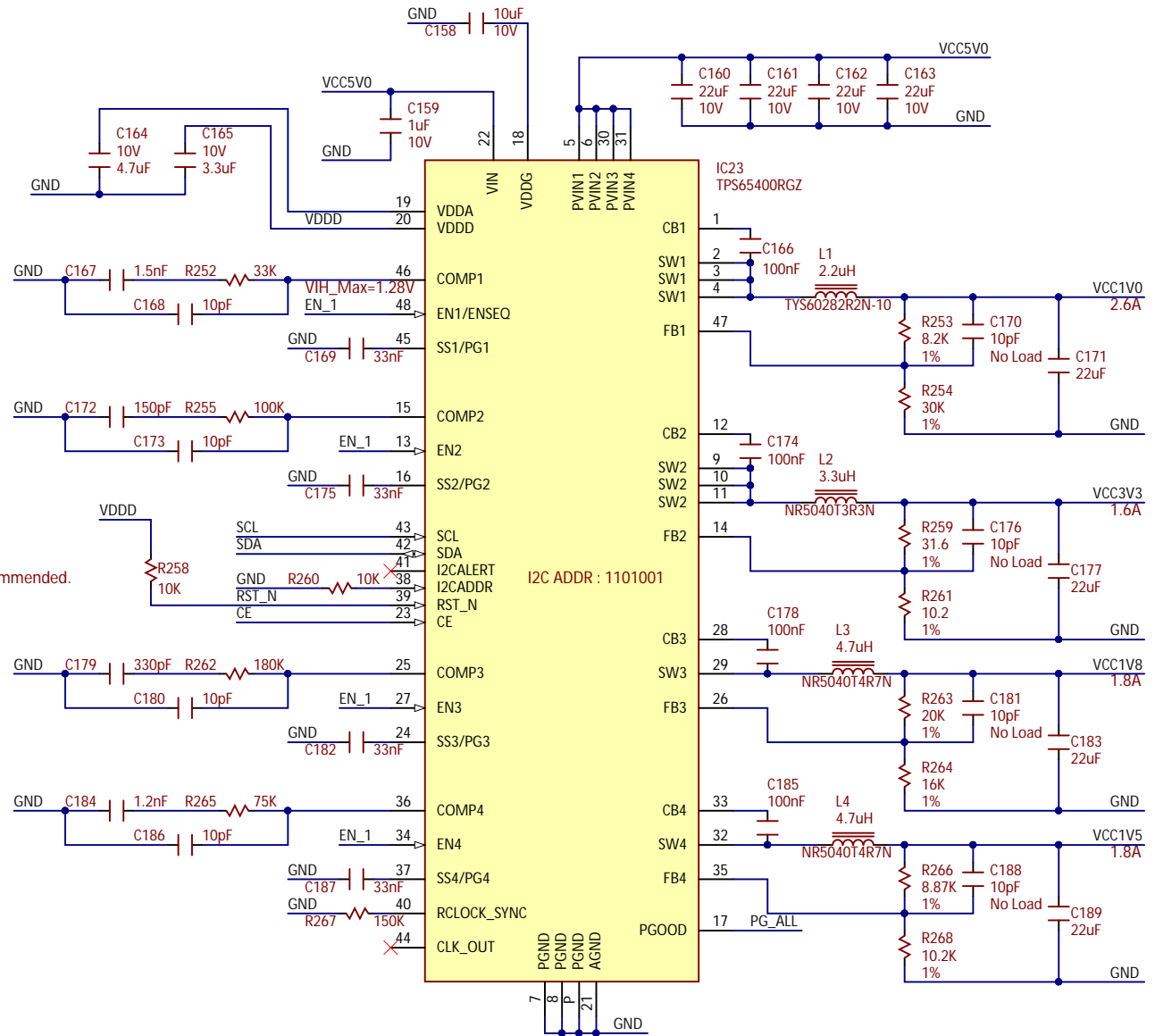
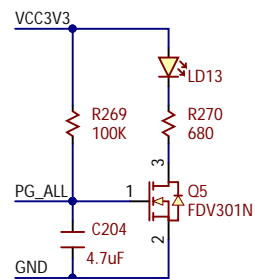
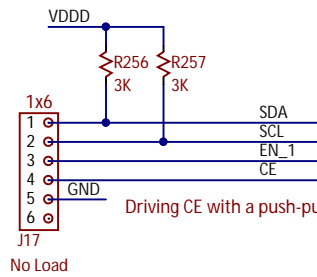


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Circuit FPGA Power		
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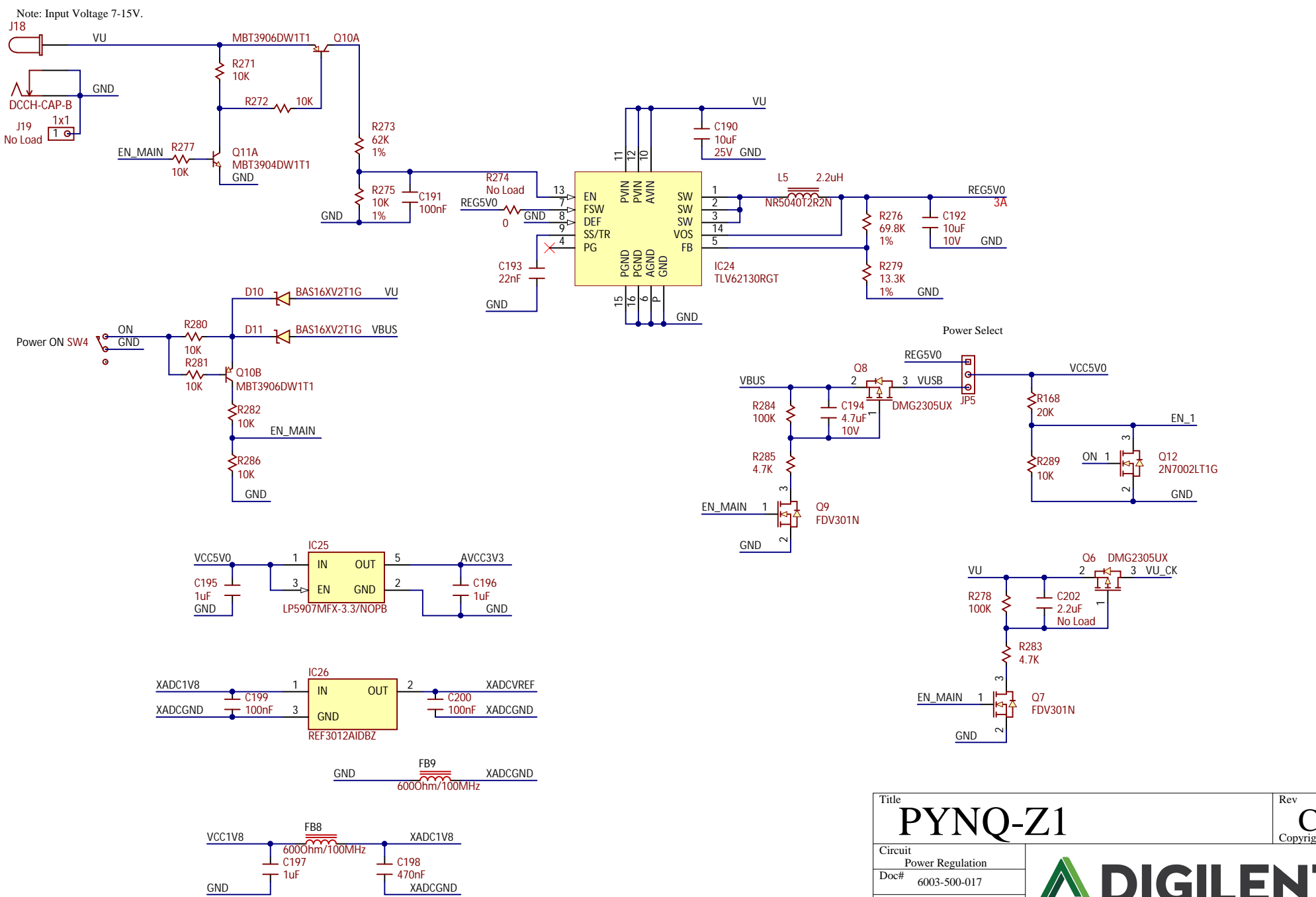


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Circuit DDR3 Memory	Doc# 6003-500-017	 DIGILENT [®] <i>A National Instruments Company</i>
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1. VCC1V0
2. VCC1V8
3. VCC1V5
4. VCC3V3



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