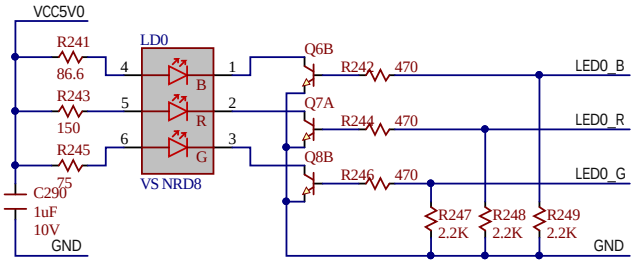
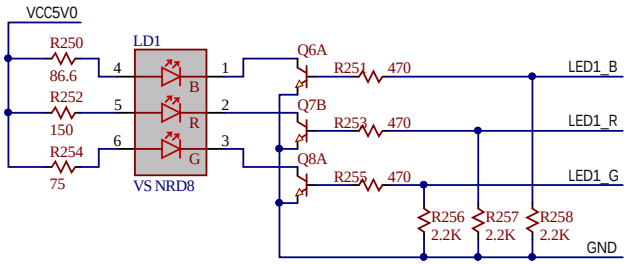
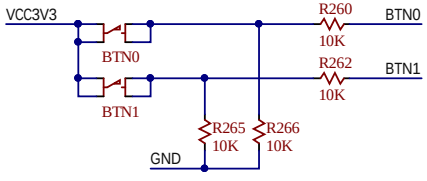
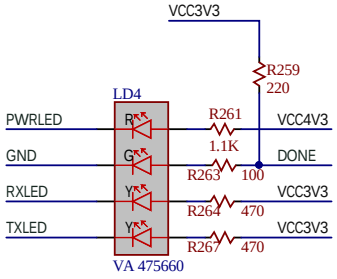
Sheet	Circuit
1.	LEDs, Buttons
2.	PMOD Ports
3.	SYZYGY Ports
4.	Ethernet and SD Card
5.	USB OTG
6.	FPGA Configuration
7.	DDR and MIO Banks
8.	FPGA Banks
9.	FPGA Power
10.	DDR3L Memory
11.	DDR3L Termination
12.	Platform MCU
13.	Power Regulation
14.	Power Regulation
15.	Power Regulation and Sequencer









Foot F1

Foot F2

Title	Eclypse Z7
Rev	B.1
Copyright	2019
Circuit	LEDs, Buttons
Doc#	500-393
Engineer	MTA
Author	GMA
Date	9/11/2019
Sheet#	1 out of 15

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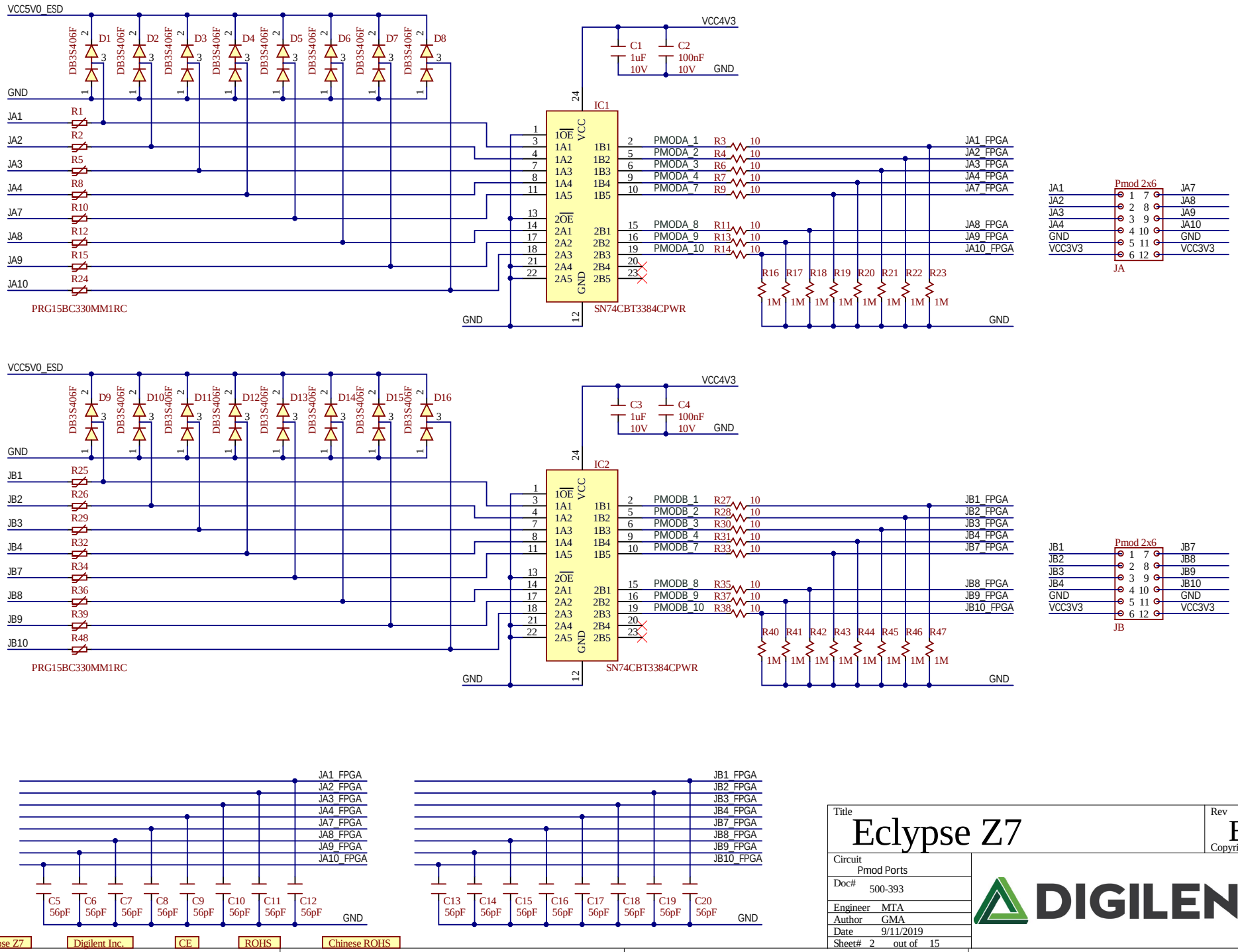

Title	Eclypse Z7
Rev	B.1
Copyright	2019
Circuit	Pmod Ports
Doc#	500-393
Engineer	MTA
Author	GMA
Date	9/11/2019
Sheet#	2 out of 15

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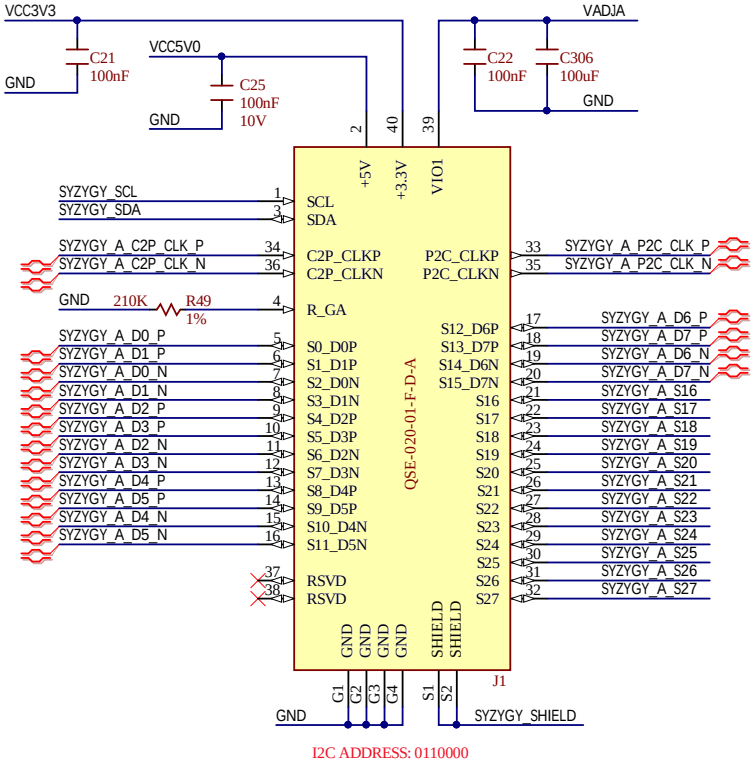

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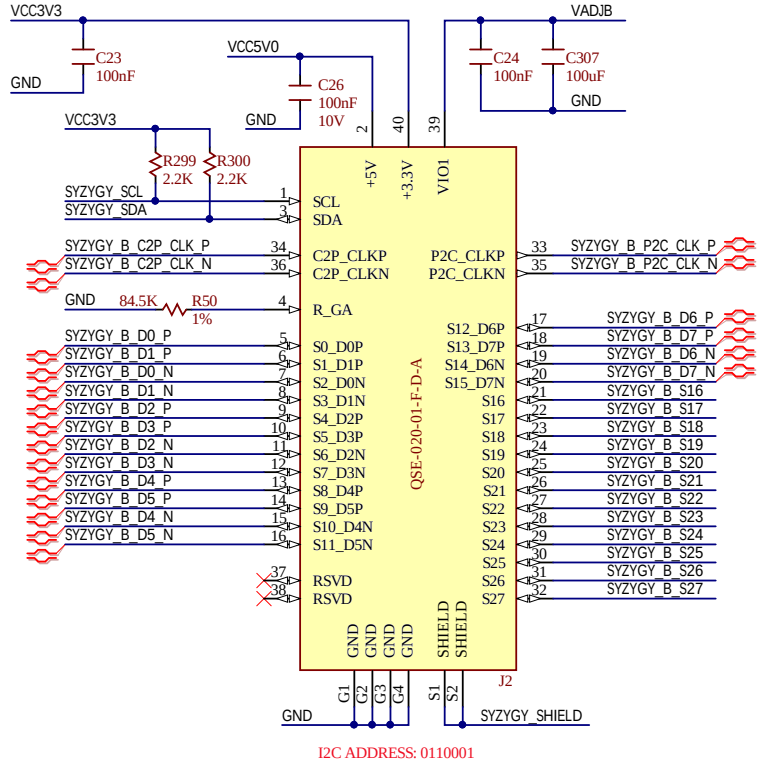

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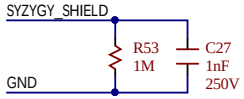

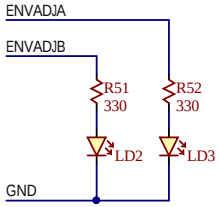

Title	Eclypse Z7
Rev	B.1
Copyright	2019
Circuit	SYZYGY Ports
Doc#	500-393
Engineer	MTA
Author	GMA
Date	9/11/2019
Sheet#	3 out of 15

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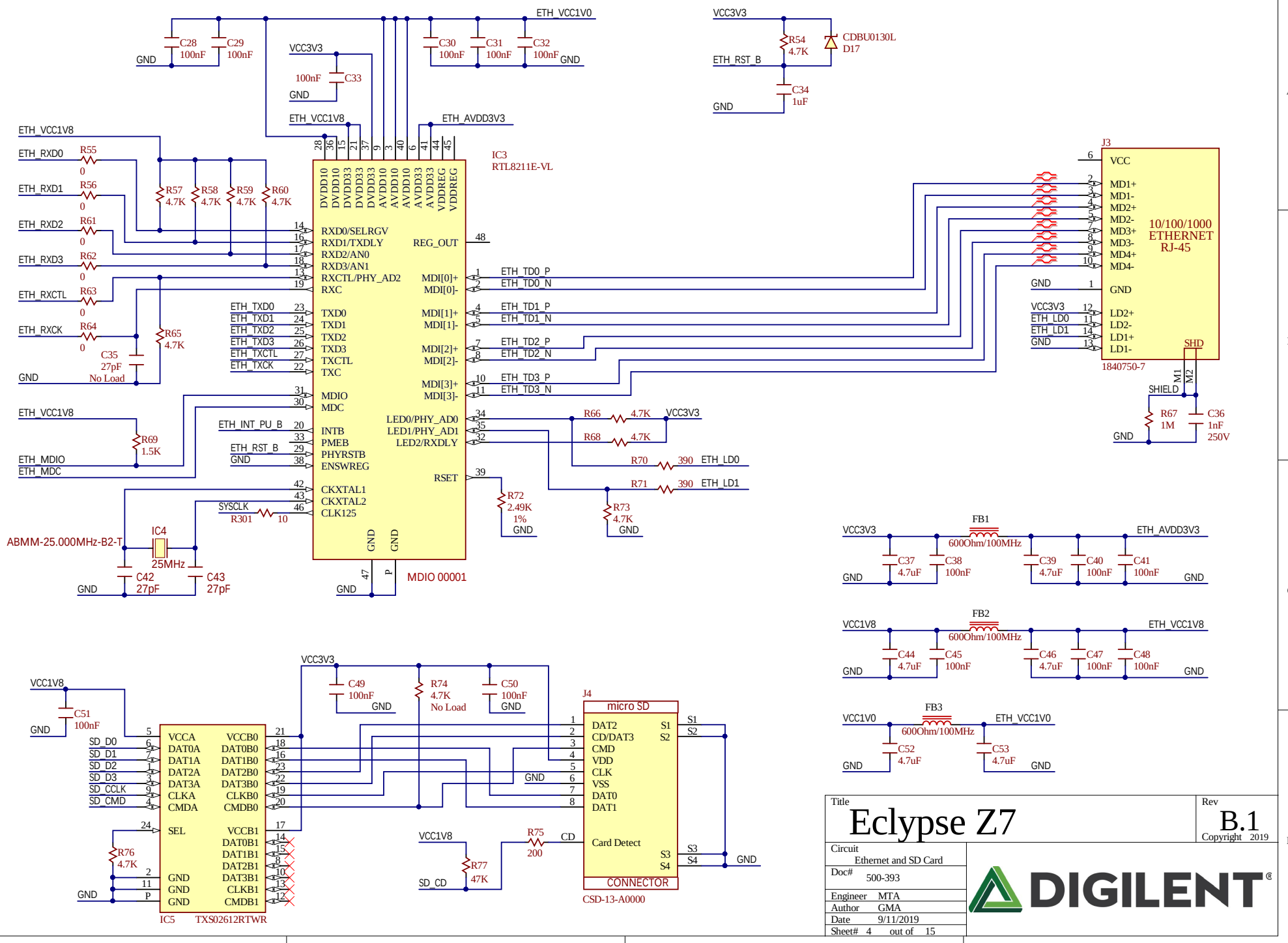
ETH_VCC1V0
C28 100nF
C29 100nF
C30 100nF
C31 100nF
C32 100nF
GND
VCC3V3
C33 100nF
ETH_VCC1V8
ETH_AVDD3V3
IC3
RTL8211E-VL
DVDD10
DVDD33
AVDD10
AVDD33
VDDREG
RXD0/SELRGV
RXD1/TXDLY
RXD2/AN0
RXD3/AN1
RXCTL/PHY_AD2
RXC
TXD0
TXD1
TXD2
TXD3
TXCTL
TXC
MDIO
MDC
INTB
PMEB
PHYRSTB
ENSWREG
CKXTAL1
CKXTAL2
CLK125
REG_OUT
MDI[0]+
MDI[0]-
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
MDI[3]+
MDI[3]-
LED0/PHY_AD0
LED1/PHY_AD1
LED2/RXDLY
RSET
ETH_RXD0
ETH_RXD1
ETH_RXD2
ETH_RXD3
ETH_RXCTL
ETH_RXCK
R55 0
R56 0
R57 4.7K
R58 4.7K
R59 4.7K
R60 4.7K
R61 0
R62 0
R63 0
R64 0
R65 4.7K
C35 27pF No Load
ETH_TXD0
ETH_TXD1
ETH_TXD2
ETH_TXD3
ETH_TXCTL
ETH_TXCK
ETH_TD0_P
ETH_TD0_N
ETH_TD1_P
ETH_TD1_N
ETH_TD2_P
ETH_TD2_N
ETH_TD3_P
ETH_TD3_N
ETH_MDIO
ETH_MDC
R69 1.5K
ETH_INT_PU_B
ETH_RST_B
R66 4.7K
R68 4.7K
R70 390 ETH_LD0
R71 390 ETH_LD1
R72 2.49K 1%
R73 4.7K
SYSCLK
R301 10
IC4
ABMM-25.000MHz-B2-T
25MHz
C42 27pF
C43 27pF
MDIO 00001
VCC3V3
R54 4.7K
CDBU0130L
D17
ETH_RST_B
C34 1uF
J3
10/100/1000
ETHERNET
RJ-45
1840750-7
VCC
MD1+
MD1-
MD2+
MD2-
MD3+
MD3-
MD4+
MD4-
LD2+
LD2-
LD1+
LD1-
SHD
SHIELD
M1
M2
R67 1M
C36 1nF 250V
FB1
600Ohm/100MHz
C37 4.7uF
C38 100nF
C39 4.7uF
C40 100nF
C41 100nF
FB2
C44 4.7uF
C45 100nF
C46 4.7uF
C47 100nF
C48 100nF
FB3
C52 4.7uF
C53 4.7uF
VCC1V8
C51 100nF
C49 100nF
R74 4.7K No Load
C50 100nF
IC5
TXS02612RTWR
VCCA
VCCB0
DAT0A
DAT0B0
DAT1A
DAT1B0
DAT2A
DAT2B0
DAT3A
DAT3B0
CLKA
CLKB0
CMDA
CMDB0
SEL
VCCB1
DAT0B1
DAT1B1
DAT2B1
DAT3B1
CLKB1
CMDB1
SD_D0
SD_D1
SD_D2
SD_D3
SD_CCLK
SD_CMD
R76 4.7K
J4
micro SD
DAT2
CD/DAT3
CMD
VDD
CLK
VSS
DAT0
DAT1
Card Detect
CONNECTOR
CSD-13-A0000
R75 200
R77 47K
SD_CD
CD
S1
S2
S3
S4
Title
Eclypse Z7
Rev
B.1
Copyright 2019
Circuit
Ethernet and SD Card
Doc#
500-393
Engineer MTA
Author GMA
Date 9/11/2019
Sheet# 4 out of 15
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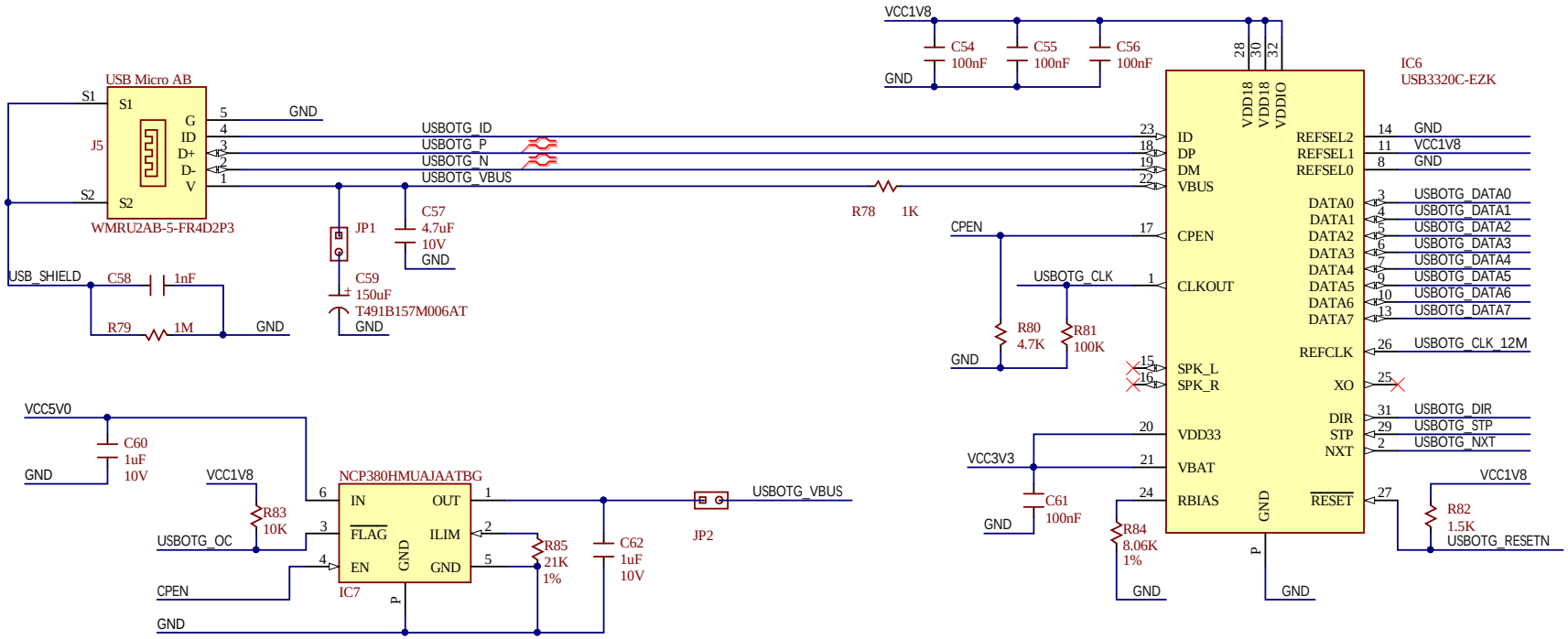

Title	Eclypse Z7
Rev	B.1
Circuit	UST OTG
Doc#	500-393
Engineer	MTA
Author	GMA
Date	9/11/2019
Sheet#	5 out of 15

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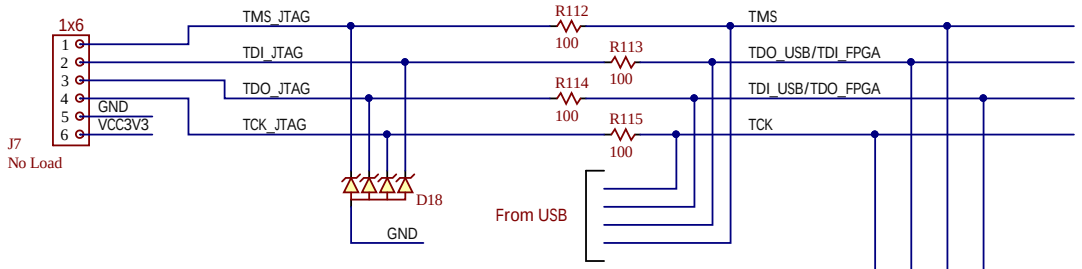

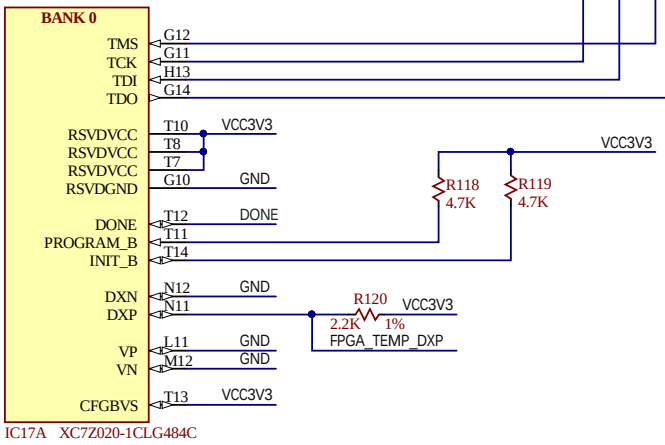

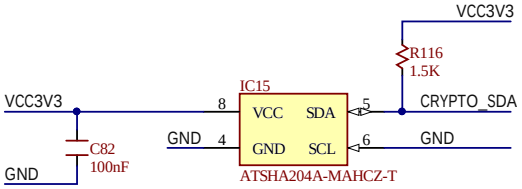

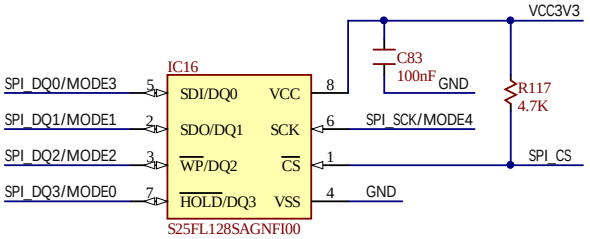

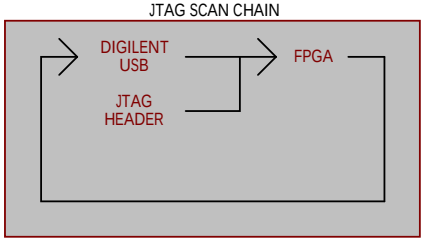

Title	Eclypse Z7
Rev	B.1
Copyright	2019
Circuit	FPGA Configuration
Doc#	500-393
Engineer	MTA
Author	GMA
Date	9/11/2019
Sheet#	6 out of 15

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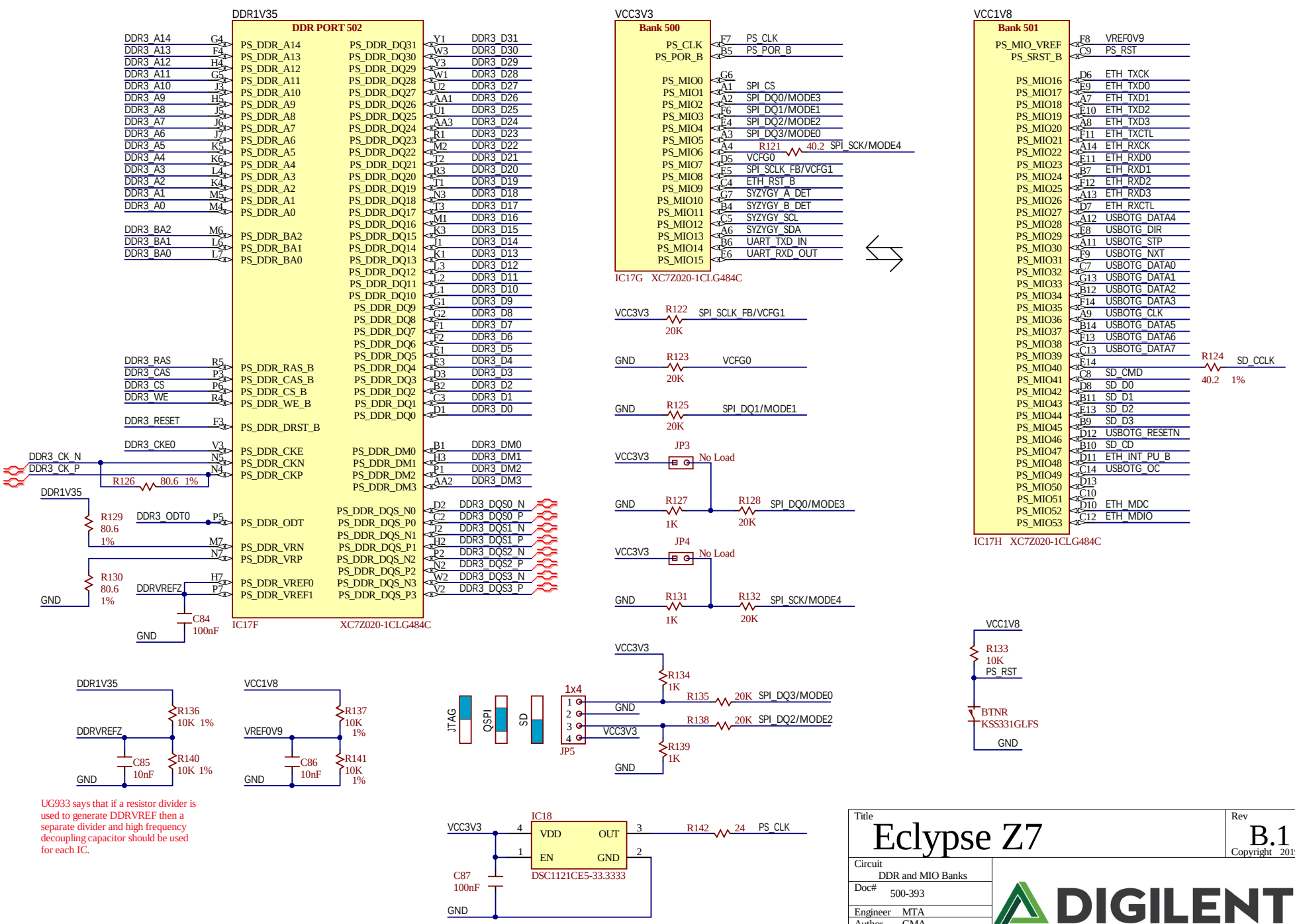
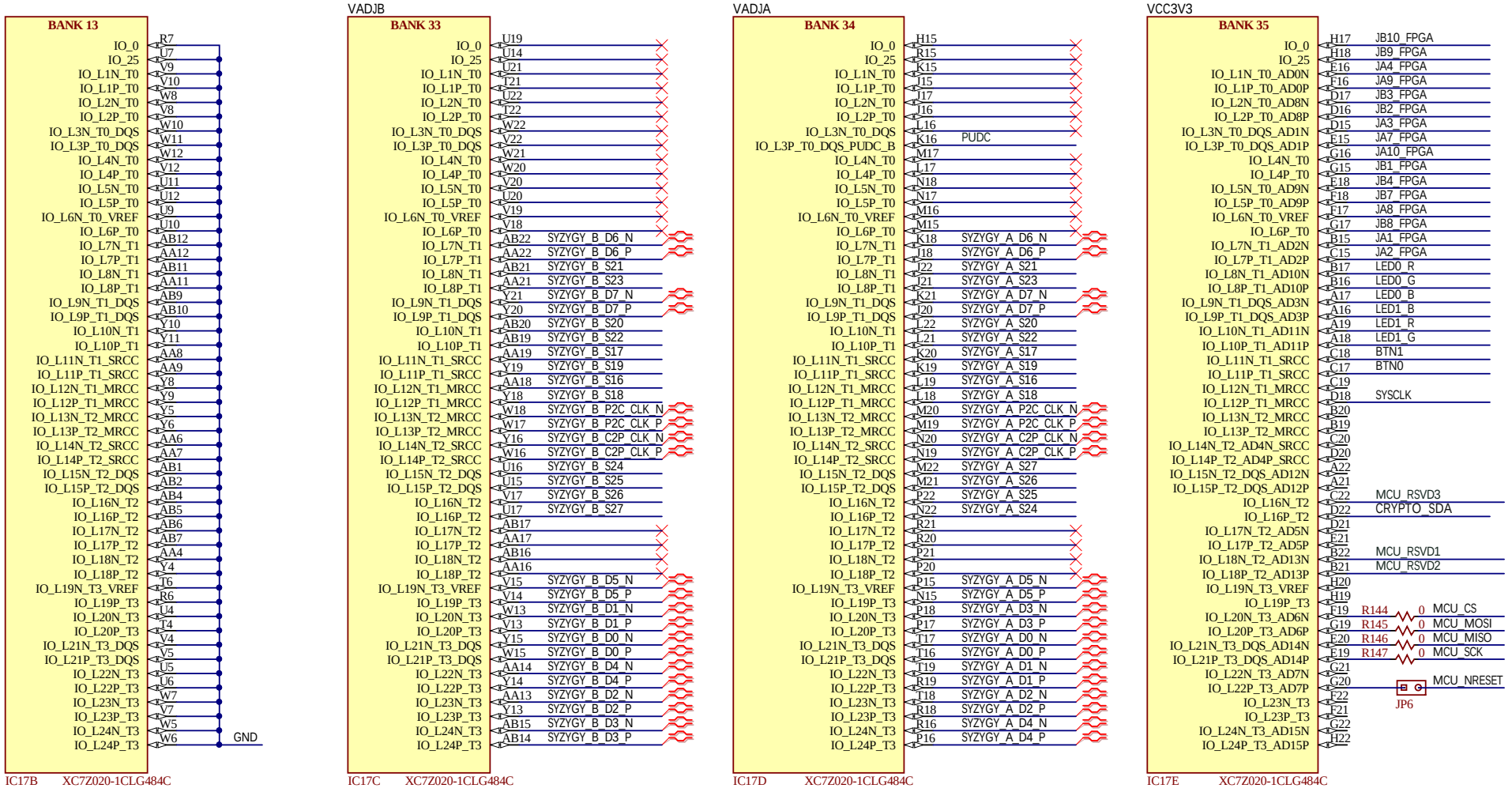

DDR1V35
DDR PORT 502
DDR3_A14 G4
DDR3_A13 F4
DDR3_A12 H4
DDR3_A11 G5
DDR3_A10 J4
DDR3_A9 H5
DDR3_A8 J5
DDR3_A7 J6
DDR3_A6 J7
DDR3_A5 K5
DDR3_A4 K6
DDR3_A3 L4
DDR3_A2 K4
DDR3_A1 M5
DDR3_A0 M4
DDR3_BA2 M6
DDR3_BA1 L6
DDR3_BA0 L7
DDR3_RAS R5
DDR3_CAS P3
DDR3_CS P6
DDR3_WE R4
DDR3_RESET F3
DDR3_CKE0 V3
DDR3_CK_N N5
DDR3_CK_P N4
PS_DDR_A14
PS_DDR_A13
PS_DDR_A12
PS_DDR_A11
PS_DDR_A10
PS_DDR_A9
PS_DDR_A8
PS_DDR_A7
PS_DDR_A6
PS_DDR_A5
PS_DDR_A4
PS_DDR_A3
PS_DDR_A2
PS_DDR_A1
PS_DDR_A0
PS_DDR_BA2
PS_DDR_BA1
PS_DDR_BA0
PS_DDR_RAS_B
PS_DDR_CAS_B
PS_DDR_CS_B
PS_DDR_WE_B
PS_DDR_DRST_B
PS_DDR_CKE
PS_DDR_CKN
PS_DDR_CKP
PS_DDR_ODT
PS_DDR_VRN
PS_DDR_VRP
PS_DDR_VREF0
PS_DDR_VREF1
PS_DDR_DQ31
PS_DDR_DQ30
PS_DDR_DQ29
PS_DDR_DQ28
PS_DDR_DQ27
PS_DDR_DQ26
PS_DDR_DQ25
PS_DDR_DQ24
PS_DDR_DQ23
PS_DDR_DQ22
PS_DDR_DQ21
PS_DDR_DQ20
PS_DDR_DQ19
PS_DDR_DQ18
PS_DDR_DQ17
PS_DDR_DQ16
PS_DDR_DQ15
PS_DDR_DQ14
PS_DDR_DQ13
PS_DDR_DQ12
PS_DDR_DQ11
PS_DDR_DQ10
PS_DDR_DQ9
PS_DDR_DQ8
PS_DDR_DQ7
PS_DDR_DQ6
PS_DDR_DQ5
PS_DDR_DQ4
PS_DDR_DQ3
PS_DDR_DQ2
PS_DDR_DQ1
PS_DDR_DQ0
PS_DDR_DM0
PS_DDR_DM1
PS_DDR_DM2
PS_DDR_DM3
PS_DDR_DQS_N0
PS_DDR_DQS_P0
PS_DDR_DQS_N1
PS_DDR_DQS_P1
PS_DDR_DQS_N2
PS_DDR_DQS_P2
PS_DDR_DQS_N3
PS_DDR_DQS_P3
DDR3_D31 Y1
DDR3_D30 W3
DDR3_D29 Y3
DDR3_D28 W1
DDR3_D27 J2
DDR3_D26 AA1
DDR3_D25 U1
DDR3_D24 AA3
DDR3_D23 R1
DDR3_D22 M2
DDR3_D21 T2
DDR3_D20 R3
DDR3_D19 T1
DDR3_D18 N3
DDR3_D17 P3
DDR3_D16 M1
DDR3_D15 K3
DDR3_D14 J1
DDR3_D13 K1
DDR3_D12 L3
DDR3_D11 L2
DDR3_D10 L1
DDR3_D9 G1
DDR3_D8 G2
DDR3_D7 F1
DDR3_D6 F2
DDR3_D5 E1
DDR3_D4 E3
DDR3_D3 D3
DDR3_D2 B2
DDR3_D1 C3
DDR3_D0 D1
DDR3_DM0 B1
DDR3_DM1 H3
DDR3_DM2 P1
DDR3_DM3 AA2
DDR3_DQS0_N D2
DDR3_DQS0_P C2
DDR3_DQS1_N J2
DDR3_DQS1_P H2
DDR3_DQS2_N P2
DDR3_DQS2_P N2
DDR3_DQS3_N W2
DDR3_DQS3_P V2
DDR3_ODT0 P5
DDRVREFZ H7 P7
R126 80.6 1%
R129 80.6 1%
R130 80.6 1%
C84 100nF
GND
IC17F XC7Z020-1CLG484C
VCC3V3
Bank 500
PS_CLK F7
PS_POR_B B5
PS_MIO0 G6
PS_MIO1 A1 SPI_CS
PS_MIO2 A2 SPI_DQ0/MODE3
PS_MIO3 F6 SPI_DQ1/MODE1
PS_MIO4 E4 SPI_DQ2/MODE2
PS_MIO5 A3 SPI_DQ3/MODE0
PS_MIO6 A4 R121 40.2 SPI_SCK/MODE4
PS_MIO7 D5 VCFG0
PS_MIO8 E5 SPI_SCLK_FB/VCFG1
PS_MIO9 C4 ETH_RST_B
PS_MIO10 G7 SYZYGY_A_DET
PS_MIO11 B4 SYZYGY_B_DET
PS_MIO12 C5 SYZYGY_SCL
PS_MIO13 A6 SYZYGY_SDA
PS_MIO14 B6 UART_TXD_IN
PS_MIO15 E6 UART_RXD_OUT
IC17G XC7Z020-1CLG484C
VCC1V8
Bank 501
PS_MIO_VREF F8 VREF0V9
PS_SRST_B C9 PS_RST
PS_MIO16 D6 ETH_TXCK
PS_MIO17 E9 ETH_TXD0
PS_MIO18 A7 ETH_TXD1
PS_MIO19 E10 ETH_TXD2
PS_MIO20 A8 ETH_TXD3
PS_MIO21 F11 ETH_TXCTL
PS_MIO22 A14 ETH_RXCK
PS_MIO23 E11 ETH_RXD0
PS_MIO24 B7 ETH_RXD1
PS_MIO25 F12 ETH_RXD2
PS_MIO26 A13 ETH_RXD3
PS_MIO27 D7 ETH_RXCTL
PS_MIO28 A12 USBOTG_DATA4
PS_MIO29 E8 USBOTG_DIR
PS_MIO30 A11 USBOTG_STP
PS_MIO31 F9 USBOTG_NXT
PS_MIO32 C7 USBOTG_DATA0
PS_MIO33 G13 USBOTG_DATA1
PS_MIO34 B12 USBOTG_DATA2
PS_MIO35 F14 USBOTG_DATA3
PS_MIO36 A9 USBOTG_CLK
PS_MIO37 B14 USBOTG_DATA5
PS_MIO38 F13 USBOTG_DATA6
PS_MIO39 C13 USBOTG_DATA7
PS_MIO40 E14 R124 40.2 1% SD_CCLK
PS_MIO41 C8 SD_CMD
PS_MIO42 D8 SD_D0
PS_MIO43 B11 SD_D1
PS_MIO44 E13 SD_D2
PS_MIO45 B9 SD_D3
PS_MIO46 D12 USBOTG_RESETN
PS_MIO47 B10 SD_CD
PS_MIO48 D11 ETH_INT_PU_B
PS_MIO49 C14 USBOTG_OC
PS_MIO50 D13
PS_MIO51 C10
PS_MIO52 D10 ETH_MDC
PS_MIO53 C12 ETH_MDIO
IC17H XC7Z020-1CLG484C
VCC3V3 R122 20K SPI_SCLK_FB/VCFG1
GND R123 20K VCFG0
GND R125 20K SPI_DQ1/MODE1
JP3 No Load
GND R127 1K R128 20K SPI_DQ0/MODE3
JP4 No Load
GND R131 1K R132 20K SPI_SCK/MODE4
VCC1V8 R133 10K PS_RST
BTNR KSS331GLFS GND
DDR1V35 R136 10K 1% DDRVREFZ C85 10nF R140 10K 1% GND
VCC1V8 R137 10K 1% VREF0V9 C86 10nF R141 10K 1% GND
JTAG QSPI SD
1x4 JP5
VCC3V3 R134 1K R135 20K SPI_DQ3/MODE0 R138 20K SPI_DQ2/MODE2 R139 1K GND
UG933 says that if a resistor divider is used to generate DDRVREF then a separate divider and high frequency decoupling capacitor should be used for each IC.
IC18
VCC3V3 4 VDD OUT 3 R142 24 PS_CLK
1 EN GND 2
C87 100nF
DSC1121CE5-33.3333
GND
Title
Eclypse Z7
Rev
B.1
Copyright 2019
Circuit
DDR and MIO Banks
Doc#
500-393
Engineer MTA
Author GMA
Date 9/11/2019
Sheet# 7 out of 15
DIGILENT


BANK 13
IO_0 R7
IO_25 U7
IO_L1N_T0 V9
IO_L1P_T0 V10
IO_L2N_T0 W8
IO_L2P_T0 V8
IO_L3N_T0_DQS W10
IO_L3P_T0_DQS W11
IO_L4N_T0 W12
IO_L4P_T0 V12
IO_L5N_T0 U11
IO_L5P_T0 U12
IO_L6N_T0_VREF U9
IO_L6P_T0 U10
IO_L7N_T1 AB12
IO_L7P_T1 AA12
IO_L8N_T1 AB11
IO_L8P_T1 AA11
IO_L9N_T1_DQS AB9
IO_L9P_T1_DQS AB10
IO_L10N_T1 Y10
IO_L10P_T1 Y11
IO_L11N_T1_SRCC AA8
IO_L11P_T1_SRCC AA9
IO_L12N_T1_MRCC Y8
IO_L12P_T1_MRCC Y9
IO_L13N_T2_MRCC Y5
IO_L13P_T2_MRCC Y6
IO_L14N_T2_SRCC AA6
IO_L14P_T2_SRCC AA7
IO_L15N_T2_DQS AB1
IO_L15P_T2_DQS AB2
IO_L16N_T2 AB4
IO_L16P_T2 AB5
IO_L17N_T2 AB6
IO_L17P_T2 AB7
IO_L18N_T2 AA4
IO_L18P_T2 Y4
IO_L19N_T3_VREF Y6
IO_L19P_T3 R6
IO_L20N_T3 U4
IO_L20P_T3 T4
IO_L21N_T3_DQS V4
IO_L21P_T3_DQS V5
IO_L22N_T3 U5
IO_L22P_T3 V6
IO_L23N_T3 W7
IO_L23P_T3 V7
IO_L24N_T3 W5
IO_L24P_T3 W6
GND
IC17B XC7Z020-1CLG484C
VADJB
BANK 33
IO_0 U19
IO_25 U14
IO_L1N_T0 U21
IO_L1P_T0 T21
IO_L2N_T0 U22
IO_L2P_T0 T22
IO_L3N_T0_DQS W22
IO_L3P_T0_DQS V22
IO_L4N_T0 W21
IO_L4P_T0 W20
IO_L5N_T0 Y20
IO_L5P_T0 U20
IO_L6N_T0_VREF V19
IO_L6P_T0 V18
IO_L7N_T1 AB22 SYZYGY_B_D6_N
IO_L7P_T1 AA22 SYZYGY_B_D6_P
IO_L8N_T1 AB21 SYZYGY_B_S21
IO_L8P_T1 AA21 SYZYGY_B_S23
IO_L9N_T1_DQS Y21 SYZYGY_B_D7_N
IO_L9P_T1_DQS Y20 SYZYGY_B_D7_P
IO_L10N_T1 AB20 SYZYGY_B_S20
IO_L10P_T1 AB19 SYZYGY_B_S22
IO_L11N_T1_SRCC AA19 SYZYGY_B_S17
IO_L11P_T1_SRCC Y19 SYZYGY_B_S19
IO_L12N_T1_MRCC AA18 SYZYGY_B_S16
IO_L12P_T1_MRCC Y18 SYZYGY_B_S18
IO_L13N_T2_MRCC W18 SYZYGY_B_P2C_CLK_N
IO_L13P_T2_MRCC W17 SYZYGY_B_P2C_CLK_P
IO_L14N_T2_SRCC Y16 SYZYGY_B_C2P_CLK_N
IO_L14P_T2_SRCC W16 SYZYGY_B_C2P_CLK_P
IO_L15N_T2_DQS U16 SYZYGY_B_S24
IO_L15P_T2_DQS U15 SYZYGY_B_S25
IO_L16N_T2 V17 SYZYGY_B_S26
IO_L16P_T2 U17 SYZYGY_B_S27
IO_L17N_T2 AB17
IO_L17P_T2 AA17
IO_L18N_T2 AB16
IO_L18P_T2 AA16
IO_L19N_T3_VREF V15 SYZYGY_B_D5_N
IO_L19P_T3 V14 SYZYGY_B_D5_P
IO_L20N_T3 W13 SYZYGY_B_D1_N
IO_L20P_T3 V13 SYZYGY_B_D1_P
IO_L21N_T3_DQS Y15 SYZYGY_B_D0_N
IO_L21P_T3_DQS W15 SYZYGY_B_D0_P
IO_L22N_T3 AA14 SYZYGY_B_D4_N
IO_L22P_T3 Y14 SYZYGY_B_D4_P
IO_L23N_T3 AA13 SYZYGY_B_D2_N
IO_L23P_T3 Y13 SYZYGY_B_D2_P
IO_L24N_T3 AB15 SYZYGY_B_D3_N
IO_L24P_T3 AB14 SYZYGY_B_D3_P
IC17C XC7Z020-1CLG484C
VADJA
BANK 34
IO_0 H15
IO_25 R15
IO_L1N_T0 K15
IO_L1P_T0 J15
IO_L2N_T0 J17
IO_L2P_T0 J16
IO_L3N_T0_DQS L16
IO_L3P_T0_DQS_PUDC_B K16 PUDC
IO_L4N_T0 M17
IO_L4P_T0 L17
IO_L5N_T0 N18
IO_L5P_T0 N17
IO_L6N_T0_VREF M16
IO_L6P_T0 M15
IO_L7N_T1 K18 SYZYGY_A_D6_N
IO_L7P_T1 J18 SYZYGY_A_D6_P
IO_L8N_T1 J22 SYZYGY_A_S21
IO_L8P_T1 J21 SYZYGY_A_S23
IO_L9N_T1_DQS K21 SYZYGY_A_D7_N
IO_L9P_T1_DQS J20 SYZYGY_A_D7_P
IO_L10N_T1 L22 SYZYGY_A_S20
IO_L10P_T1 L21 SYZYGY_A_S22
IO_L11N_T1_SRCC K20 SYZYGY_A_S17
IO_L11P_T1_SRCC K19 SYZYGY_A_S19
IO_L12N_T1_MRCC L19 SYZYGY_A_S16
IO_L12P_T1_MRCC L18 SYZYGY_A_S18
IO_L13N_T2_MRCC M20 SYZYGY_A_P2C_CLK_N
IO_L13P_T2_MRCC M19 SYZYGY_A_P2C_CLK_P
IO_L14N_T2_SRCC N20 SYZYGY_A_C2P_CLK_N
IO_L14P_T2_SRCC N19 SYZYGY_A_C2P_CLK_P
IO_L15N_T2_DQS M22 SYZYGY_A_S27
IO_L15P_T2_DQS M21 SYZYGY_A_S26
IO_L16N_T2 P22 SYZYGY_A_S25
IO_L16P_T2 N22 SYZYGY_A_S24
IO_L17N_T2 R21
IO_L17P_T2 R20
IO_L18N_T2 P21
IO_L18P_T2 P20
IO_L19N_T3_VREF P15 SYZYGY_A_D5_N
IO_L19P_T3 N15 SYZYGY_A_D5_P
IO_L20N_T3 P18 SYZYGY_A_D3_N
IO_L20P_T3 P17 SYZYGY_A_D3_P
IO_L21N_T3_DQS T17 SYZYGY_A_D0_N
IO_L21P_T3_DQS T16 SYZYGY_A_D0_P
IO_L22N_T3 T19 SYZYGY_A_D1_N
IO_L22P_T3 R19 SYZYGY_A_D1_P
IO_L23N_T3 T18 SYZYGY_A_D2_N
IO_L23P_T3 R18 SYZYGY_A_D2_P
IO_L24N_T3 R16 SYZYGY_A_D4_N
IO_L24P_T3 P16 SYZYGY_A_D4_P
IC17D XC7Z020-1CLG484C
VCC3V3
BANK 35
IO_0 H17 JB10_FPGA
IO_25 H18 JB9_FPGA
IO_L1N_T0_AD0N E16 JA4_FPGA
IO_L1P_T0_AD0P F16 JA9_FPGA
IO_L2N_T0_AD8N D17 JB3_FPGA
IO_L2P_T0_AD8P D16 JB2_FPGA
IO_L3N_T0_DQS_AD1N D15 JA3_FPGA
IO_L3P_T0_DQS_AD1P E15 JA7_FPGA
IO_L4N_T0 G16 JA10_FPGA
IO_L4P_T0 G15 JB1_FPGA
IO_L5N_T0_AD9N F18 JB4_FPGA
IO_L5P_T0_AD9P F18 JB7_FPGA
IO_L6N_T0_VREF F17 JA8_FPGA
IO_L6P_T0 G17 JB8_FPGA
IO_L7N_T1_AD2N B15 JA1_FPGA
IO_L7P_T1_AD2P C15 JA2_FPGA
IO_L8N_T1_AD10N B17 LED0_R
IO_L8P_T1_AD10P B16 LED0_G
IO_L9N_T1_DQS_AD3N A17 LED0_B
IO_L9P_T1_DQS_AD3P A16 LED1_B
IO_L10N_T1_AD11N A19 LED1_R
IO_L10P_T1_AD11P A18 LED1_G
IO_L11N_T1_SRCC C18 BTN1
IO_L11P_T1_SRCC C17 BTN0
IO_L12N_T1_MRCC C19
IO_L12P_T1_MRCC D18 SYSCLK
IO_L13N_T2_MRCC B20
IO_L13P_T2_MRCC B19
IO_L14N_T2_AD4N_SRCC C20
IO_L14P_T2_AD4P_SRCC D20
IO_L15N_T2_DQS_AD12N A22
IO_L15P_T2_DQS_AD12P A21
IO_L16N_T2 C22 MCU_RSVD3
IO_L16P_T2 D22 CRYPTO_SDA
IO_L17N_T2_AD5N D21
IO_L17P_T2_AD5P E21
IO_L18N_T2_AD13N B22 MCU_RSVD1
IO_L18P_T2_AD13P B21 MCU_RSVD2
IO_L19N_T3_VREF H20
IO_L19P_T3 H19
IO_L20N_T3_AD6N F19 R144 0 MCU_CS
IO_L20P_T3_AD6P G19 R145 0 MCU_MOSI
IO_L21N_T3_DQS_AD14N E20 R146 0 MCU_MISO
IO_L21P_T3_DQS_AD14P F19 R147 0 MCU_SCK
IO_L22N_T3_AD7N G21
IO_L22P_T3_AD7P G20 MCU_NRESET
IO_L23N_T3 F22 JP6
IO_L23P_T3 F21
IO_L24N_T3_AD15N G22
IO_L24P_T3_AD15P H22
IC17E XC7Z020-1CLG484C
UG933 says to connect the I/O pins of an unused bank to the same potential as the VCCO pins of that bank.
SYZYGY_B_P2C_CLK_P
1% R148 80.6
No Load
SYZYGY_B_P2C_CLK_N
SYZYGY_A_P2C_CLK_P
1% R150 80.6
No Load
SYZYGY_A_P2C_CLK_N
VADJA
No Load R149 1K
PUDC
R151 1K
GND
Title
Eclypse Z7
Rev
B.1
Copyright 2019
Circuit
FPGA Banks
Doc# 500-393
Engineer MTA
Author GMA
Date 9/11/2019
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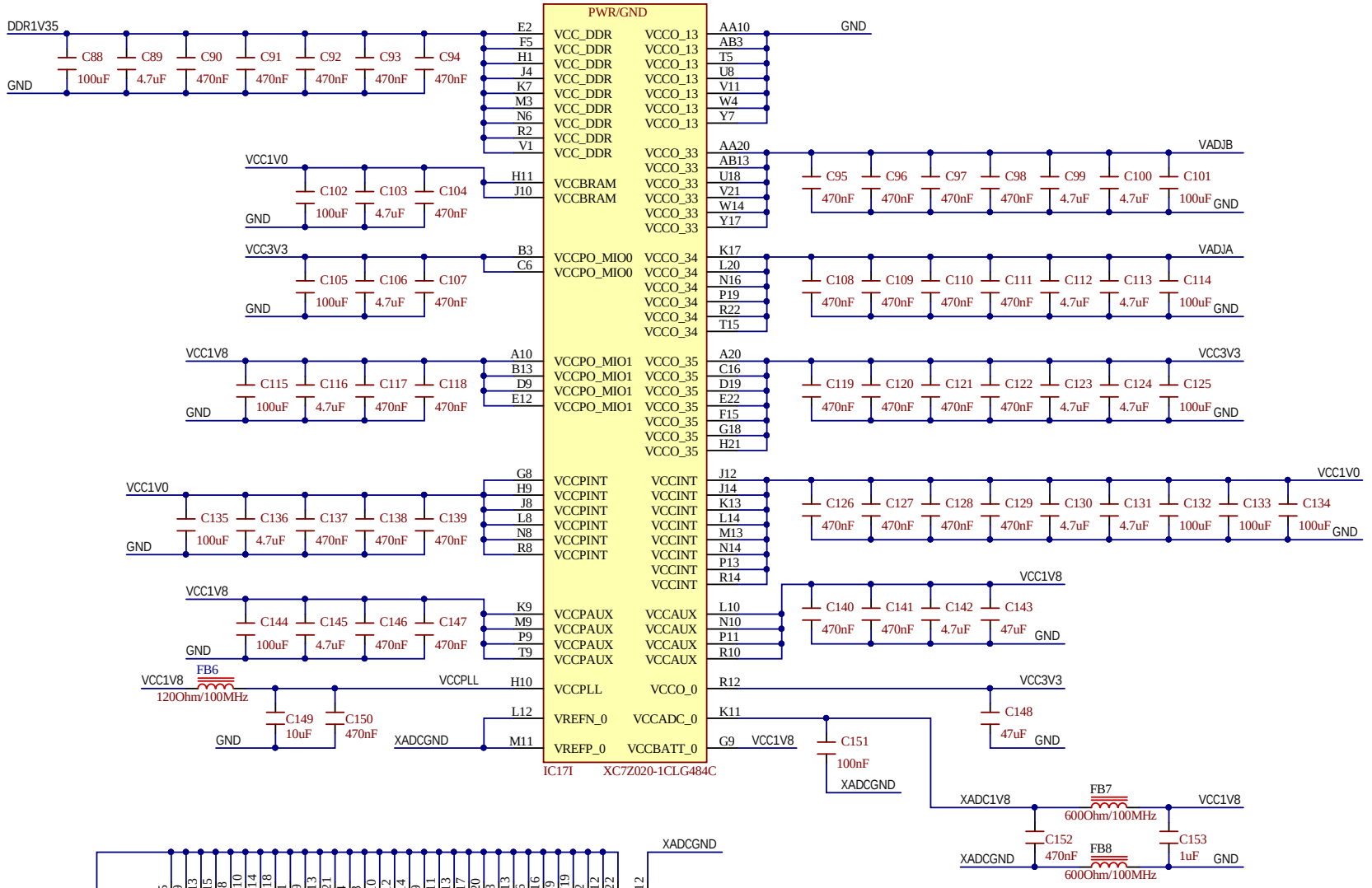

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Rev	B.1
Copyright	2019
Circuit	FPGA Power
Doc#	500-393
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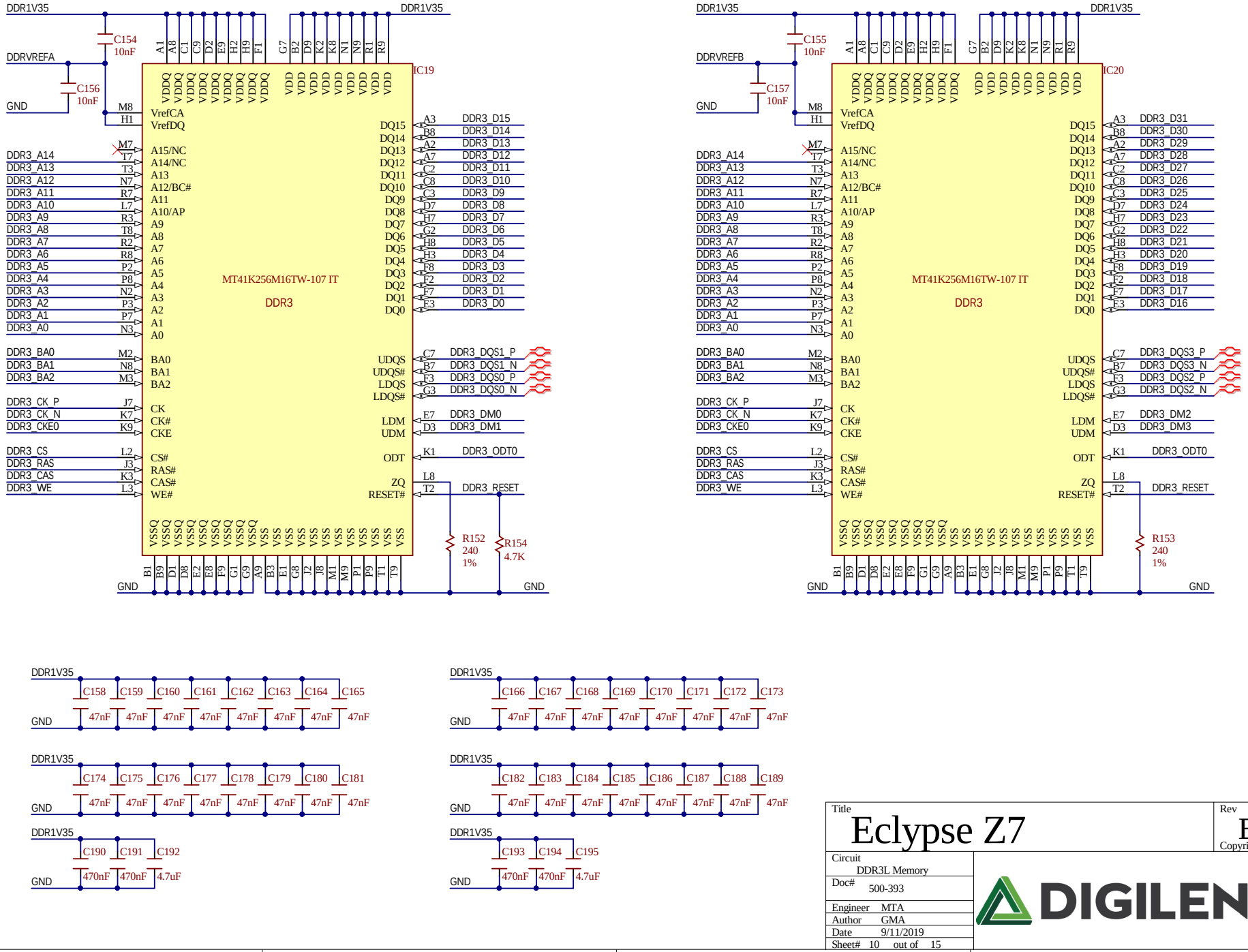

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Circuit	DDR3L Memory
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Author	GMA
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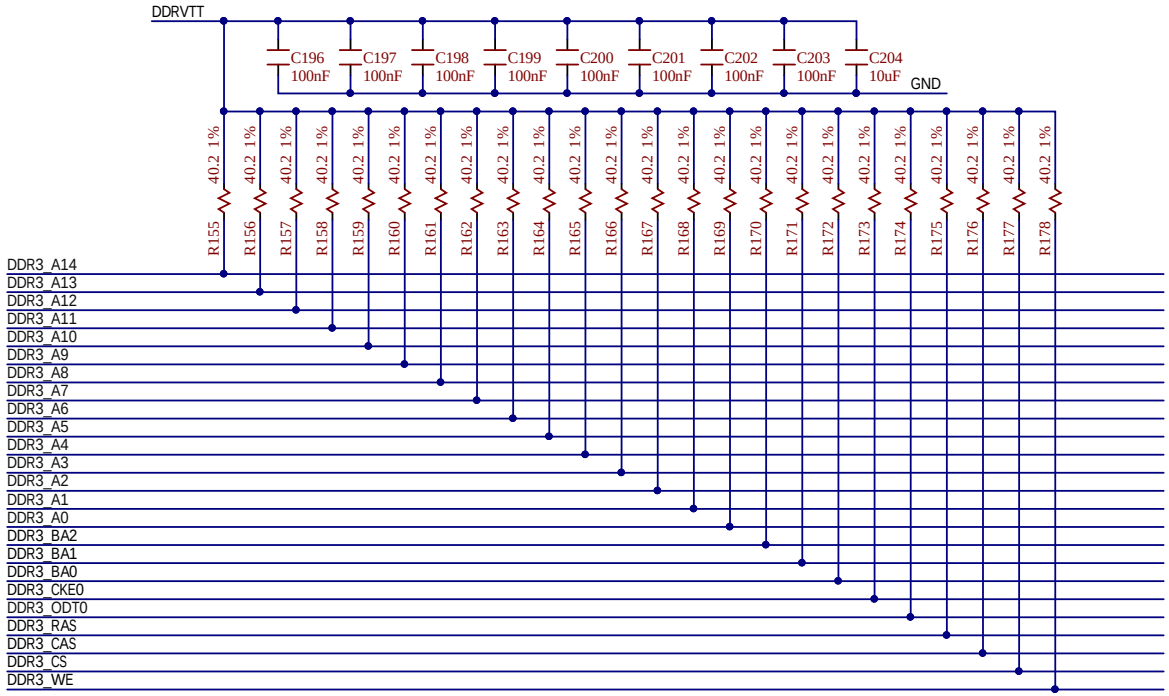
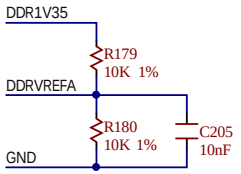
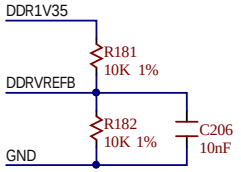
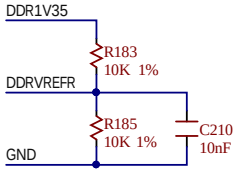
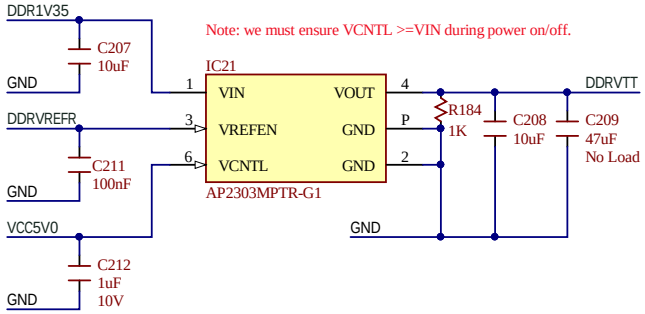


UG933 says that if a resistor divider is used to generate DDRVREF then a separate divider and high frequency decoupling capacitor should be used for each IC.









Title	Eclypse Z7
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Circuit	DDR3L Termination
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Author	GMA
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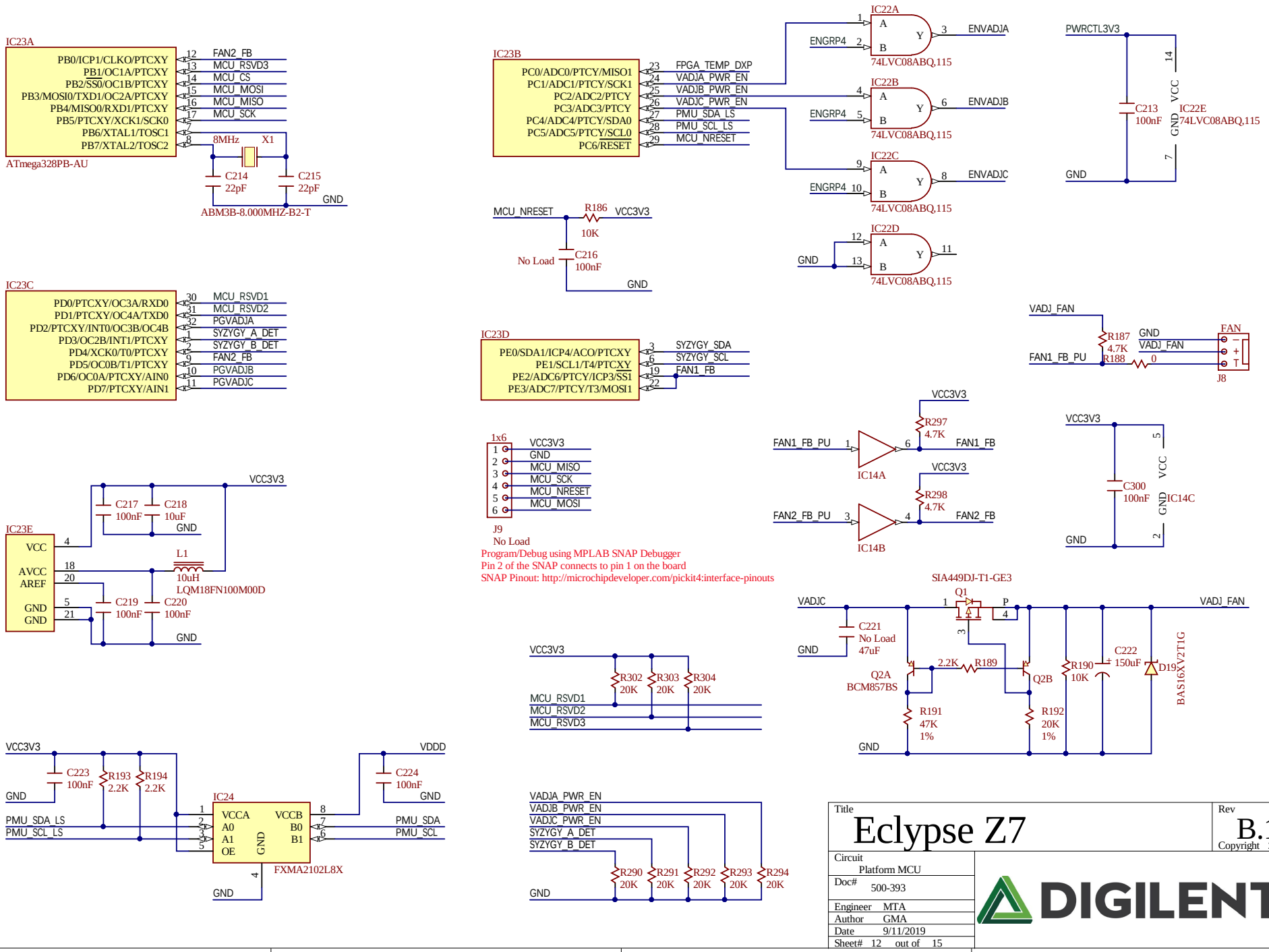
IC23A
PB0/ICP1/CLKO/PTCXY
PB1/OC1A/PTCXY
PB2/SS0/OC1B/PTCXY
PB3/MOSI0/TXD1/OC2A/PTCXY
PB4/MISO0/RXD1/PTCXY
PB5/PTCXY/XCK1/SCK0
PB6/XTAL1/TOSC1
PB7/XTAL2/TOSC2
12 FAN2_FB
13 MCU_RSVD3
14 MCU_CS
15 MCU_MOSI
16 MCU_MISO
17 MCU_SCK
8MHz
X1
C214 22pF
C215 22pF
GND
ATmega328PB-AU
ABM3B-8.000MHZ-B2-T
IC23B
PC0/ADC0/PTCY/MISO1
PC1/ADC1/PTCY/SCK1
PC2/ADC2/PTCY
PC3/ADC3/PTCY
PC4/ADC4/PTCY/SDA0
PC5/ADC5/PTCY/SCL0
PC6/RESET
23 FPGA_TEMP_DXP
24 VADJA_PWR_EN
25 VADJB_PWR_EN
26 VADJC_PWR_EN
27 PMU_SDA_LS
28 PMU_SCL_LS
29 MCU_NRESET
IC22A
ENGRP4
ENVADJA
74LVC08ABQ,115
IC22B
ENGRP4
ENVADJB
74LVC08ABQ,115
IC22C
ENGRP4
ENVADJC
74LVC08ABQ,115
IC22D
GND
74LVC08ABQ,115
PWRCTL3V3
C213 100nF
VCC
GND
IC22E
74LVC08ABQ,115
GND
MCU_NRESET
R186 10K
VCC3V3
No Load
C216 100nF
GND
IC23C
PD0/PTCXY/OC3A/RXD0
PD1/PTCXY/OC4A/TXD0
PD2/PTCXY/INT0/OC3B/OC4B
PD3/OC2B/INT1/PTCXY
PD4/XCK0/T0/PTCXY
PD5/OC0B/T1/PTCXY
PD6/OC0A/PTCXY/AIN0
PD7/PTCXY/AIN1
30 MCU_RSVD1
31 MCU_RSVD2
32 PGVADJA
1 SYZYGY_A_DET
2 SYZYGY_B_DET
9 FAN2_FB
10 PGVADJB
11 PGVADJC
IC23D
PE0/SDA1/ICP4/ACO/PTCXY
PE1/SCL1/T4/PTCXY
PE2/ADC6/PTCY/ICP3/SS1
PE3/ADC7/PTCY/T3/MOSI1
3 SYZYGY_SDA
6 SYZYGY_SCL
19 FAN1_FB
22
VADJ_FAN
R187 4.7K
R188
GND
VADJ_FAN
FAN1_FB_PU
FAN
J8
1x6
1 VCC3V3
2 GND
3 MCU_MISO
4 MCU_SCK
5 MCU_NRESET
6 MCU_MOSI
J9
No Load
Program/Debug using MPLAB SNAP Debugger
Pin 2 of the SNAP connects to pin 1 on the board
SNAP Pinout: http://microchipdeveloper.com/pickit4:interface-pinouts
VCC3V3
R297 4.7K
FAN1_FB_PU
FAN1_FB
IC14A
R298 4.7K
FAN2_FB_PU
FAN2_FB
IC14B
C300 100nF
IC14C
VCC3V3
C217 100nF
C218 10uF
GND
IC23E
VCC
AVCC
AREF
GND
GND
L1
10uH
LQM18FN100M00D
C219 100nF
C220 100nF
GND
SIA449DJ-T1-GE3
Q1
VADJC
VADJ_FAN
C221 No Load 47uF
GND
Q2A BCM857BS
2.2K
R189
Q2B
R190 10K
C222 150uF
D1
BAS16XV2T1G
R191 47K 1%
R192 20K 1%
GND
VCC3V3
R302 20K
R303 20K
R304 20K
MCU_RSVD1
MCU_RSVD2
MCU_RSVD3
VCC3V3
C223 100nF
R193 2.2K
R194 2.2K
GND
PMU_SDA_LS
PMU_SCL_LS
IC24
VCCA
A0
A1
OE
GND
VCCB
B0
B1
FXMA2102L8X
VDDD
C224 100nF
GND
PMU_SDA
PMU_SCL
GND
VADJA_PWR_EN
VADJB_PWR_EN
VADJC_PWR_EN
SYZYGY_A_DET
SYZYGY_B_DET
R290 20K
R291 20K
R292 20K
R293 20K
R294 20K
GND
Title
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Circuit
Platform MCU
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Author GMA
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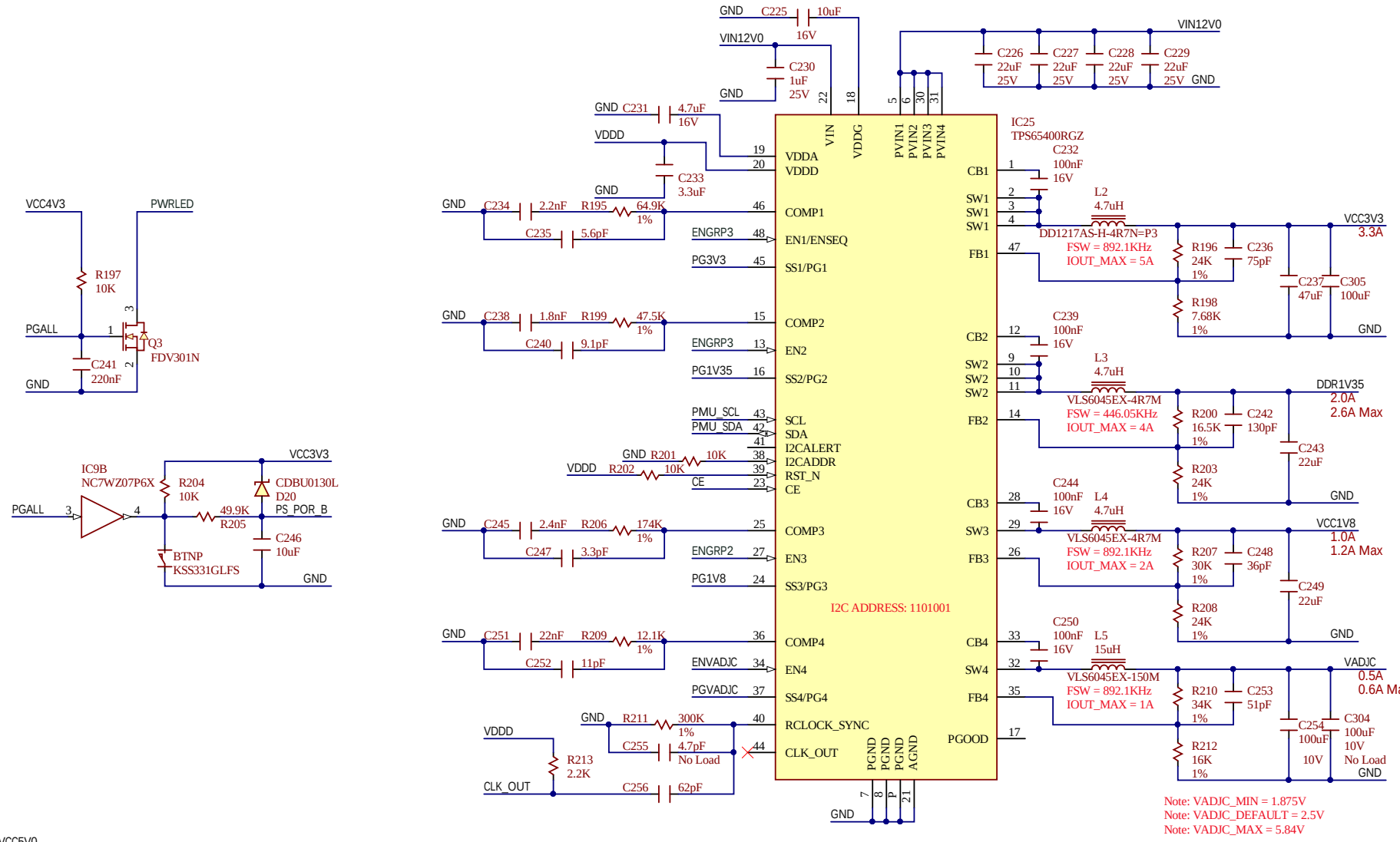

Title	Eclypse Z7
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Circuit	Power Regulation
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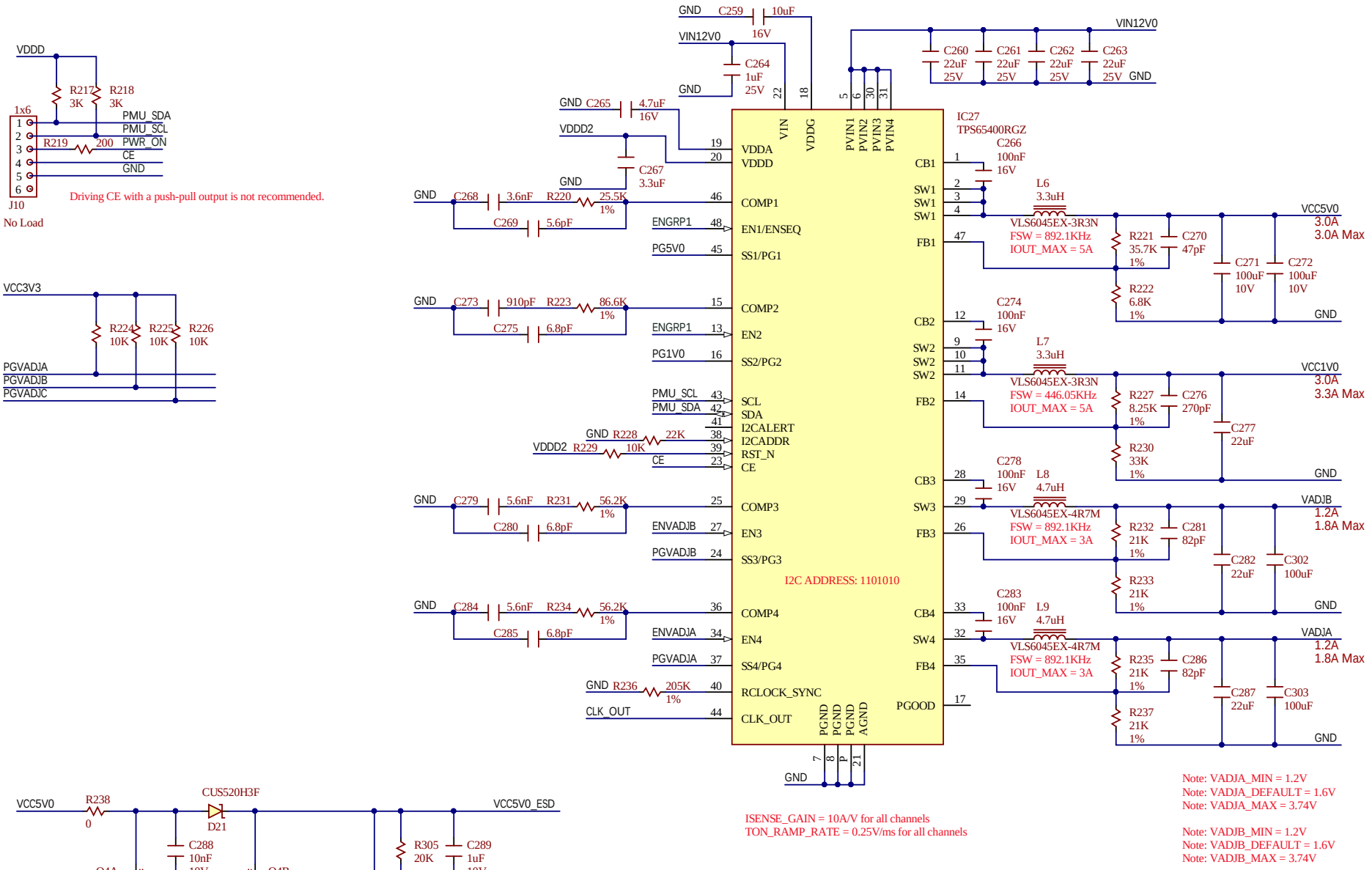
VDDD
R217 3K
R218 3K
1x6
PMU_SDA
PMU_SCL
R219 200
PWR_ON
CE
GND
J10
No Load
Driving CE with a push-pull output is not recommended.
VCC3V3
R224 10K
R225 10K
R226 10K
PGVADJA
PGVADJB
PGVADJC
GND C259 10uF 16V
VIN12V0
C264 1uF 25V
GND C265 4.7uF 16V
VDDD2
C267 3.3uF
GND C268 3.6nF R220 25.5K 1%
C269 5.6pF
ENGRP1
PG5V0
GND C273 910pF R223 86.6K 1%
C275 6.8pF
ENGRP1
PG1V0
PMU_SCL
PMU_SDA
GND R228 22K
VDDD2 R229 10K
CE
GND C279 5.6nF R231 56.2K 1%
C280 6.8pF
ENVADJB
PGVADJB
GND C284 5.6nF R234 56.2K 1%
C285 6.8pF
ENVADJA
PGVADJA
GND R236 205K 1%
CLK_OUT
VIN
VDDG
PVIN1
PVIN2
PVIN3
PVIN4
VDDA
VDDD
COMP1
EN1/ENSEQ
SS1/PG1
COMP2
EN2
SS2/PG2
SCL
SDA
I2CALERT
I2CADDR
RST_N
CE
COMP3
EN3
SS3/PG3
I2C ADDRESS: 1101010
COMP4
EN4
SS4/PG4
RCLOCK_SYNC
CLK_OUT
PGND
PGND
PGND
AGND
PGOOD
GND
VIN12V0
C260 22uF 25V
C261 22uF 25V
C262 22uF 25V
C263 22uF 25V GND
IC27
TPS65400RGZ
CB1
SW1
SW1
SW1
FB1
C266 100nF 16V
L6 3.3uH
VLS6045EX-3R3N
FSW = 892.1KHz
IOUT_MAX = 5A
R221 35.7K 1%
C270 47pF
R222 6.8K 1%
C271 100uF 10V
C272 100uF 10V
VCC5V0
3.0A
3.0A Max
GND
CB2
SW2
SW2
SW2
FB2
C274 100nF 16V
L7 3.3uH
VLS6045EX-3R3N
FSW = 446.05KHz
IOUT_MAX = 5A
R227 8.25K 1%
C276 270pF
R230 33K 1%
C277 22uF
VCC1V0
3.0A
3.3A Max
GND
CB3
SW3
FB3
C278 100nF 16V
L8 4.7uH
VLS6045EX-4R7M
FSW = 892.1KHz
IOUT_MAX = 3A
R232 21K 1%
C281 82pF
R233 21K 1%
C282 22uF
C302 100uF
VADJB
1.2A
1.8A Max
GND
CB4
SW4
FB4
C283 100nF 16V
L9 4.7uH
VLS6045EX-4R7M
FSW = 892.1KHz
IOUT_MAX = 3A
R235 21K 1%
C286 82pF
R237 21K 1%
C287 22uF
C303 100uF
VADJA
1.2A
1.8A Max
GND
ISENSE_GAIN = 10A/V for all channels
TON_RAMP_RATE = 0.25V/ms for all channels
Note: VADJA_MIN = 1.2V
Note: VADJA_DEFAULT = 1.6V
Note: VADJA_MAX = 3.74V
Note: VADJB_MIN = 1.2V
Note: VADJB_DEFAULT = 1.6V
Note: VADJB_MAX = 3.74V
VCC5V0
R238 0
CUS520H3F
D21
C288 10nF 10V
Q4A MBT3906DW1T1
Q4B MBT3906DW1T1
R239 2.2K
R240 2.2K
Q5 FZT869
R305 20K
C289 1uF 10V
VCC5V0_ESD
GND
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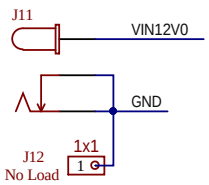
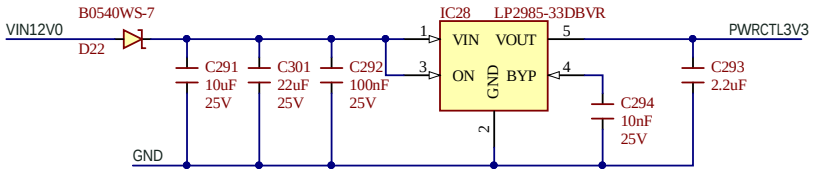
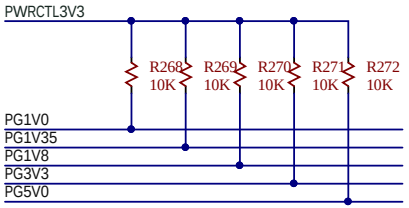
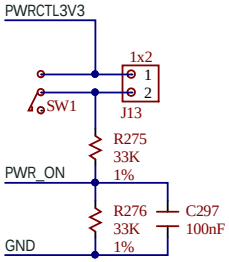
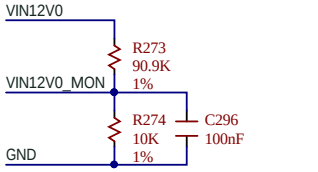
Note: Input Voltage 12V only!



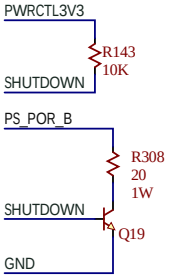


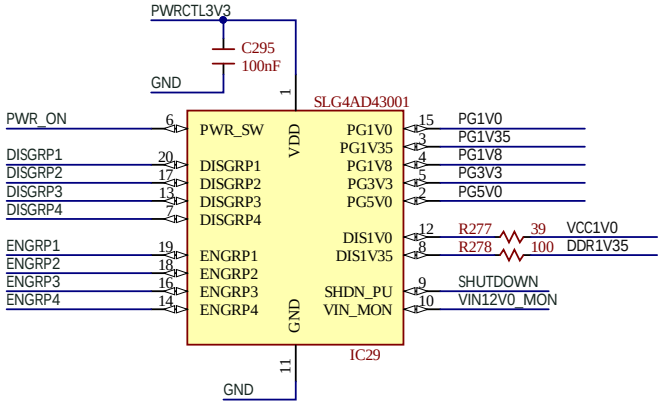


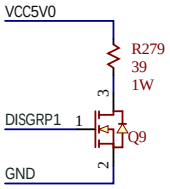


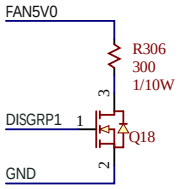


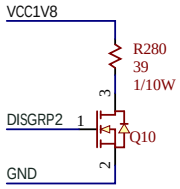
Input Voltage Enable Threshold			
	MIN	TYPICAL	MAX
TURN ON	10.038V	10.221V	10.407V
TURN OFF	9.791V	9.969V	10.150V

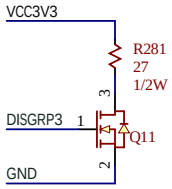


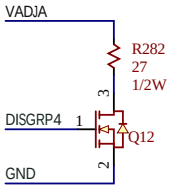


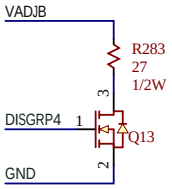


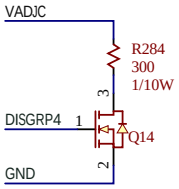


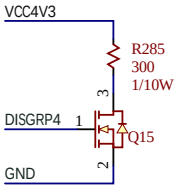


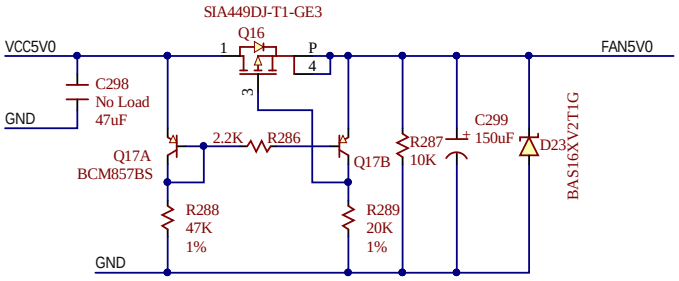


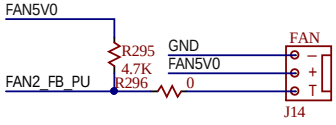












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