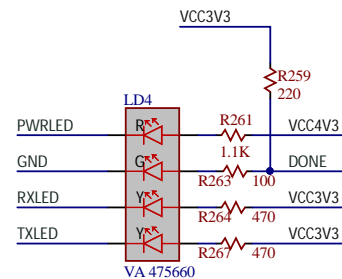
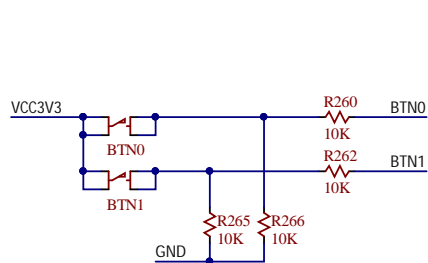
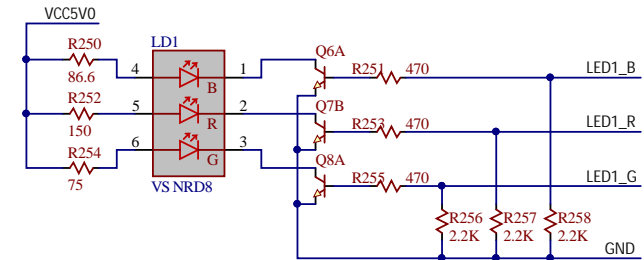
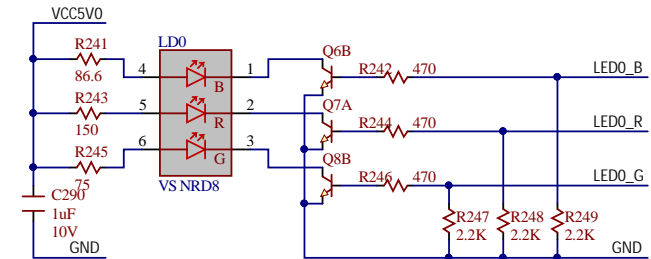


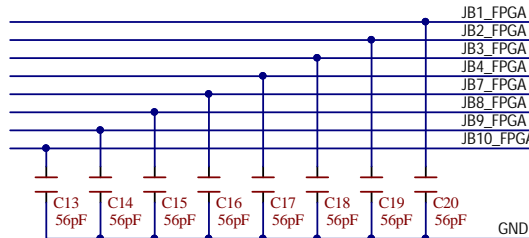
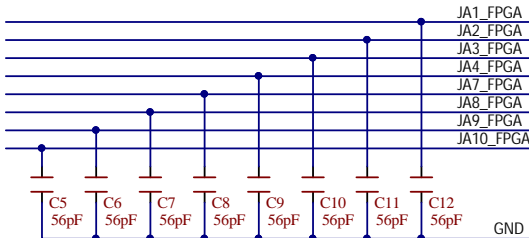
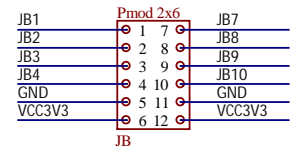
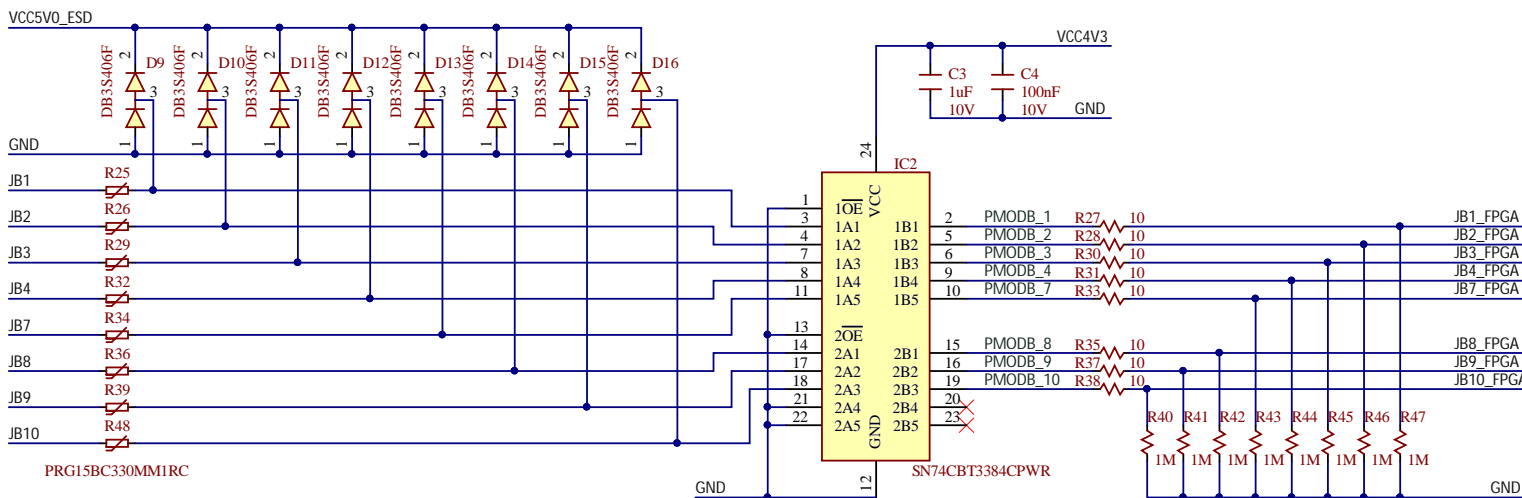
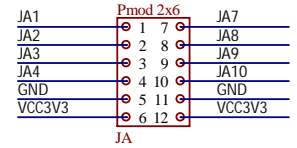
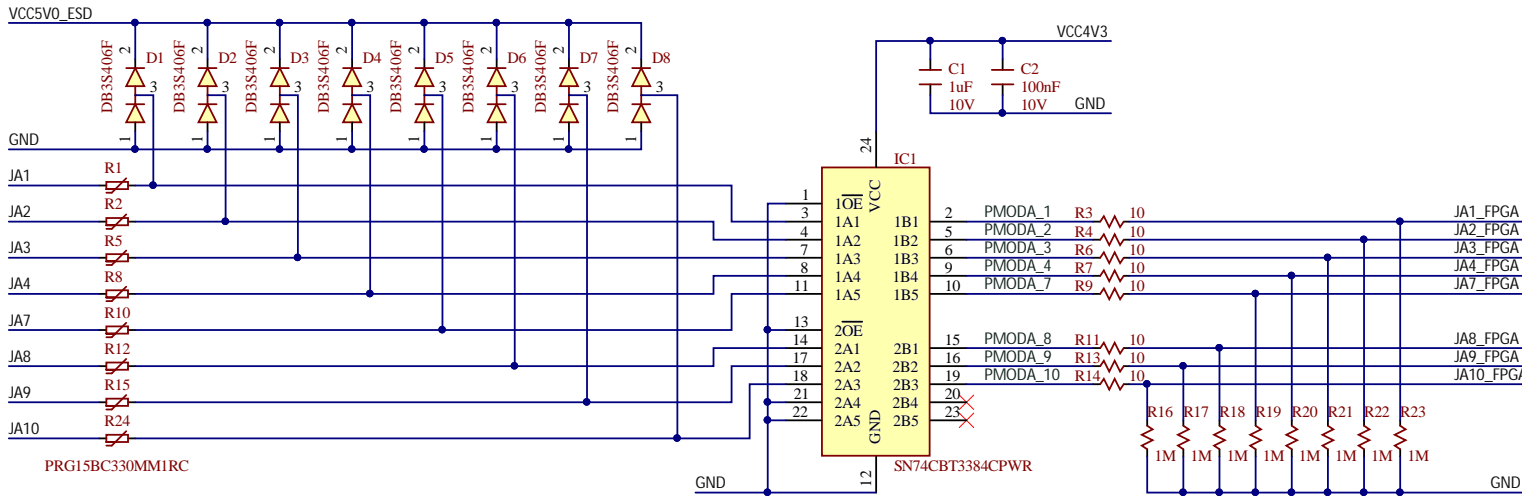
**Sheet      Circuit**

1.      **LEDs, Buttons**
2.      **PMOD Ports**
3.      **SYZYGY Ports**
4.      **Ethernet and SD Card**
5.      **USB OTG**
6.      **FPGA Configuration**
7.      **DDR and MIO Banks**
8.      **FPGA Banks**
9.      **FPGA Power**
10.     **DDR3L Memory**
11.     **DDR3L Termination**
12.     **Platform MCU**
13.     **Power Regulation**
14.     **Power Regulation**
15.     **Power Regulation and Sequencer**

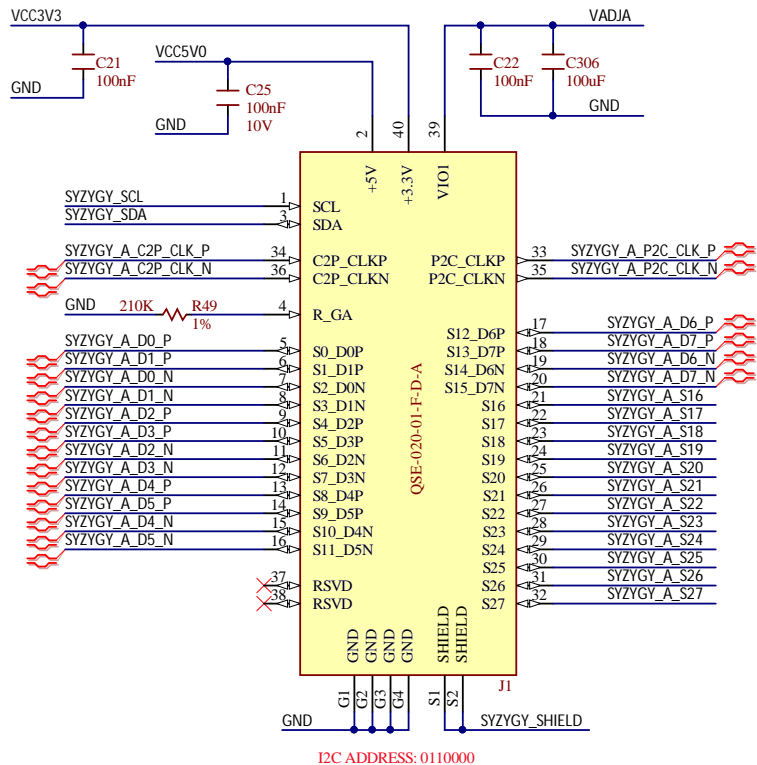


Foot  
F1  
Foot  
F2

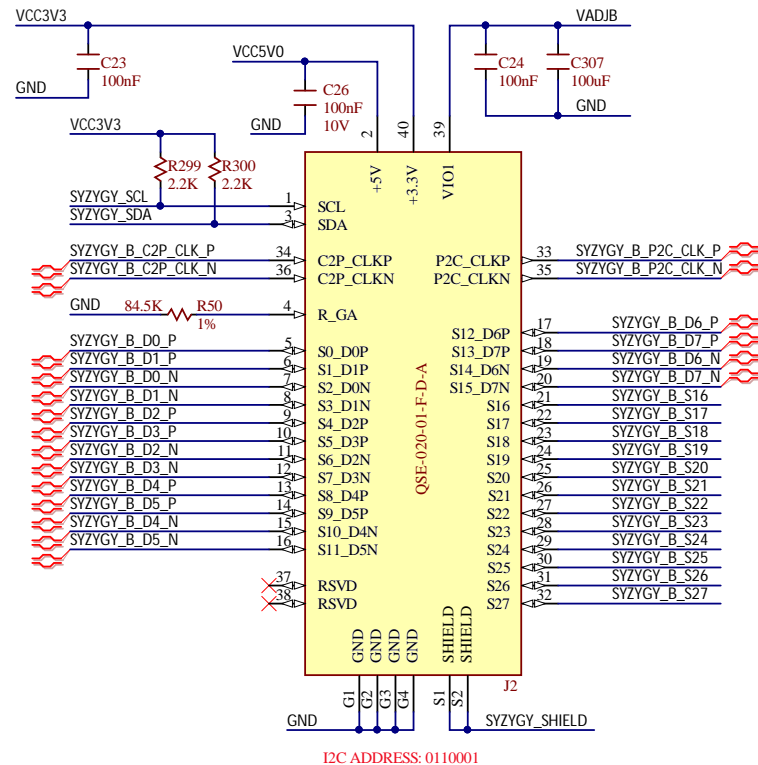
Title <b>Eclipse Z7</b>		Rev <b>B.1</b> Copyright 2019
Circuit LEDs, Buttons		
Doc# 500-393		
Engineer MTA		
Author GMA		
Date 9/11/2019		
Sheet# 1 out of 15		



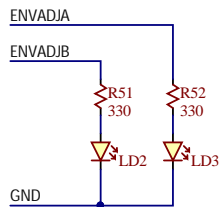
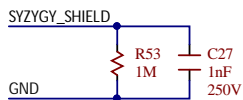
Title		Rev
<b>Eclipse Z7</b>		<b>B.1</b>
Circuit		Copyright 2019
Pmod Ports		
Doc#	500-393	
Engineer	MTA	
Author	GMA	
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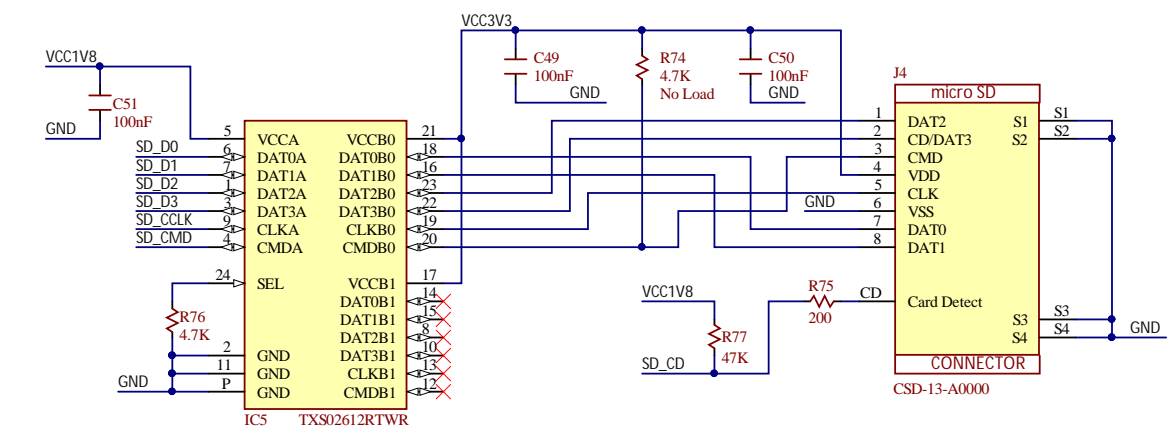
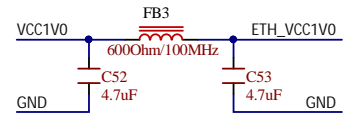
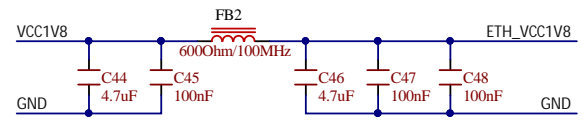
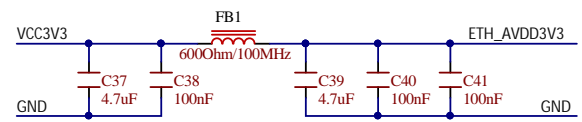
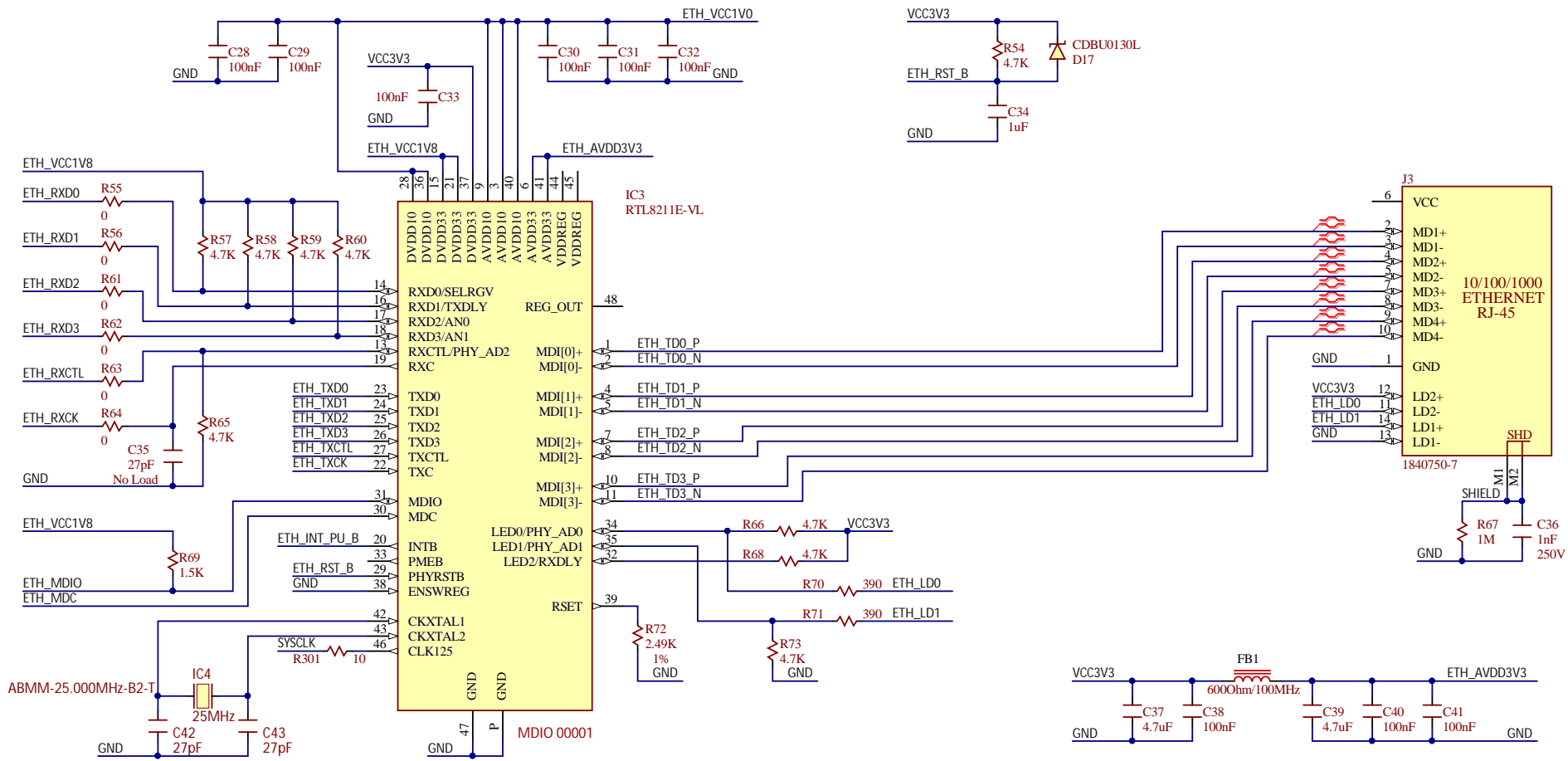
I2C ADDRESS: 0110000



I2C ADDRESS: 0110001

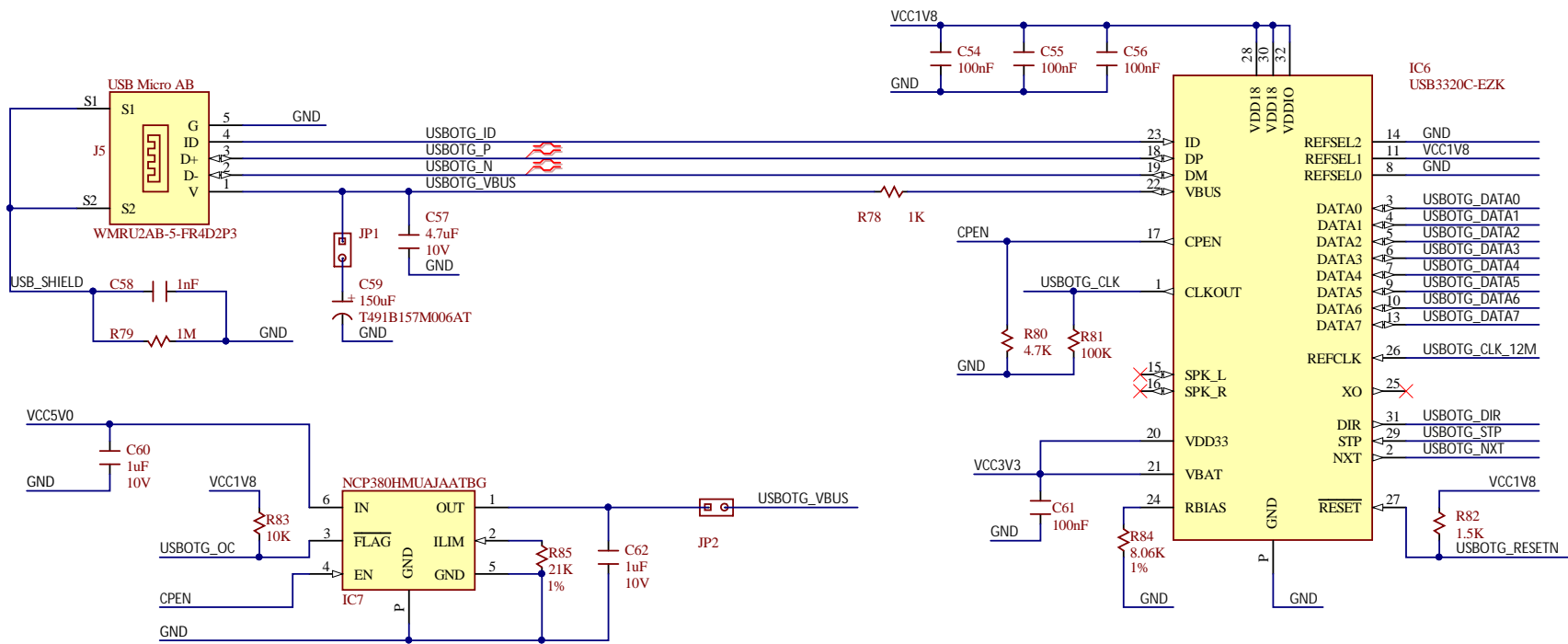


Title <b>Eclipse Z7</b>		Rev <b>B.1</b> Copyright 2019
Circuit SYZYGY Ports	Doc# 500-393	
Engineer MTA	Author GMA	
Date 9/11/2019	Sheet# 3 out of 15	



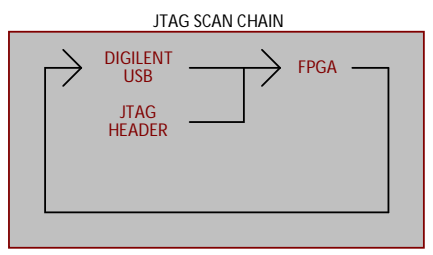
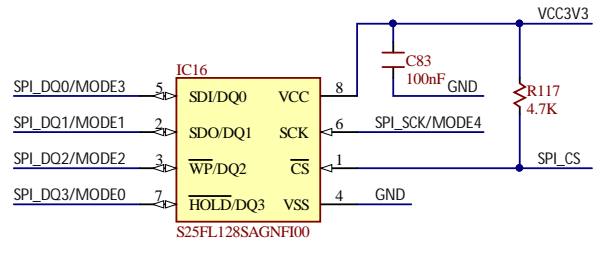
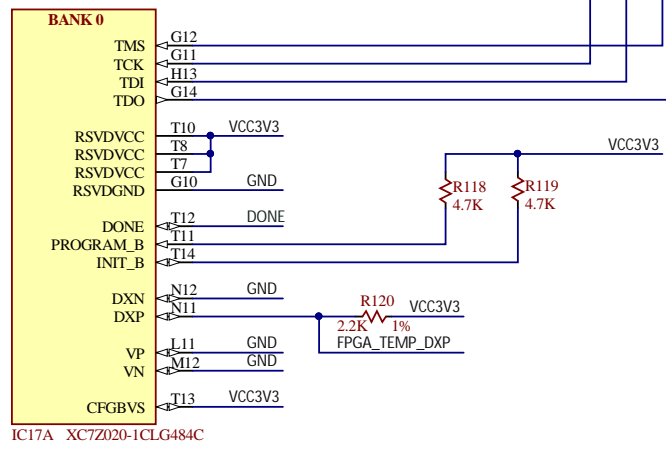
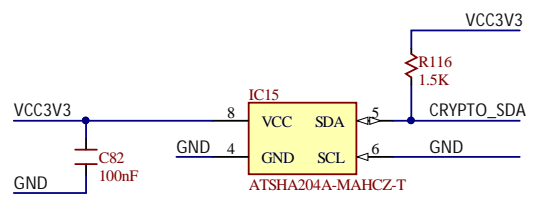
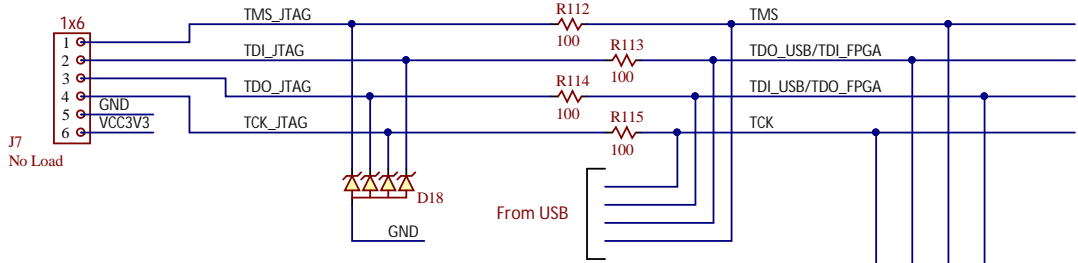
Title		Rev
<b>Eclipse Z7</b>		<b>B.1</b>
		Copyright 2019
Circuit	Ethernet and SD Card	
Doc#	500-393	
Engineer	MTA	
Author	GMA	
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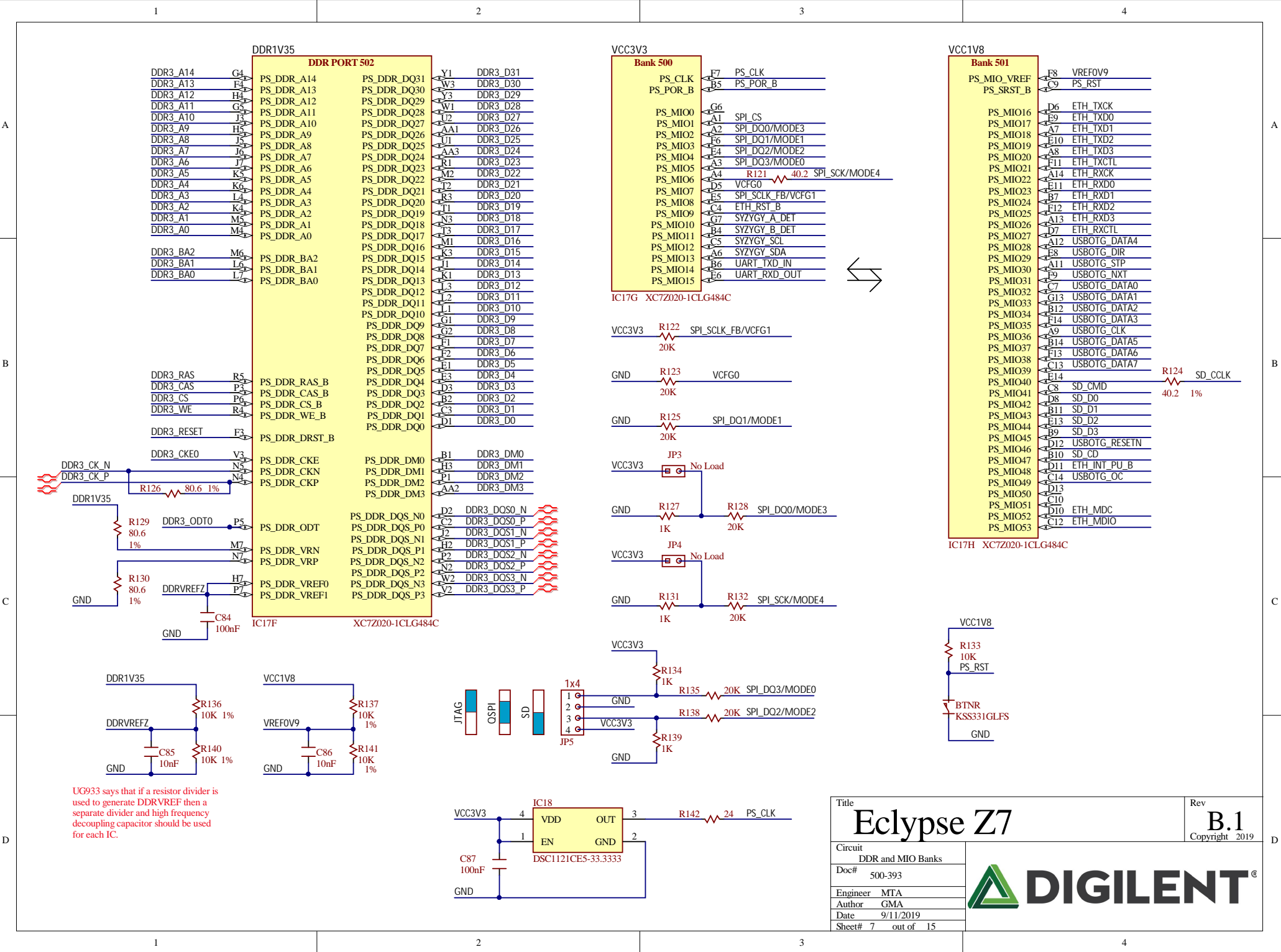


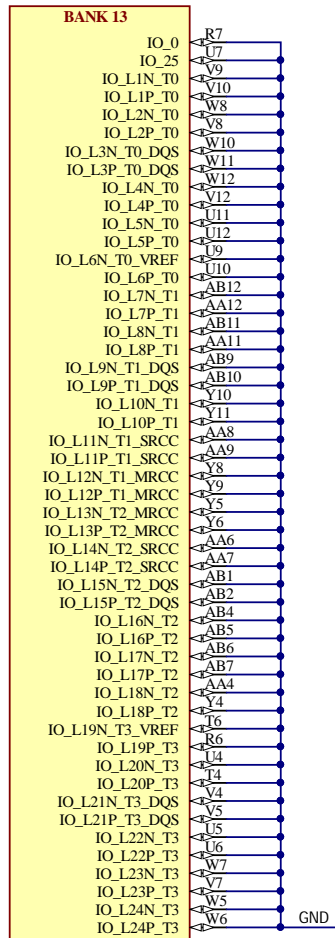
Title		Rev
Eclipse Z7		B.1
		Copyright 2019
Circuit	UST OTG	
Doc#	500-393	
Engineer	MTA	
Author	GMA	
Date	9/11/2019	
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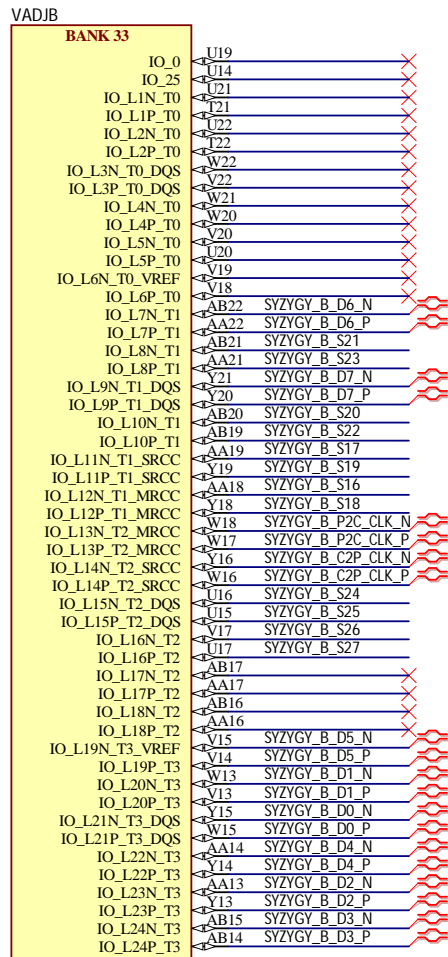


Title <b>Eclipse Z7</b>		Rev <b>B.1</b> Copyright 2019
Circuit FPGA Configuration		
Doc#	500-393	
Engineer	MTA	
Author	GMA	
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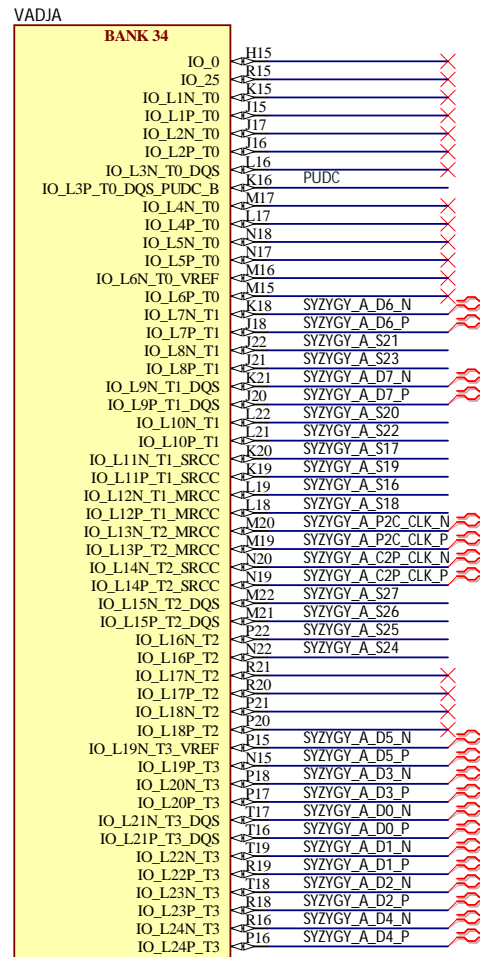




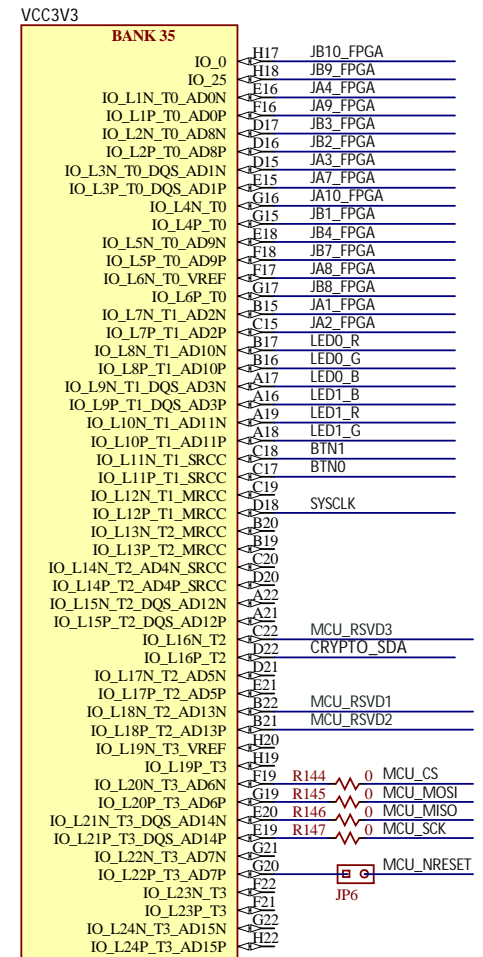
IC17B XC7Z020-1CLG484C



IC17C XC7Z020-1CLG484C

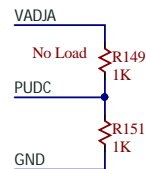
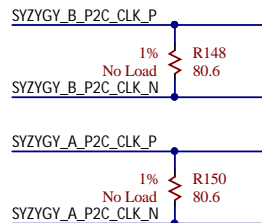


IC17D XC7Z020-1CLG484C



IC17E XC7Z020-1CLG484C

UG933 says to connect the I/O pins of an unused bank to the same potential as the VCCO pins of that bank.

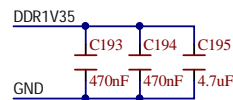
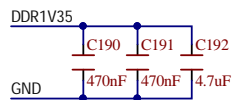
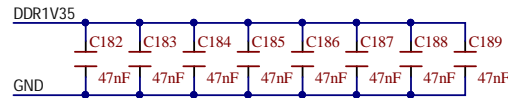
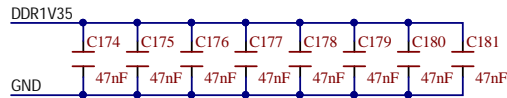
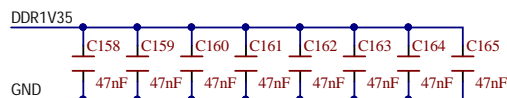
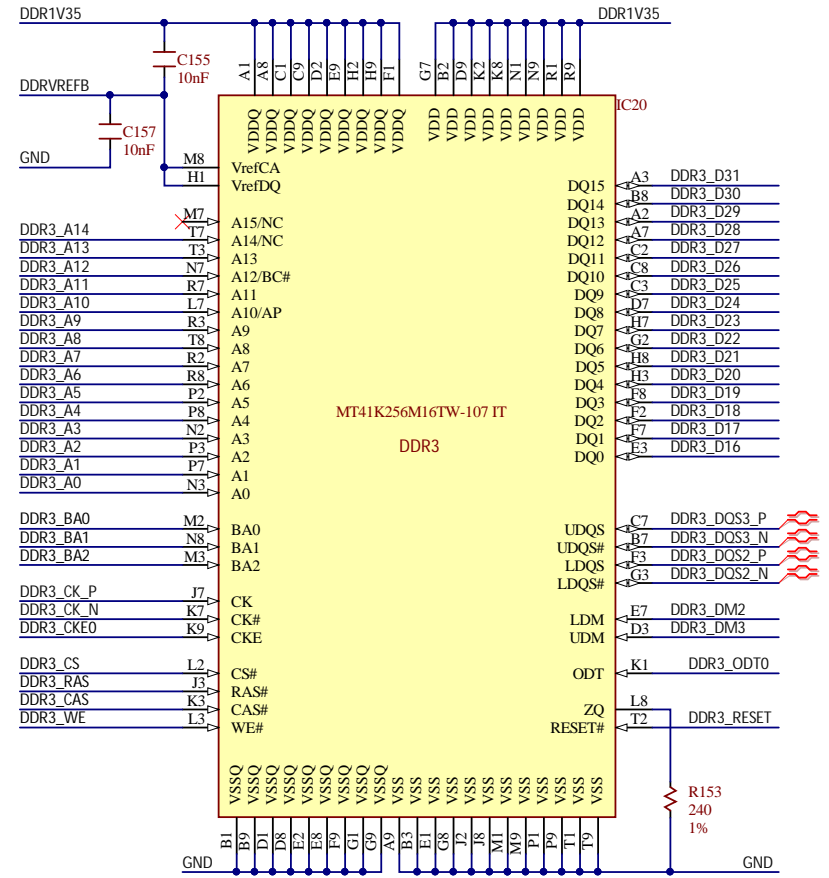
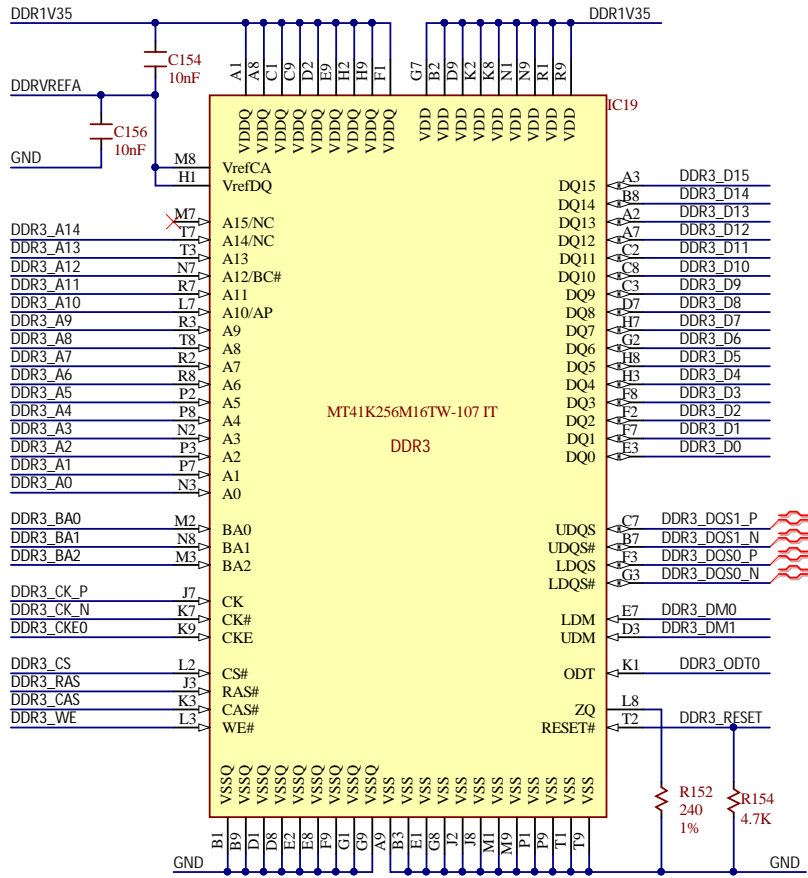


Title		Rev
<b>Eclipse Z7</b>		<b>B.1</b>
Circuit		Copyright 2019
FPGA Banks		
Doc#	500-393	
Engineer	MTA	
Author	GMA	
Date	9/11/2019	
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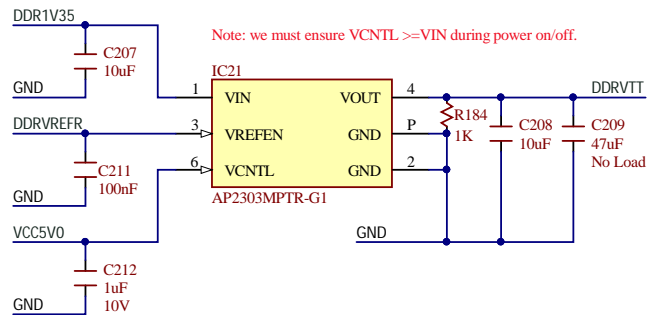
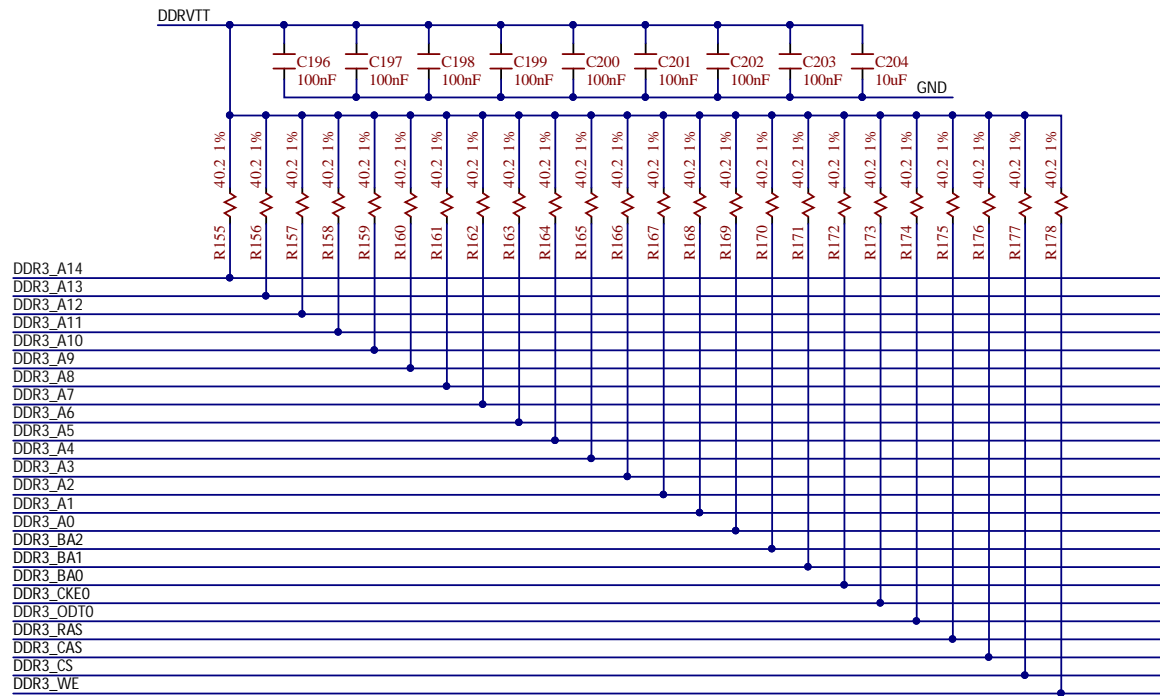




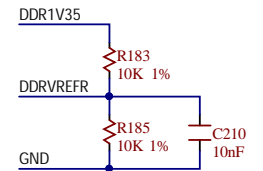
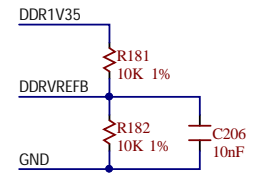
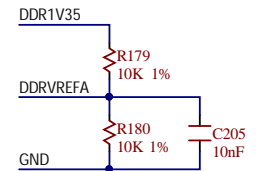




Title		Rev
<b>Eclipse Z7</b>		<b>B.1</b>
Circuit		Copyright 2019
DDR3L Memory		
Doc#	500-393	
Engineer	MTA	
Author	GMA	
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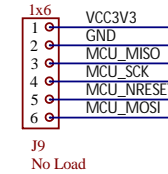
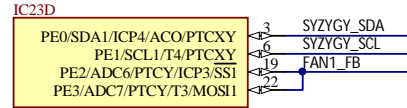
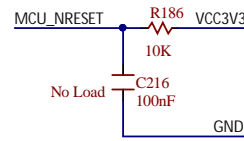
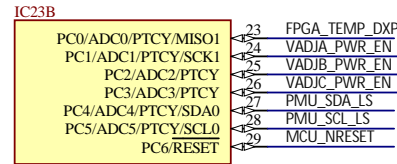
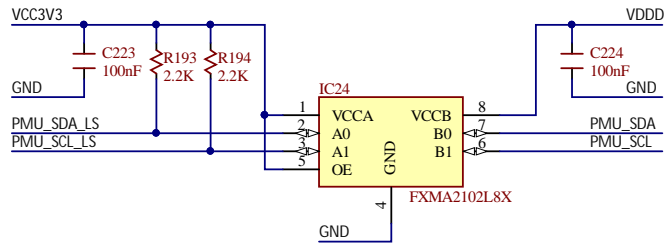
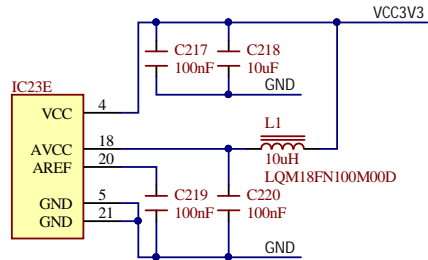
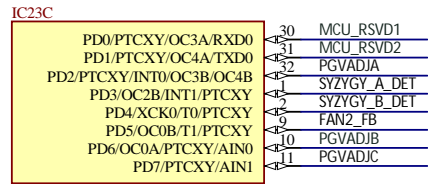
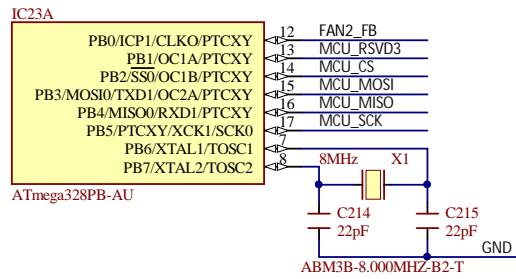


UG933 says that if a resistor divider is used to generate DDRVREF then a separate divider and high frequency decoupling capacitor should be used for each IC.

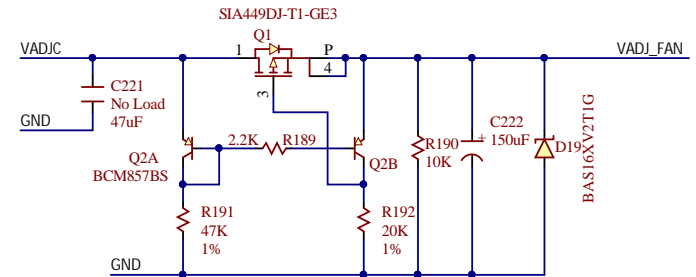
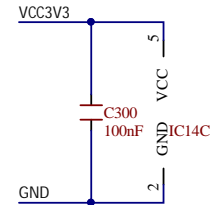
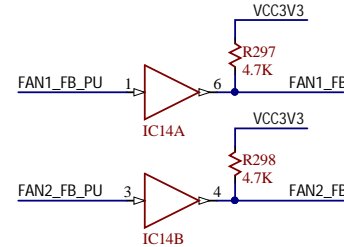
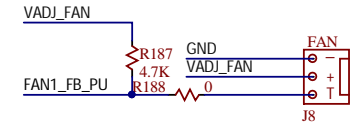
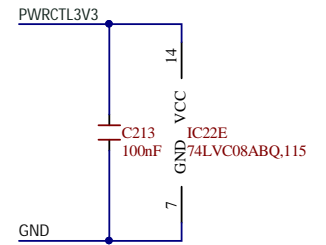
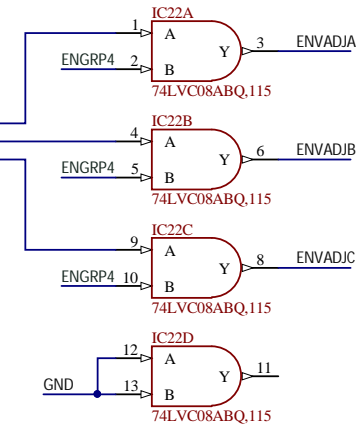
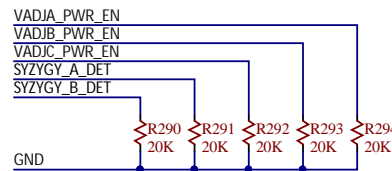
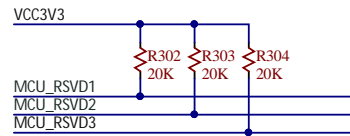


Title <b>Eclipse Z7</b>		Rev <b>B.1</b> Copyright 2019
Circuit DDR3L Termination		
Doc# 500-393		
Engineer MTA		
Author GMA		
Date 9/11/2019		
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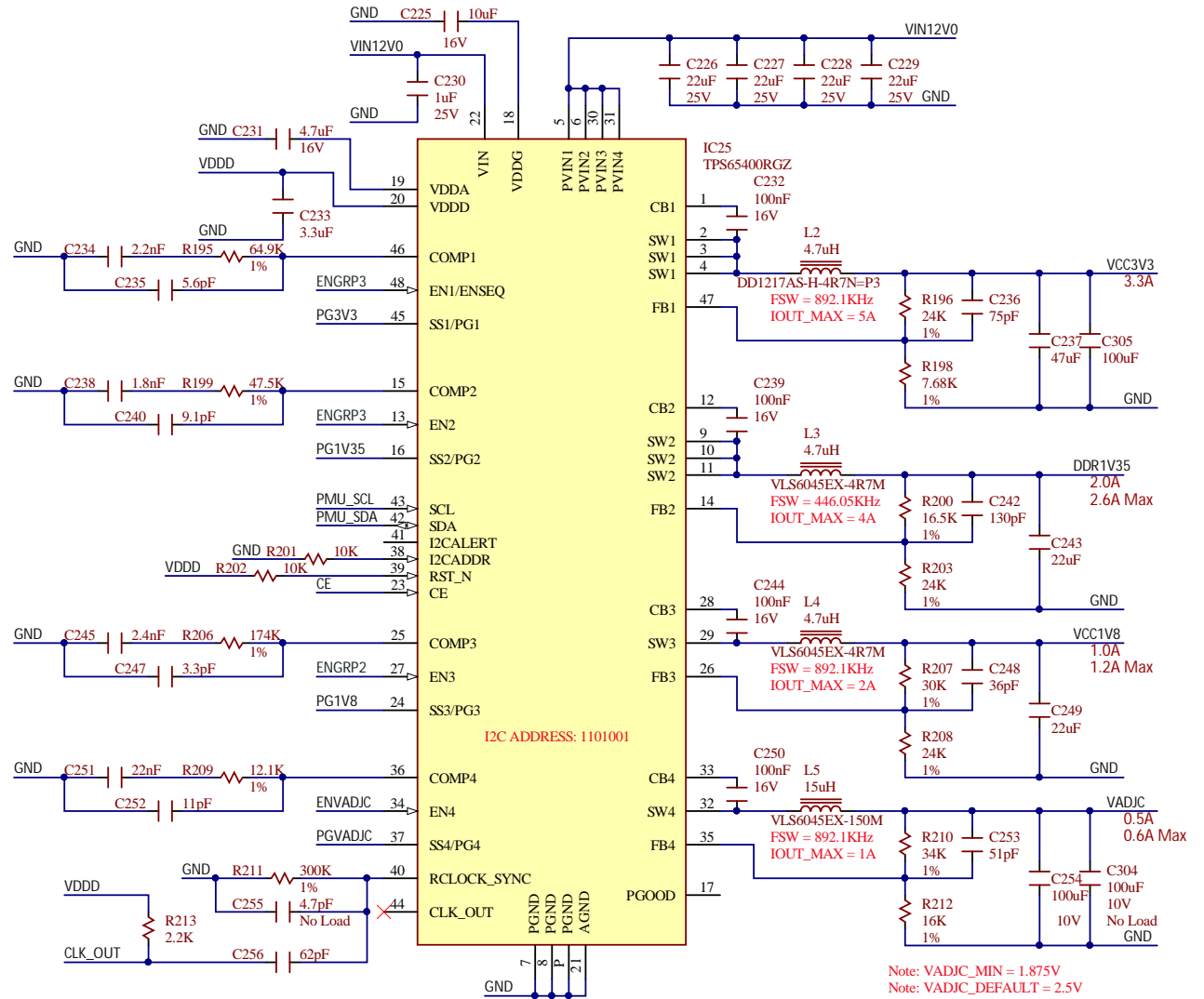
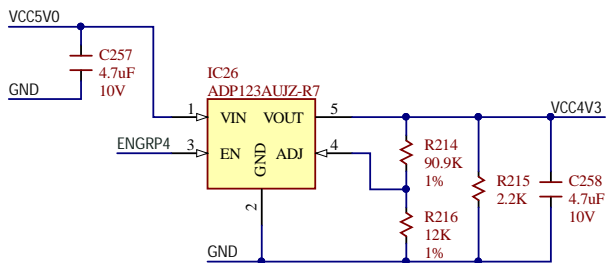
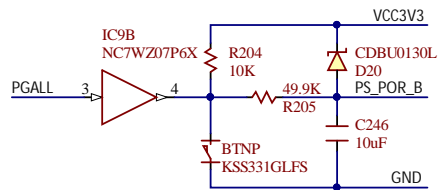
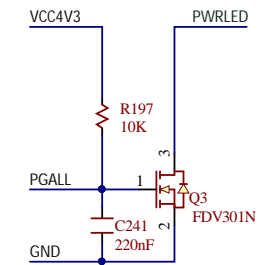


J9 No Load  
 Program/Debug using MPLAB SNAP Debugger  
 Pin 2 of the SNAP connects to pin 1 on the board  
 SNAP Pinout: <http://microchipdeveloper.com/pickit4-interface-pinouts>



Title		Rev
<b>Eclipse Z7</b>		<b>B.1</b>
Circuit		Copyright 2019
Platform MCU		
Doc#	500-393	
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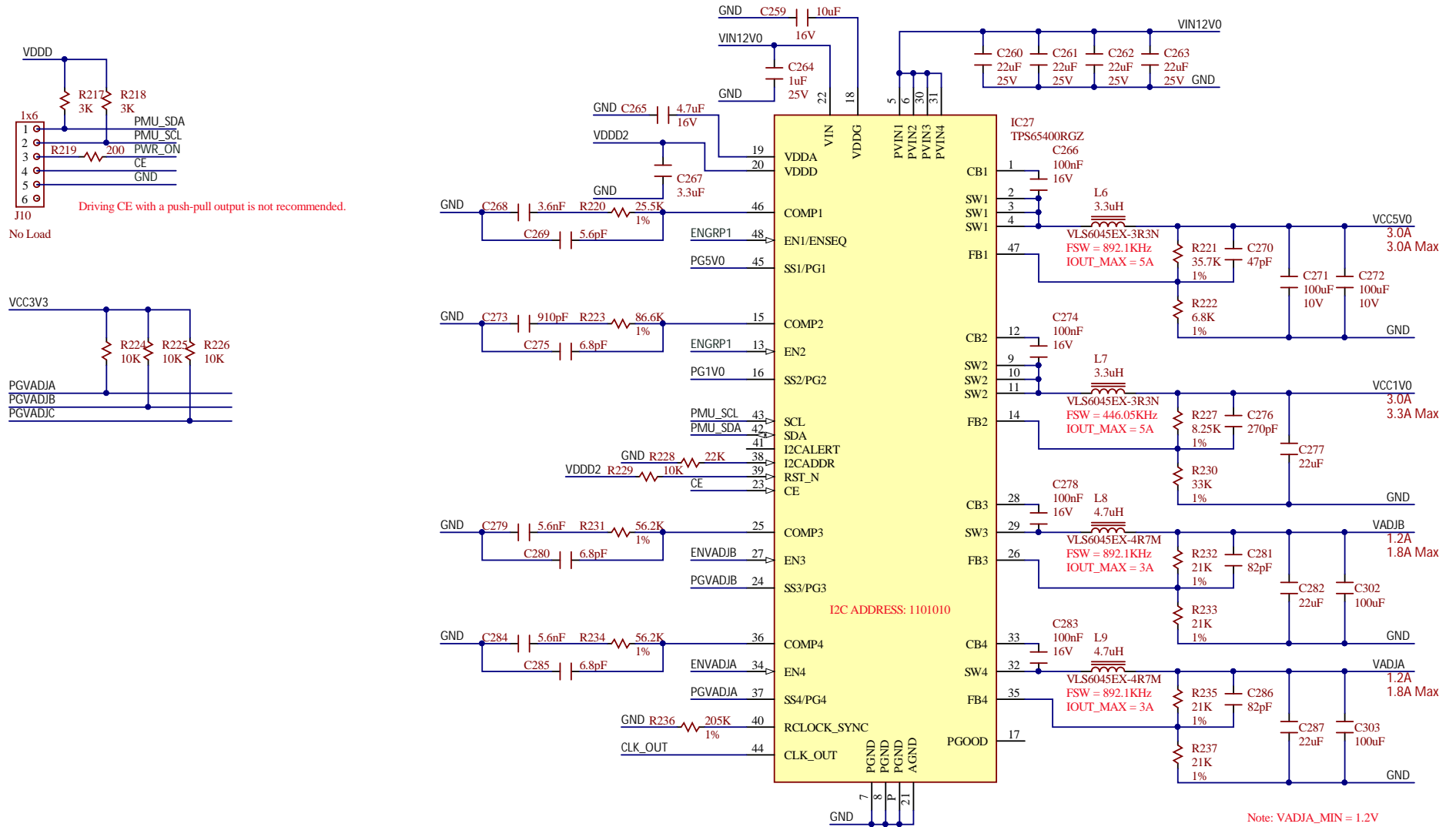
Note: VADJC\_MIN = 1.875V  
 Note: VADJC\_DEFAULT = 2.5V  
 Note: VADJC\_MAX = 5.84V

ISENSE\_GAIN = 10A/V for all channels  
 TON\_RAMP\_RATE = 0.25V/ms for all channels

Note: our desired switching frequency is 892.1KHz, which would typically require a 205K resistor connected to RCLOCK\_SYNC. However, because we want to synchronize to an external 892.1KHz clock we must use a resistor that sets the switching frequency approximately 30% lower than the external clock. Therefore we use a 300K resistor to set the internal switching frequency to 621.8KHz.

Title		Rev
<h1>Eclipse Z7</h1>		<h2>B.1</h2>
		Copyright 2019
Circuit	Power Regulation	
Doc#	500-393	
Engineer	MTA	
Author	GMA	
Date	9/11/2019	
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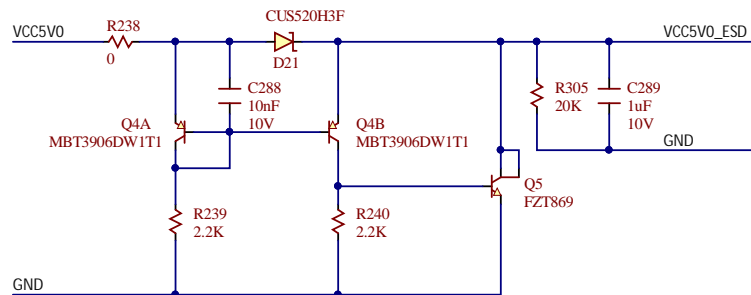




ISENSE\_GAIN = 10A/V for all channels  
TON\_RAMP\_RATE = 0.25V/ms for all channels

Note: VADIA\_MIN = 1.2V  
Note: VADIA\_DEFAULT = 1.6V  
Note: VADIA\_MAX = 3.74V

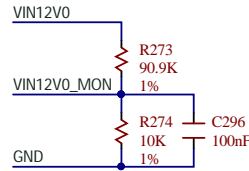
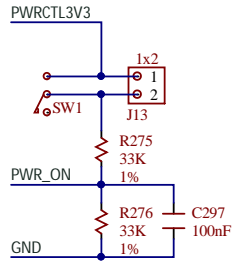
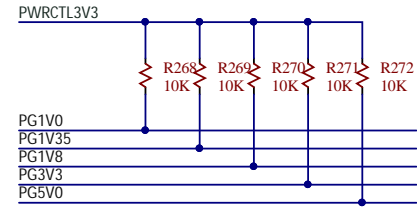
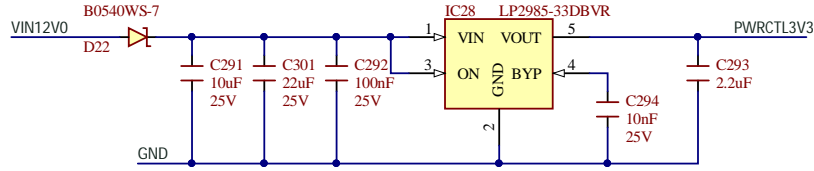
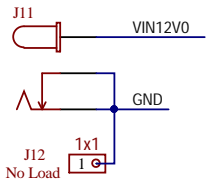
Note: VADJB\_MIN = 1.2V  
Note: VADJB\_DEFAULT = 1.6V  
Note: VADJB\_MAX = 3.74V



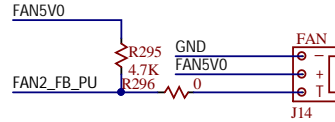
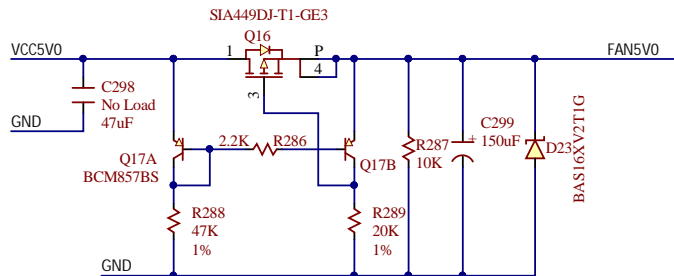
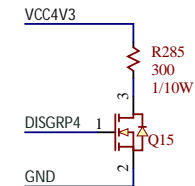
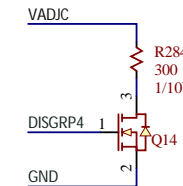
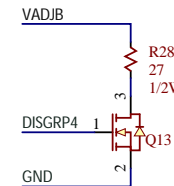
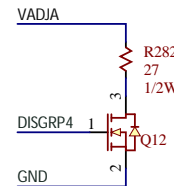
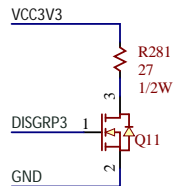
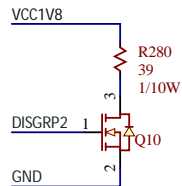
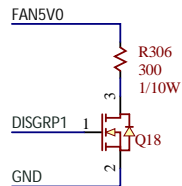
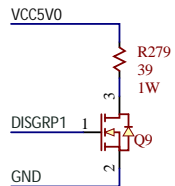
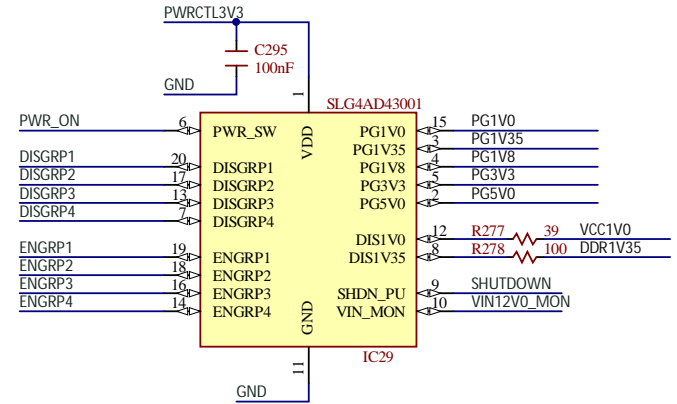
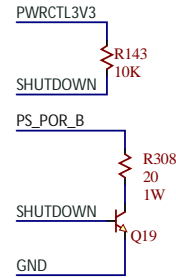
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Eclypse Z7		B.1
Circuit		Power Regulation
Doc#	500-393	Copyright 2019
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Author	GMA	
Date	9/11/2019	
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Note: Input Voltage 12V only!



Input Voltage Enable Threshold			
	MIN	TYPICAL	MAX
TURN ON	10.038V	10.221V	10.407V
TURN OFF	9.791V	9.969V	10.150V



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Date	9/11/2019	
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