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JTAG SCAN CHAIN

DIGILENT USB

JTAG HEADER

FPGA

BD

C

D

Title: Eclypse Z7

Engineer: MFA

Doc# 500-393

Author: GMA

Date: 10/28/2020

Sheet#: B.2

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NOTE: Please select Micron MT41K256M16 RE-125 as the Memory Part in the Vivado DDR Configuration.
Note: we must ensure VCNTL >= VIN during power on/off.

UU0933 says that if a resistor divider is used to generate DDRVREF then a separate divider and high frequency decoupling capacitor should be used for each IC.
Note: our desired switching frequency is 892.1KHz, which would typically require a 20.5K resistor connected to RCLOCK_SYNC. However, because we want to synchronize to an external 892.1KHz clock we must use a resistor that sets the switching frequency approximately 30% lower than the external clock. Therefore we use a 300K resistor to set the internal switching frequency to 621.8KHz.
ISENSE_GAIN = 10A/V for all channels
TON_RAMP_RATE = 0.25V/ms for all channels

Driving CE with a push-pull output is not recommended.

IOUT_MAX = 3A
FSW = 892.1KHz
VLS6045EX-4R7M

IOUT_MAX = 5A
FSW = 446.05KHz
VLS6045EX-4R7M

IOUT_MAX = 5A
FSW = 892.1KHz

Note: Input Voltage 12V only!