Digilent Reference Design

Digital to Analog Conversion using the X-board and PModDA2

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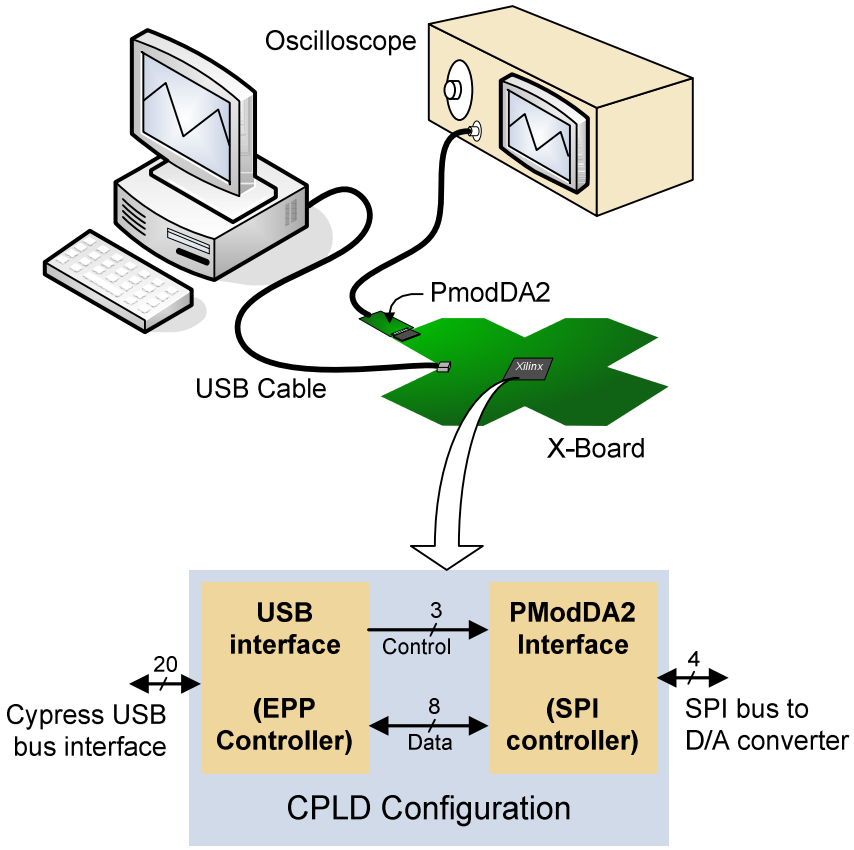
Overview

This reference design demonstrates digital to analog conversion using the X-board and PModDA2 to generate voltages based on sample data sent from a PC.

The X-board is a CPLD demonstration board based on a Xilinx CoolRunner-2 CPLD. The PModDA2 is a Digilent Peripheral Module board that contains two National Semiconductor DAC121S101 D/A converters. These converters consume 12-bit data and feature an 8us settling time.

Digilent's Adept software is used to program the reference design into the CPLD, and to move sample data from the PC to the X-board. Please refer to the Reference Manuals listed below for more detailed information.



References

Digilent X-board Reference Manual Schematic
Digilent PModDA2 Reference Manual and Schematic
Digilent Adept Reference Manual
Digilent Application Note AN0040 "Digilent Asynchronous Parallel Interface"
National Semiconductor DAC121S101 Data sheet
Xilinx CoolRunner-2 Data Sheet

Set-up

This reference design requires a PC running the Xilinx ISE or WebPack tools, Digilent's Adept software, an X-board, a Digilent PModDA2, and an oscilloscope or voltmeter.

Set the clock frequency select jumper (J11) on the X-board to select 100KHz.

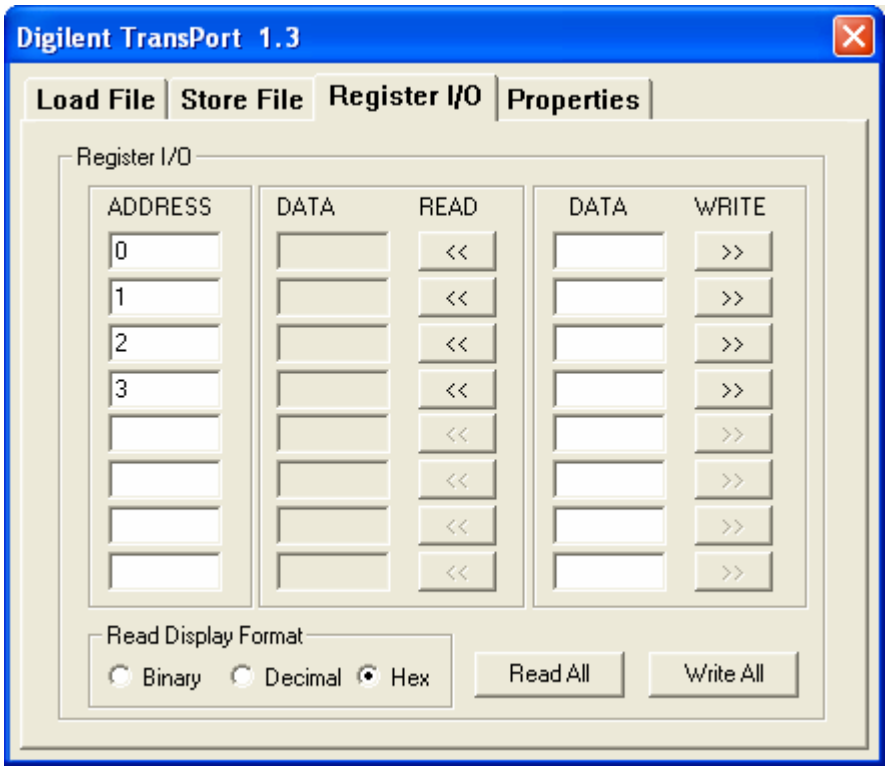
Description

This reference design is composed of two major blocks: a USB interface that implements registers in the CPLD that Adept can read and write; and a SPI controller that can read and write data from the D/A converter on the PModDA2. A simple 8-bit control bus, the Digilent asynchronous parallel interface bus (based on the Enhanced Parallel Port, or EPP, specification), is used to move data internally between these two blocks.

The USB interface block works with firmware in the USB controller to implement four writable 8-bit registers in the CPLD. Registers can be written from the Transport application that is available as a part of Digilent's freely available Adept software (alternatively, the API's available through Adept can be used to create custom applications to access CPLD registers). Register writes are communicated from the USB interface block to the SPI controller using Digilent's asynchronous parallel interface bus. Bus timings and signal definitions closely follow the EPP specification; please see application note AN0040 available at www.digilentinc.com for a detailed description of bus timing and control.

Since the USB interface is based on 8-bit registers, and 12-bit sample data is sent to the PModDA2, Transport must perform two consecutive writes to transfer all 12 bits to each D/A channel. Writing the second register of the pair assigned to a channel will start a new conversion for that channel. The CPLD uses the write request from Transport to start a new conversion by driving the SPI bus to the D/A converter as required. The write request to the second register will immediately start the D/A conversion. The SPI controller in the CPLD uses SPI mode 0 protocol to transfer data from the A/D converter.

To use the reference design "as is", build a project in the Xilinx tools using the VHDL and UCF files that are downloaded from the Digilent website as a part of this reference design. Attach the PModDA2 to the J1 port on the X-board, and attach a meter or other device to the D/A outputs. Program the CPLD on the X-board with the JED file created from the downloaded source files, and then run Digilent's Transport application (available as a part of the Adept software freely available at the Digilent website). Select the Register I/O tab, and add register addresses 1-4 to the address fields as shown. Add sample data to registers 0 and 1 for D/A channel A, and to data registers 2 & 3 for channel B. Writing register addresses 0 and 2 will simply write the data; writing addresses 1 and 3 will write the data and start a new conversion.



Note that user-written, custom applications can acquire sample data from the X-Board / PModDA2 hardware using the API's available as a part of Adept.

The following table summarizes the address definitions used in the reference design.

Address	Op	Channel	Data	Comments
0	Write	A	LSB	Write data for lower byte of Channel A data
1	Write	A	MSB	Write data for upper 4 four bits of Channel A, write starts conversion
2	Write	B	LSB	Write data for lower byte of Channel B data
3	Write	B	MSB	Write data for upper 4 four bits of Channel B, write starts conversion