PmodAD2 & PmodDA1 Demo

1300 NE Henley Court, Suite 3
Pullman, WA 99163
(509) 334 6306 Voice | (509) 334 6300 Fax

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Overview

This document describes the VHDL implementation of a controller for a PmodDA1 and a PmodAD2 connected in a loopback configuration. The controlling board will count from 0 to 255, setting the PmodDA1's output to this value. The produced voltage is read back by the PmodAD2, and stored internally so that Xilinx Chipscope Pro™ may be used to observe the operation of the system. This project was developed in Xilinx ISE 13.4 for the Digilent Nexys3 FPGA board, but may easily be reconfigured for another device.

Functional Description

The Analog Loopback 2 reference project implements an SPI-like controller for interfacing with the PmodDA1, and a TWI controller for interfacing with the PmodAD2. It is an extension of the Analog Loopback Reference Project replacing the PmodAD1 used in the original project with a PmodAD2.

The Nexys3's onboard 100 MHz oscillator is used to generate a 100 kHz and a 100 Hz signal. The 100 kHz signal is used as a data clock for the serial controllers and the 100 Hz signal drives a counter (controlling the value passed into the PmodDA1) as well as indicating when to update the PmodDA1, and when to poll the state of the PmodAD2. The controller board uses a serial interface to set the desired analog output on channel A1 of the PmodDA1. The output of the PmodDA1 is connected to the input of the PmodAD2, and the analog value actually read by the PmodAD2. When the Nexys3 is connected to a PC, Chipscope may be used to view and compare the desired analog value, and the returned value. As the PmodDA1 utilizes 8-bit output resolution while the PmodAD2 utilizes 12-bit input resolution, thus the bottom 4-bits of the value returned by the PmodAD2 should be considered noise.

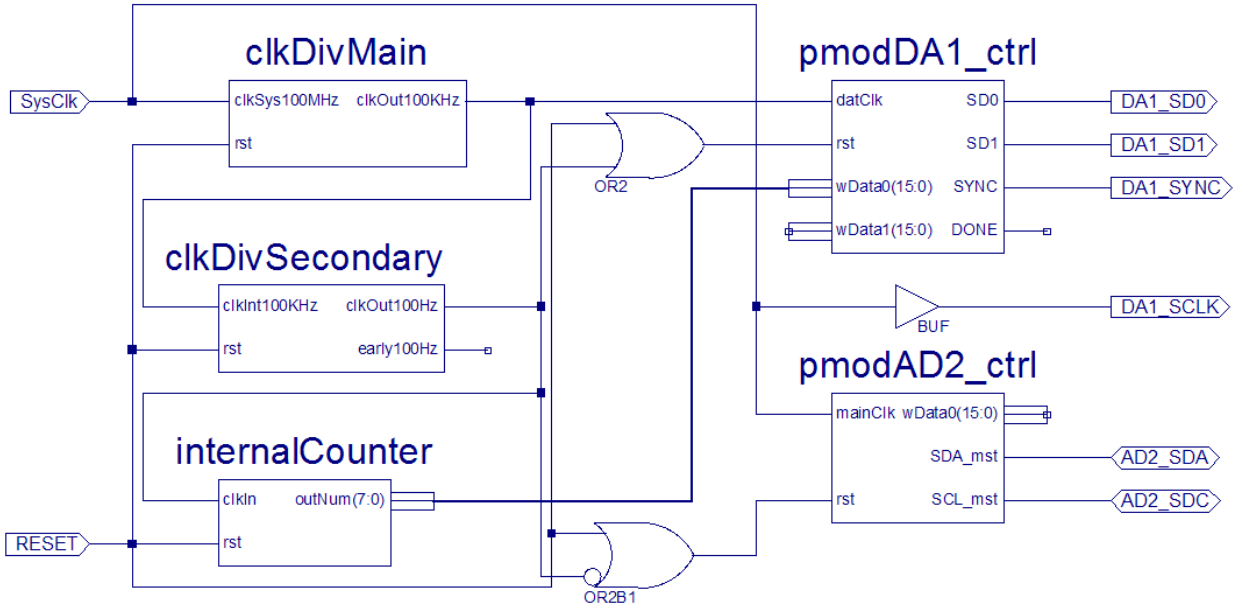

Figure 1 Analog Loopback 2 Reference Project Approximate Block Diagram

Block Description

PmodDA1 Controller Behavior

The PmodDA1 is controlled through a simple serial data scheme. A clock line is driven by the host and the output of SD0 and SD1 are sampled by the peripheral on the rising edge of the clock when the SYNC line is pulled low. Thus, on the first falling edge of the 100 kHz clock after coming out of reset, the host pulls the sync line low and outputs the first bit of the 16-bit input word to the data line. On each failing edge the bit is updated until the final bit is output, and the SYNC line is brought high. The DONE signal is then asserted to indicate that the controller has finished outputting the word to the PmodDA1.

To transmit another word pair to the PmodDA1, the module must be reset. For this reason, the module's reset is connected to system the reset line as well the 100 Hz clock. When the clock is high, the module will be reset. Thus, on the falling edge of the clock, the new value from the internal counter will be sent out to the PmodDA1.

PmodAD2 Controller Behavior

The PmodAD2 is controlled via a TWI controller implemented by Digilent Romania. The system is a black box connected to the output directly on the board. The only addition on the output side of the TWI controller is a Xilinx Pull-up primitive. This primitive can be removed if physical pull up circuitry is placed on the TWI bus.

To receive the sampled value from the PmodAD2 the host device sends out a low signal on the data line and starts clocking to indicate the start of transmission. Then a 7-bit address is clocked out along with a read or write bit. Data is then controlled by the master or slave, and the data is sent on the falling clock edge by the sending device, and sampled on the rising edge.

Using Chipscope to probe the Circuit

This section details how to use a Nexys3 onboard JTAG interface to monitor and review the circuit's output using Chipscope.

Prior to starting

Before Chipscope is launched, ensure that the system has met the following conditions.

1. The Nexys3 has been programmed with the reference design
2. The Digilent Plugin for Xilinx Tools is installed on the PC probing the system.
3. A PmodAD2 is connected to pins 3-6 and 9-12 (the side with VCC and GND) on JA1.
4. A PmodDA1 is connected to pins 1-6 (the top row) on JC1.
5. A 6 pin cable connector is connecting the PmodAD2 and the PmodDA1 with the mark on the cable on the right side of both jumpers.

Using Chipscope™

Start by starting Chipscope by selecting Chipscope Pro ➔ Analyzer under the Xilinx ISE Design Suite folder. Select JTAG Chain ➔ Open Plugin from the menu, and type in digilent_plugin and click OK. After a few moments a window should open up showing a list of devices that were found connected to the PC, click OK to close this window.

To start the test, select Trigger Setup ➔ Run. The test should take a few seconds to complete.

At this point, twenty individual data signals have been returned to Chipscope. These signals represent the 12-bits returned by the PmodAD2 and the 8-bits the PmodDA1 was provided to create the desired analog voltage. To view these signals as a signal value they need to be grouped into a bus within Chipscope. To do this, click on the icon to the left of the "Data Port" in the signals pane. Select CH4 through CH11, right click, and select Move to Bus ➔ New Bus. Rename this bus to PmodAD2. Then select CH12 through CH19, right click, and select Move to Bus ➔ New Bus. Rename this bus to PmodDA1.

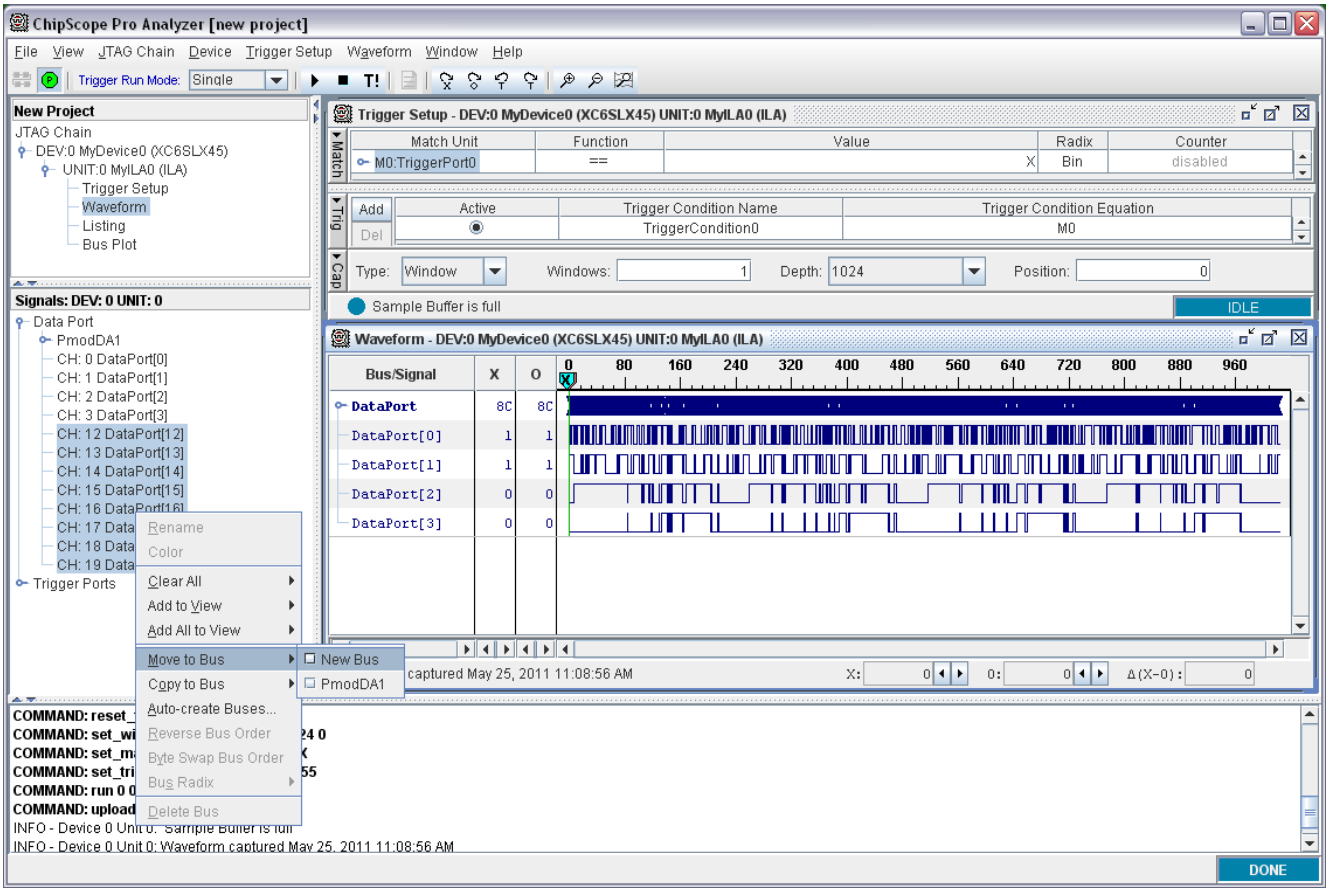

Figure 2 Moving Signals to a bus

Finally, double click on Bus Plot in the New Project pane. Click on the two check-boxes under Bus Selection. These will plot the aggregated bus signals PmodAD2 and PmodDA1 as numbers.

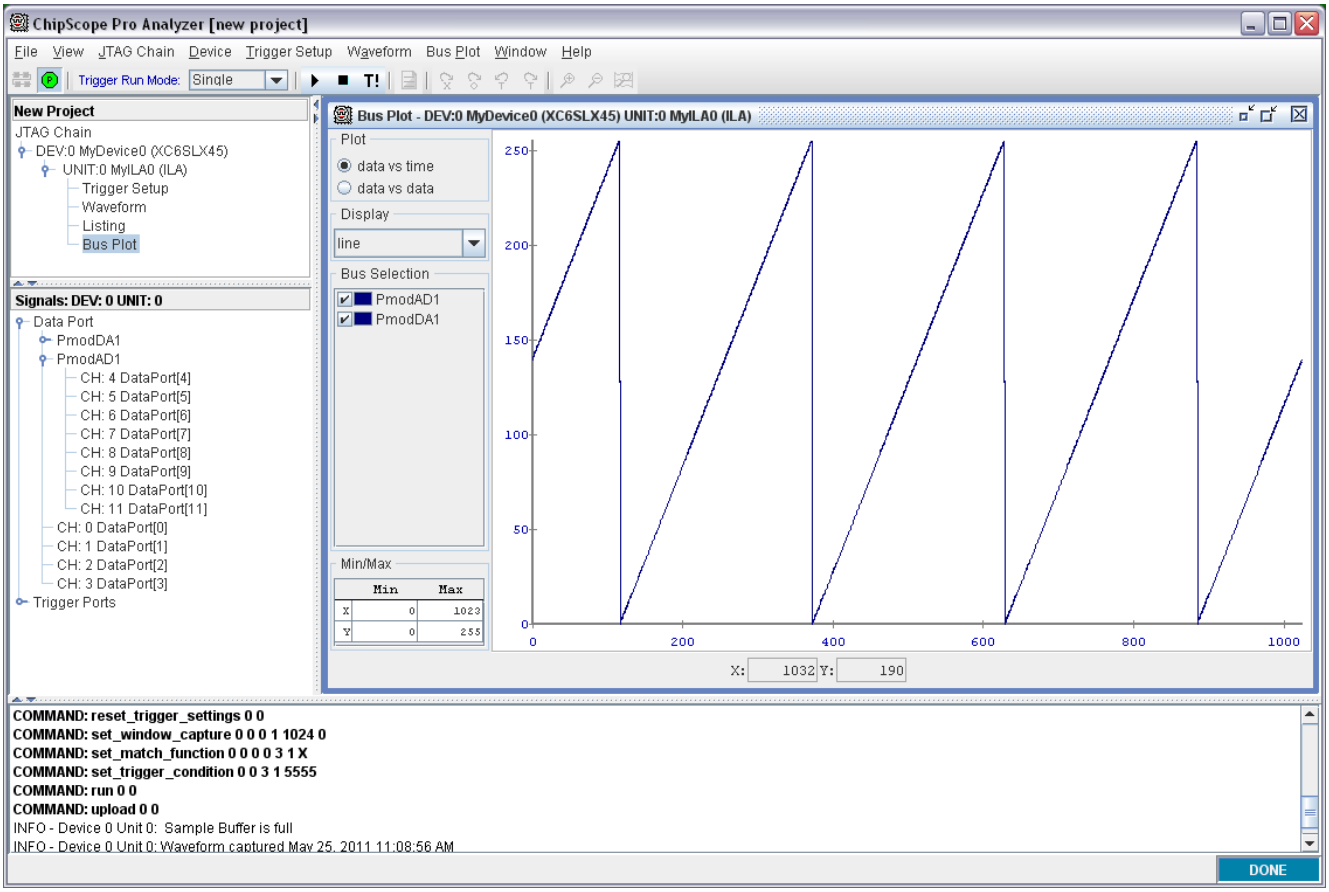

Figure 3 Viewing bus signals

More information on using Chipscope can be found in the *Chipscope Pro Software and Cores User Guide.*