## **Creating Embedded Linux Solutions**

Course Workbook

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The contents of this workbook are created by Adiuvo Engineering & Training, Ltd.

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# **Pre-Lab** Creating Embedded Linux Solutions

**Pre-Lab** 

#### **Required Hardware**

Arty Z7-20 SD Card Micro USB Cable

#### **Pre-Lab**

#### **Downloads and Installations**

**Step 1 –** Download and install the following at least 1 day prior to the workshop. This may take a significant amount of time and drive space.

Watch the video available <u>here</u> to show how to configure the installation

Vitis 2021.1	Download
PetaLinux 2021.1	Download

**Step 1 –** Using a Linux Development machine with PetaLinux 2021.1 installed create a new project

File Edit View Search Terminal Help
adiuvo@adiuvo:~/petalinux_projects\$ petalinux-create <mark>t</mark> ype projecttemplate zynqname lab3
Ι

Step 2 – Change directory into the project, import the XSA exported from Lab One



Step 3 – Exit the dialog which is opened following the XSA Import.

misc/config System Configuration         Arrow keys navigate the menu. <enter> selects submenus&gt; (or empty submenus). Highlighted letters are hotkeys. Pressing <y> includes, <n> excludes, <m> modularizes features. Press <esc><to <?="" exit,=""> for Help,  for Search. Legend: [*] built-in [] excluded <m> module          -*- ZYNQ Configuration      &gt;         Auto Config Settings&gt;         Auto Config Settings&gt;         -*- Subsystem AUTO Hardware Settings&gt;         FSBL Configuration&gt;         FSBL Configuration&gt;         FSBL Configuration&gt;         Inux Configuration&gt;</m></to></esc></m></n></y></enter>	File Edit View Search Terminal Help /home/adiuvo/petalinux_projects/lab3/project-spec/configs/config - misc/config System Configuration 
-*- ZYNQ Configuration Linux Components Selection> Auto Config Settings> -*- Subsystem AUTO Hardware Settings> DTG Settings> FSBL Configuration> FPGA Manager> u-boot Configuration> Linux Configuration> Image Packaging Configuration> 4(+)	<pre>misc/config System Configuration Arrow keys navigate the menu. <enter> selects submenus&gt; (or empty submenus). Highlighted letters are hotkeys. Pressing <y> includes, <n> excludes, <m> modularizes features. Press <esc><esc> to exit, <?> for Help,  for Search. Legend: [*] built-in [] excluded <m> module &lt;&gt; module capable</m></esc></esc></m></n></y></enter></pre>
Linux Configuration> Image Packaging Configuration> 4(+)	-*- ZYNQ Configuration Linux Components Selection> Auto Config Settings> -*- Subsystem AUTO Hardware Settings> DTG Settings> FSBL Configuration> FPGA Manager> u-boot Configuration>
	Linux Configuration> Image Packaging Configuration> J(+) <select> &lt; Exit &gt; &lt; Help &gt; &lt; Save &gt; &lt; Load &gt;</select>

**Step 4 –** When asked save any changes

nome/adiuvo/petalinux_projects/1	Lab3/project-spec/configs/config - misc/config System Configuration	
	Do you wish to save your new configuration? (Press <esc><esc> to continue kernel configuration.) &lt; Yes &gt; &lt; No &gt;</esc></esc>	

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**Step 5 –** Enter the command petalinux-config –c rootfs to examine the rootfs dialog. Close without saving changes after exploring the settings.

le Edit View Search Terminal Help home/adiuvo/petalinux_projects/lab3/project-spec/configs/rootfs_config - Configuration
Configuration Arrow keys navigate the menu. <enter> selects submenus&gt; (or empty submenus). Highlighted letters are hotkeys. Pressing <y> includes, <n> excludes, <m> modularizes features. Press <esc><esc> to exit, <? > for Help,  for Search. Legend: [*] built-in [] excluded <m> module &lt; &gt; module capable</m></esc></esc></m></n></y></enter>
Filesystem Packages      >         Petalinux Package Groups      >         Image Features      >         apps      >         user packages      >         PetaLinux RootFS Settings      >
<pre><select> &lt; Exit &gt; &lt; Help &gt; &lt; Save &gt; &lt; Load &gt;</select></pre>

**Step 6 –** Enter the command petalinux-config –c kernel to view the config settings, do not change anything and exist after exploring.

ile Edit View Terminal Tabs Help config - Linux/arm 5 10 0 Kernel Configuration
Linux/arm 5.10.0 Kernel Configuration Arrow keys navigate the menu. <enter> selects submenus&gt; (or empty submenus). Highlighted letters are hotkeys. Pressing <y> includes, <n> excludes, <m> modularizes features. Press <esc><esc> to exit, <? > for Help,  for Search. Legend: [*] built-in []</esc></esc></m></n></y></enter>
General setup> -*- Patch physical to virtual translations at runtime System Type> Bus support> Kernel Features> Boot options> CPU Power Management> Floating point emulation> Power management options>
Firmware Drivers      >         v(+)

**Step 7 –** Build the petalinux project with the command petalinux-build – this may take some time.

File Edit View Search Terminal Help
adiuvo@adiuvo:~/petalinux_projects\$ cd lab3/ adiuvo@adiuvo:~/petalinux_projects/lab3\$ petalinux-configget-hw-description=/home/adiuvo/petalinux_projects/lab3 [INFO] Sourcing buildtools INFO: Getting hardware description INFO: Renaming design_1_wrapper.xsa to system.xsa [INFO] Generating Kconfig for project [INFO] Menuconfig project configuration written to /home/adiuvo/petalinux_projects/lab3/project-spec/configs/config
*** End of the configuration. *** Execute 'make' to start the build or try 'make help'.
<pre>[INFO] Extracting yocto SDK to components/yocto. This may take time! [INFO] Sourcing build environment [INFO] Generating kconfig for Rootfs [INFO] Silentconfig rootfs [INFO] Generating plnxtool conf [INFO] Adding user layers [INFO] Generating workspace directory adiuvo@adiuvo:~/petalinux_projects/lab3\$ petalinux-build</pre>

#### Step 8 – Package the petalinux project to create the boot.bin necessary

File Edit View Search Terminal Help	
adiuvo@adiuvo:~/petalinux_projects/lab3\$ cd images/linux/ adiuvo@adiuvo:~/petalinux_projects/lab3/images/linux\$ petalinux-packagebootfsbl zynq_fs system.bitforce	bl.elfu-boot u-boot.elffpga
INFO: Getting system flash information INFO: File in BOOT BIN: "/home/adiuvo/petalinux_projects/lab3/images/linux/zynq_fsbl.elf" INFO: File in BOOT BIN: "/home/adiuvo/petalinux_projects/lab3/images/linux/system.bit" INFO: File in BOOT BIN: "/home/adiuvo/petalinux_projects/lab3/images/linux/u-boot.elf" INFO: File in BOOT BIN: "/home/adiuvo/petalinux_projects/lab3/images/linux/u-boot.elf" INFO: File in BOOT BIN: "/home/adiuvo/petalinux_projects/lab3/images/linux/system.dtb" INFO: File in BOOT BIN: "/home/adiuvo/petalinux_projects/lab3/images/linux/system.dtb"	I
***** Xilinx Bootgen v2021.1 **** Build date : May 28 2021-21:36:22 ** Copyright 1986-2021 Xilinx, Inc. All Rights Reserved.	
[INFO] : Bootimage generated successfully	
INFO: Binary is ready. WARNING: Unable to access the TFTPBOOT folder /tftpboot!!! WARNING: Skip file copy to TFTPBOOT folder!!! adiuvo@adiuvo:~/petalinux_projects/lab3/images/linux\$	

**Step 9 –** Copy the image.ub boot.bin and boot.scr to the SD Card, insert in the Arty Z7 – ensure it is set for SD Card boot. Connect the power and Ethernet cable.



**Step 10 –** Vitis will start and ask for the workspace, create a new directory using browse to store the projects.

elect a directory	as workspace				
Vitis IDE uses the w	orkspace directory to	store its preferences	and development artifa	cts.	
Workspace: C:\hd	l_projects\lab3			~	<u>B</u> rowse
🗌 lles this as the d	fault and do not ack				
<u>U</u> se this as the de		again			
<u>Kestore other We</u>	orkspace				
<u>Recent Workspace</u>	es				

**Step 11 –** Select Create Application Project



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Step 12 – Select the XSA downloaded with GitHub Repository under lab three



#### Step 13 – Click next

Edit Search Xilinx Project Window H	Vew Application Project	— 🗆 ×	
□ Welcome 🖾	latform		
	Note: A platform project will be generated automatically in workspace for the selected XSA. It can be customized later.		
🔨 VITIS. 👘	Select a platform from repository		
	Hardware Specification		
	C:\GIT\Digilent_bootcamp\03_Session_Three\XSA\design_1_wrapper.xsa		
	vck190 vck190_es1		
	vmk180 vmk180_es1		
	XSA File: zc702	Browse	
	zcu102		
	zed		
	C:\GIT\Digilent_bootcamp\03_Session_Three\XSA\design_1_wrapper.xsa		
	Boot Components		
	Generate boot components		
	Platform name: design_1_wrapper		
	? < Back Next >	Finish Cancel	

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**Step 14 –** Enter a name for the project and select the processors in SMP configuration

oplication project name: test			
System Project			
Create a new system project for the appli	cation or select an existing one from the v	vorkpsace 🚺	
Select a system project	System project details		
Create new	System project name:	test system	
		,	
	arget processor		
	Select target processor	or the Application project.	
	Processor	Associated applications	
	ps7_cortexa9_0		
	ps7_cortexa9 SMP	test	

**Step 15 –** Click Next on the Domain page

lect the domain that the application would I	ink to or create a new domain	
elect a demain created by this wizard will h	have all the requirements of the application temp	late selected in the next step
Create new	Name:	linux_ps7_cortexa9
	Display Name: Operating System:	linux_ps7_cortexa9
	Processor: Architecture:	ps7_cortexa9 32-bit ~
	Application setting	IS
	Sysroot path:	Brows
	Kernel Image:	Brows

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**Step 16 –** Select the Linux Hello World application and click finish



**Step 17 –** Click on the Hammer to build the application



**Step 18 –** Select the arrow by the green debug icon and select debug configuration



#### Step 19 – Select System Project Debug and click new

V Debug Configurations		- D X
Create, manage, and run configurations Debug a system using Vitis Debugger.		Ť.
Image: Second State Sta	<ul> <li>Configure launch settings from this dialog:</li> <li>Press the 'New Configuration' button to create a configuration of the selected type.</li> <li>Press the 'New Prototype' button to create a launch configuration prototype of the selected type.</li> <li>Press the 'New Prototype' button to export the selected configurations.</li> <li>Press the 'Duplicate' button to copy the selected configuration.</li> <li>Press the 'Delete' button to configure filtering options.</li> <li>Edit or view an existing configuration by selecting it.</li> <li>Select launch configuration(s) and then select 'Unlink Prototype' menu item to unlink a prototype.</li> <li>Select launch configuration(s) and then select 'New Prototype Values' menu item to reset with prototype values.</li> <li>Configure launch perspective settings from the 'Perspectives' preference page.</li> </ul>	
Filter matched 10 of 22 items		
?		Debug Close

**Step 20 –** Open a serial terminal 115200:n:1 and type the command ifconfig to list the IP Address of the board



#### Step 21 – Change the build configuration to Hardware and for Linux TCF Agent select new

mDebugger_test_system  arget Setup)  Environment  Common  test_system  Browse  Browse  Browse  erver:  Local New  gent: Linux Agent  New
mDebugger_test_system  Iarget Setup) To Environment Common  Itest_system  Idbefore launch  uration: Use Active  erver: Local V New  ugent: Linux Agent V New
Iarget Setup     Image:     Local     New     Inux Agent v     New
Itest_system     Browse       wild before launch     uration:       Use Active        erver:     Local       New       urgent:     Linux Agent v
erver: Local New egent: Local New
erver: Local Vew Agent New New
gent: Linux Agent 🗸 New
ly selected applications
king Directory: //mnt/sd-mmcblk0p1/
uments: <u>E</u> dit
Re <u>v</u> ert Apply
Debug Close
g on App Worl

**Step 22 –** Enter a name and enter the Ethernet IP address – Click test connection to verify the board can be seen.

✓ Target Connection Details	×
New Target Connection	
Creates new configuration for connecting to a target.	
Target Name ArtyZ7	
Set as default target	
Specify the connection type and properties	
Type Linux TCF Agent	$\sim$
Host 172.16.102.155	
Port 1534	
Advanced >>	
?	Test Connection OK Cancel
$\odot$	

**Step 23 –** Click OK when the connection is successful, click OK on the target connection and the click debug

Debug Configurations  Create, manage, and run configurations Debug a system using Vitis Debugger.      Provember 2015      Content of the system of the	Name       SystemDet       I Target Connection Details         Main       I Target Connection         Project:       Connection successful!         Build Configuration       Connection successful!         I Target       Second         I Target       Successful!         Specify       OK         I Target       OK         I Target       Advanced >>         Program Argume       I Test Connection	Bgowse
Filter matched 11 of 23 items		▼ Re <u>v</u> ert Apply

**Step 24 –** The application will be downloaded to the target and paused for execution, press the run button

✔ lab3 - test/src/helloworld.c - Vitis IDE					- 0 ×
File Edit Run Search Xilinx Project Window Help → □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	× ∞ .e = ∞ = ∞				Q Design 🎄 Debug
#≥ Debug ⊠	👗 test system 🛛 🛠 test	helloworld.c	 (x)= Variables 🔀 🔍	Breakpoints 🛷 Expressions 🛋	Modules
<pre>% Debug %</pre>	<pre>&amp; test_system</pre>	<pre>ld hellowordd: 33 l2 Xilinx, Inc. All rights reserved. lx Xilinx, Inc. All rights reserved. lx Xilinx, Inc. All rights reserved. lx Advantage of the second of the se</pre>	(A)= Variables 22 Name Mame Mamory 23 Monitors	Breakpoints of Expressions  Type  Type  Expression  Type  Expression  Express	Modules IIII Registers □ □
L toplorer IX ↓Assistant design_1_wrapper test_system {design_1_wrapper} v {d} test {[max_sp1_contexe]} > } blincludes > } bebbug v e> src > @ heldwoorddc > be jde * {test_prj L test_system.sprj	Console 🖾 🖼 Vitis Serial 1 TCF Debug Process Terminal - PS	erminal 💽 Executables 👔 Debug Shell 📗 Vitis Log 🍸 Problems 🙀 Debugger Console 15	 V III VIIII VIIIII VIIII	CT Console [3] Emulation Cons Process i Info: 515 (target 2) Stopp () at/src/helloworld.c: 2 printf("Hello World\n");	ole <b>a</b> C ed at 0x470514 (Suspended 3

Step 25 – Click on the run button and you will see the hello world appear in the console.

