Creating Your First ArtyZ7 Application

Course Workbook

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About this Workbook

The contents of this workbook are created by Adiuvo Engineering & Training, Ltd.

If you have any questions about the contents, or need assistance, please contact Adam Taylor at adam@adiuvoengineering.com.

Pre-Lab

Workshop Pre-requisites

Required Hardware

ArtyZ7-20

Usb cable

Downloads and Installations

Step 1 – Download and install the following at least 1 day prior to the workshop. This may take a significant amount of time and drive space.

Watch the video available here to show how to configure the installation

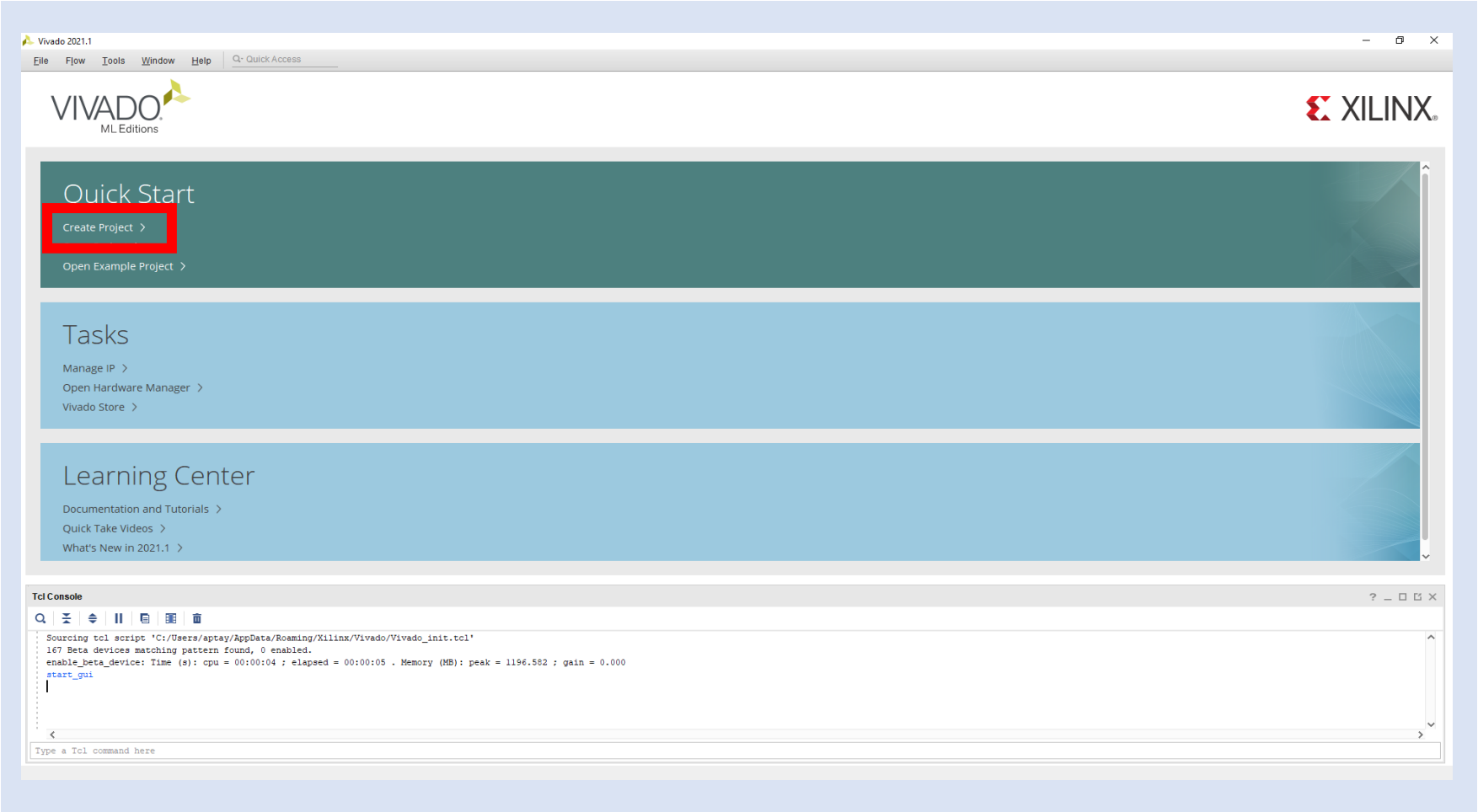
Vitis 2021.1	Download

Lab 1

Project creation & Flow

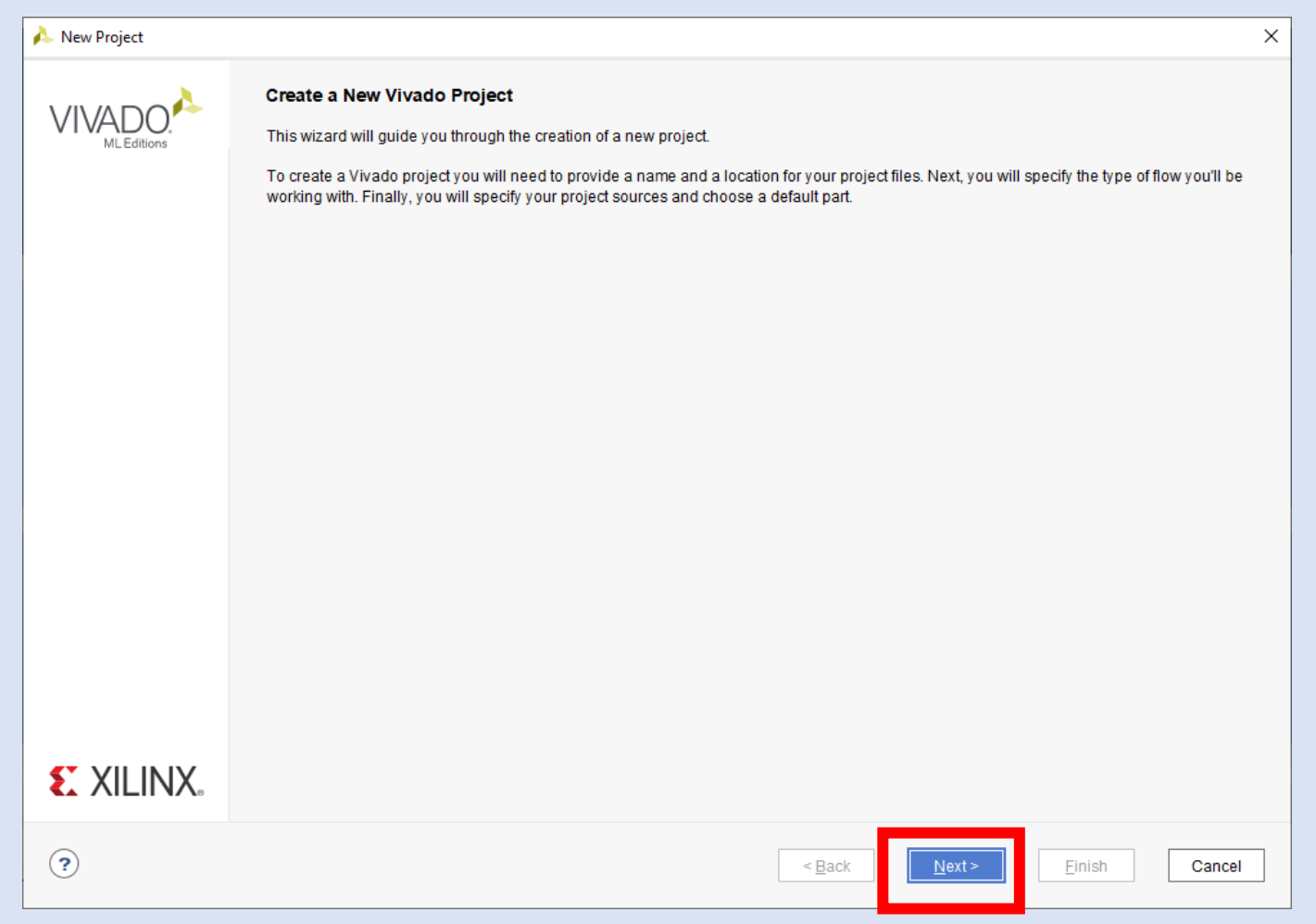
Lab 1: Understanding Vitis Project creation & Flow

Step 1 – Open Vivado 2021.1 – Click Create New Project



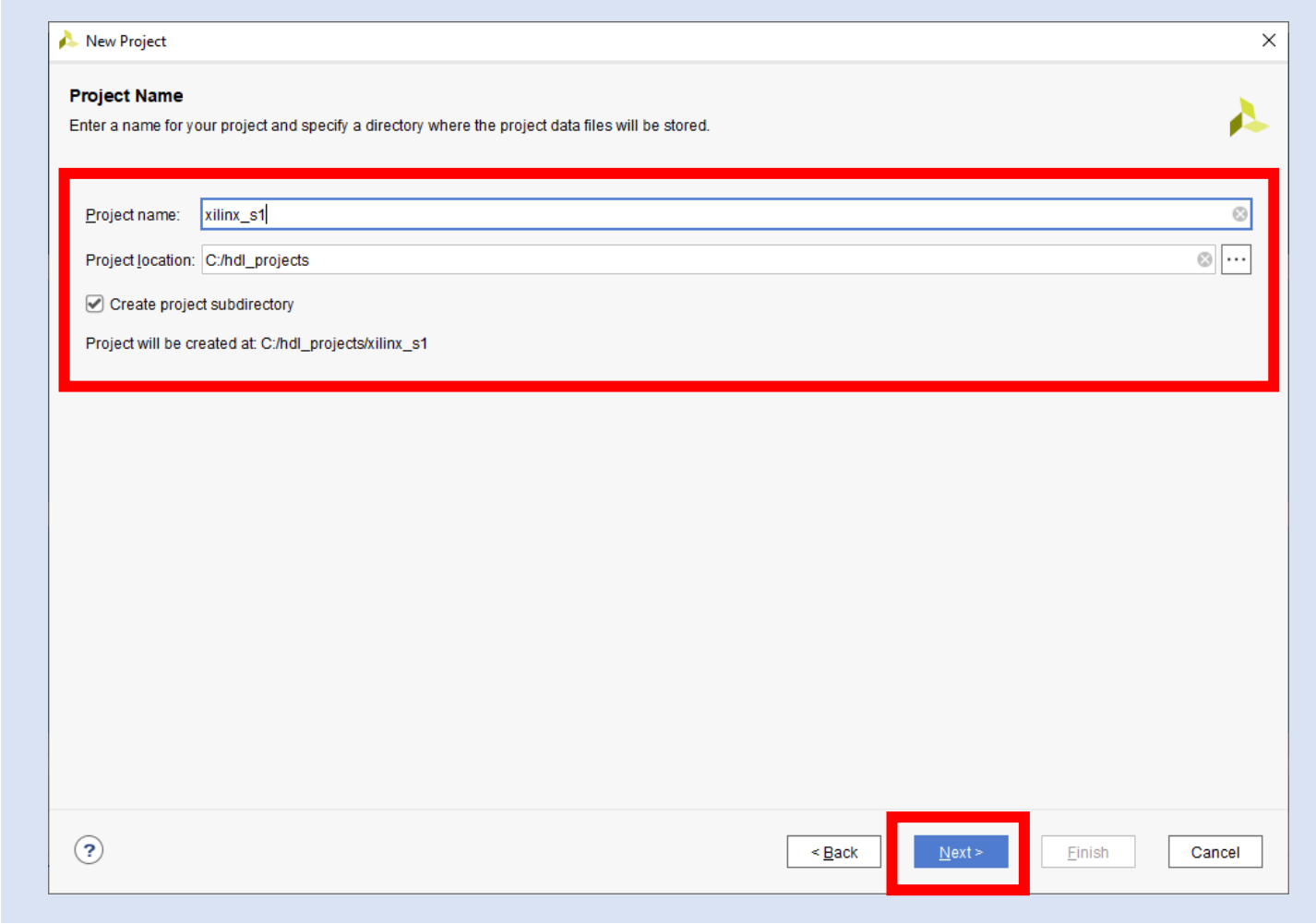
Lab 1: Understanding Vitis Project creation & Flow

Step 2 – Click Next



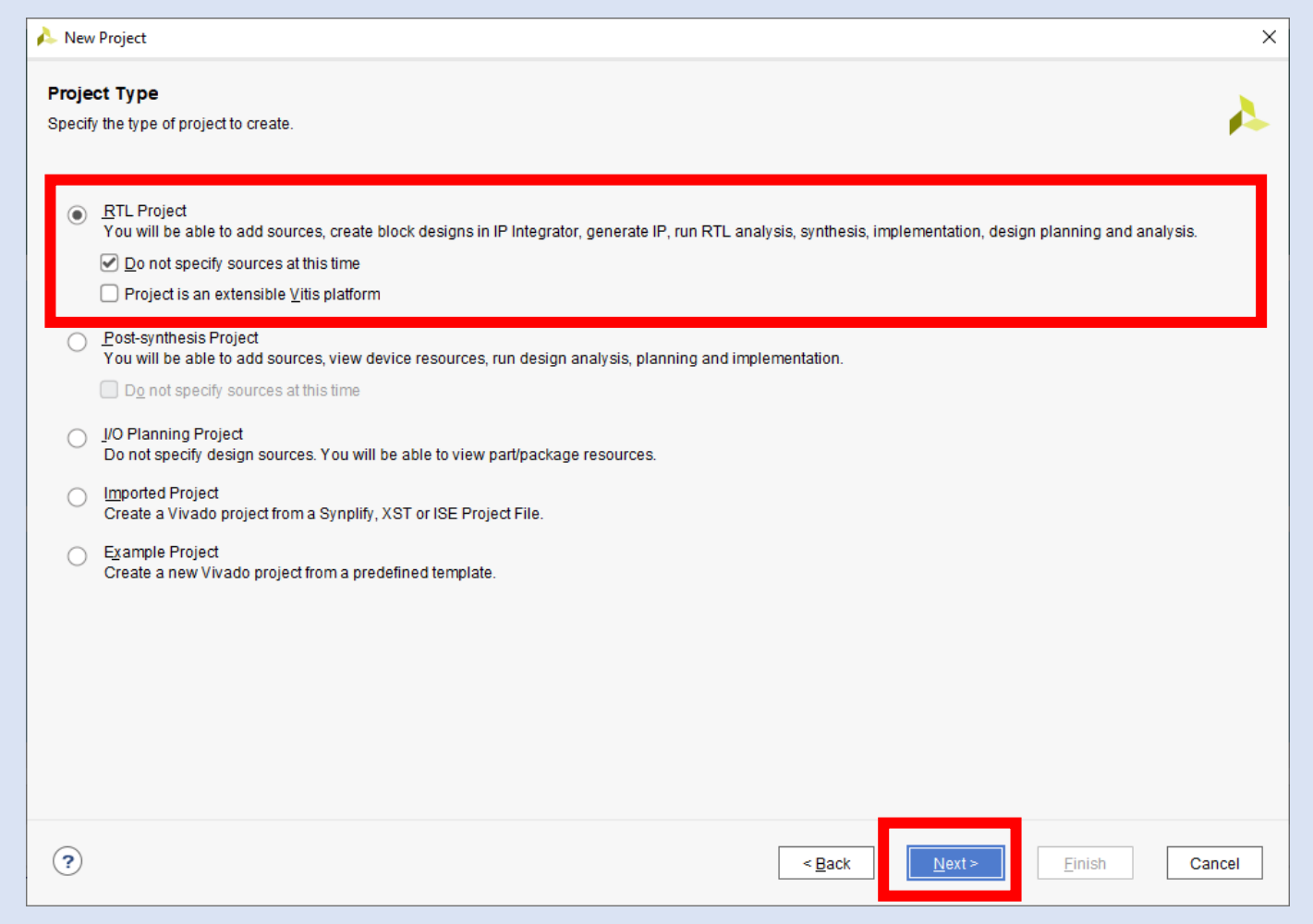
Lab 1: Understanding Vitis Project creation & Flow

Step 3 – Enter a project name and location to save the project, click next



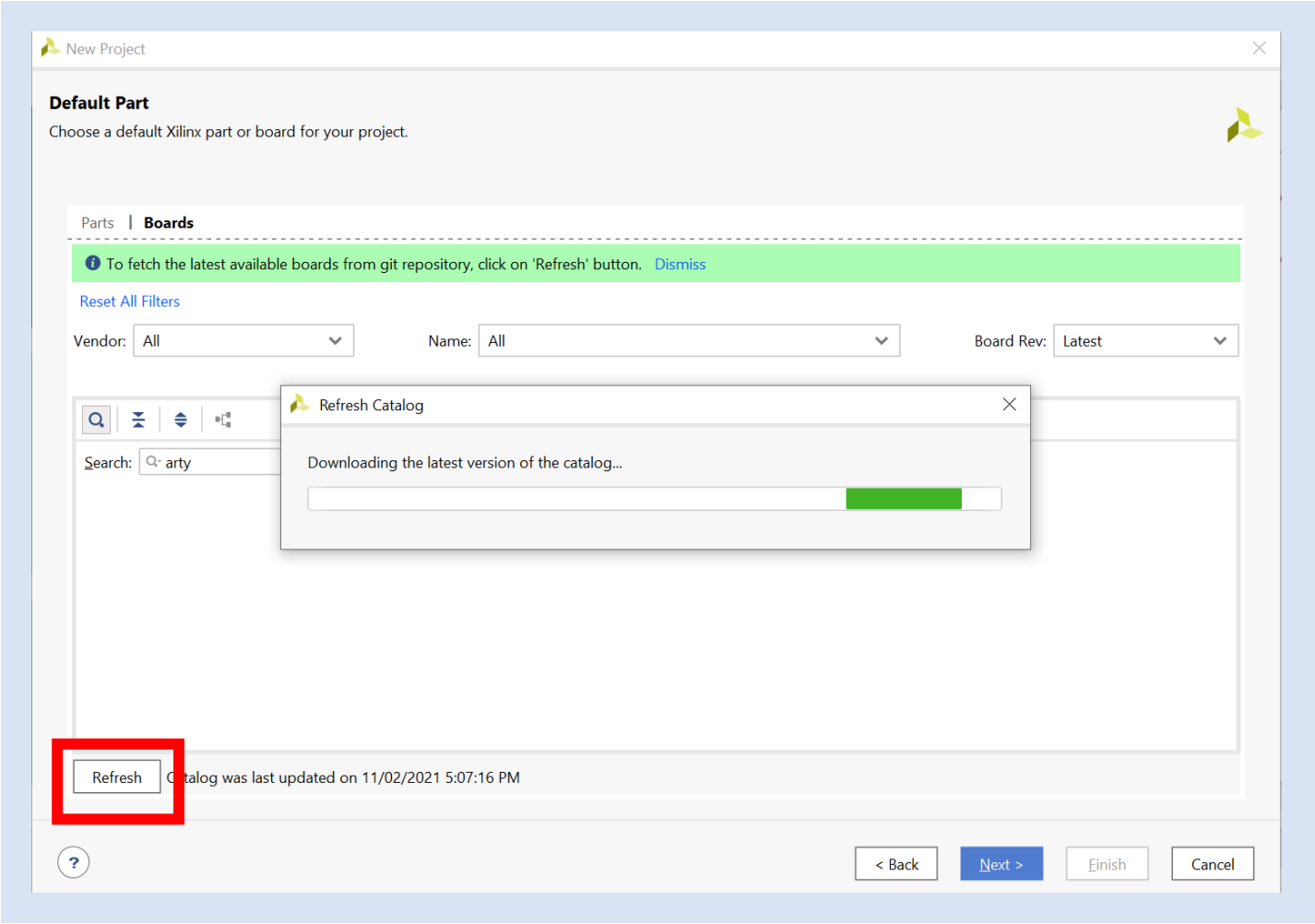
Lab 1: Understanding Vitis Project creation & Flow

Step 4 – Select RTL project and check do not include sources, click next



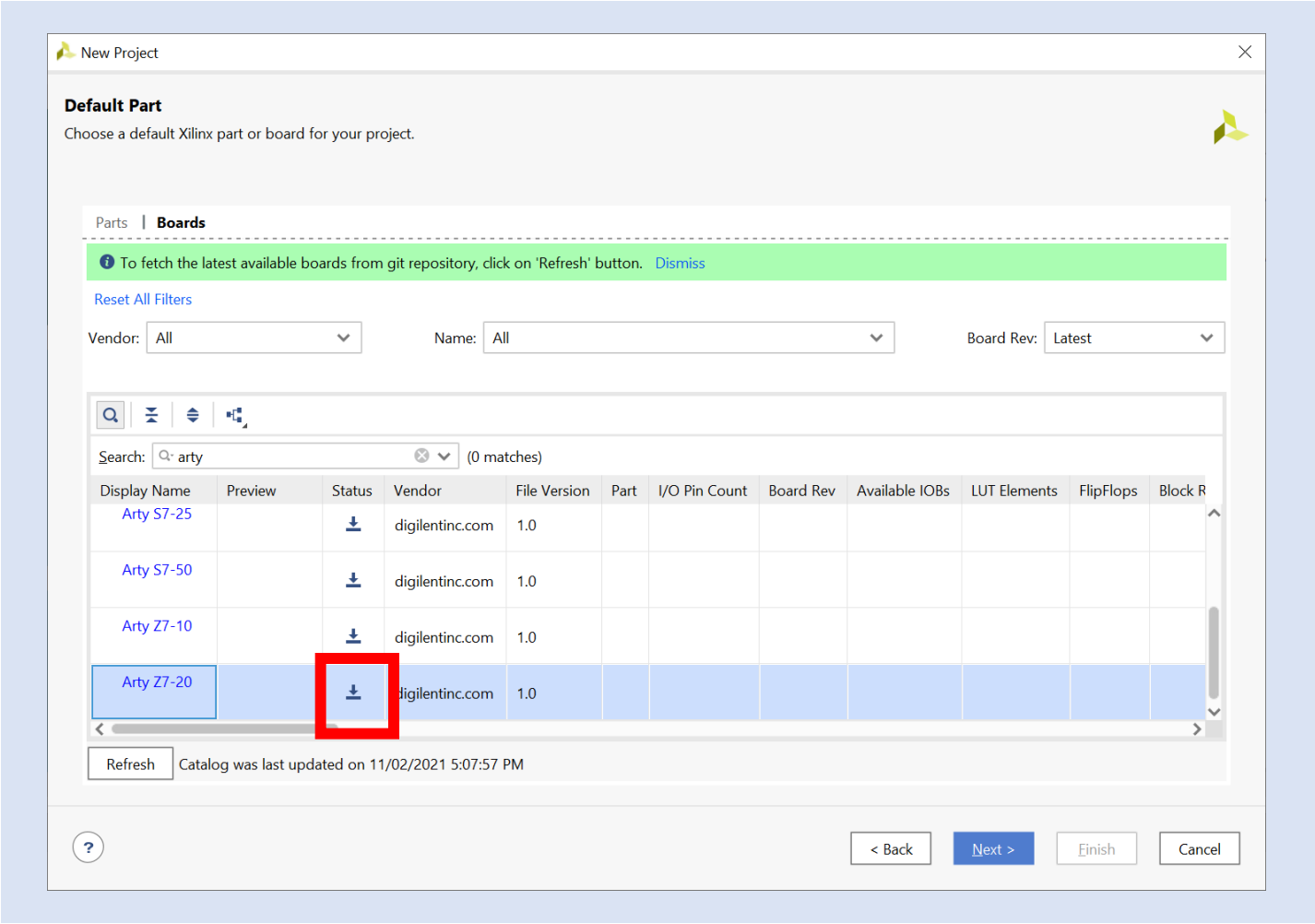
Lab 1: Understanding Vitis Project creation & Flow

Step 5 – If the Arty Z7 isn't in the list of boards select Refresh and the board list will be updated



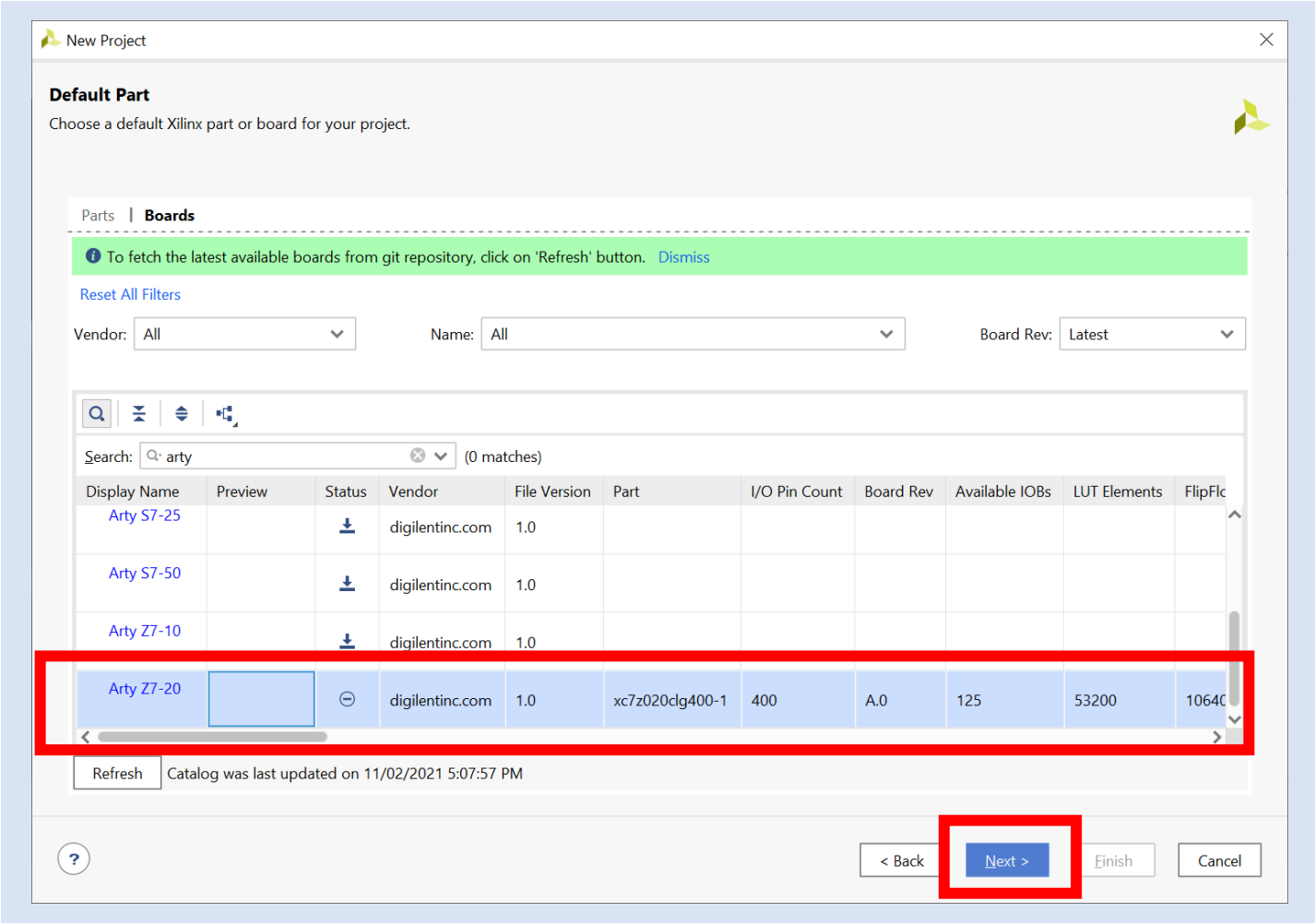
Lab 1: Understanding Vitis Project creation & Flow

Step 6 – Select the download and the board will install



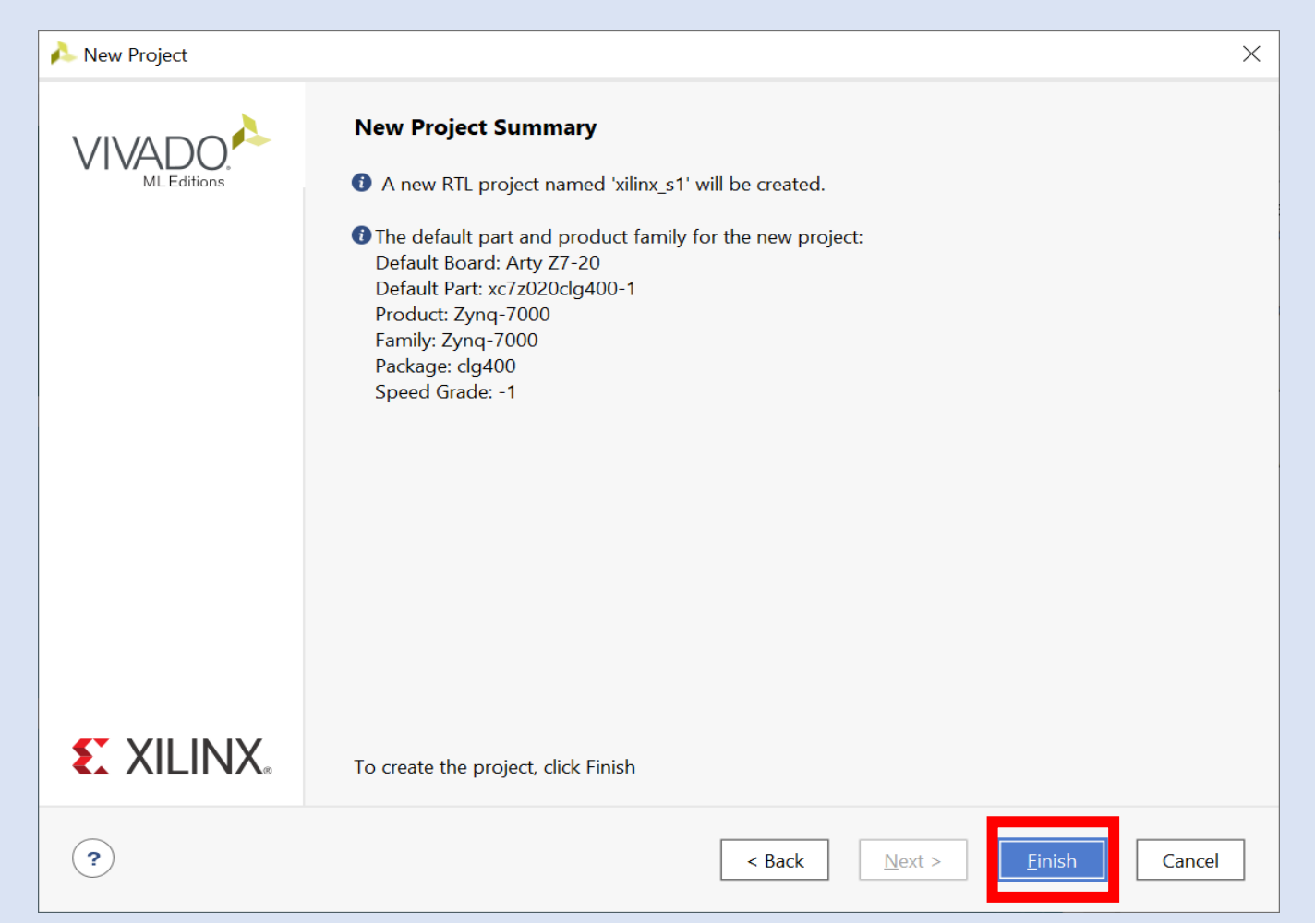
Lab 1: Understanding Vitis Project creation & Flow

Step 7 – Select Vendor Diglentinc and Arty Z7-20, click next



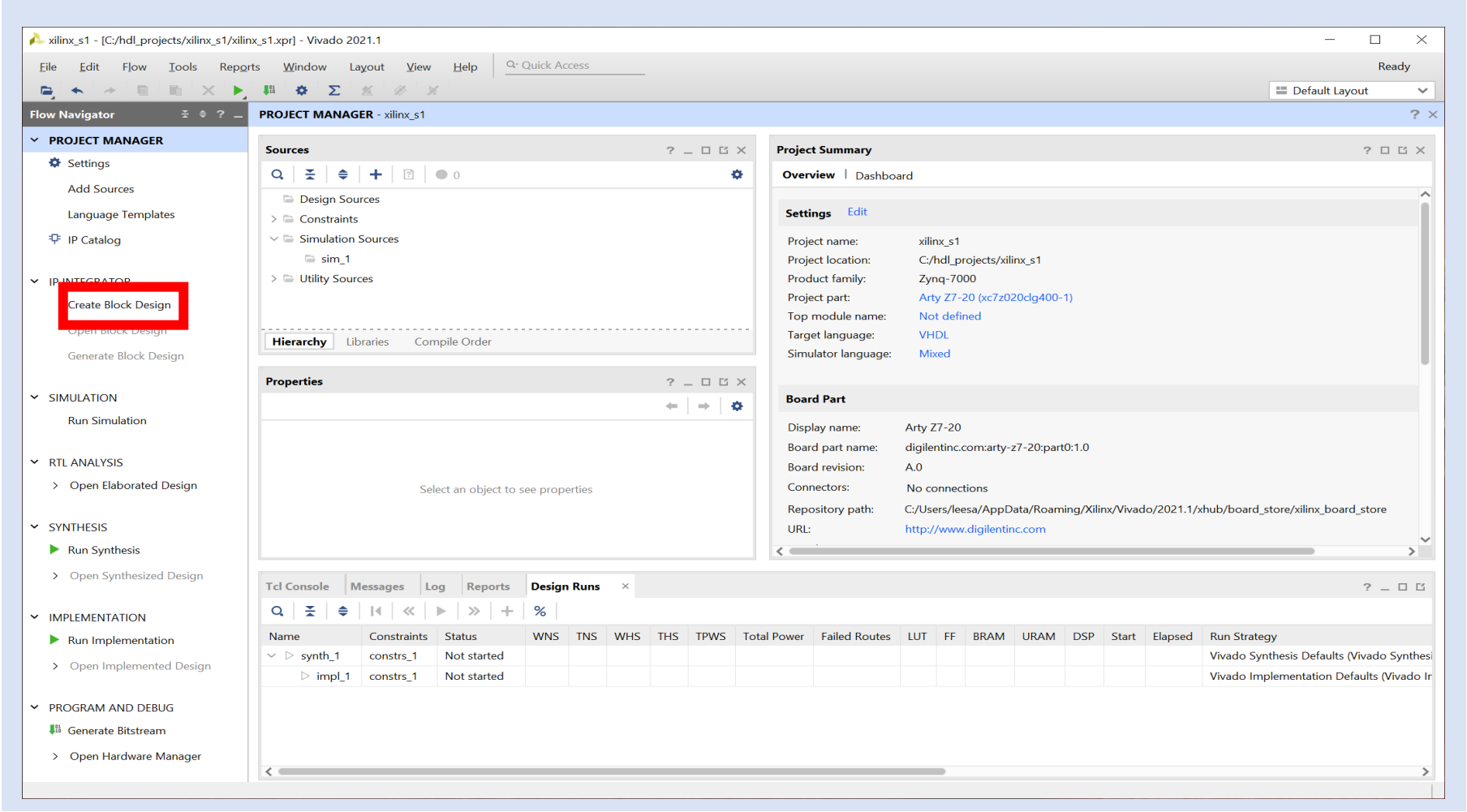
Lab 1: Understanding Vitis Project creation & Flow

Step 8 – Click Finish



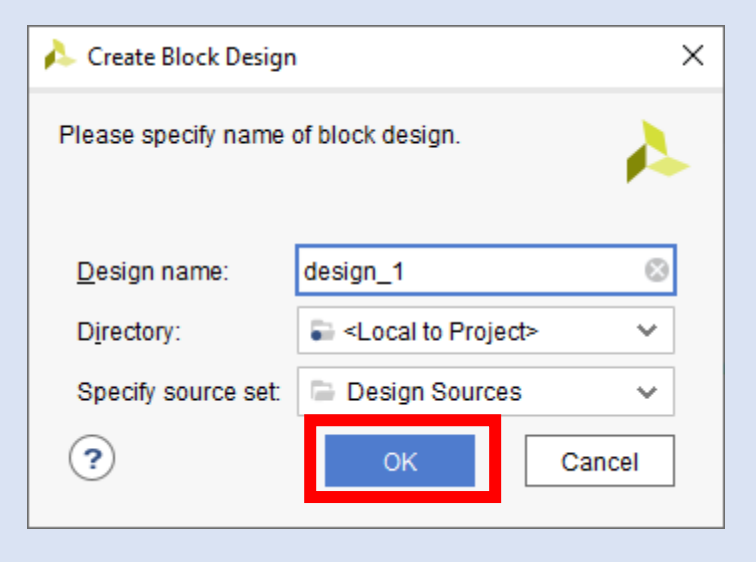
Lab 1: Understanding Vitis Project creation & Flow

Step 9 – Click on Create Block Diagram – This will open IP editor



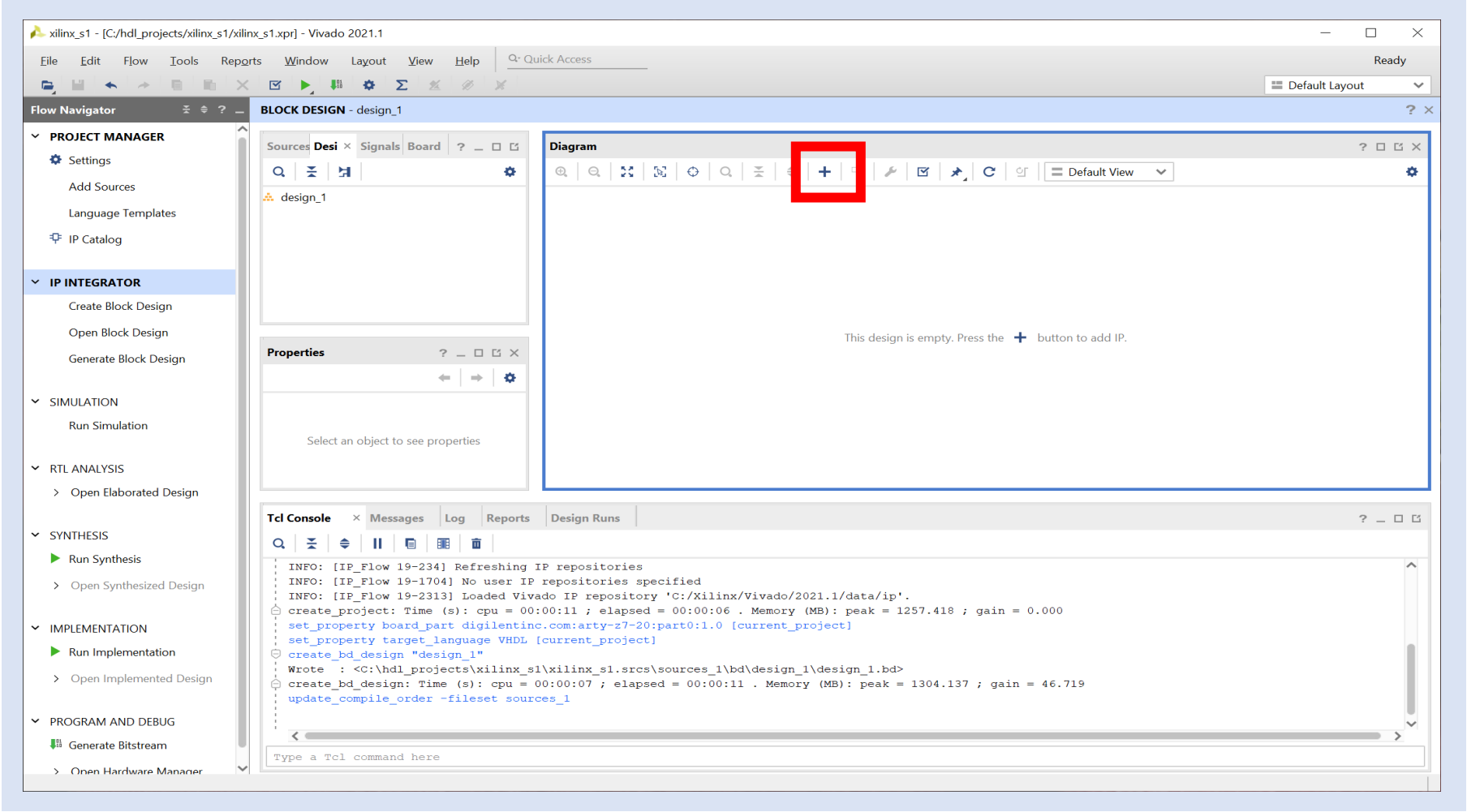
Lab 1: Understanding Vitis Project creation & Flow

Step 10 – Leave the settings as default and click OK



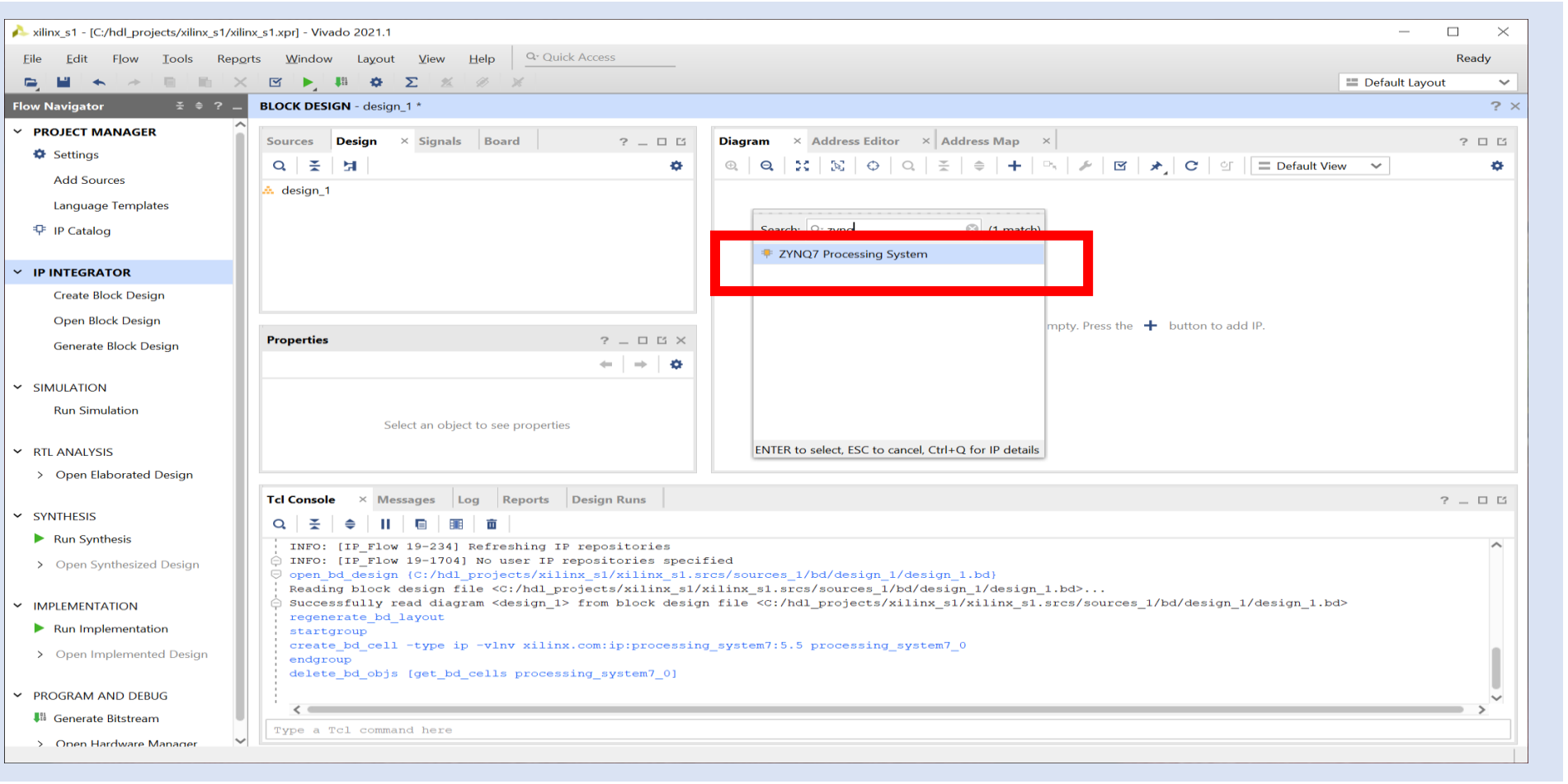
Lab 1: Understanding Vitis Project creation & Flow

Step 11 – Click on the + button to open the IP list



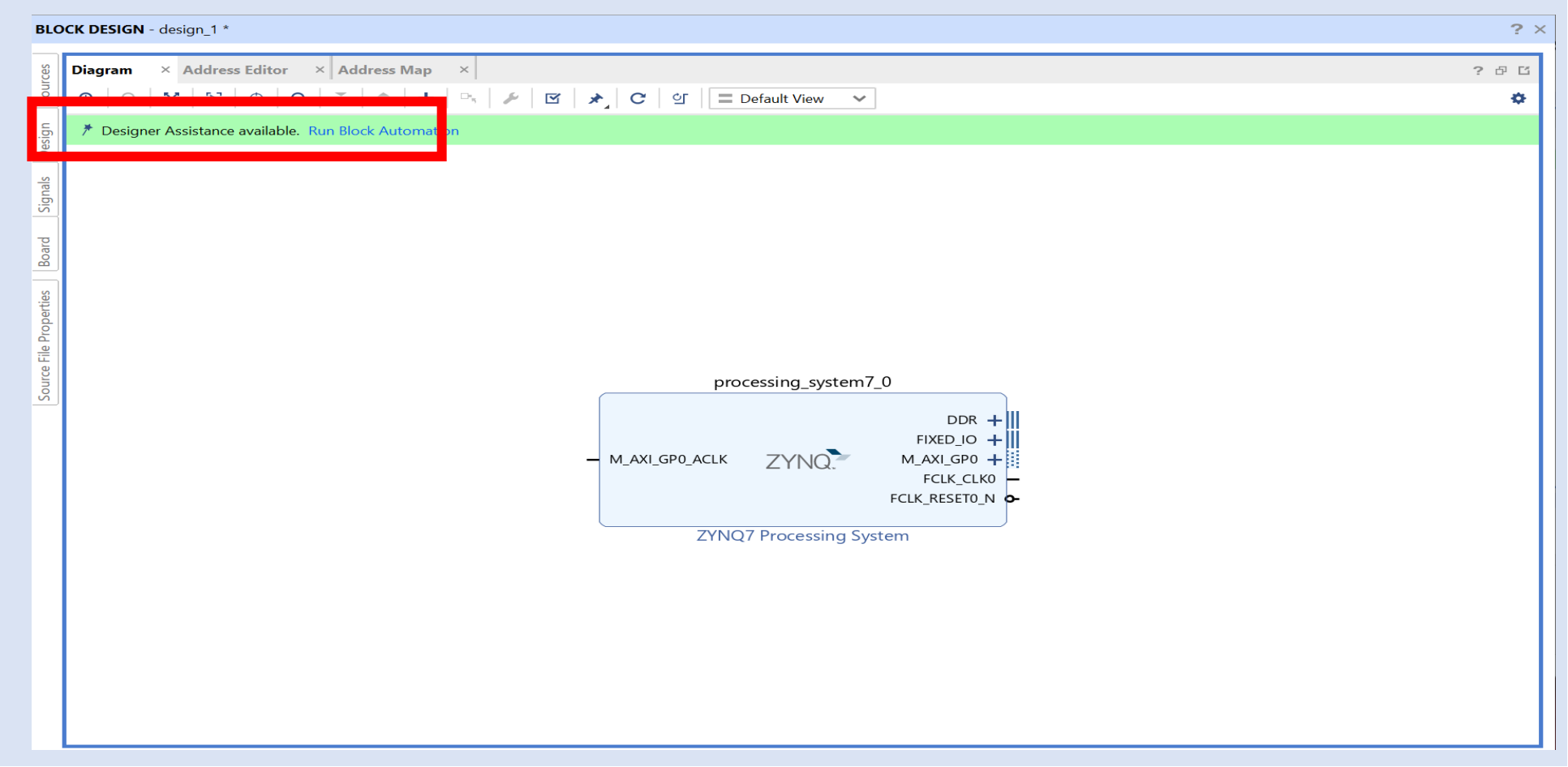
Lab 1: Understanding Vitis Project creation & Flow

Step 12 – In the search bar, type Ultra and select the Zynq UltraScale+ MPSoC block. Double click on this to insert the IP block.



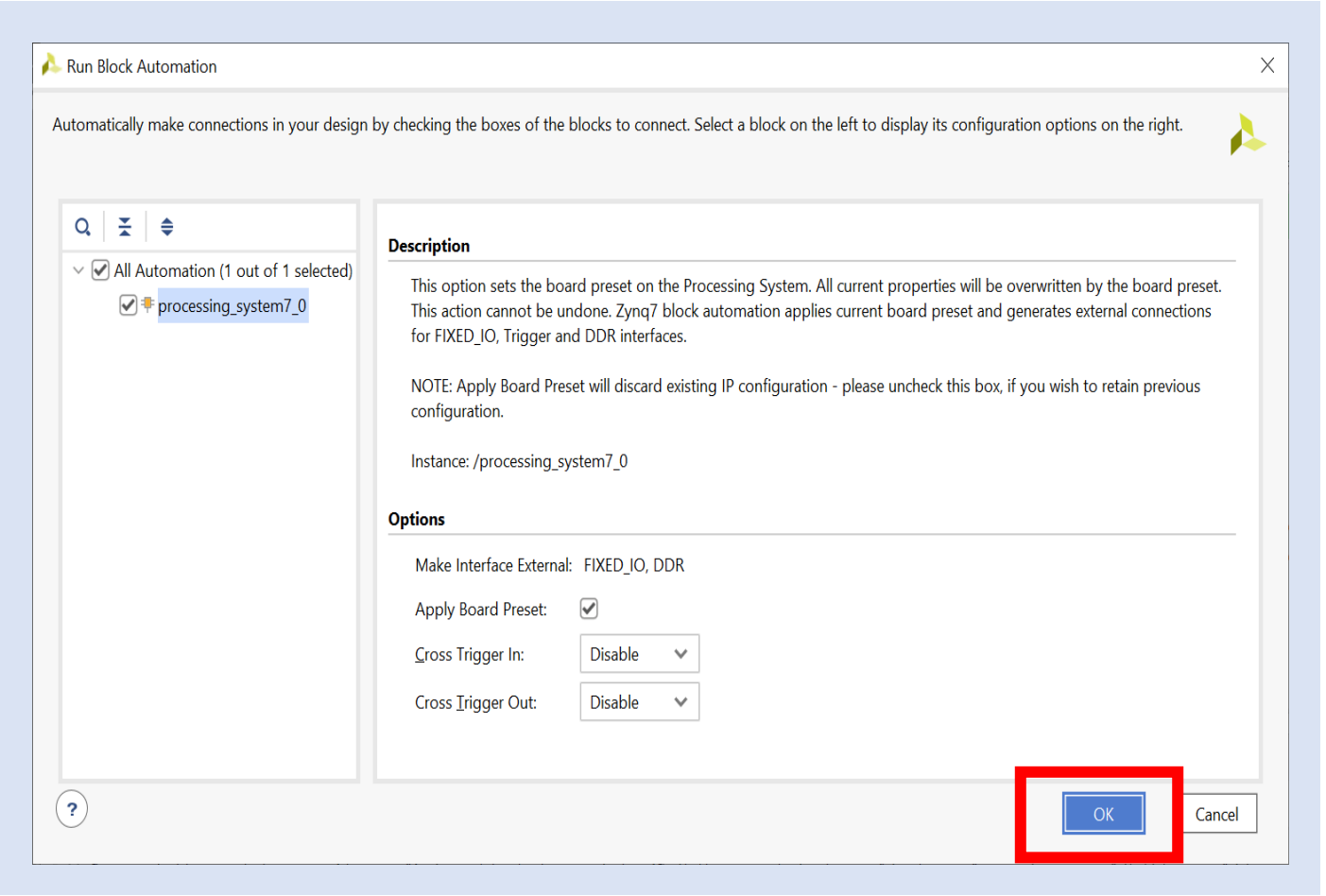
Lab 1: Understanding Vitis Project creation & Flow

Step 13 – Select Run Block Automation – This will configure the Processing System for the ArtyZ7 setting e.g. DDR timing, Clocking etc.



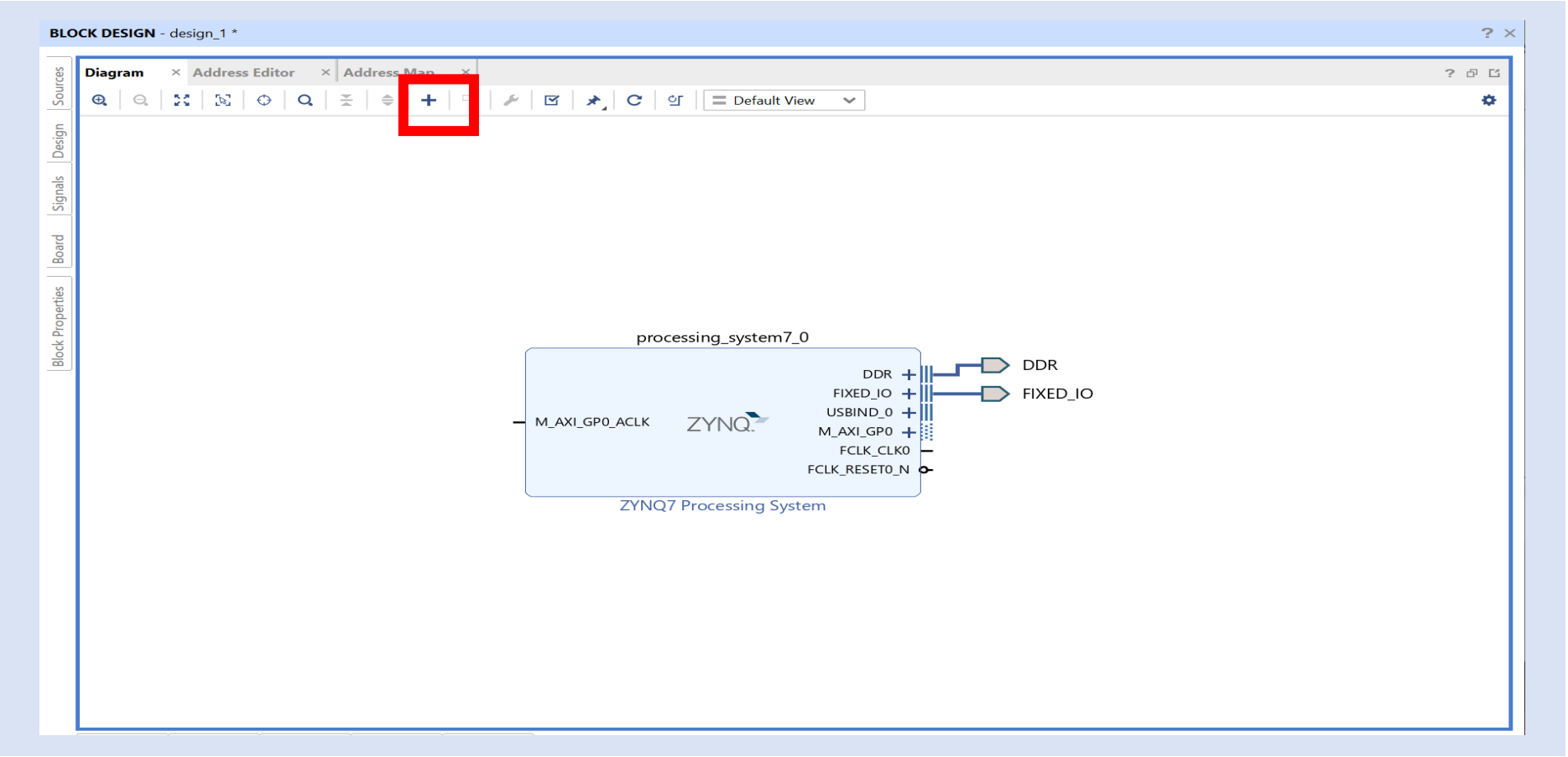
Lab 1: Understanding Vitis Project creation & Flow

Step 14 – Click on the OK button, the automation will run and configure the processing block for the ArtyZ7.



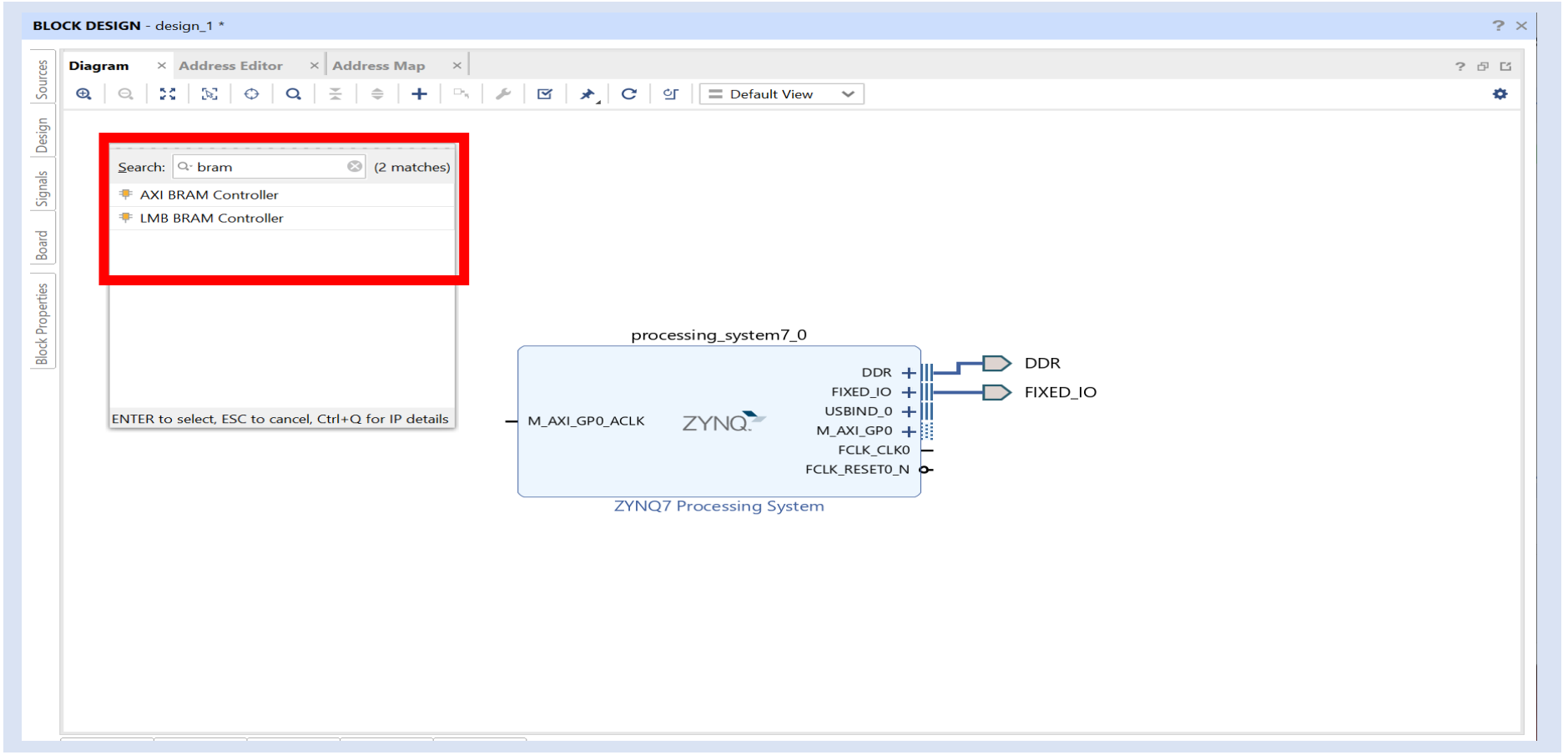
Lab 1: Understanding Vitis Project creation & Flow

Step 15 – Click on the + Symbol



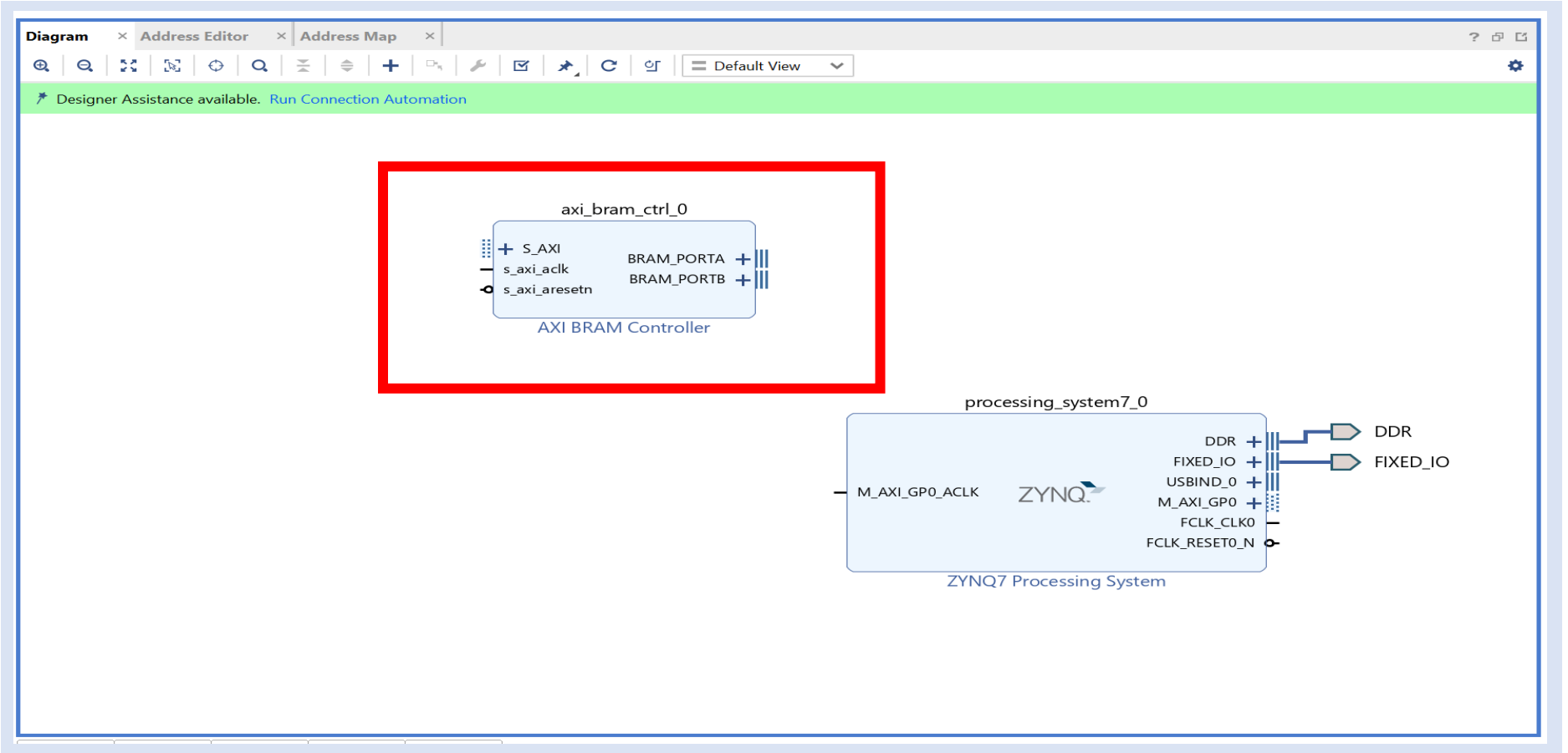
Lab 1: Understanding Vitis Project creation & Flow

Step 16 – Type in BRAM and double click on AXI BRAM Controller to add the IP



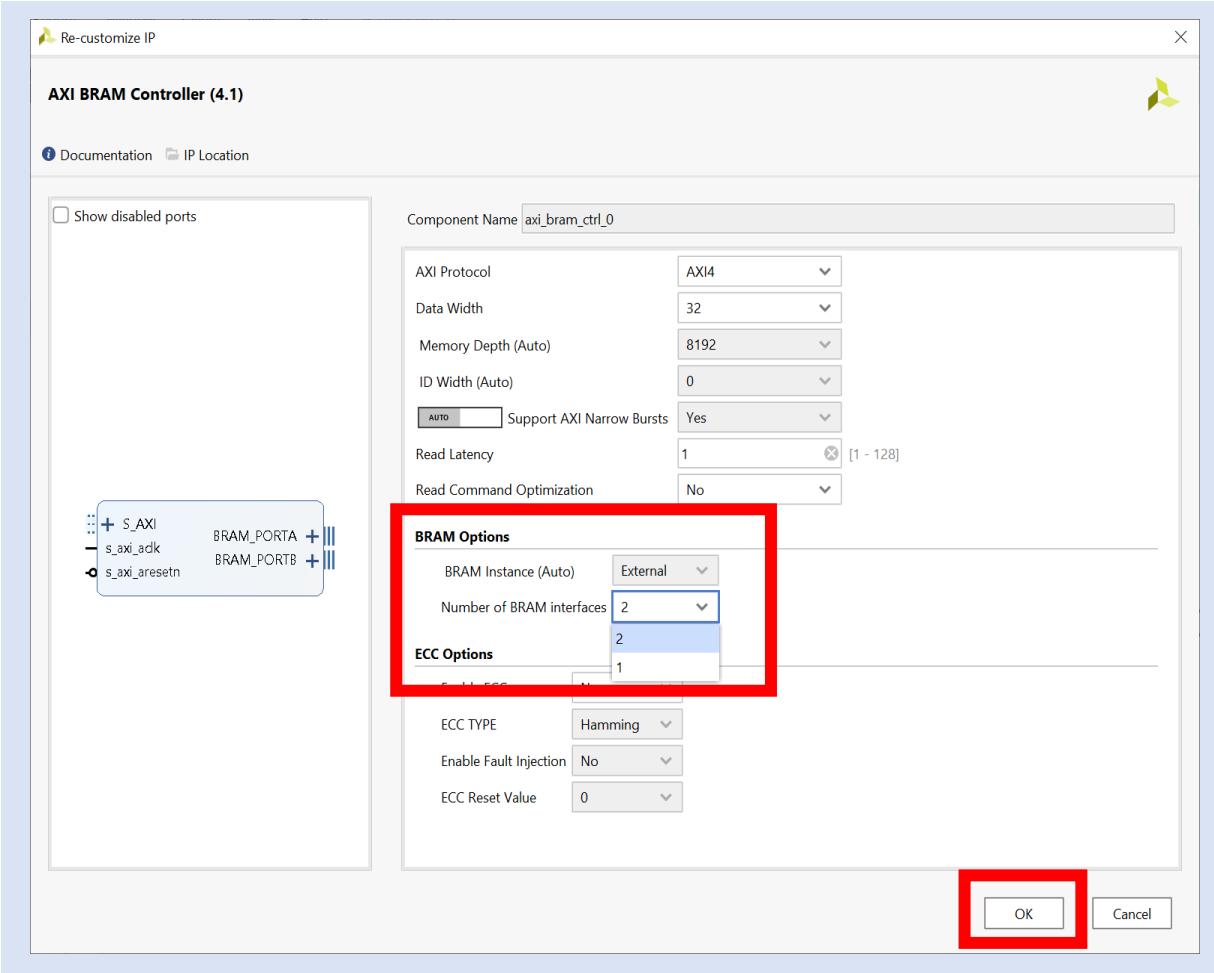
Lab 1: Understanding Vitis Project creation & Flow

Step 17 – Double click on the AXI BRAM Controller



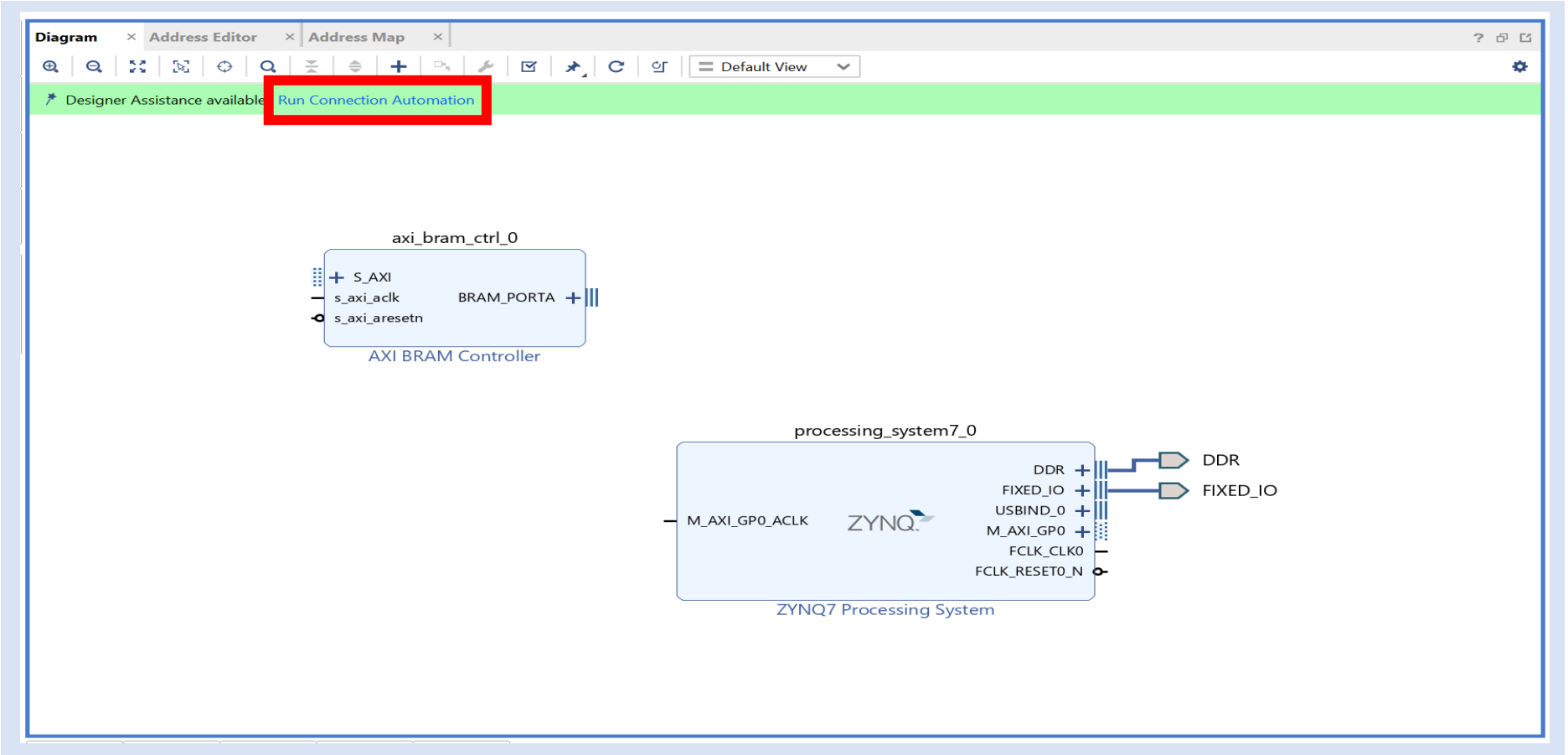
Lab 1: Understanding Vitis Project creation & Flow

Step 18 – Change the Number of BRAM Interfaces to 1, click OK



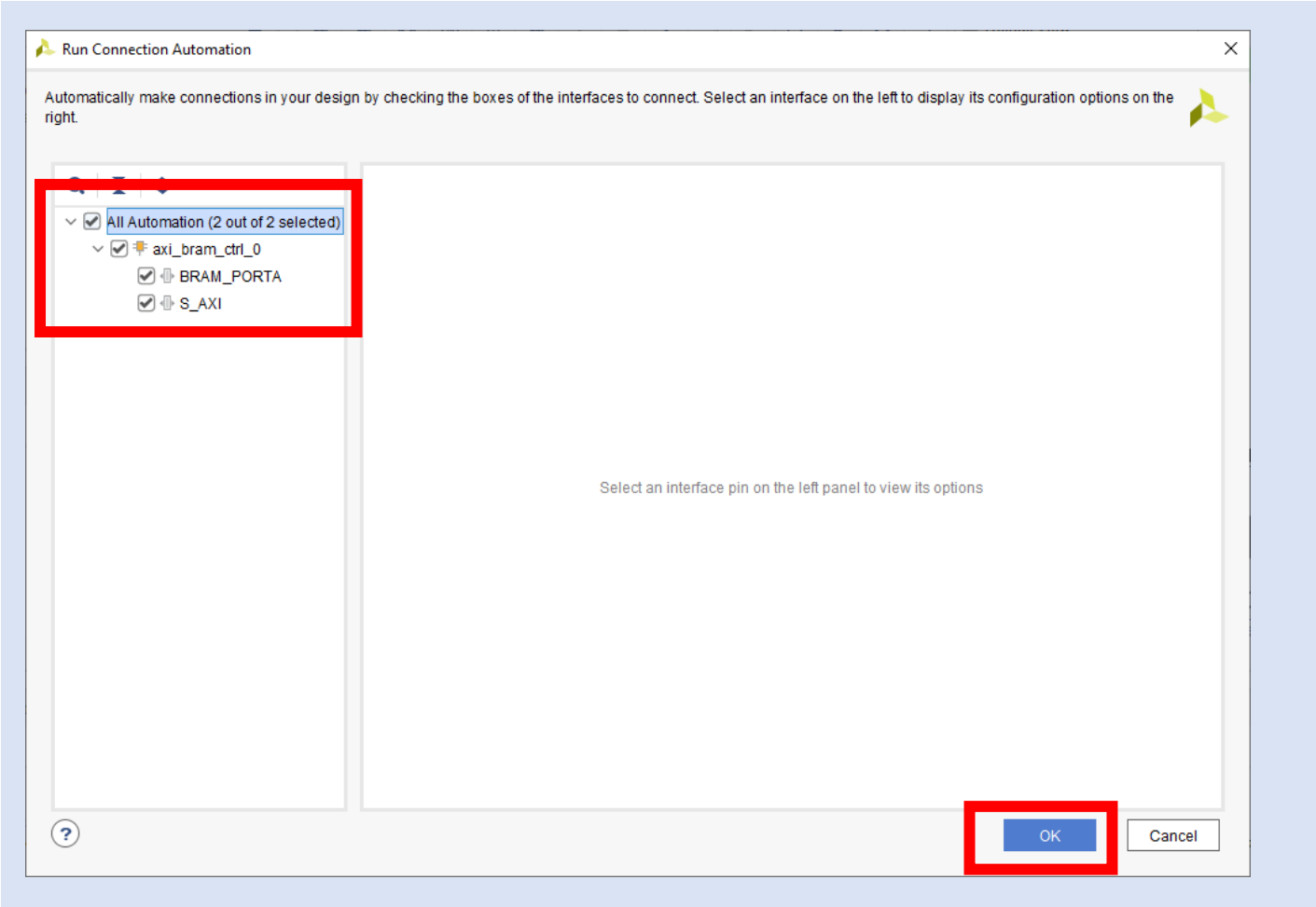
Lab 1: Understanding Vitis Project creation & Flow

Step 19 – Click on Run Connection Automation



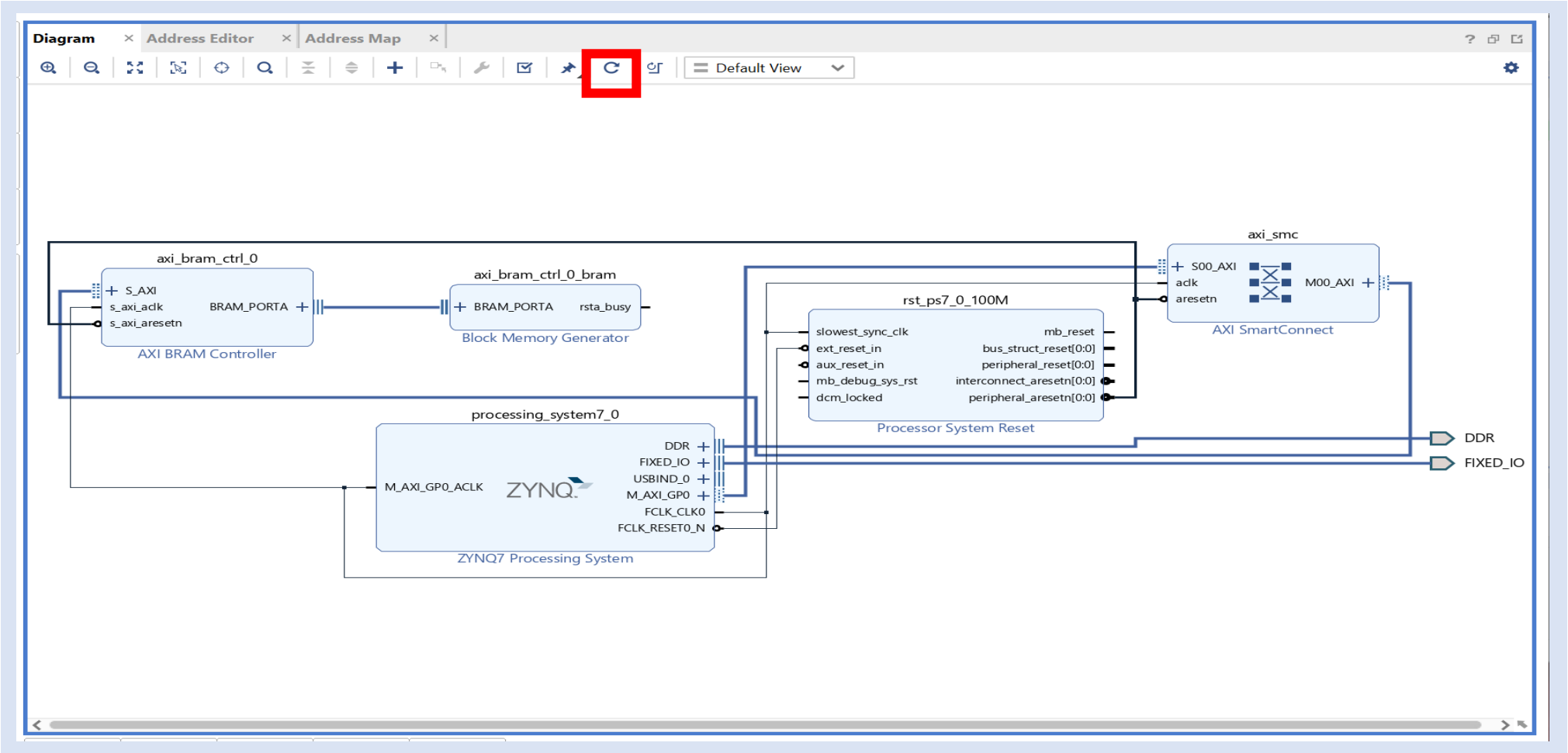
Lab 1: Understanding Vitis Project creation & Flow

Step 20 – Check all the boxes, click OK



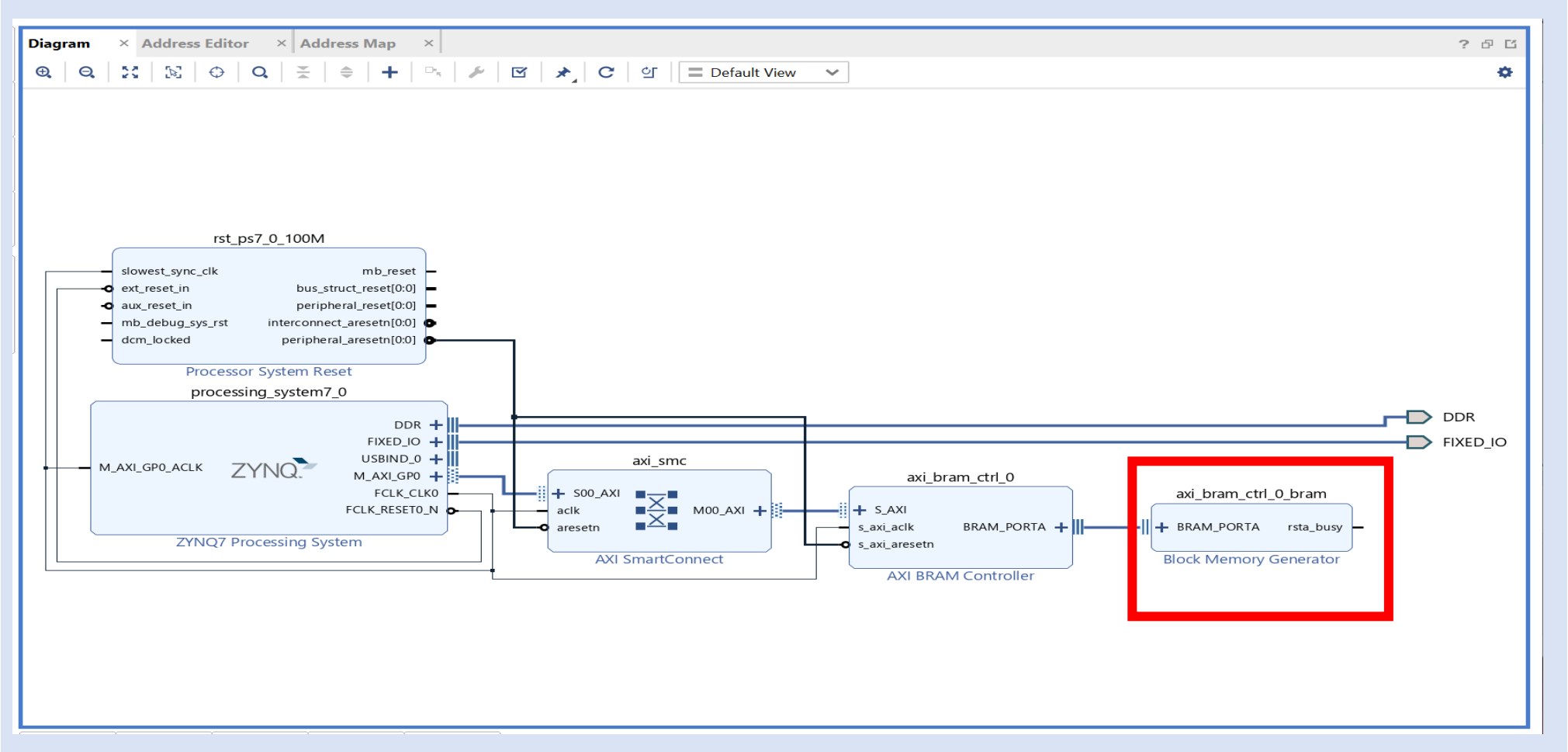
Lab 1: Understanding Vitis Project creation & Flow

Step 21 – Click on the Regenerate Layout – This will mage the diagram more logical



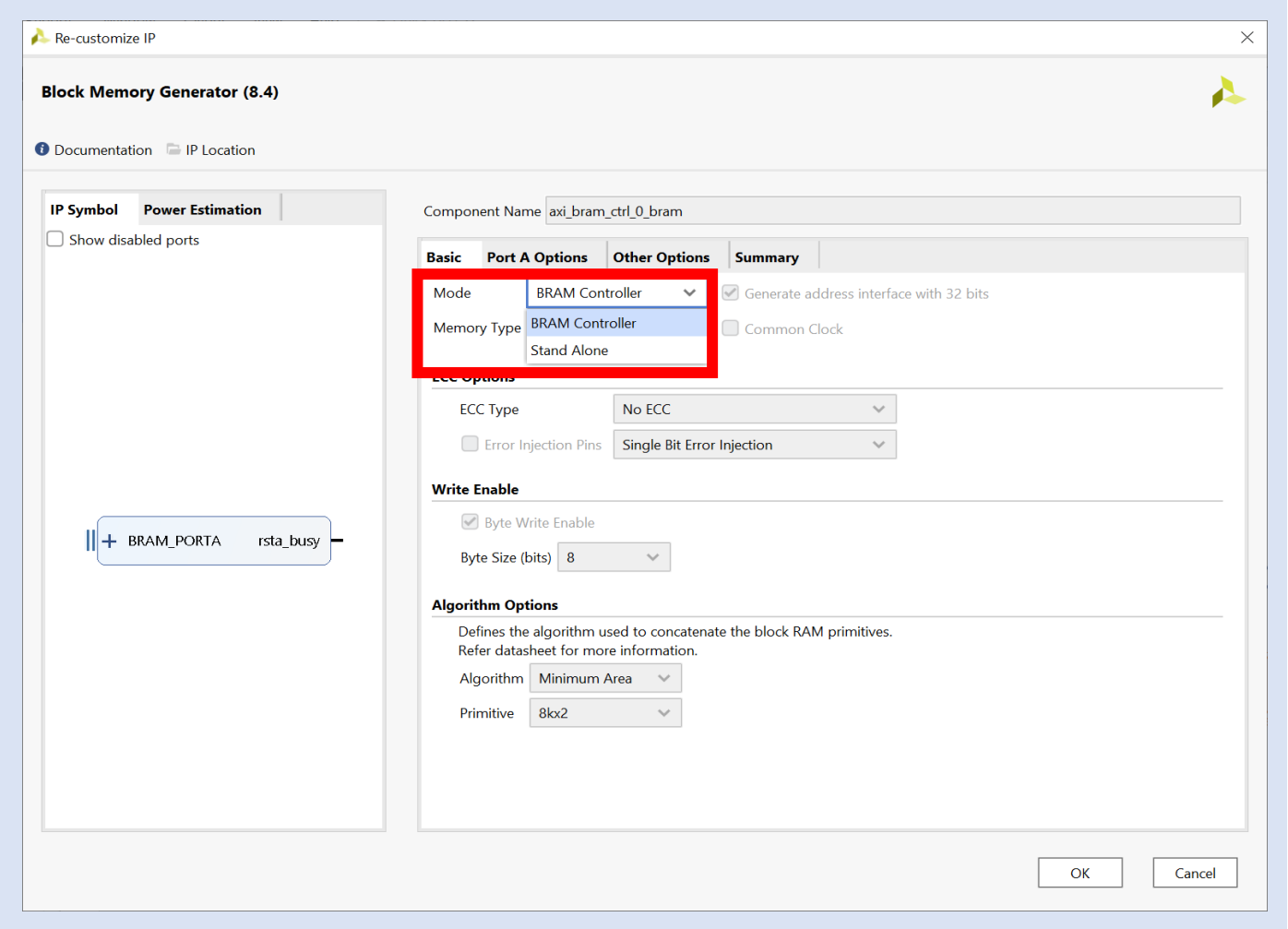
Lab 1: Understanding Vitis Project creation & Flow

Step 22 – Double Click on the BRAM Block



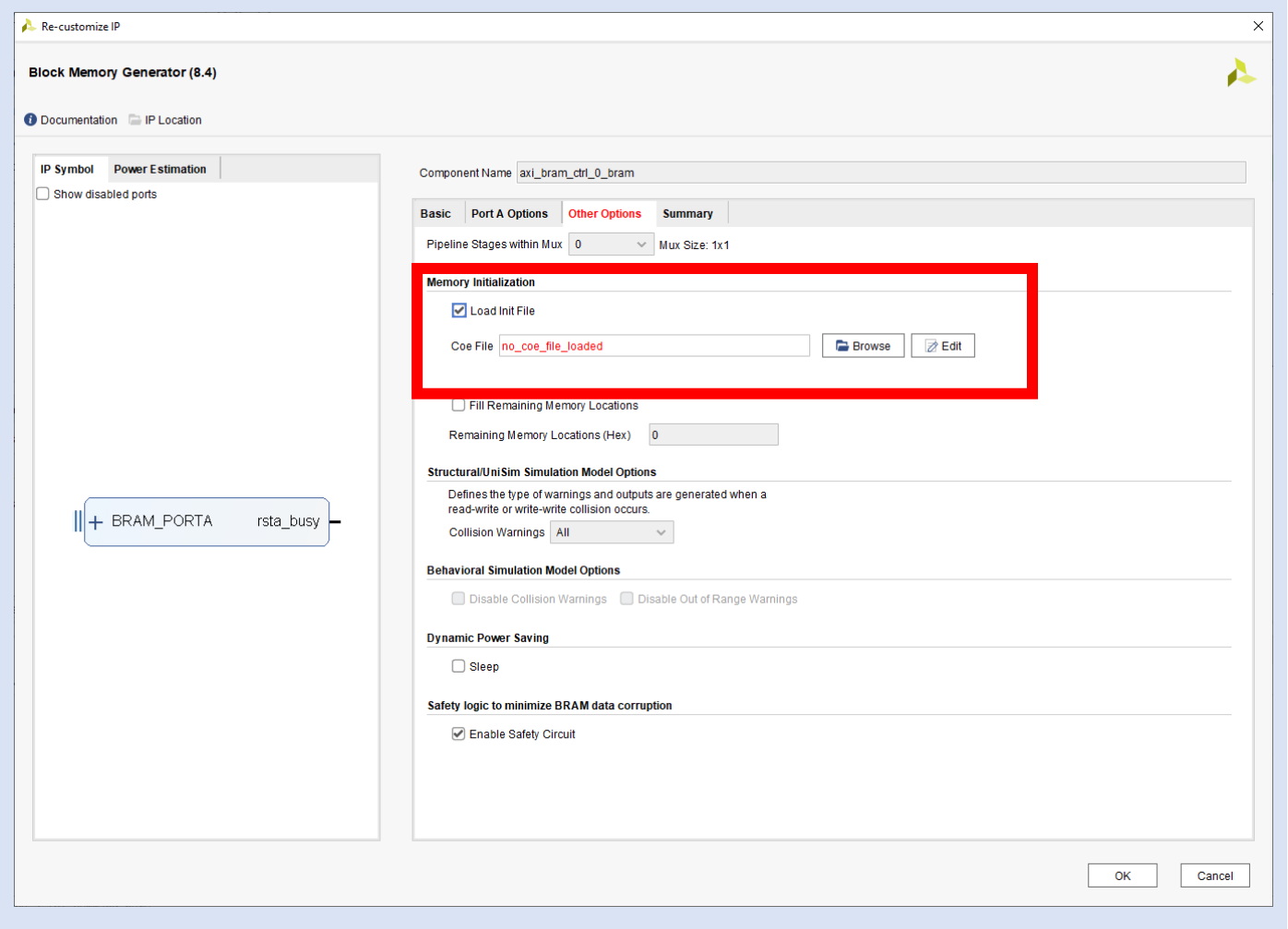
Lab 1: Understanding Vitis Project creation & Flow

Step 23 – Change the mode to Standalone, make sure check use 32 bit addressing is set



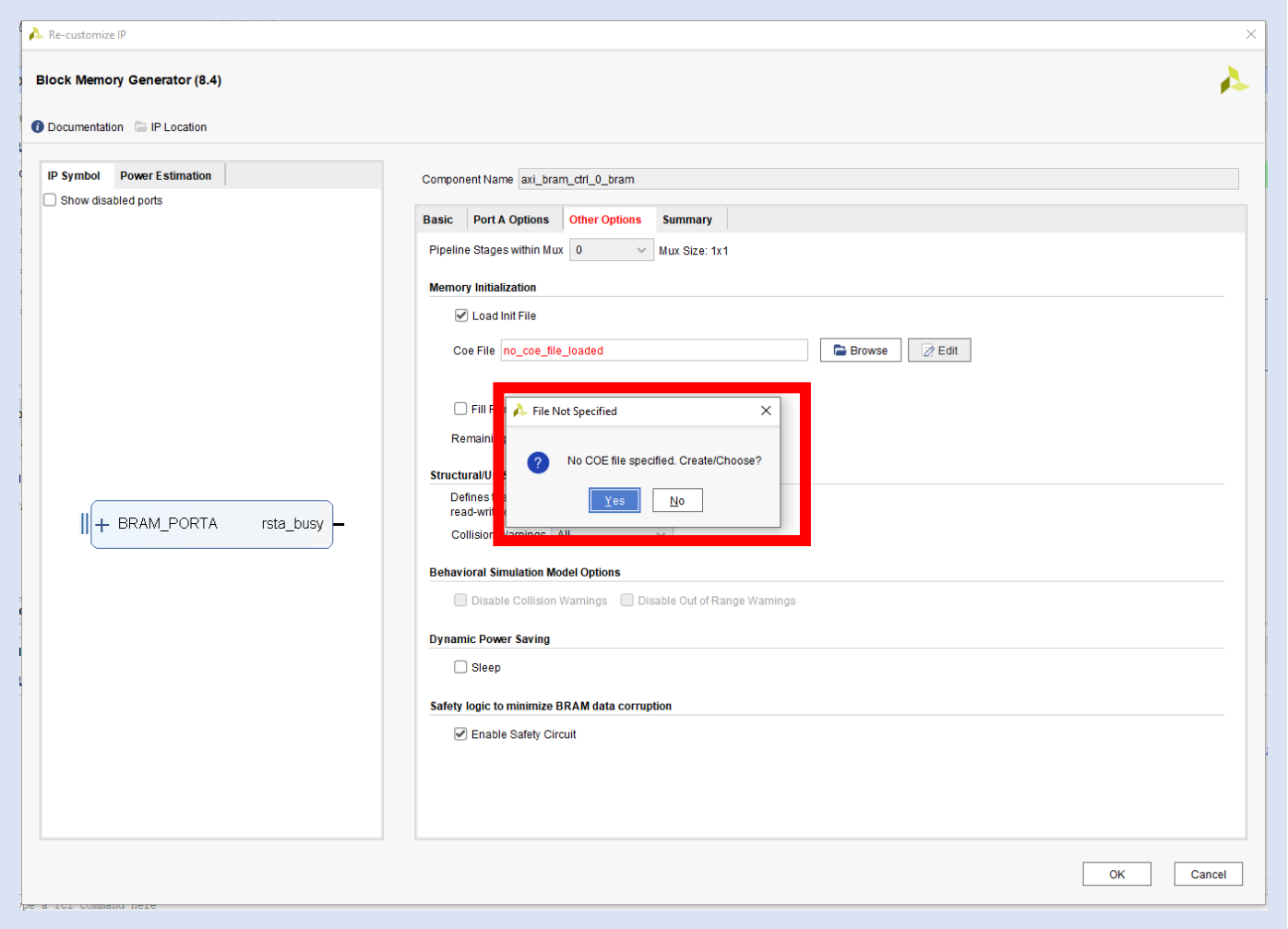
Lab 1: Understanding Vitis Project creation & Flow

Step 24 – Check load Init File, click on edit continue to step 25



Lab 1: Understanding Vitis Project creation & Flow

Step 25 – Click Yes



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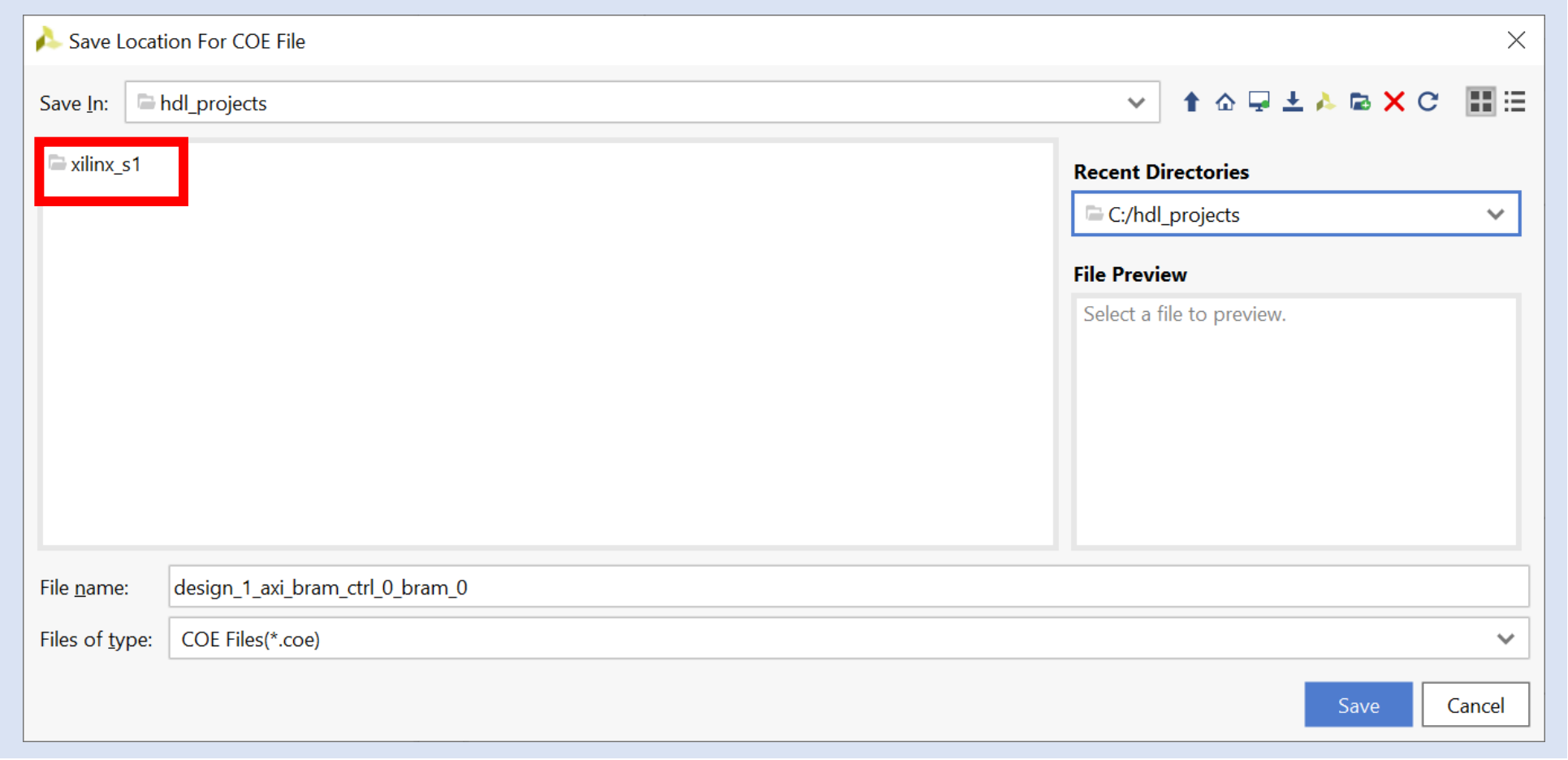
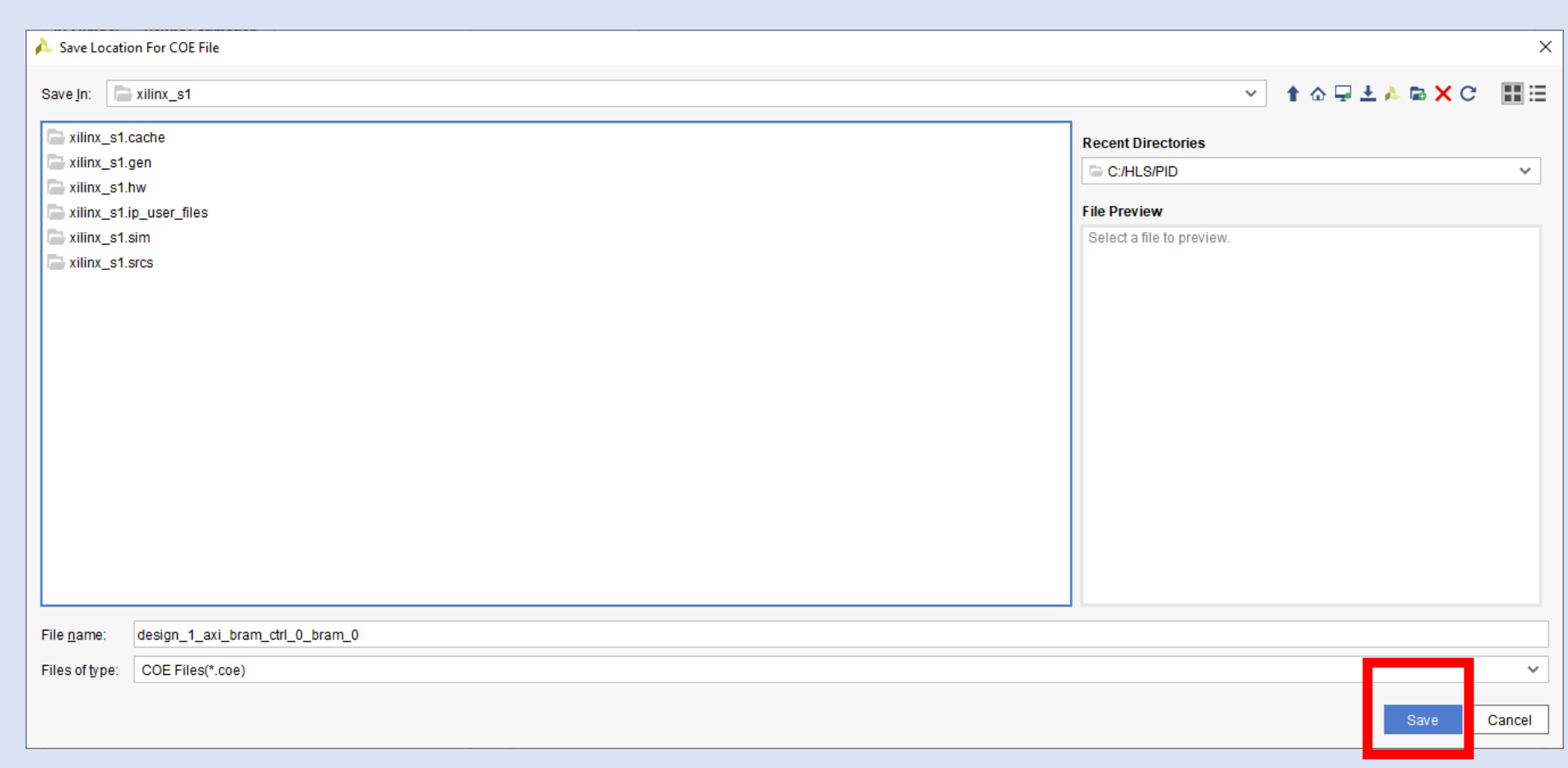
Step 26 – Select the project folder and continue to step 27



Lab 1: Understanding Vitis Project creation & Flow

Step 27 – Select a location inside the project to save the file and select OK

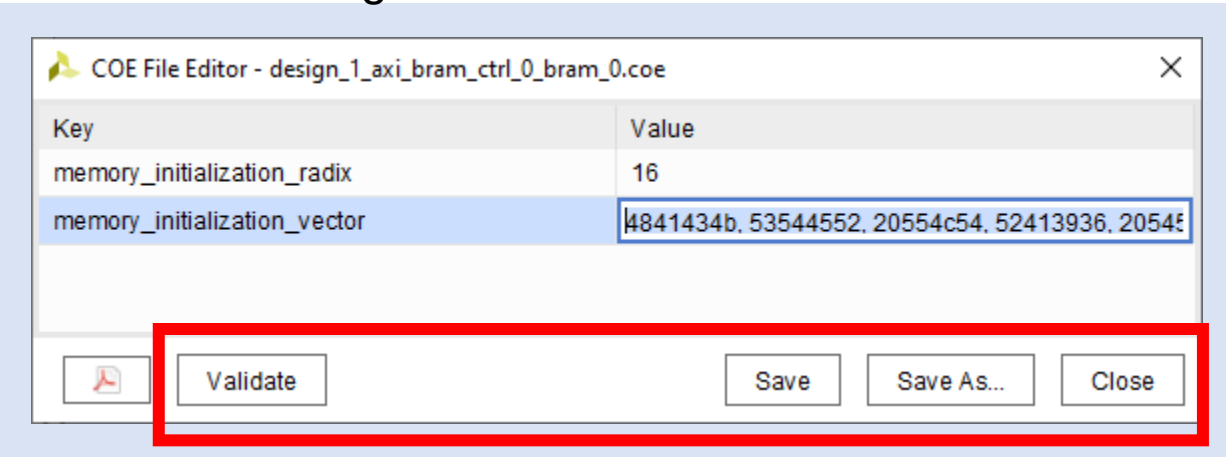


Lab 1: Understanding Vitis Project creation & Flow

Step 28 – Enter the following

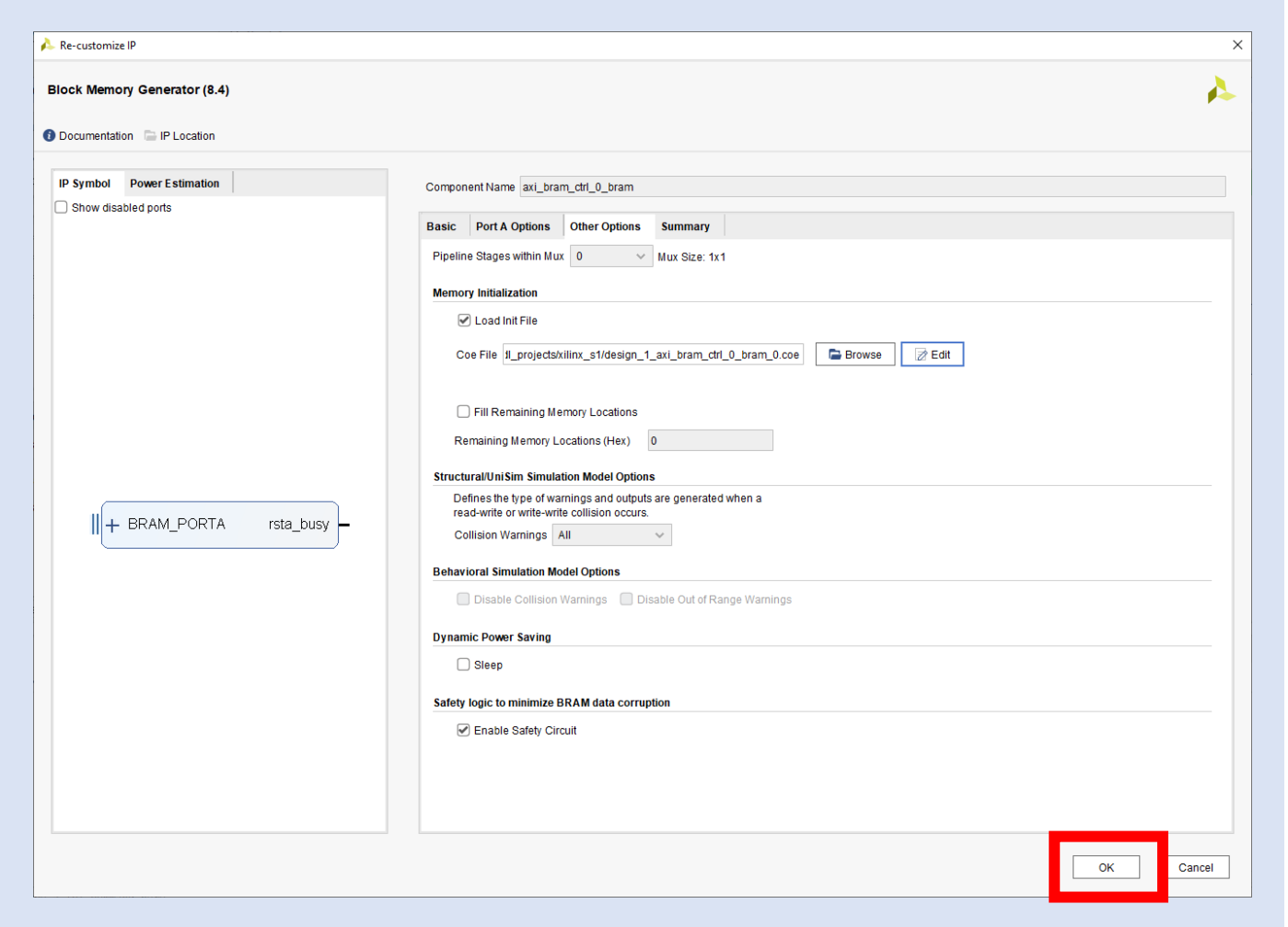
Memory Initialization Radix = 16
Memory Initialization Vector = 4841434b, 53544552, 20554c54, 52413936, 20545554, 4f524941, 0000004c,

Click Save, then Validate before closing



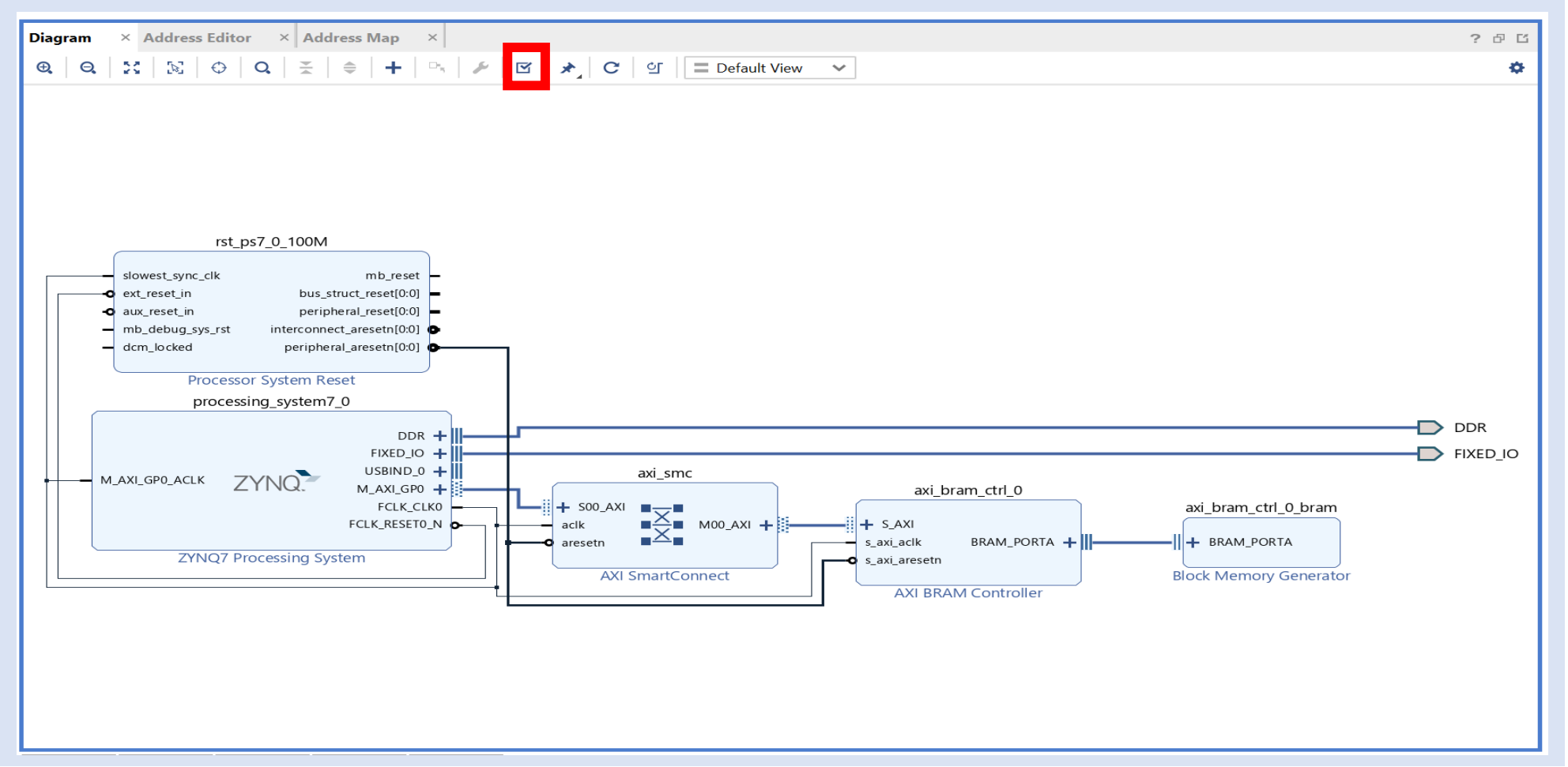
Lab 1: Understanding Vitis Project creation & Flow

Step 29 – Click OK



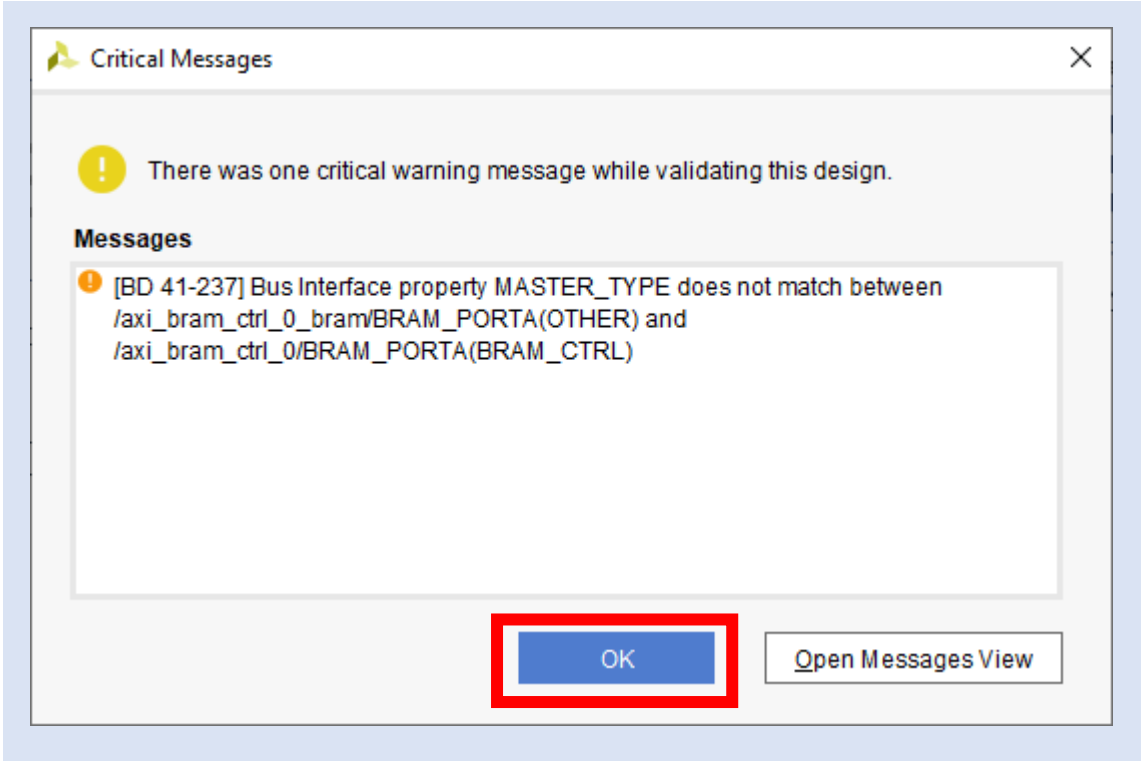
Lab 1: Understanding Vitis Project creation & Flow

Step 30 – Click on Validate the design



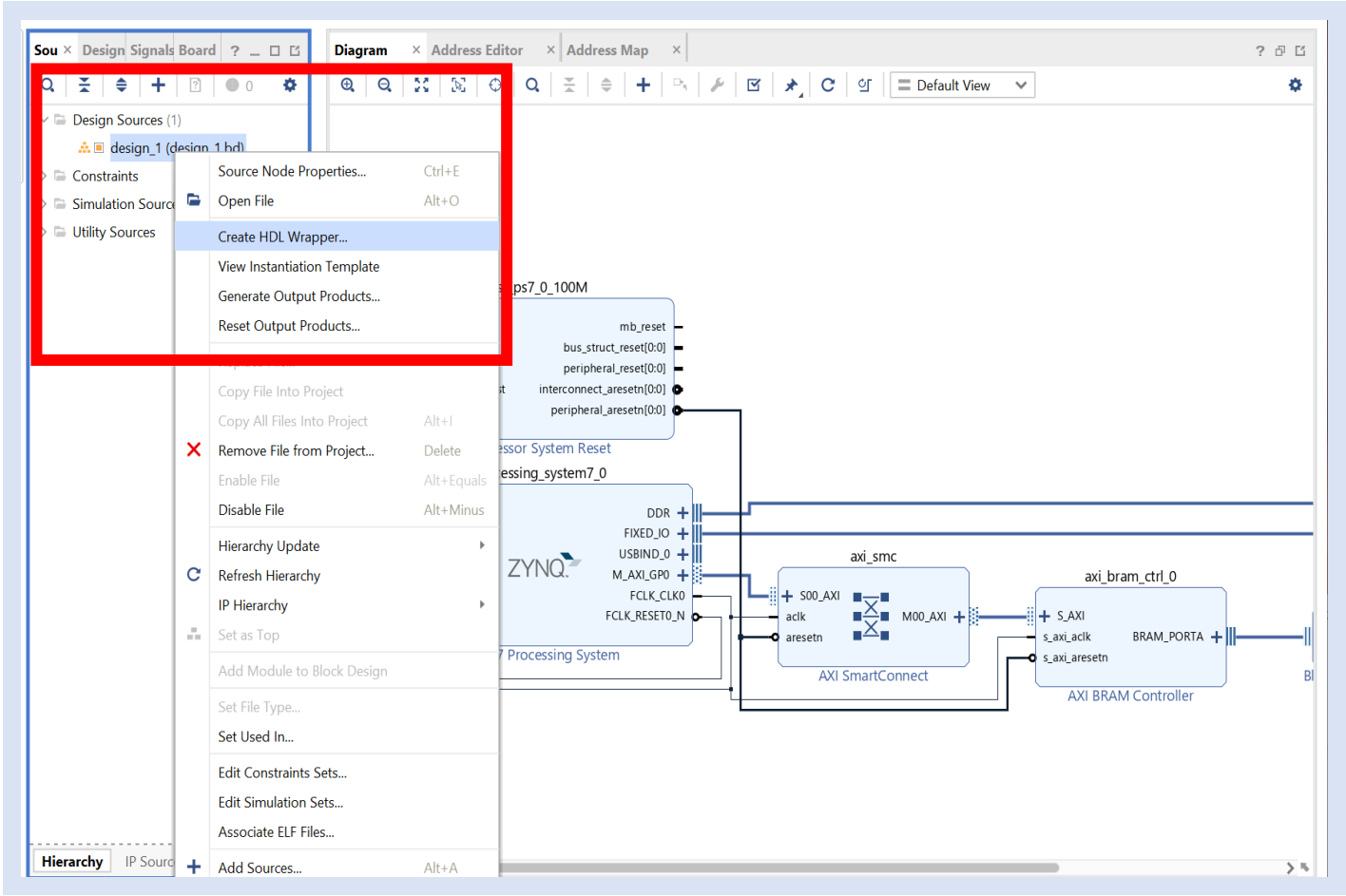
Lab 1: Understanding Vitis Project creation & Flow

Step 31 – Click On OK the warning is due to the change from AXI BRAM control



Lab 1: Understanding Vitis Project creation & Flow

Step 32 – In the sources tab, right click on the block diagram and select create HDL Wrapper



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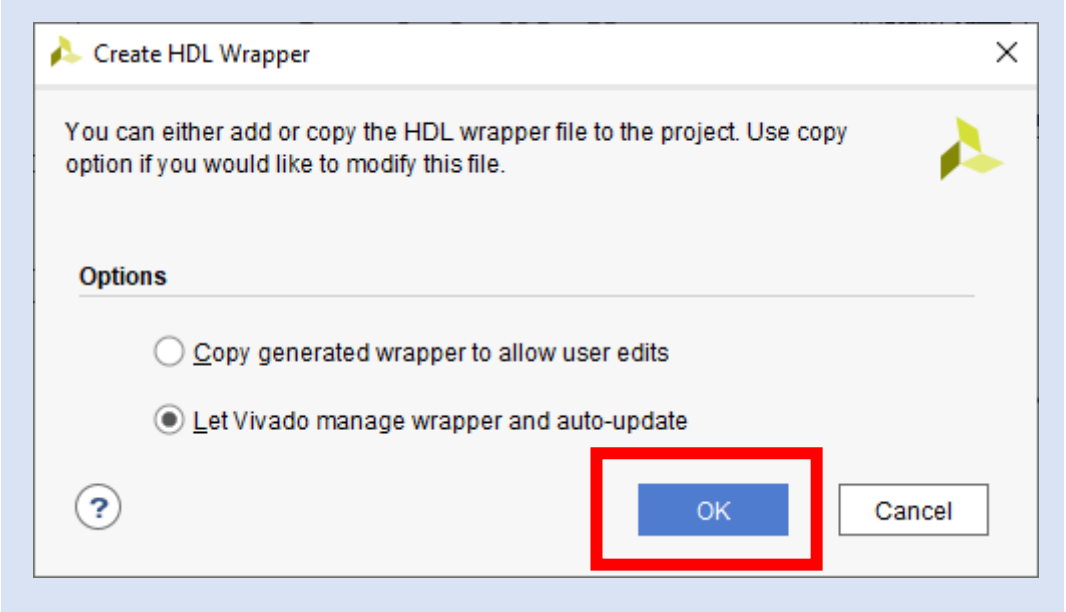
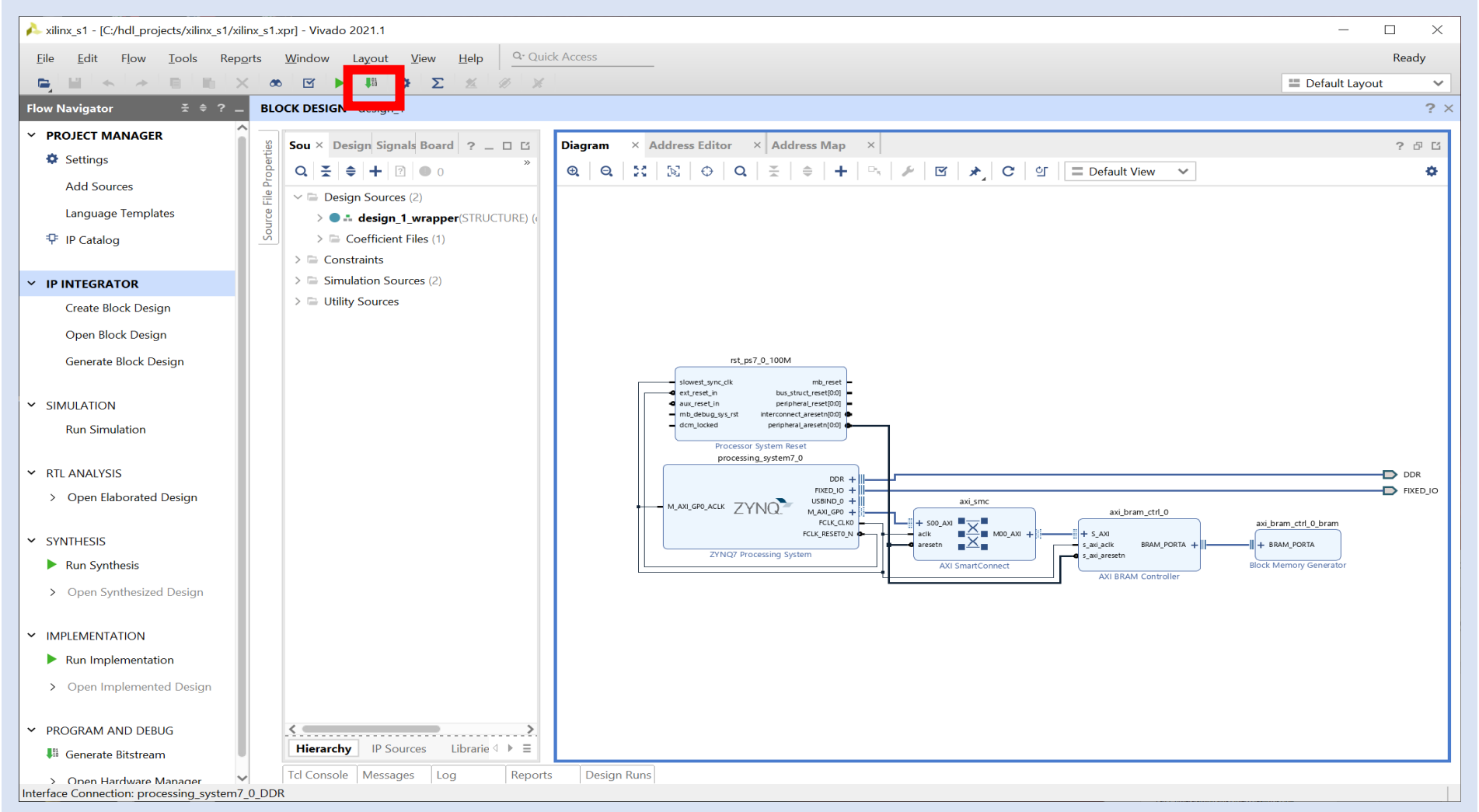
Step 33 – leave the options as set and let Vivado manage the wrapper, click OK



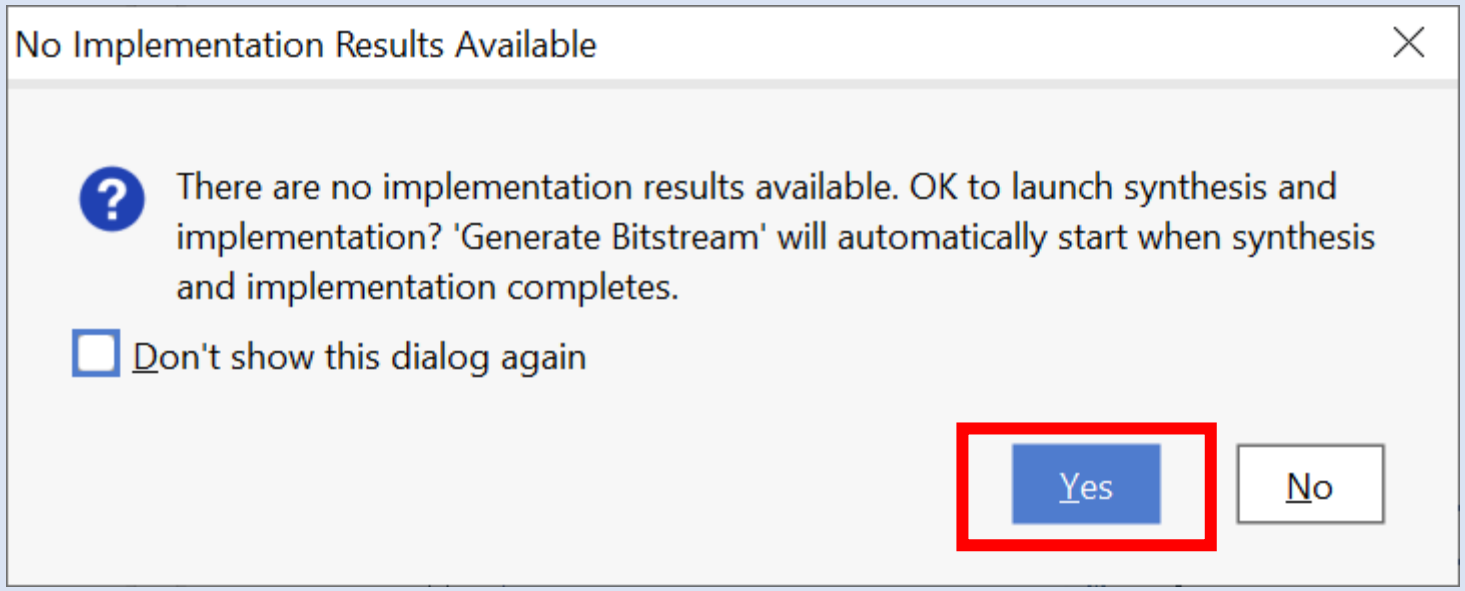
Lab 1: Understanding Vitis Project creation & Flow

Step 34 – Click on Generate Bit Stream



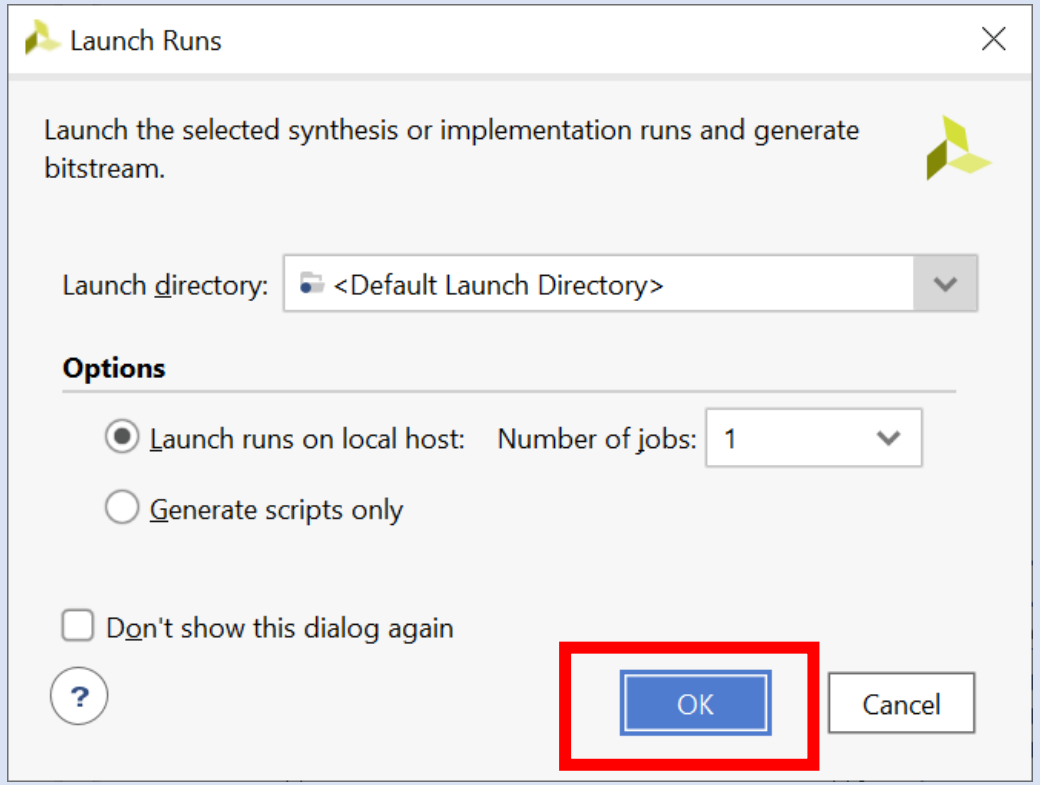
Lab 1: Understanding Vitis Project creation & Flow

Step 35 – Click yes



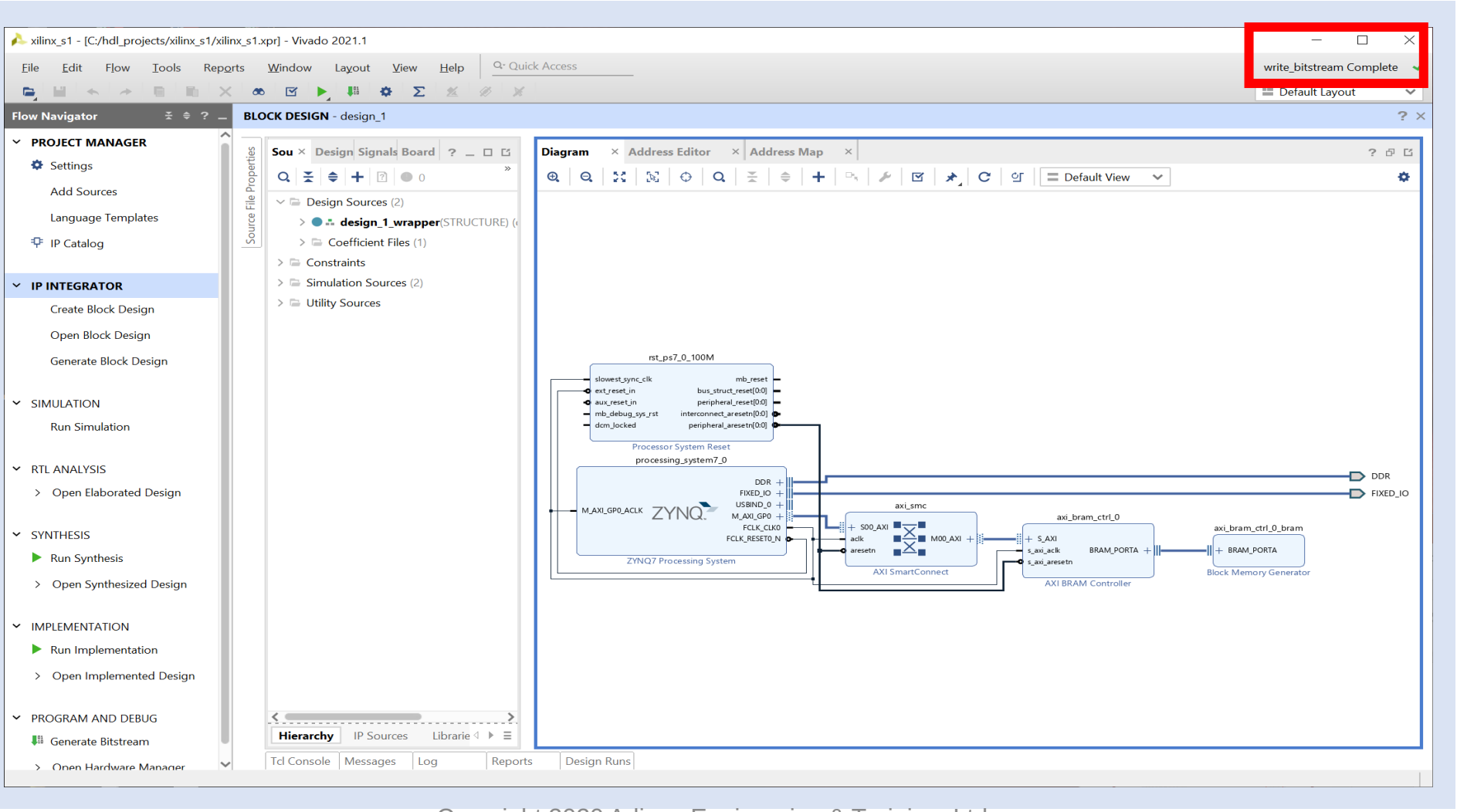
Lab 1: Understanding Vitis Project creation & Flow

Step 36 – Click Ok



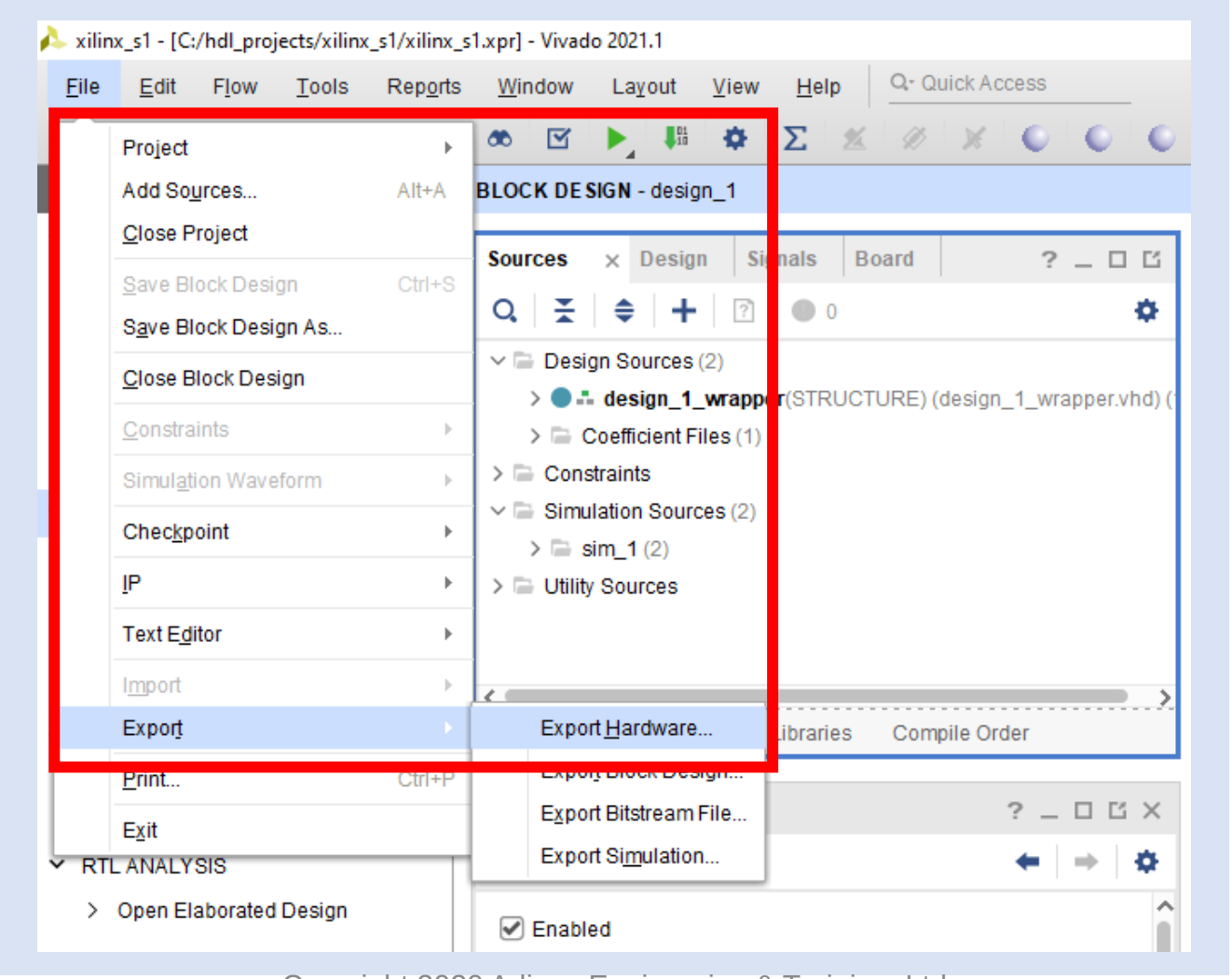
Lab 1: Understanding Vitis Project creation & Flow

Step 37 – Wait until the bit stream is complete



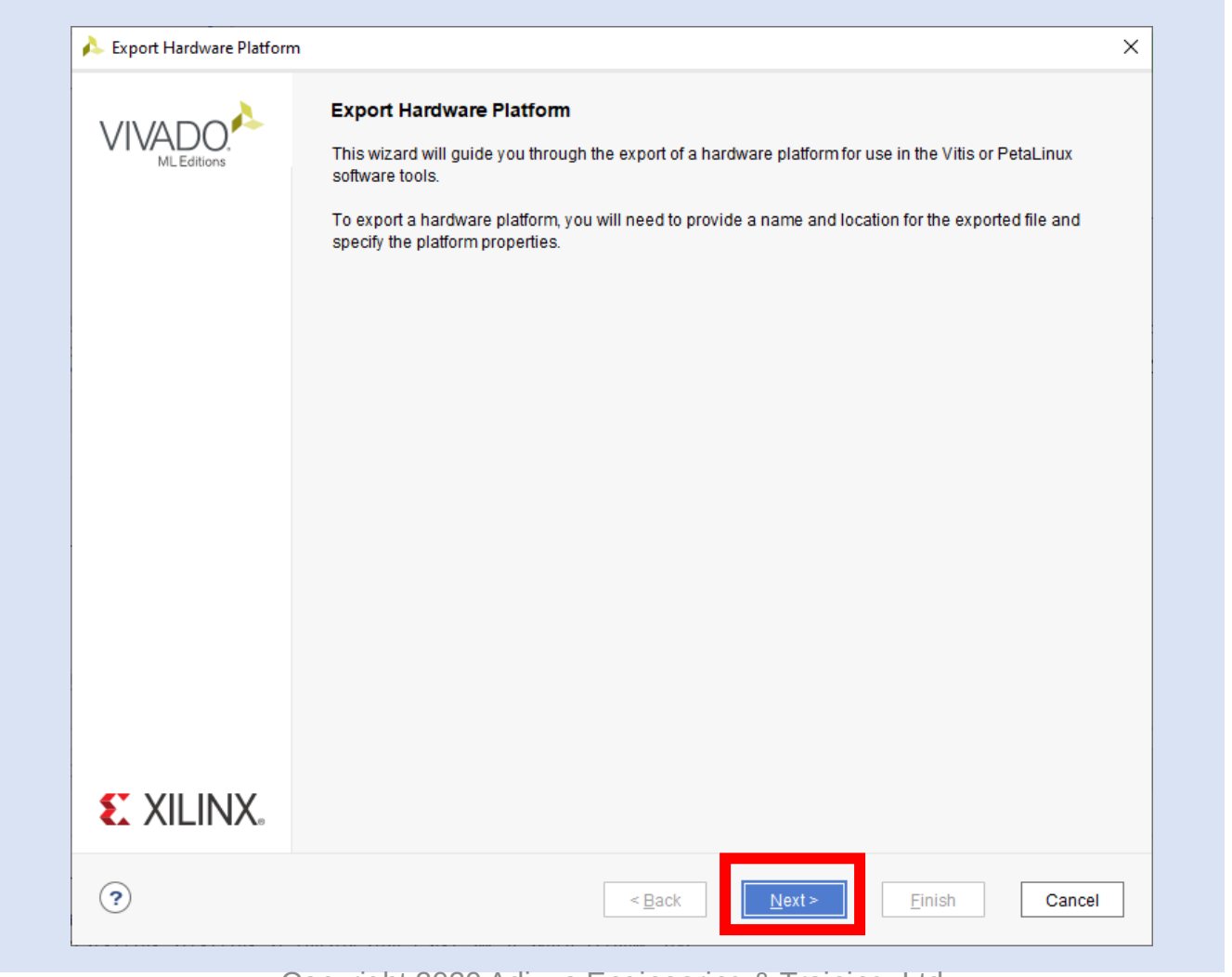
Lab 1: Understanding Vitis Project creation & Flow

Step 38 – From the File Menu select Export->Export Hardware



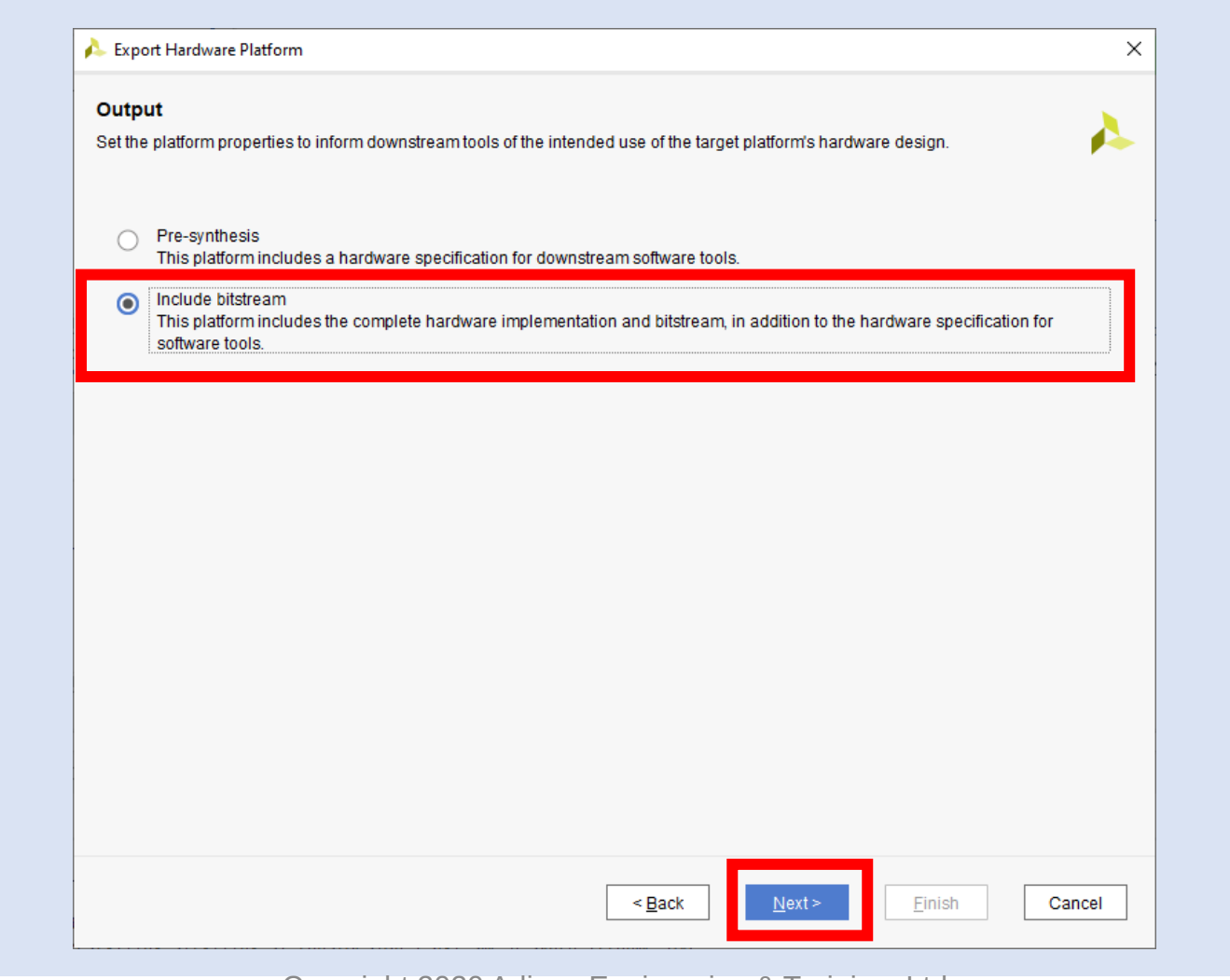
Lab 1: Understanding Vitis Project creation & Flow

Step 39 – Click on Next



Lab 1: Understanding Vitis Project creation & Flow

Step 40 – Ensure Include Bitstream is selected and click OK



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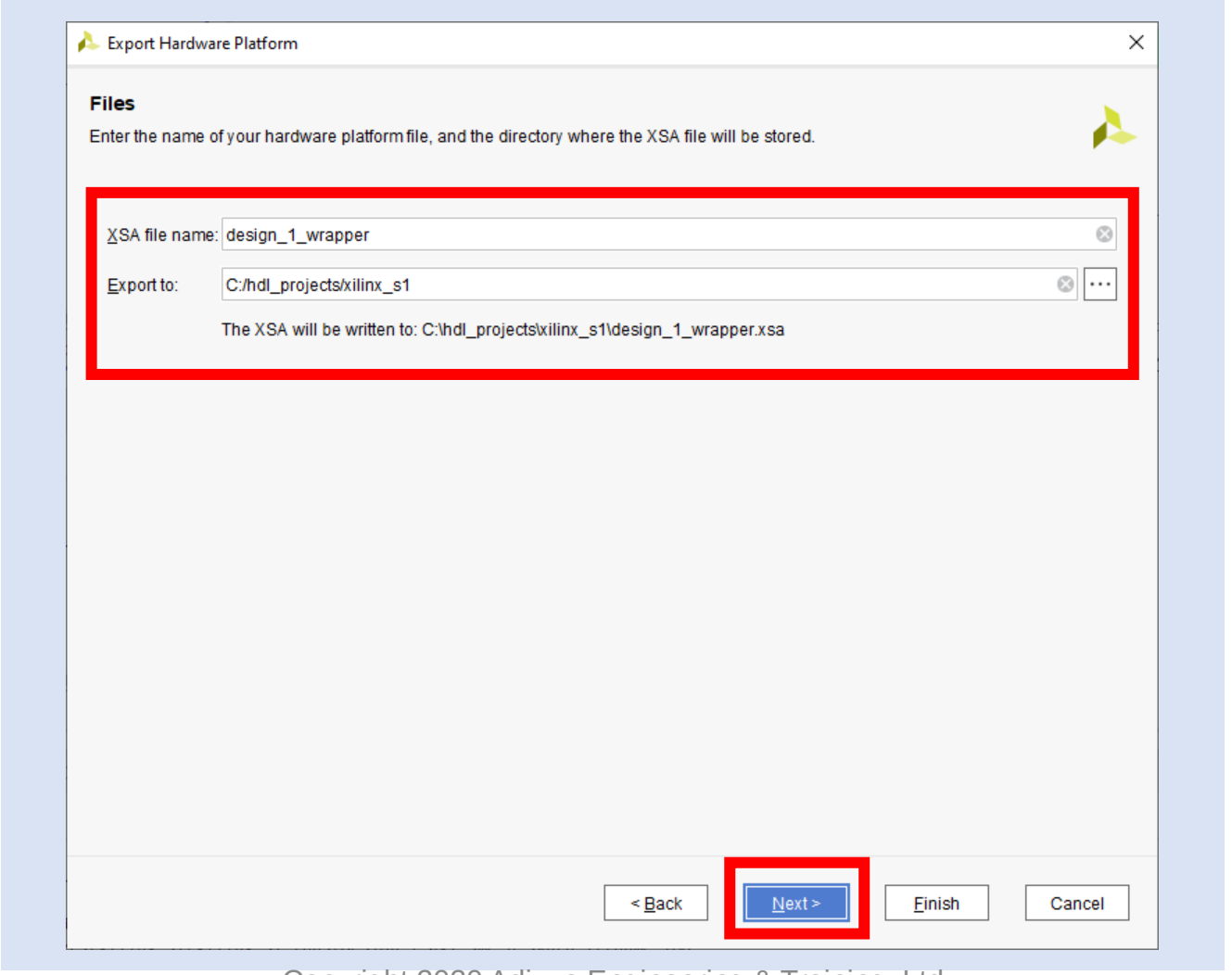
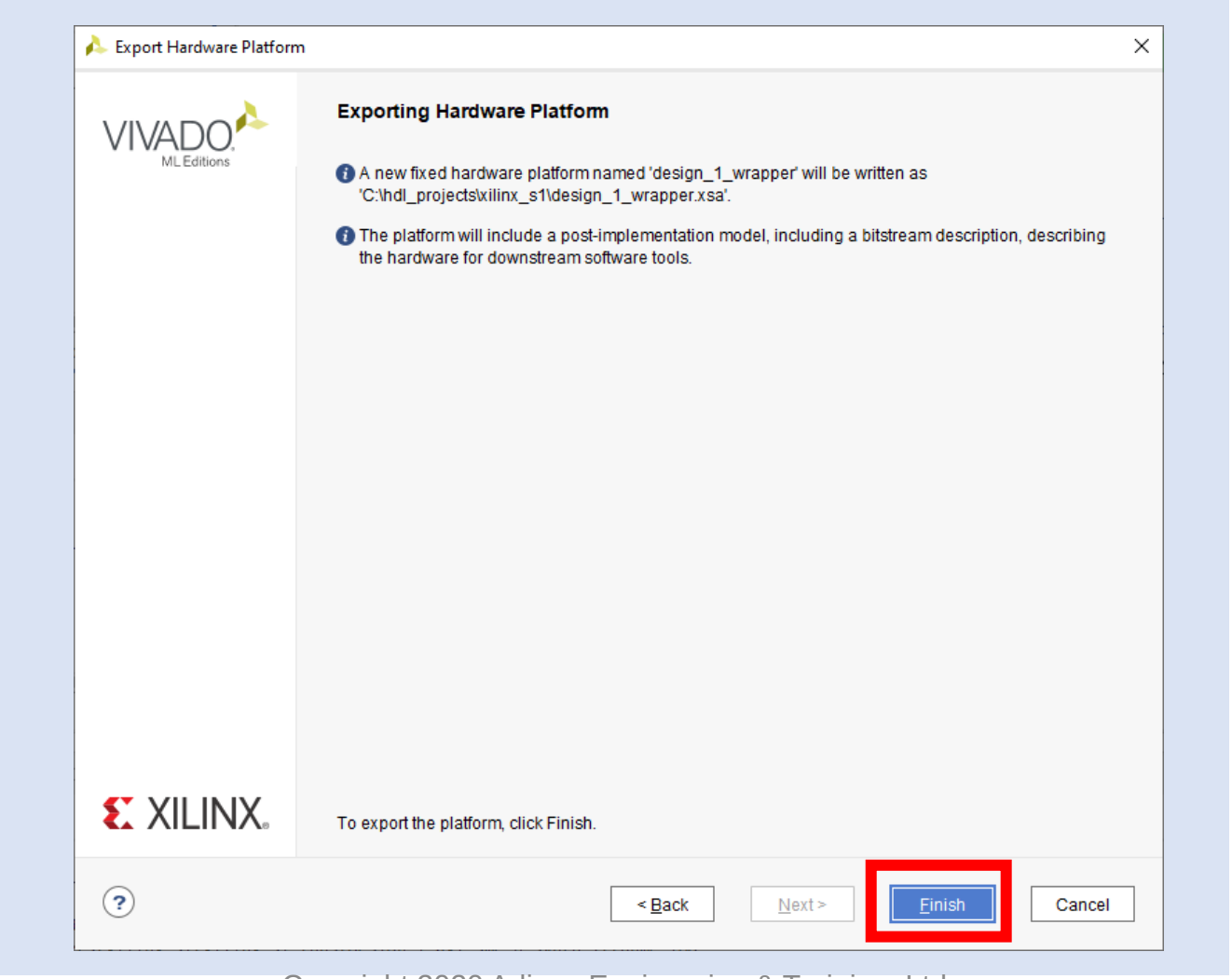
Step 41 – Leave the defaults as is and click on Next



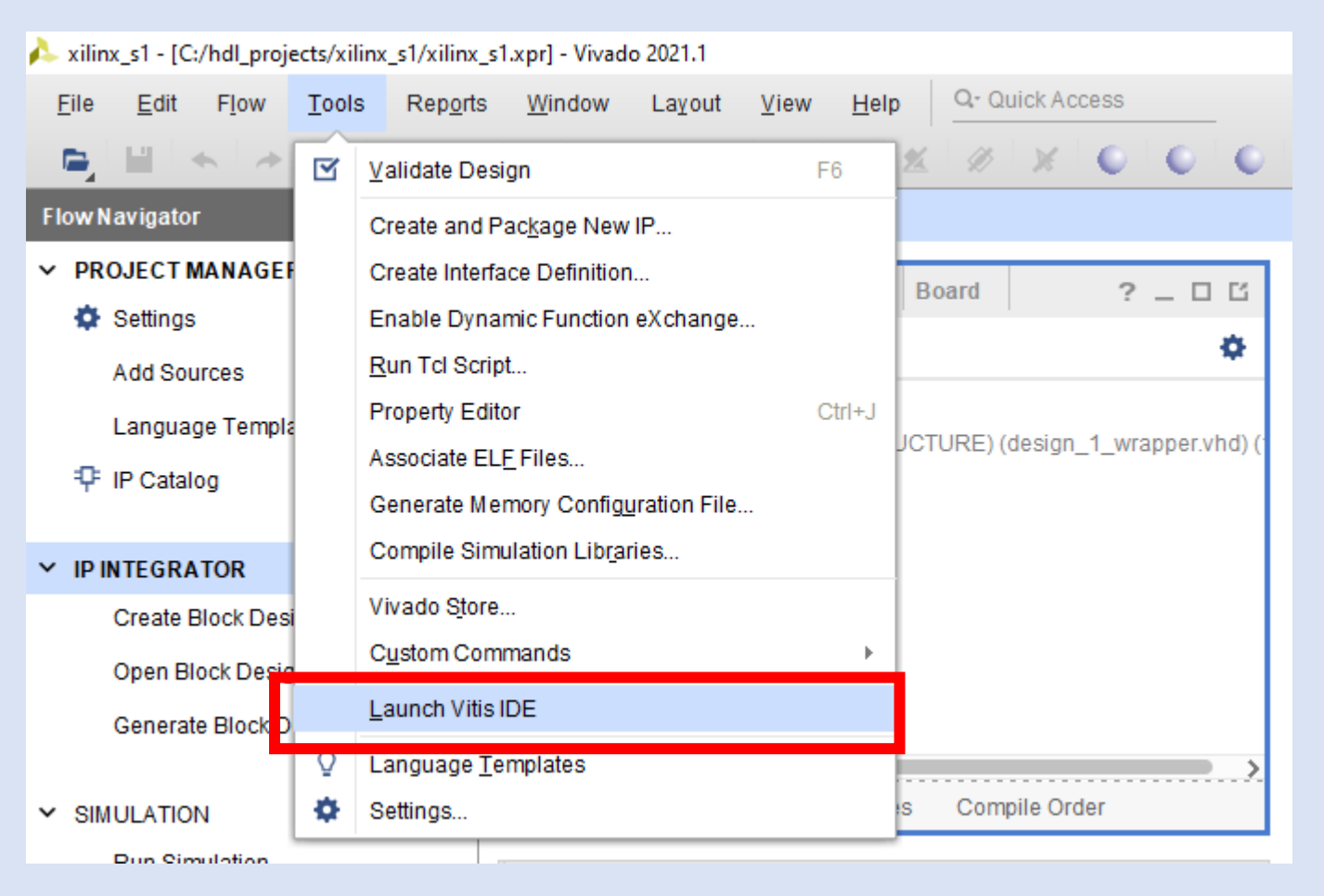
Lab 1: Understanding Vitis Project creation & Flow

Step 42 – Click Finish



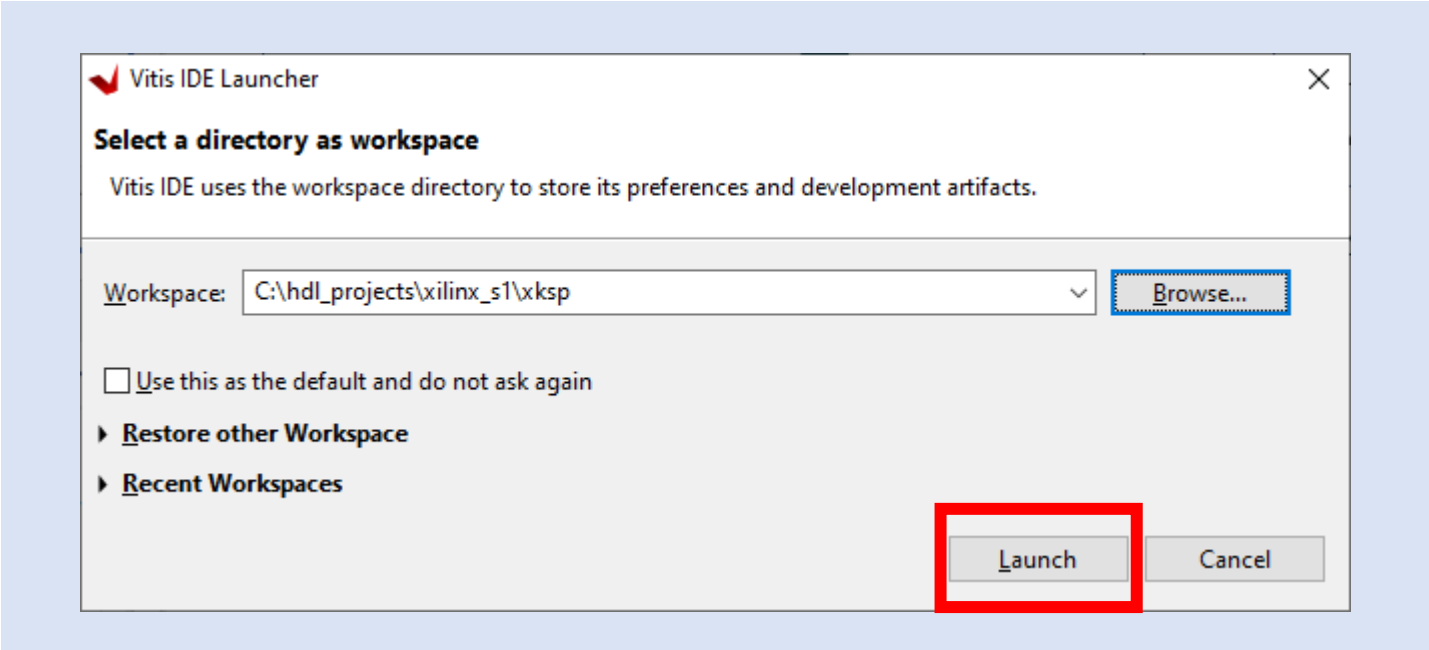
Lab 1: Understanding Vitis Project creation & Flow

Step 43 – From the Tools menu select Launch Vitis IDE



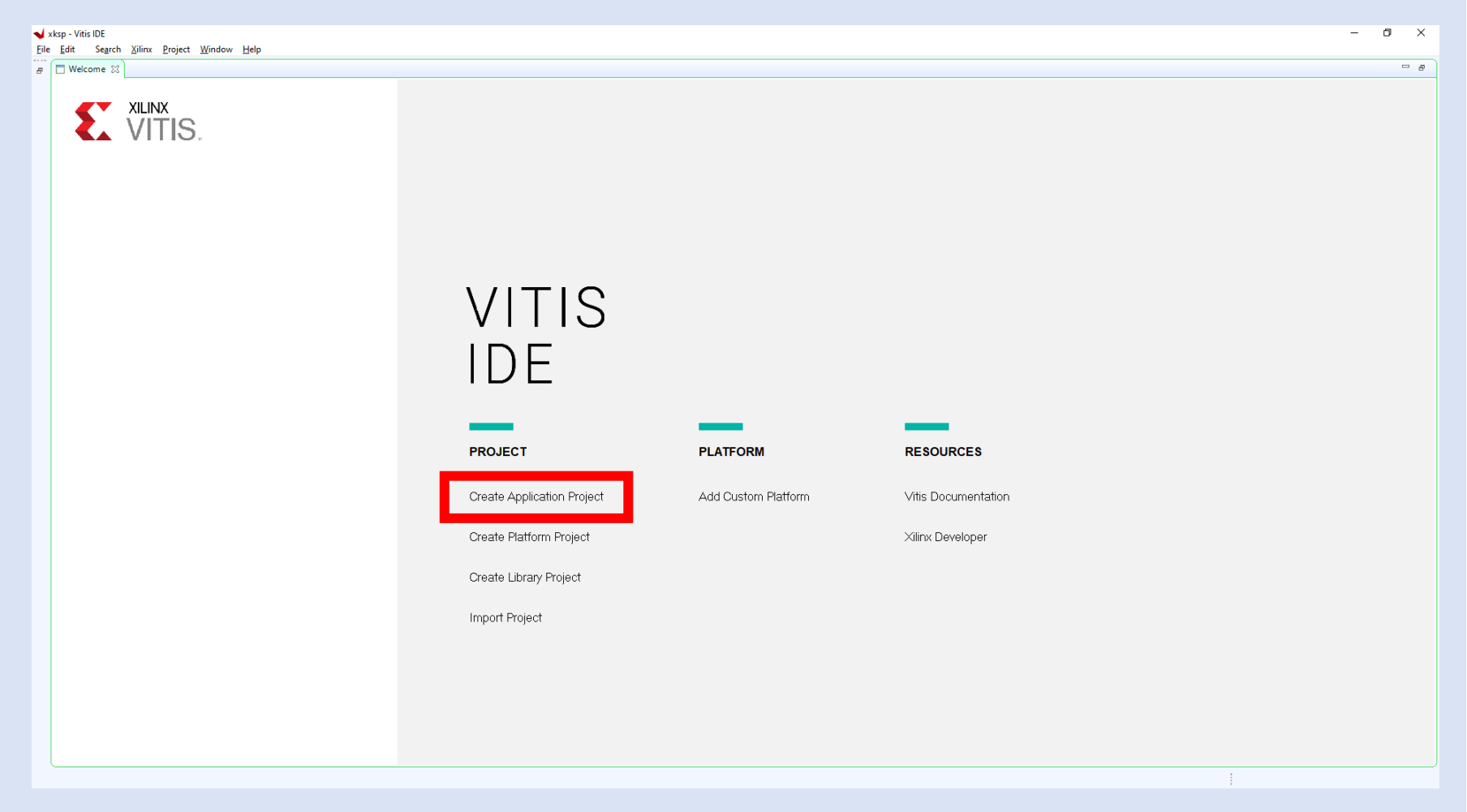
Lab 1: Understanding Vitis Project creation & Flow

Step 44 – At the dialog, create a new folder in your project directory and select launch



Lab 1: Understanding Vitis Project creation & Flow

Step 45 – Click on Create Application Project



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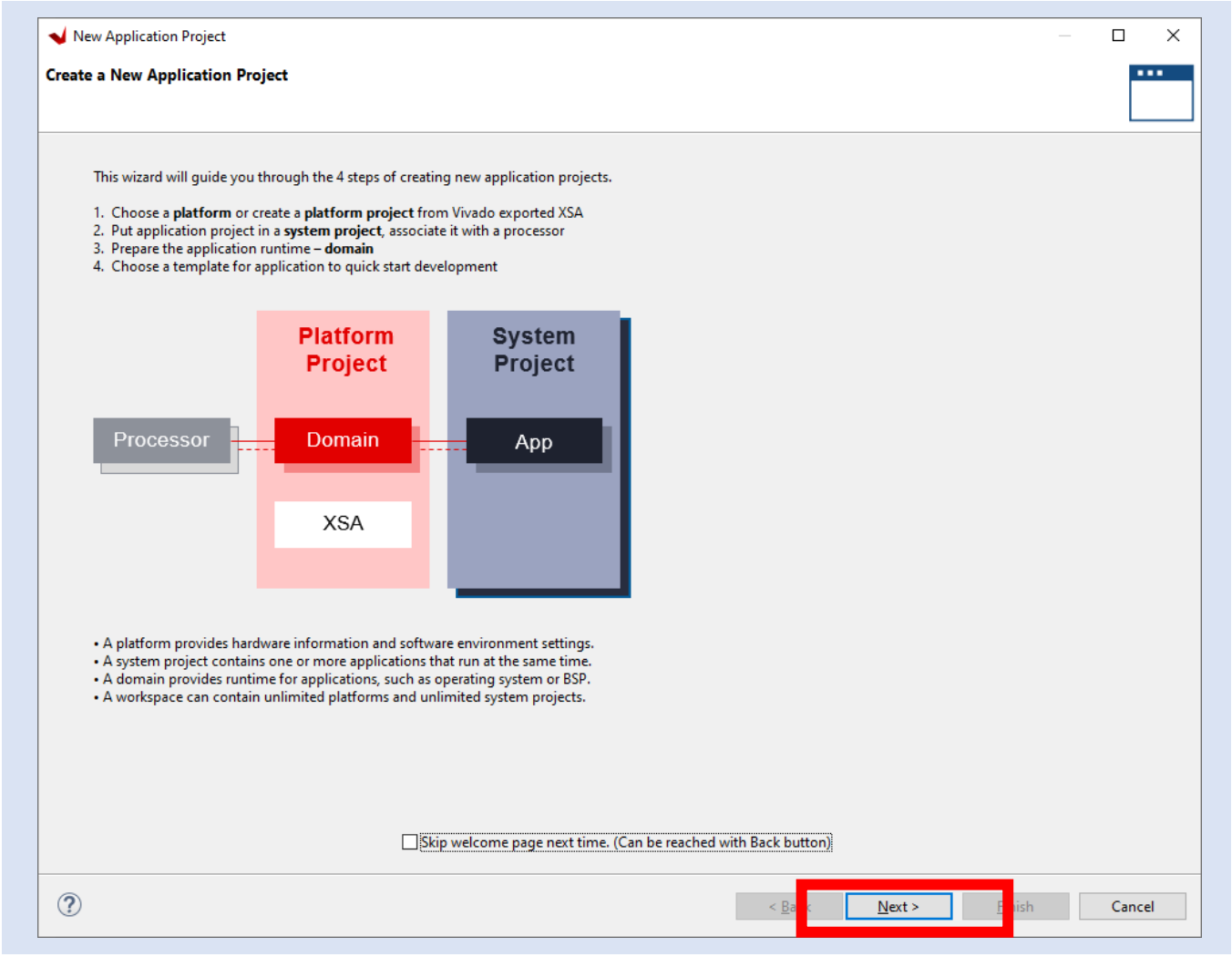
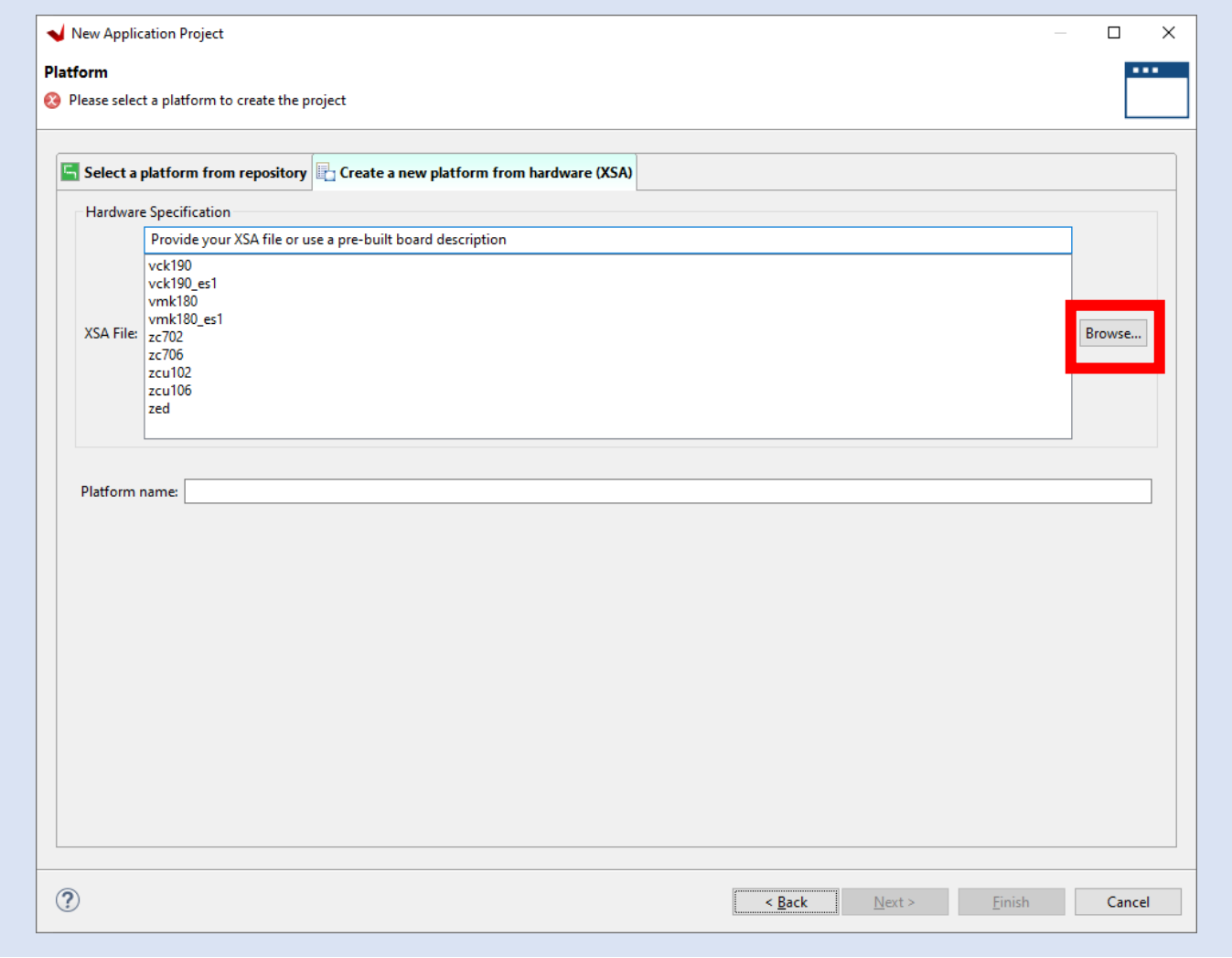
Step 46 – Click on next



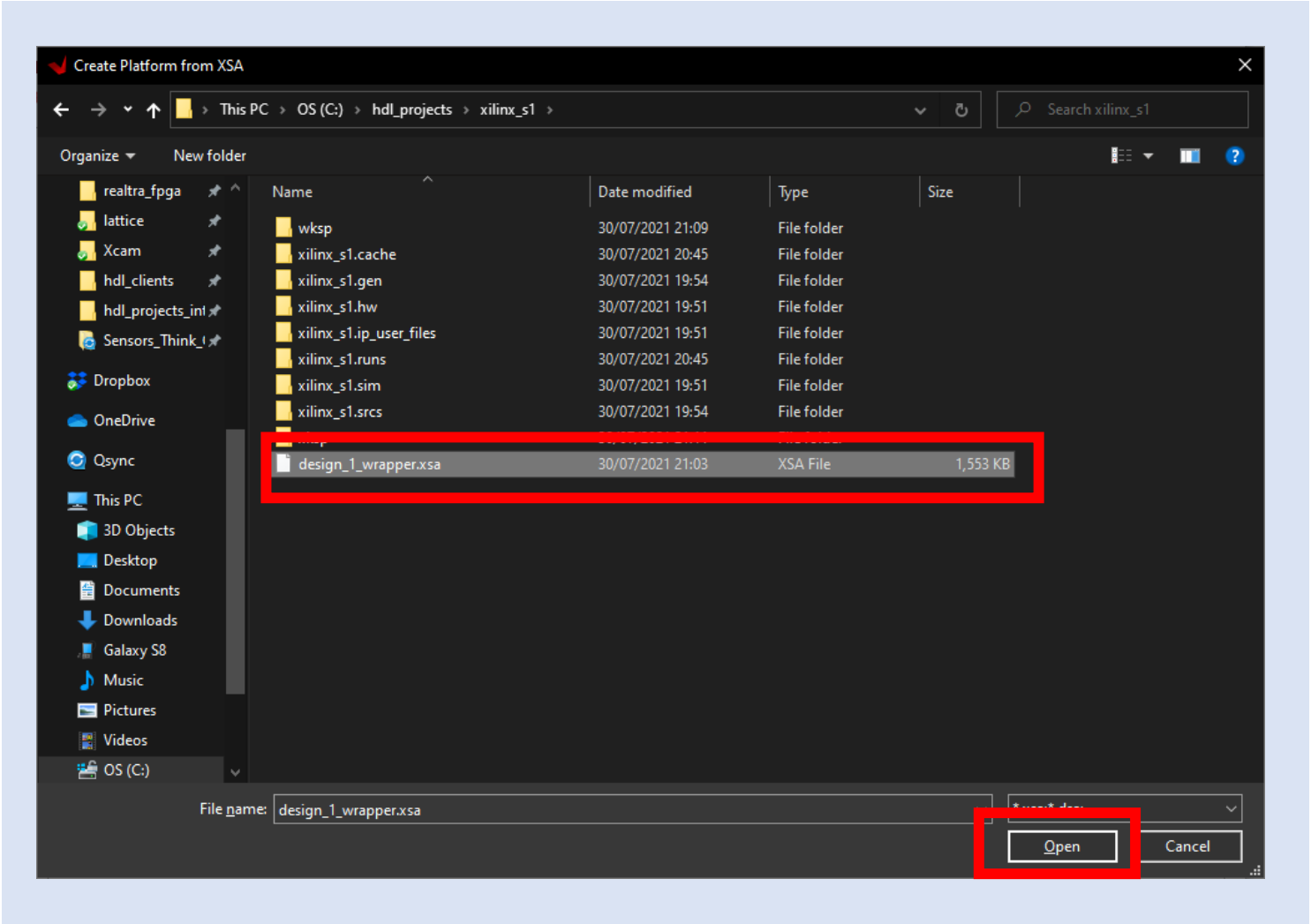
Lab 1: Understanding Vitis Project creation & Flow

Step 47 – Click on Create a New Platform from Hardware (XSA) and select browse



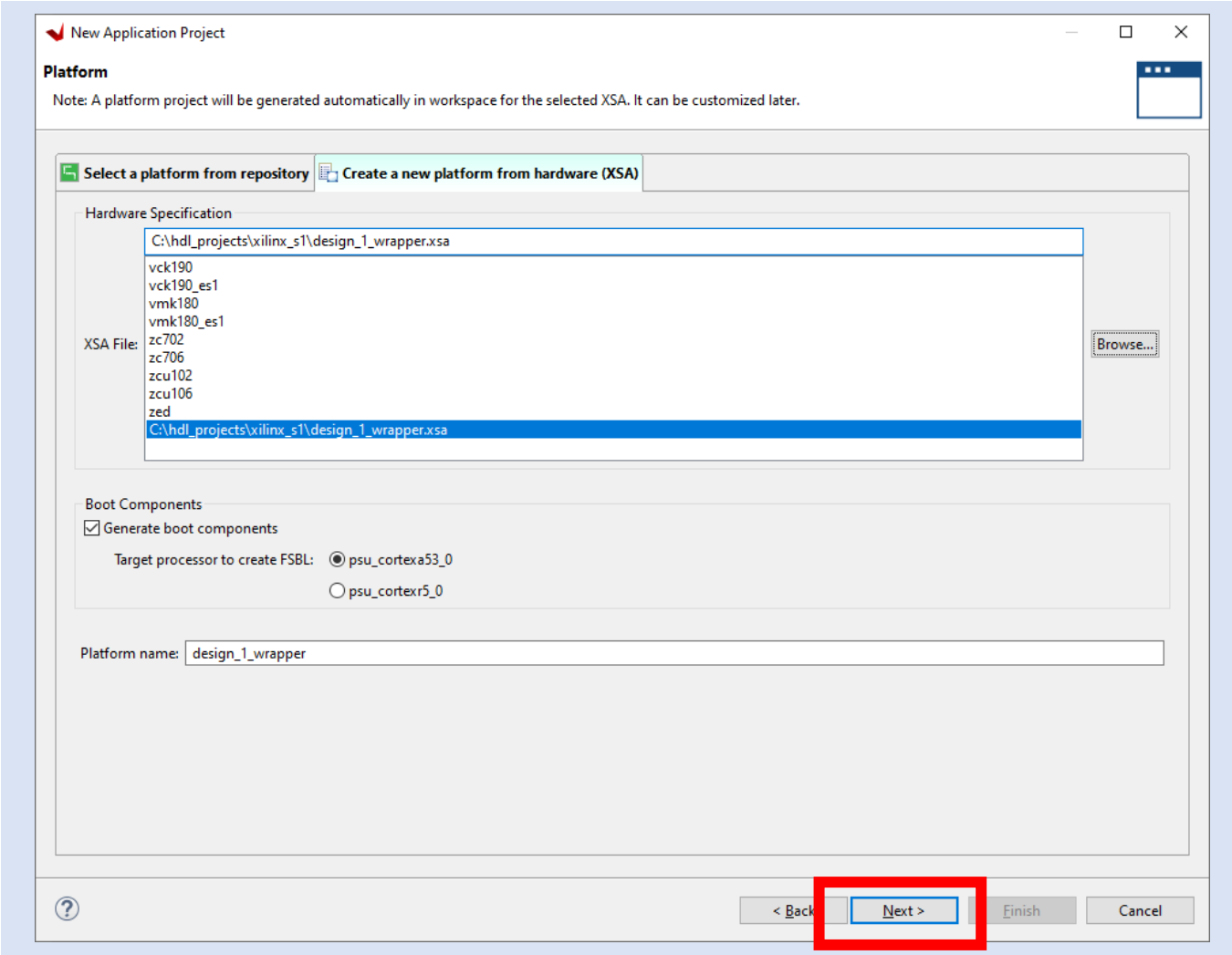
Lab 1: Understanding Vitis Project creation & Flow

Step 48 – Browse to the project directory, select the exported XSA and Click Open



Lab 1: Understanding Vitis Project creation & Flow

Step 49 – Click on OK



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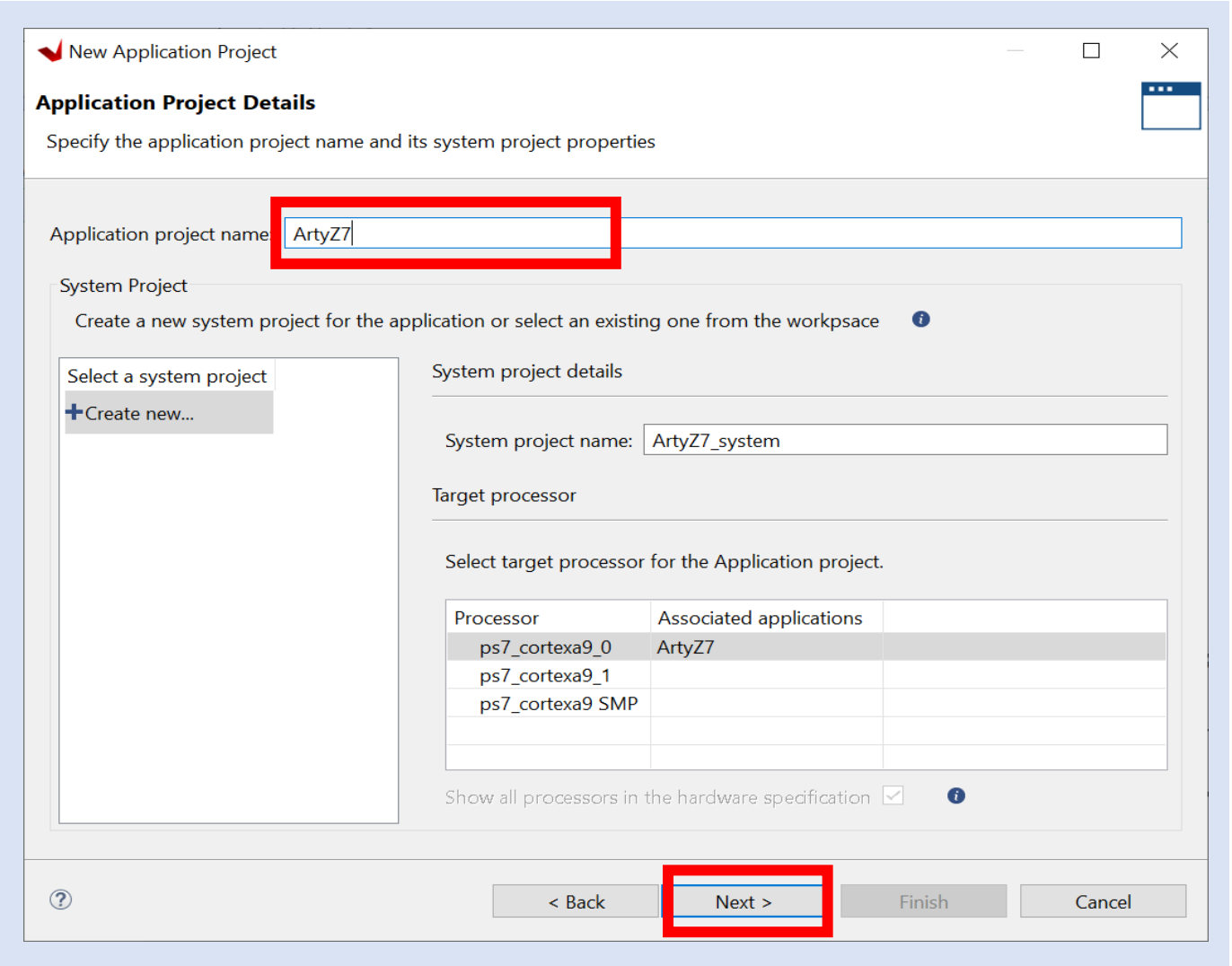
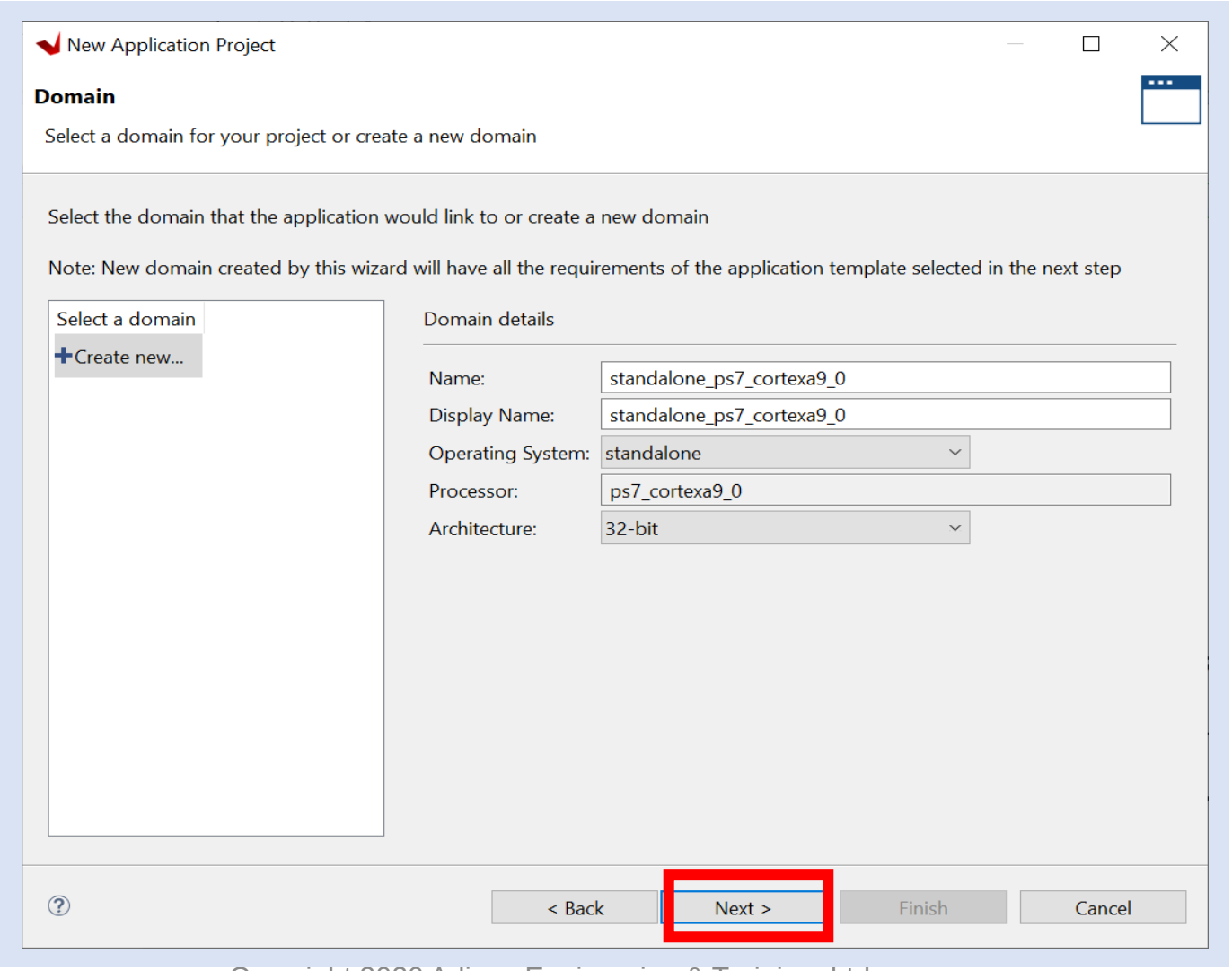
Step 50 – Enter a project name and select Next



Lab 1: Understanding Vitis Project creation & Flow

Step 51 – Click Next



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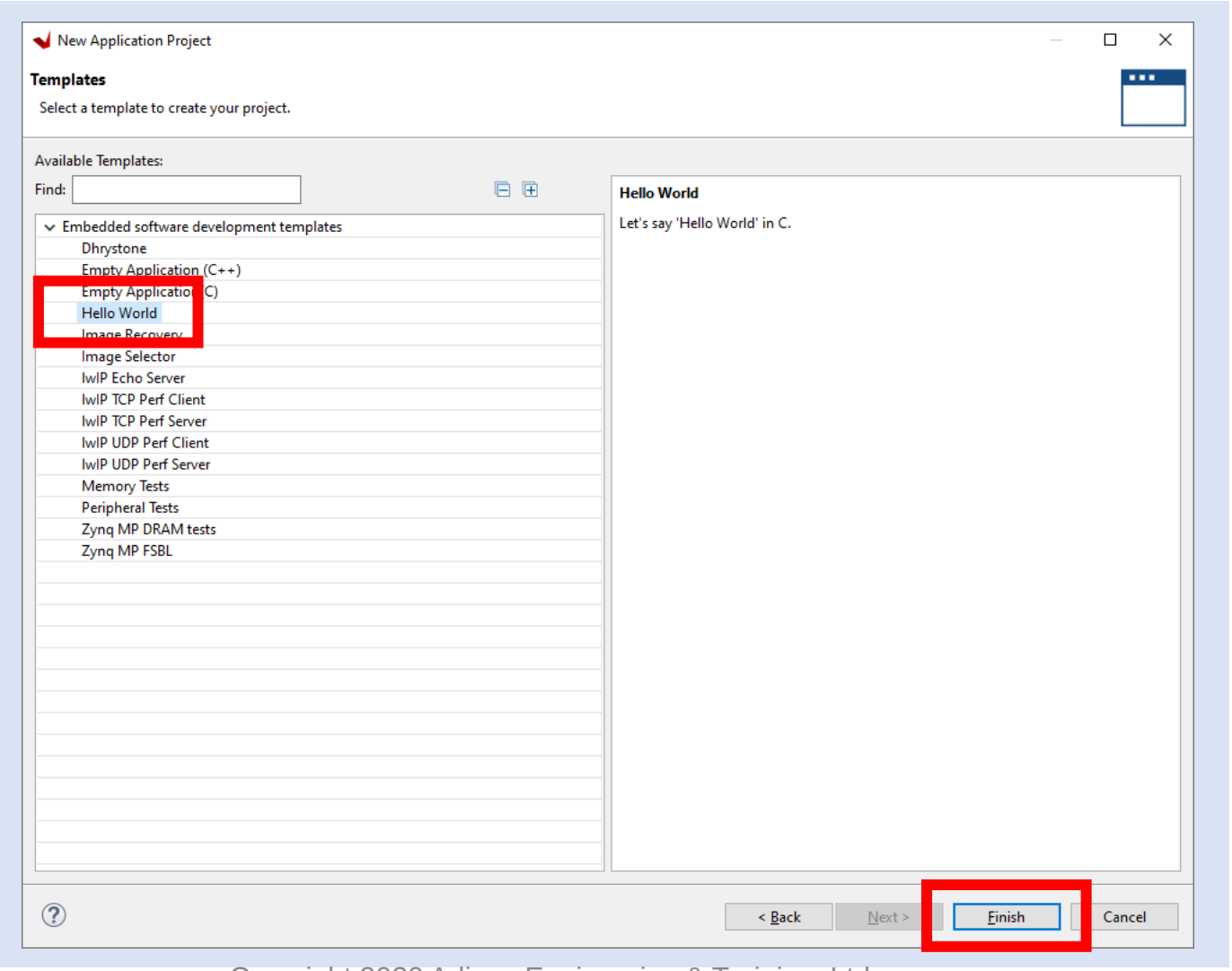
Step 52 - Select Hello World and click finish



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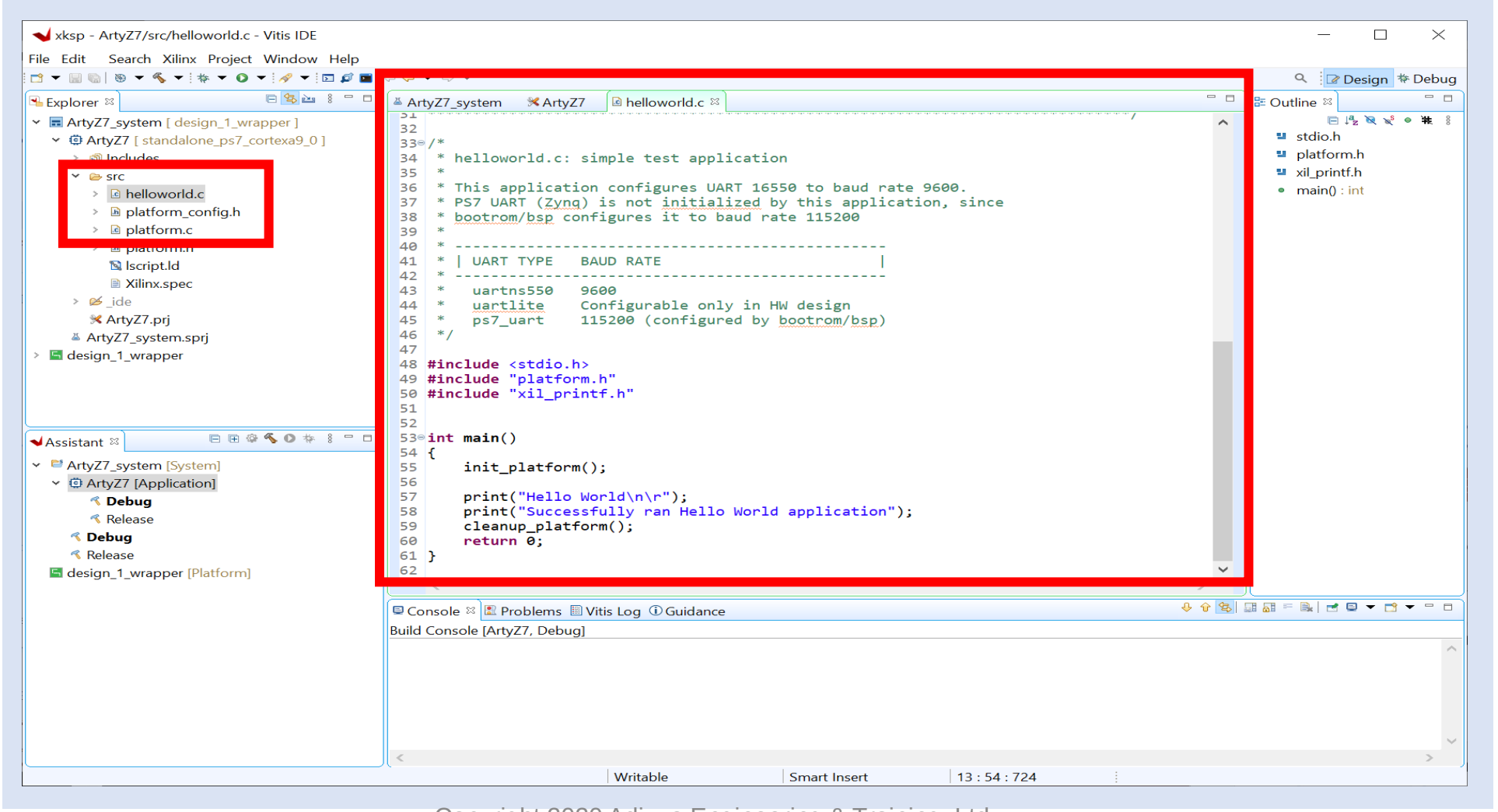
Step 53 - From the application / src folder double click and open the helloworld.c



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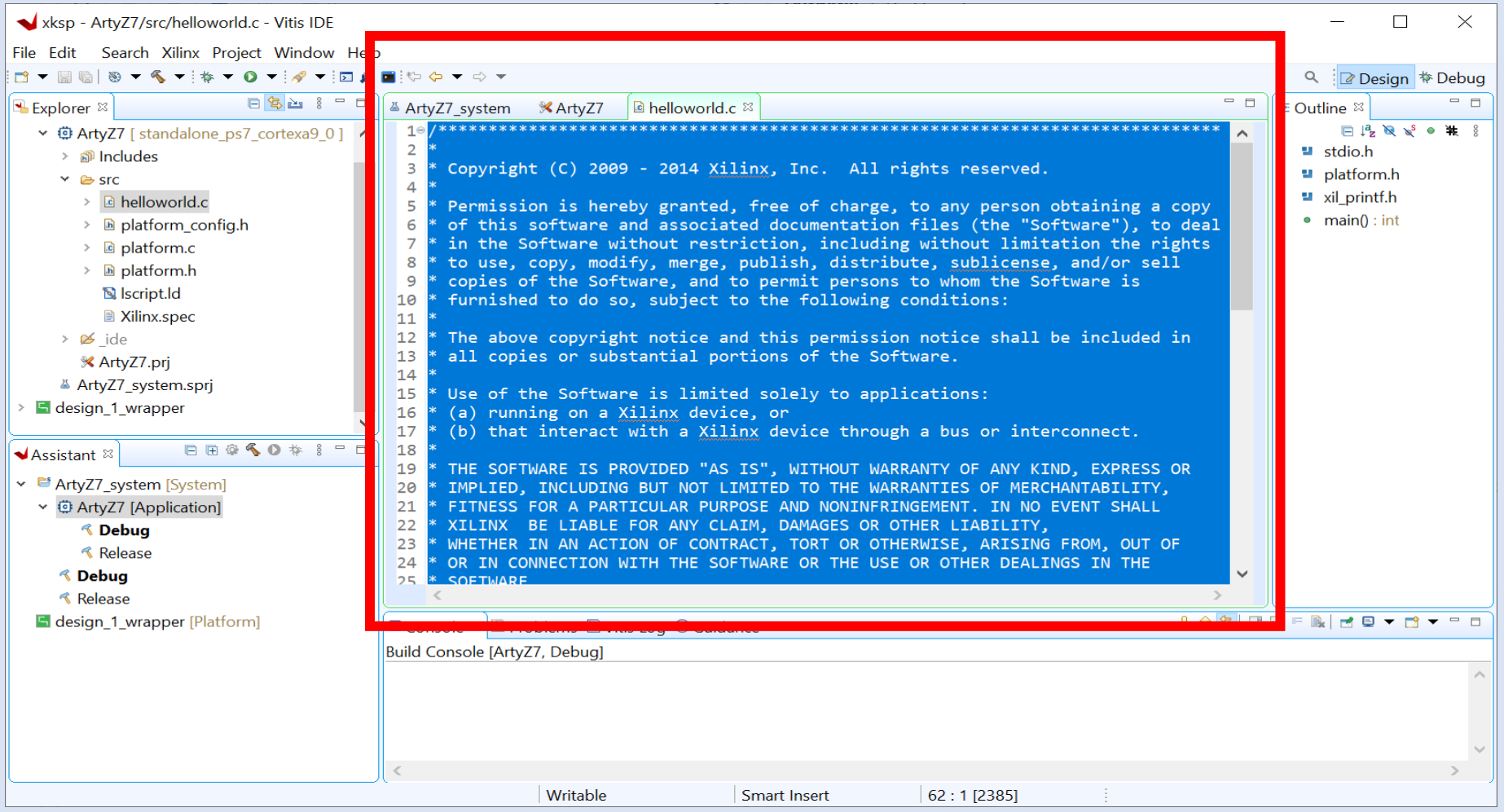
Step 54 - Click CNTRL-A to select all the code in the file and delete it



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Step 55 - Copy and paste in the code from the Github repo session one lab

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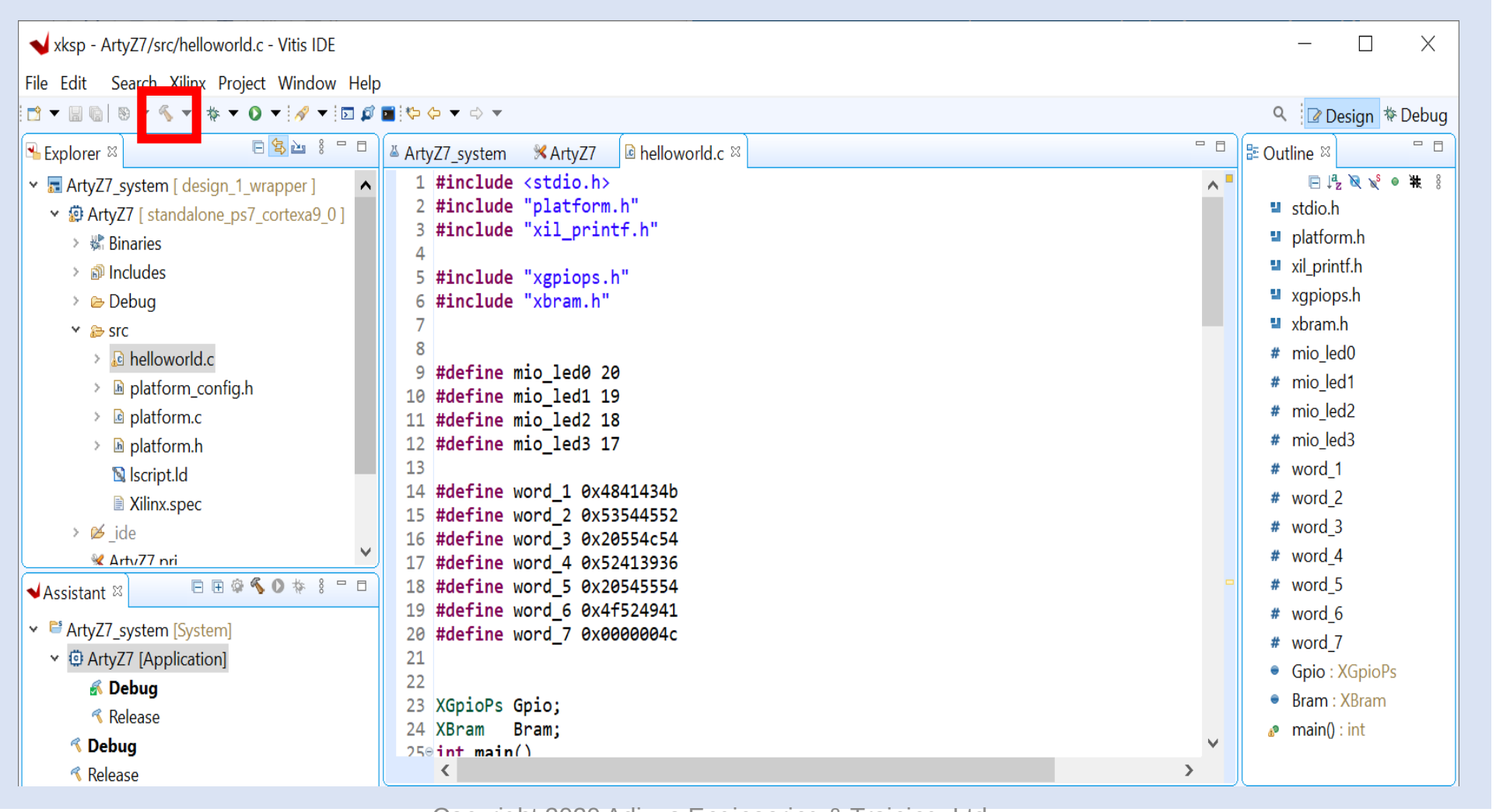
Step 56 - Click on the Hammer to Build the project



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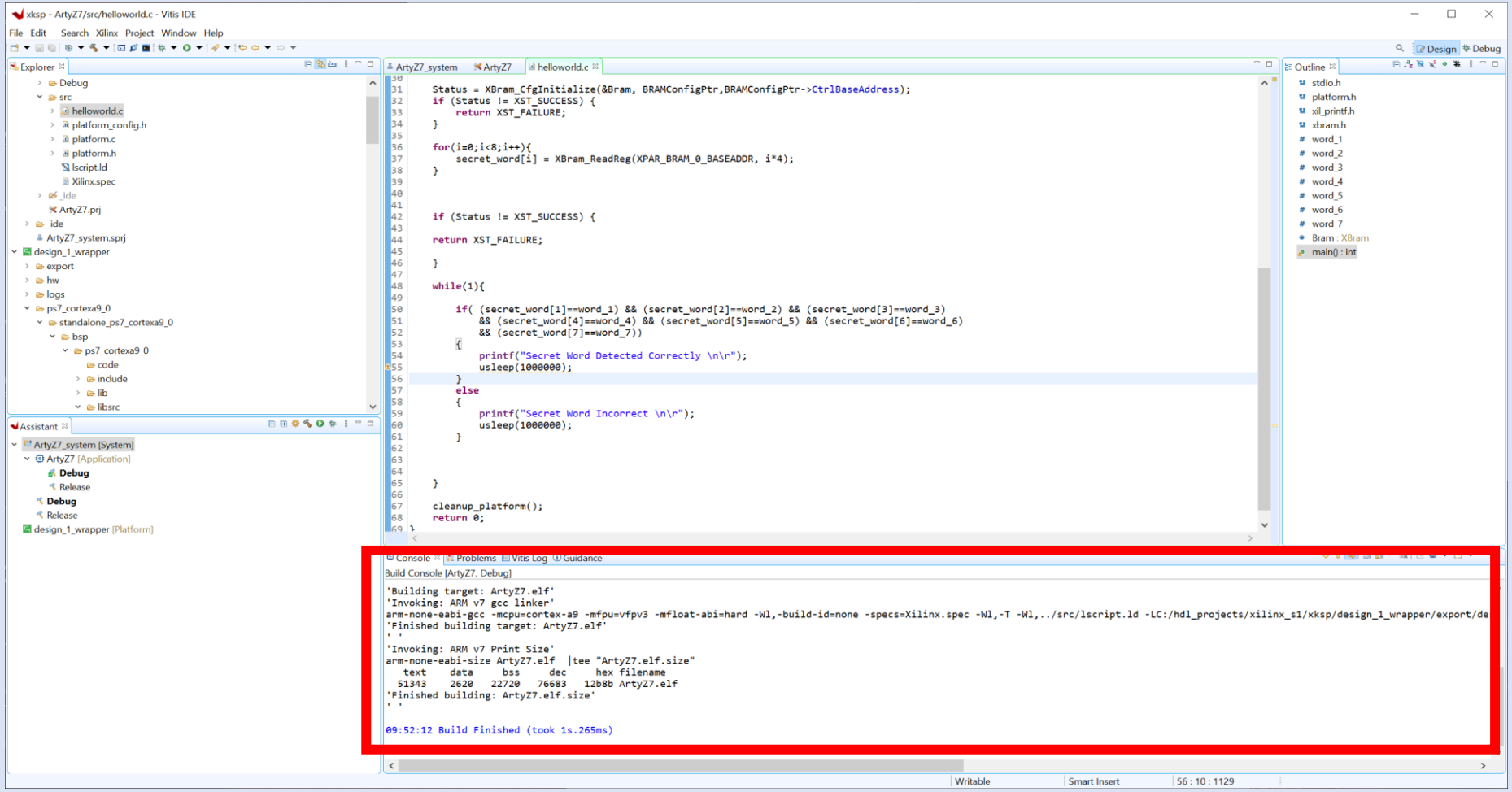
Step 57 - It will take a few minutes to compile. Successful completion will show as below



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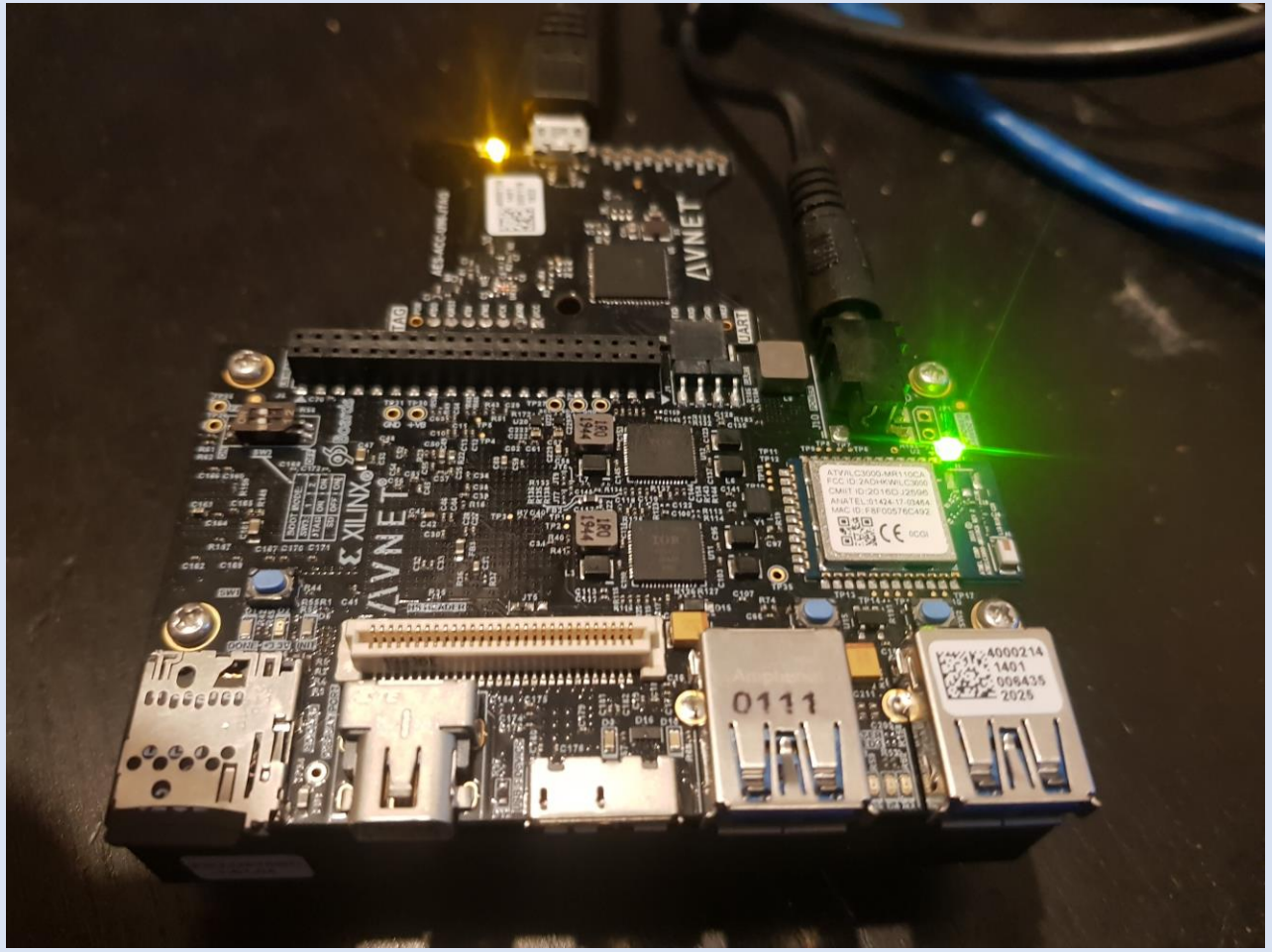
Step 58 - Connect the USB to the ArtyZ7, Check the book Mode is JTAG. Power on the board.



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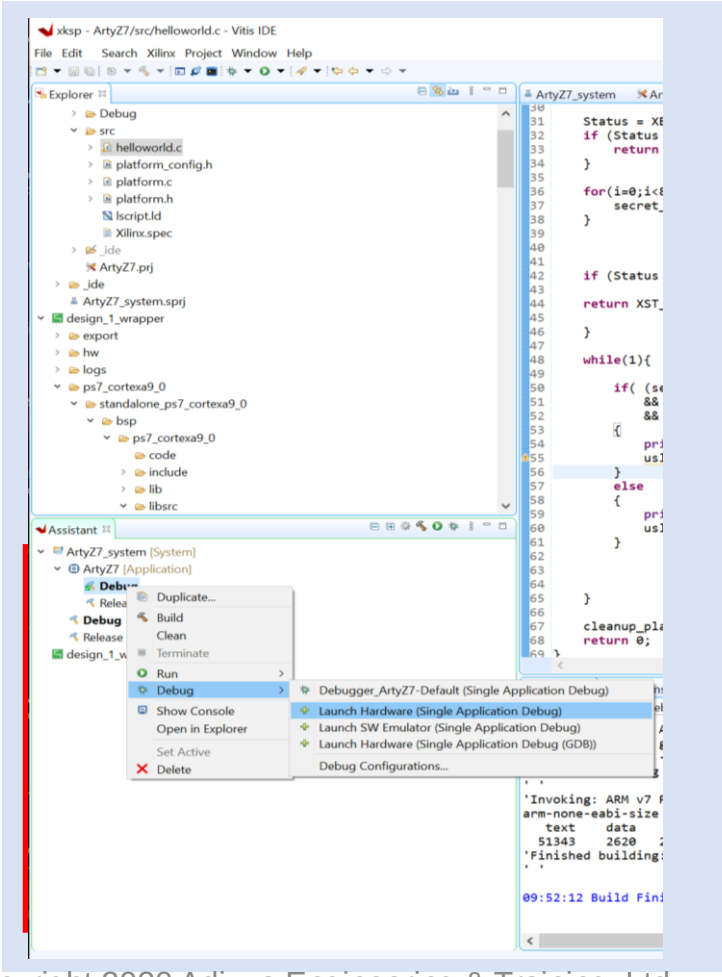
Step 59 - From the assistant view, right click on debug and select debug-> launch on Hardware. This will configure the ArtyZ7, download the PL and the application.



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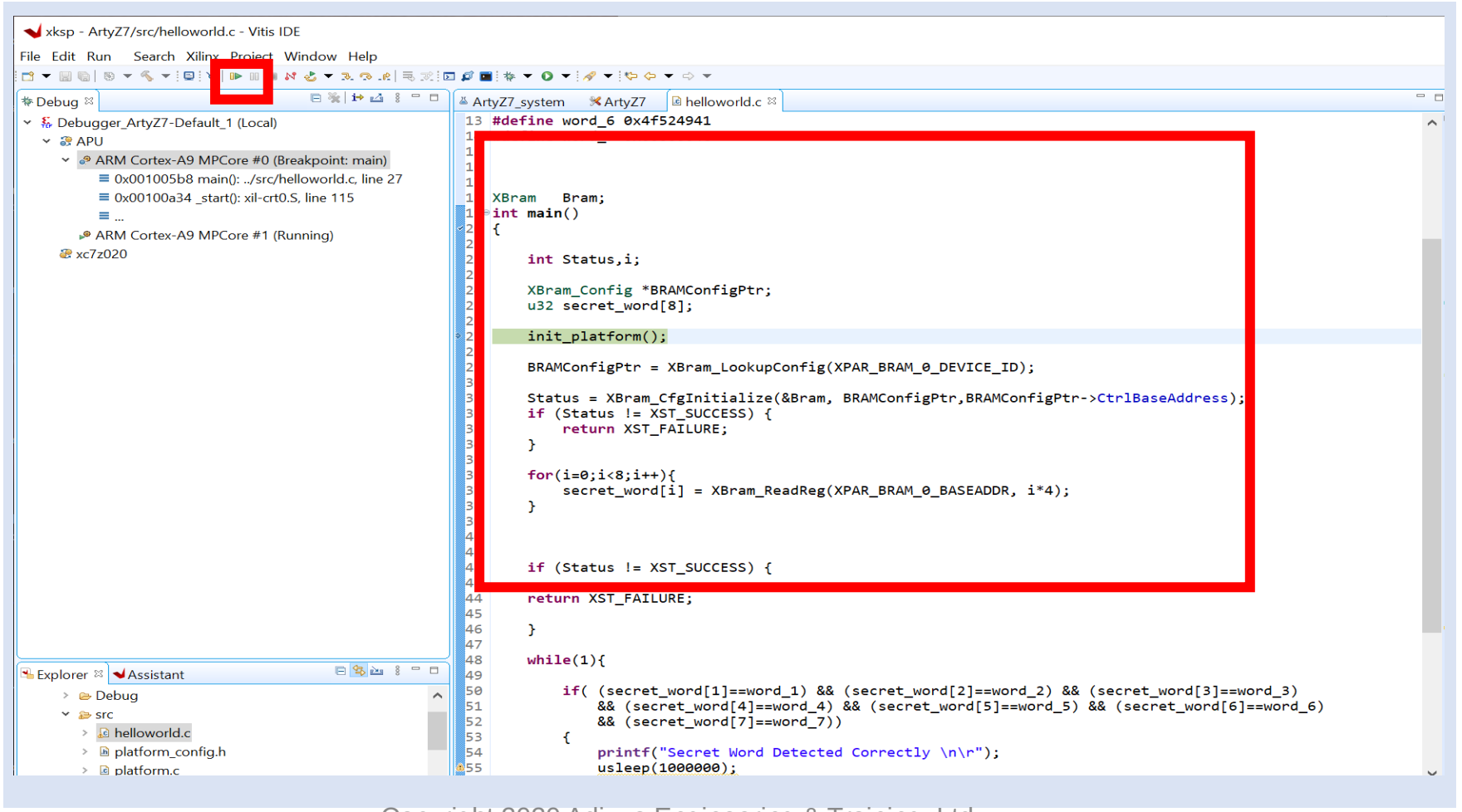
Step 60 - The application will pause at the first instruction on the ArtyZ7. Click the Run Arrow



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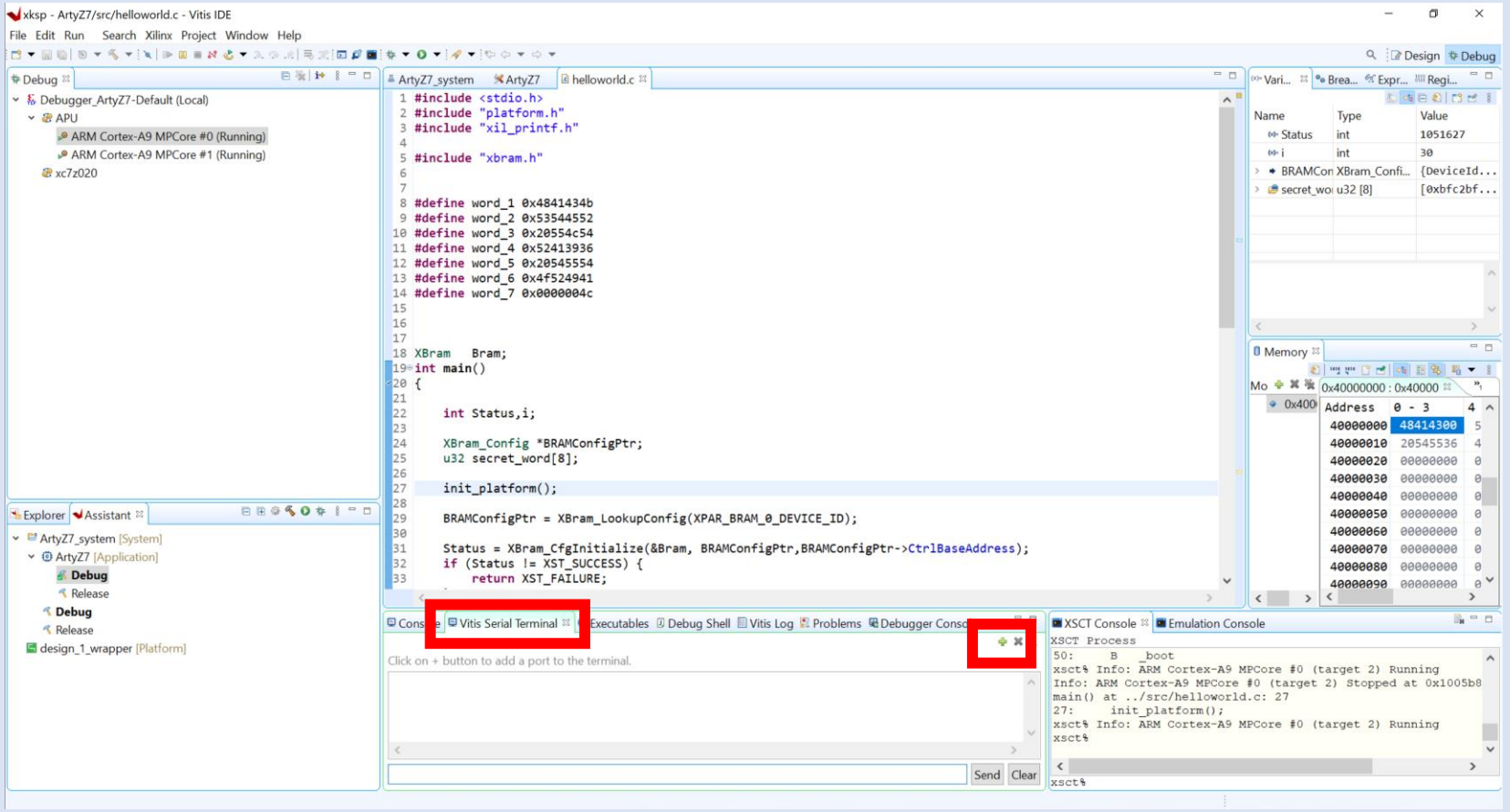
Step 61 – Project will run, Click on Vitis Serial Terminal and Click +



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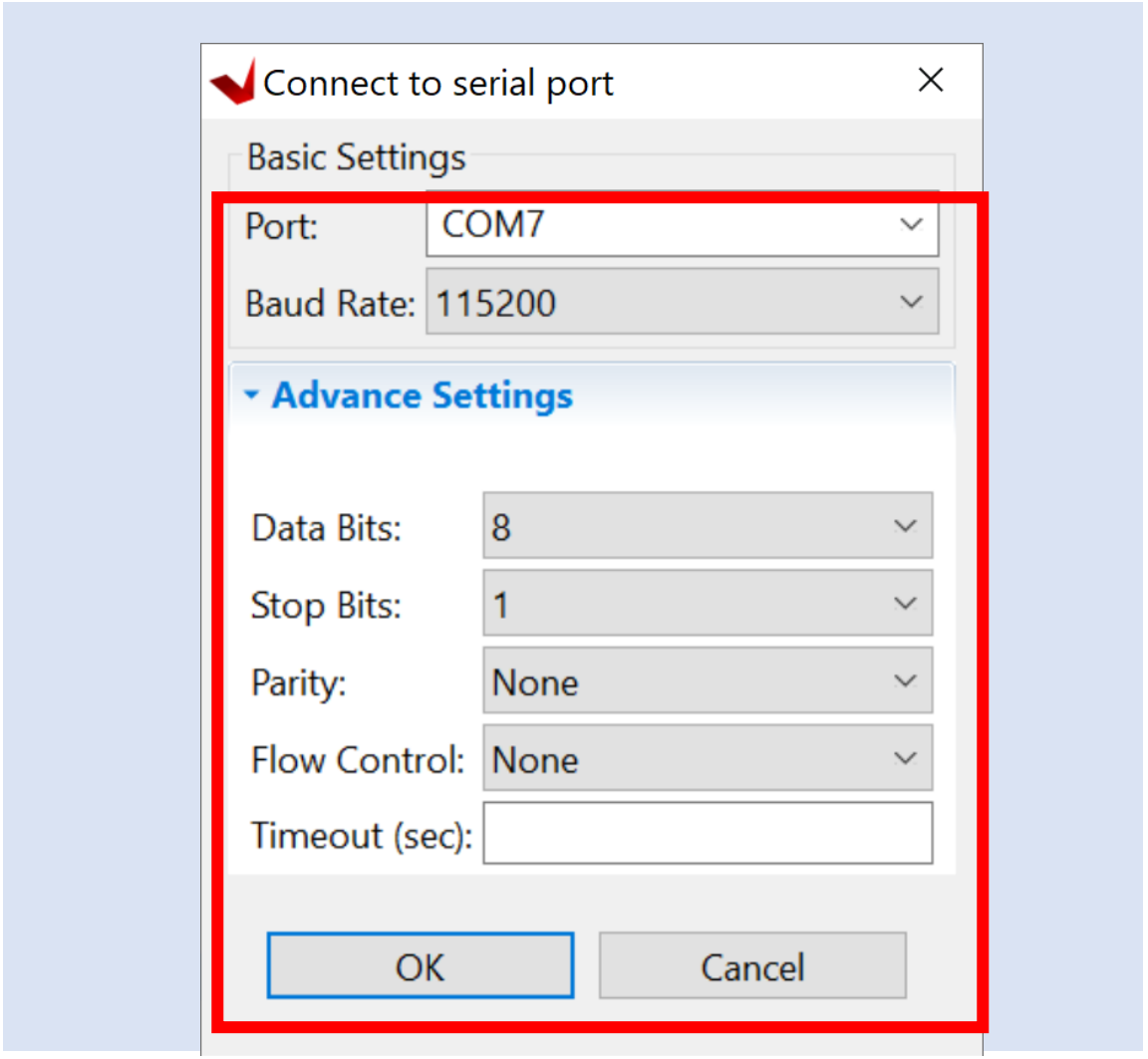
Step 62 – Add the following settings to the pop up and click ok



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Step 63 – Check the terminal window, secret word should be detected correctly