Creating Your First ArtyZ7 Application

Course Workbook

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The contents of this workbook are created by Adiuvo Engineering & Training, Ltd.

If you have any questions about the contents, or need assistance, please contact Adam Taylor at <u>adam@adiuvoengineering.com</u>.

Pre-Lab Workshop Pre-requisites

Required Hardware

ArtyZ7-20 Usb cable **Pre-Lab**

Pre-Lab

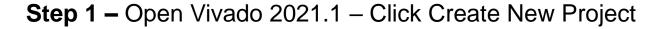
Downloads and Installations

Step 1 – Download and install the following at least 1 day prior to the workshop. This may take a significant amount of time and drive space.

Watch the video available <u>here</u> to show how to configure the installation

Vitis 2021.1	Download

Lab 1 Project creation & Flow



Wwado 2021.1 Eile Flow Iools Window Help Q: Quick Access	- 0 ×
ML Editions	€ XILINX.
Ouick Start Create Project > Open Example Project >	
Tasks Manage IP > Open Hardware Manager > Vivado Store >	
Learning Center Documentation and Tutorials > Quick Take Videos > What's New in 2021.1 >	
Tcl Console	? _ D 🛙 X
Q X Image: Ima	,

Step 2 – Click Next

À New Project		×
MLEditions	Create a New Vivado Project This wizard will guide you through the creation of a new project. To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.	
E XILINX.	< Back Finish Cancel	

Step 3 – Enter a project name and location to save the project, click next

<u>P</u> roject name:	xilinx_s1				
Project location	C:/hdl_projects				\otimes
Create proje	ct subdirectory				
Project will be c	reated at: C:/hdl_projects/xilin	IX_S1			

Step 4 – Select RTL project and check do not include sources, click next

🝌 Nev	v Project	×
-	ect Type fy the type of project to create.	4
۲	<u>R</u> TL Project You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis. ✓ <u>D</u> o not specify sources at this time Project is an extensible <u>V</u> itis platform	
0	<u>P</u> ost-synthesis Project You will be able to add sources, view device resources, run design analysis, planning and implementation. Do not specify sources at this time	
0	J/O Planning Project Do not specify design sources. You will be able to view part/package resources. Imported Project Create a Vivado project from a Synplify, XST or ISE Project File.	
0	Example Project Create a new Vivado project from a predefined template.	
?	< <u>B</u> ack <u>Next></u> <u>Finish</u> Ca	ncel

Step 5 – If the Arty Z7 isn't in the list of boards select Refresh and the board list will be updated

fault Part oose a default Xilinx part or Parts Boards	r board for your pro	oject.			I
	ailable boards from	git repository, click on 'Refresh' b	utton. Dismiss		
Reset All Filters Vendor: All	~	Name: All	~	Board Rev: Latest	~
Q ★ ⇒ ■L [#] Search: Q: arty	A Refresh C Downloadi	Catalog	ıg		
Refresh C talog was	last updated on 11,	/02/2021 5:07:16 PM			

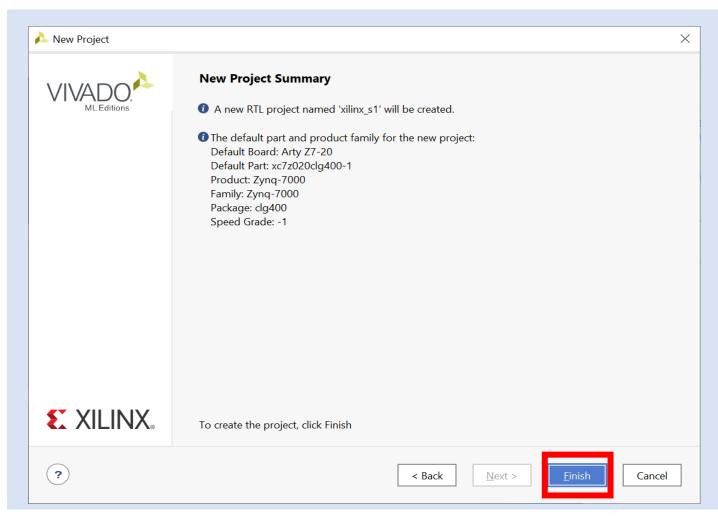
Step 6 – Select the download and the board will install

Parts B	Boards											
To fetc	h the la	test available l	boards from	git repository, clic	k on 'Refresh' I	outton.	Dismiss					
Reset All Fi Vendor: A			*	Name: A	11				*	Board Rev:	atest	~
Q ¥	\$	•6										
Search:	्र- arty			🛞 🗸 (0 ma	tches)							
Display Na		Preview	Status	Vendor	File Version	Part	I/O Pin Count	Board Rev	Available IOBs	LUT Elements	FlipFlops	Block R
Arty S	7-25		<u>+</u>	digilentinc.com	1.0							^
Arty S	7-50		<u>+</u>	digilentinc.com	1.0							
Arty Z	7-10		±	digilentinc.com	1.0							
Arty Z	7-20		<u>+</u>	ligilentinc.com	1.0							

Step 7 – Select Vendor Diglentinc and Arty Z7-20, click next

New Project	t										
efault Par t noose a defa	-	part or board	for your pro	oject.							
Parts				git repository, clic		Dissuise					
Reset All F		test available d	oards from	git repository, cita	k on Keiresh i	button. Dismiss					
Vendor:	All		~	Name: A	I			~	Board Rev:	Latest	~
Q	•	•4									
Search:	्- arty			🛯 🗸 (0 ma	tches)						
Display N		Preview	Status	Vendor	File Version	Part	I/O Pin Count	Board Rev	Available IOBs	LUT Elements	FlipFlc
Arty S	57-25		<u>+</u>	digilentinc.com	1.0						~
Arty S	S7-50		<u>+</u>	digilentinc.com	1.0						
Arty Z	Z7-10		Ŧ	digilentinc.com	1.0						
Arty Z	Z7-20		Θ	digilentinc.com	1.0	xc7z020clg400-1	400	A.0	125	53200	10640
Refresh	Catalo	og was last upo	dated on 11	/02/2021 5:07:57	PM						7
?								< Back	<u>N</u> ext >	<u>F</u> inish	Cancel

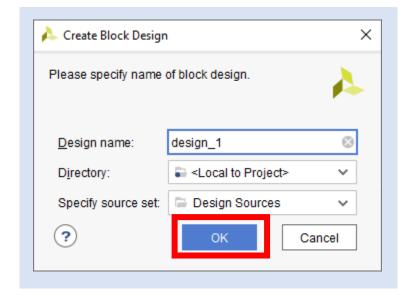
Step 8 – Click Finish



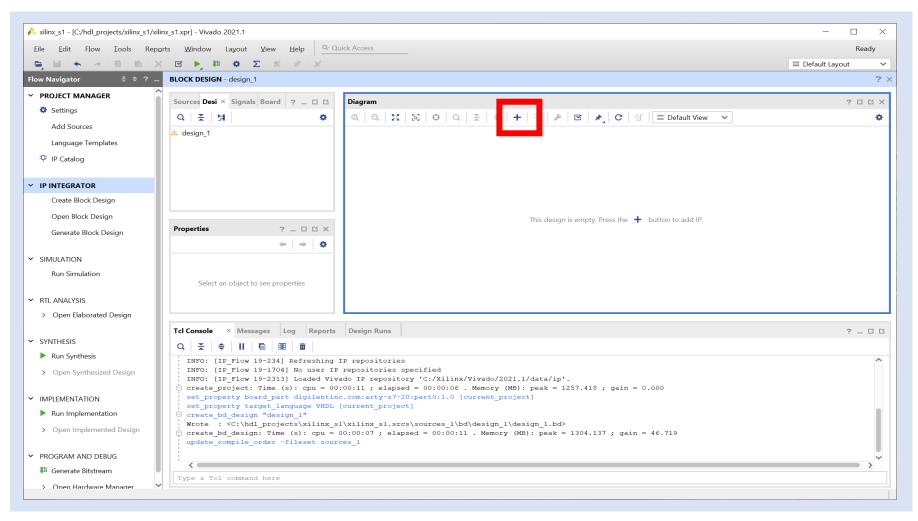
Step 9 – Click on Create Block Diagram – This will open IP editor

🏊 xilinx_s1 - [C:/hdl_projects/xilinx_s1/:	ilinx_s1.xpr] - Vivado 2021.1 — 🗌
<u>File E</u> dit Flow <u>T</u> ools Re	ports Window Layout View Help Q- Quick Access Ready
	↓ III ☆ ∑ 然 Ø X
Flow Navigator 😤 🌲 ?	PROJECT MANAGER - xilinx_s1
Y PROJECT MANAGER	Sources ? _ D 🖸 X Project Summary ? D 🗹
Settings	$Q = \frac{1}{2} + \frac{1}{2} = 0$
Add Sources	
Language Templates	 Design Sources Constraints Settings Edit
👎 IP Catalog	✓ □ Simulation Sources Project name: xilinx_s1
	sim_1 Project location: C//hdl_projects/xilinx_s1
	> 🖻 Utility Sources Product family: Zynq-7000
Create Block Design	Project part: Arty Z7-20 (xc7z020clg400-1)
Open block Design	Top module name: Not defined Target language: VHDL
Generate Block Design	Hierarchy Libraries Compile Order Target language: VHDL Simulator language: Mixed
Generate block Design	
SIMULATION	Properties ? _ D D X Board Part
Run Simulation	
	Display name: Arty Z7-20
RTL ANALYSIS	Board part name: digilentinc.com:arty-z7-20:part0:1.0 Board revision: A.0
> Open Elaborated Design	Select an object to see properties Connectors: No connections
	Repository path: C/Users/leesa/AppData/Roaming/Xilinx/Vivado/2021.1/xhub/board_store/xilinx_board_store
SYNTHESIS	URL: http://www.digilentinc.com
Run Synthesis	
> Open Synthesized Design	
	Tcl Console Messages Log Reports Design Runs ×
IMPLEMENTATION	$ Q_{A} \neq A \ll M \ll M + M $
Run Implementation	Name Constraints Status WNS TNS WHS TNS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy
> Open Implemented Design	V D synth_1 constrs_1 Not started Vivado Synthesis Defaults (Vivado Synthes
	▷ impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado
PROGRAM AND DEBUG	
👫 Generate Bitstream	
> Open Hardware Manager	
. 9-	

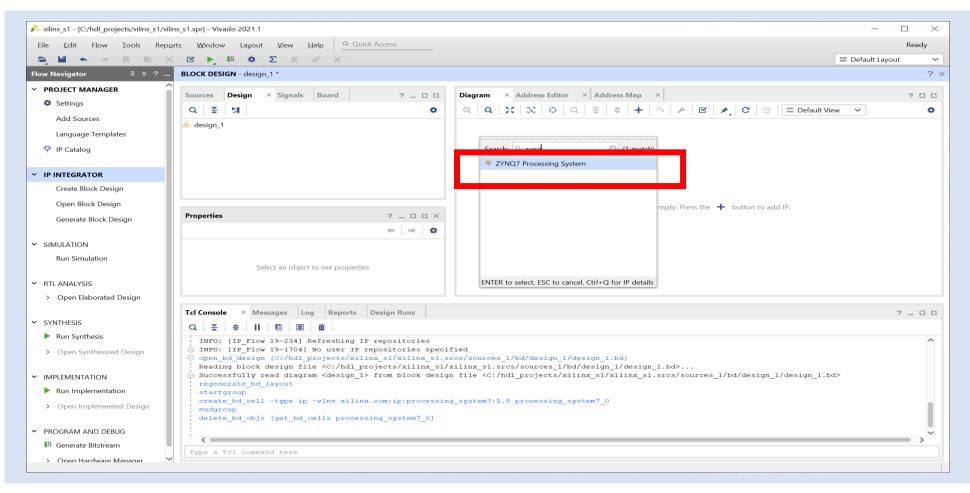
Step 10 – Leave the settings as default and click OK



Step 11 – Click on the + button to open the IP list



Step 12 – In the search bar, type Ultra and select the Zynq UltraScale+ MPSoC block. Double click on this to insert the IP block.



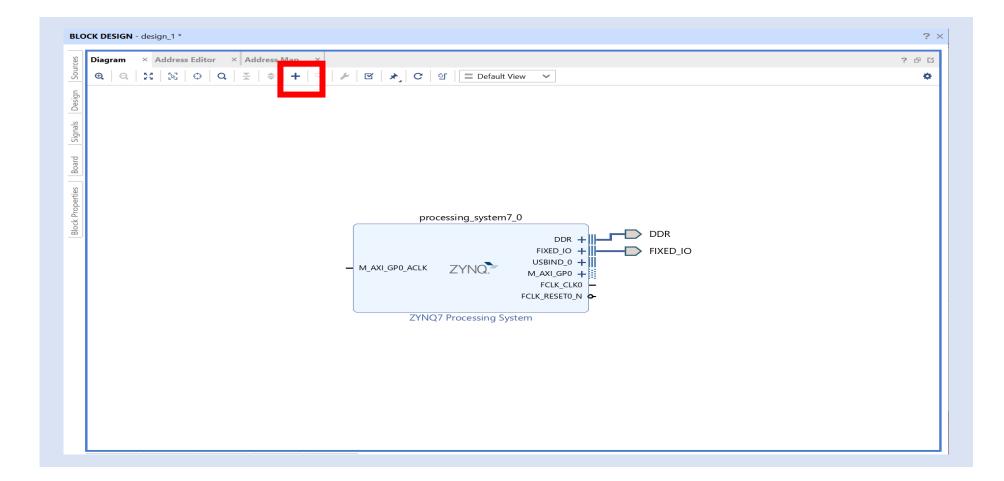
Step 13 – Select Run Block Automation – This will configure the Processing System for the ArtyZ7 setting e.g. DDR timing, Clocking etc.

BLC	OCK DESIGN - design_1 *	? ×
ources	Diagram × Address Editor × Address Map × 0 0 55 53 0 0 5 6 1 E 2 0 1 E Default View ✓ 1 <t< th=""><th>ас Ф</th></t<>	ас Ф
esign	* Designer Assistance available. Run Block Automation	
Signals		
Board		
Source File Properties	processing_system7_0 DDR + H FIXED_IO + H FIXED_IO + H M_AXI_GP0_ACLK ZYNQ FCLK_RESET0_N ZYNQ7 Processing System	

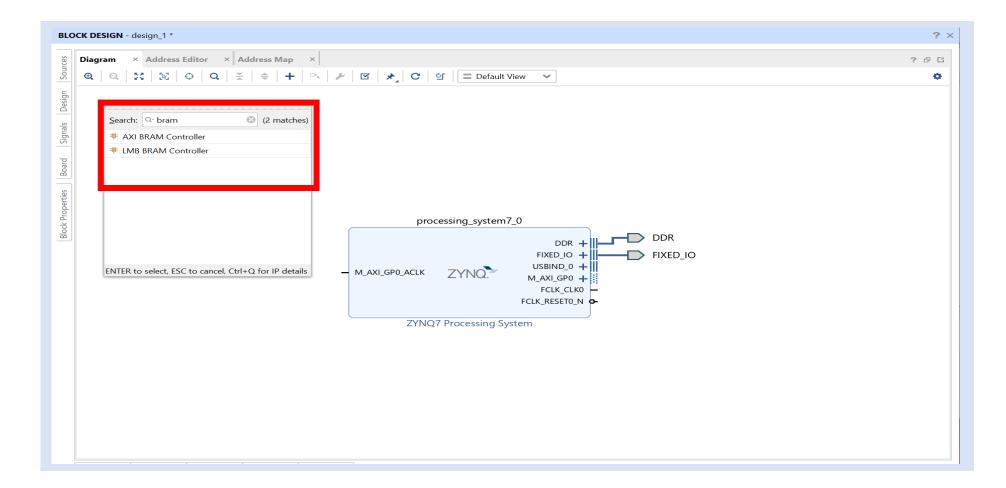
Step 14 – Click on the OK button, the automation will run and configure the processing block for the ArtyZ7.

ຊ ≚ ≑	Description
✓ ✓ All Automation (1 out of 1 selected) ✓ ♥ processing_system7_0	This option sets the board preset on the Processing System. All current properties will be overwritten by the board preset. This action cannot be undone. Zynq7 block automation applies current board preset and generates external connections for FIXED_IO, Trigger and DDR interfaces.
	NOTE: Apply Board Preset will discard existing IP configuration - please uncheck this box, if you wish to retain previous configuration.
	Instance: /processing_system7_0
	Options
	Make Interface External: FIXED_IO, DDR
	Apply Board Preset: 🖌
	<u>C</u> ross Trigger In: Disable V
	Cross Irigger Out: Disable 🗸

Step 15 – Click on the + Symbol

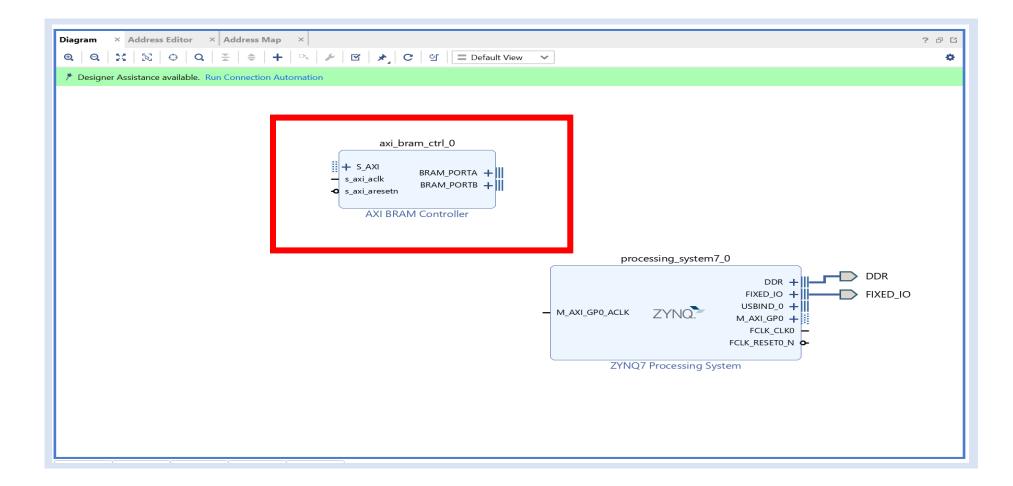


Step 16 – Type in BRAM and double click on AXI BRAM Controller to add the IP



Lab 1

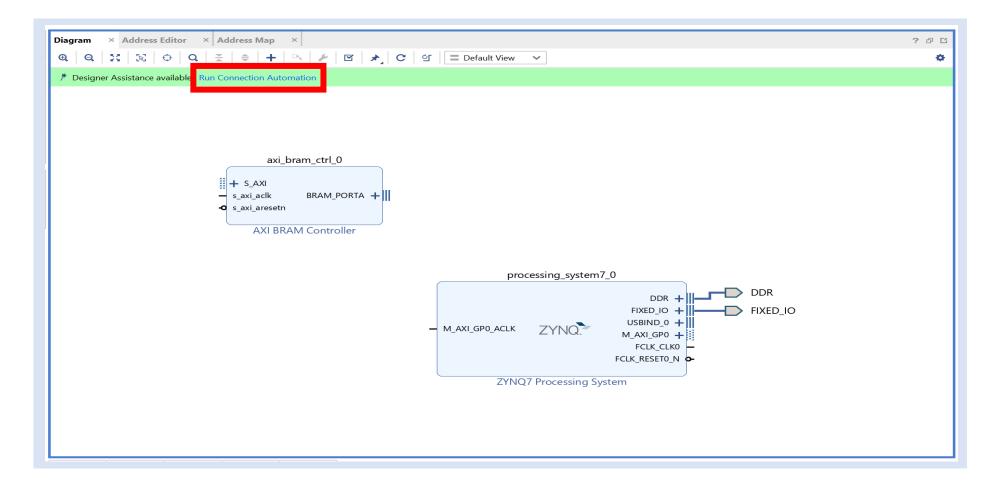
Step 17 – Double click on the AXI BRAM Controller



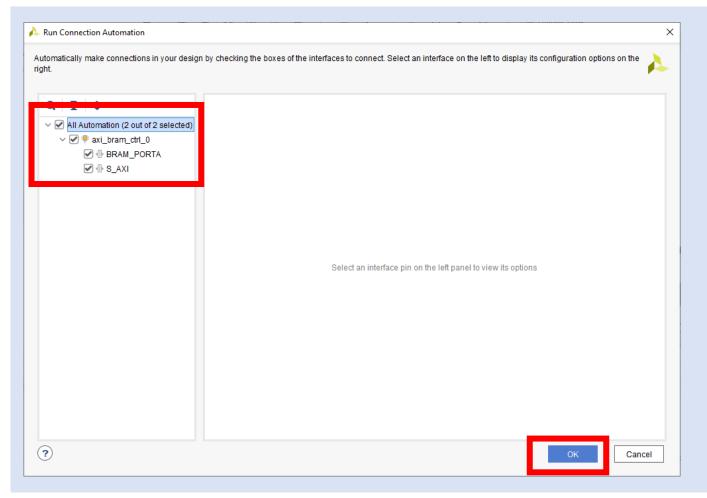
Step 18 – Change the Number of BRAM Interfaces to 1, click OK

AXI BRAM Controller (4.1)				1
Documentation 📄 IP Location				
Show disabled ports	Component Name axi_bram_ctrl_0			
	AXI Protocol	AXI4	~	
	Data Width	32	\sim	
	Memory Depth (Auto)	8192	\mathbf{v}	
	ID Width (Auto)	0	~	
	AUTO Support AXI Narrow Bursts	Yes	~	
	Read Latency	1	[1 - 128]	
•	Read Command Optimization	No	~	
+ S_AXI s_axi_adk BRAM_PORTA + BRAM_PORTB +				
• s_axi_aresetn	BRAM Instance (Auto) Externa			
	Number of BRAM interfaces 2	~		
	ECC Options			
	·······	1		
	Enable Fault Injection No			
	ECC Reset Value 0	1		
				· · · · · · · · · · · · · · · · · · ·

Step 19 – Click on Run Connection Automation



Step 20 – Check all the boxes, click OK



Step 21 – Click on the Regenerate Layout – This will mage the diagram more logical

Diagram × Address Editor × Address Q Q S S Q Z 4 axi_bram_ctrl_0 + S_axi_adk BRAM_PORTA + + +	axi_bram_ctrl_0_bram + BRAM_PORTA rsta_busy 	axi_smc
AXI BRAM Controller	Block Memory Generator Block Memory Generator Block Memory Generator Block Memory Generator Block Memory Generator ext, reset_in bus_struct_reset(0.0) mb_debug_sys_rst interconnect_aresetn[0.0] Processor System Reset DDR + FIXED_IO + USBIND_0 + M_AXI_GP0_ACLK ZYNQ? Processing System ZYNQ7 Processing System	DDR FixeD_

Step 22 – Double Click on the BRAM Block

Diagram × Address Editor × Address Map ×	2 문 단
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rst.ps7.0_100M slowers.gync_dk mb_rest grocessing_system WAXLGP0_ACLK ZYNQ FRED.0 FCLK_RESET0.0 ZYNQ7 Processing System AXI SmartConnect AXI SmartConnect AXI BRAM Controller AXI BRAM Controller	DDR Fixed_io

Step 23 – Change the mode to Standalone, make sure check use 32 bit addressing is set

🔥 Re-customize IP		×
Block Memory Generator (8.4)		A
Ocumentation IP Location		
IP Symbol Power Estimation	Component Name axi_bram_ctrl_0_bram	
Show disabled ports	Basic Port A Options Other Options Summary	
	Mode BRAM Controller Image: Controller Memory Type BRAM Controller Common Clock Stand Alone Common Clock	
	ECC Type No ECC	
	Write Enable Single Bit Error Injection Write Enable Syste Write Enable	
+ BRAM_PORTA rsta_busy	Byte Size (bits) 8	
	Algorithm Options Defines the algorithm used to concatenate the block RAM primitives. Refer datasheet for more information. Algorithm Minimum Area Primitive 8kx2	
	OK Ca	ncel

Step 24 – Check load Init File, click on edit continue to step 25

🔥 Re-customize IP		×
Block Memory Generator (8.4) Documentation B IP Location		Ą
Poulinemation Power Estimation Show disabled ports	Component Name axi_bram_ctrl_0_bram Basic Port A Options Other Options Summary Pipeline Stages within Mux 0 Mux Size: 1x1 Memory Initialization Coe File no_cce_file_loaded Browse @ Edit Fill Remaining Memory Locations Remaining Memory Locations (Hex) 0	
+ BRAM_PORTA rsta_busy -	Structural/UniSim Simulation Model Options Defines the type of warnings and outputs are generated when a read-write outputs on occurs. Collision Warnings Behavioral Simulation Model Options Disable Collision Warnings Behaviori Power Saving Enable Safety Circuit	
		OK Cancel

Step 25 – Click Yes

Block Memory Cenerator (8.4) Componentiation P Symbol Power Estimation Componenti Name ax Ltram,dtr_0_btram Basic Port A Options Uber Options Summary Pipeline Stages within Mux I I I I I I I I I I I I I I I I I I	▶ Re-customize IP		
Show disabled ports Basic Pipeline Stages within Mux I + BRAM_PORTA rsta_busy- Behavioral Simulation Model Options Behavioral Simulation Model Options Behavioral Simulation Model Options Behavioral Simulation Model Options Disable Out of Range Warnings Disable Out of Range Warnings Disable Out of Range Warnings			À
	Show disabled ports	Basic Port A Options Other Options Summary Pipeline Stages within Mux 0 Mux Size: 1x1 Memory Initialization Image: Construct of the Construction of the Const	

Step 26 – Select the project folder and continue to step 27

A Save Location For COE File	×
Save In: hdl_projects	✓ ↑ ☆ 및 ± À ▷ × C Ⅲ Ξ
axilinx_s1	Recent Directories
	C:/hdl_projects
	File Preview
	Select a file to preview.
File name: design_1_axi_bram_ctrl_0_bram_0	
Files of type: COE Files(*.coe)	~
	Save Cancel

Step 27 – Select a location inside the project to save the file and select OK

Save Location For COE File			
avejn: 🔄 xilinx_s1	×	1 🏠 🖵 土 👌 🖬 🗙 C	
xilinx_s1.cache	Recent Directories		
xilinx_s1.gen	C:/HLS/PID		~
xilinx_s1.hw			
xilinx_s1.ip_user_files	File Preview		
xilinx_s1.sim	Select a file to preview.		
xilinx_s1.srcs			
le name: design_1_axi_bram_ctrl_0_bram_0			
les of type: COE Files(*.coe)			
		Save	Canc

Step 28 – Enter the following

```
Memory Initialization Radix = 16
Memory Initialization Vector = 4841434b, 53544552, 20554c54, 52413936, 20545554, 4f524941, 0000004c,
```

Click Save, then Validate before closing

COE File Editor - design_1_axi_bram_ctrl_0_bram_(D.coe X
Кеу	Value
memory_initialization_radix	16
memory_initialization_vector	4841434b, 53544552, 20554c54, 52413936, 20545
Validate	Save Save As Close

Lab 1

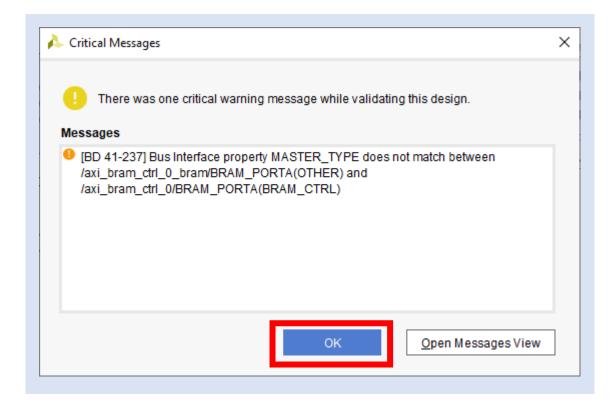
Lab 1: Understanding Vitis Project creation & Flow

Step 29 – Click OK

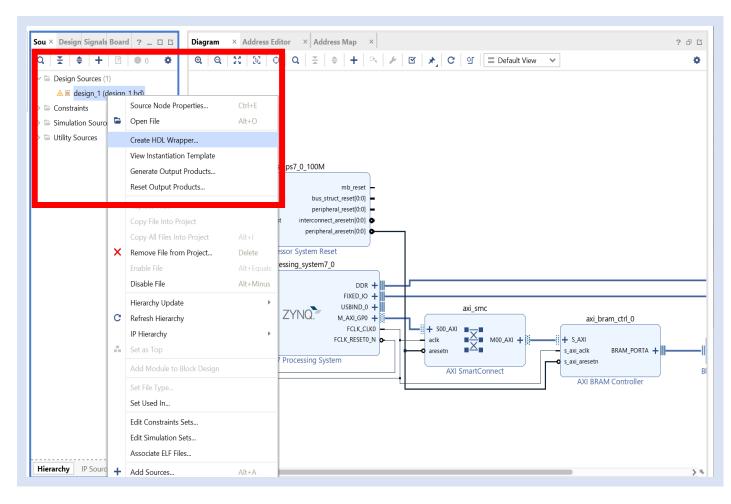
Re-customize IP		
ock Memory Generator (8.4) Documentation 📄 IP Location		
P Symbol Power Estimation	Component Name axi_bram_ctrl_0_bram	
) Show disabled ports	Basic Port A Options Other Options Summary Pipeline Stages within Mux 0 ✓ Mux Size: 1x1 Memory Initialization	
	Weimory initialization Coe File II_projects/xilinx_s1/design_1_axi_bram_ctrl_0_bram_0.coe Edit Edit	
	Fill Remaining Memory Locations Remaining Memory Locations (Hex) 0	
+ BRAM_PORTA rsta_bus	y Behavioral Simulation Model Options Behavioral Simulation Model Options	
	Disable Collision Warnings Disable Out of Range Warnings	
	Dynamic Power Saving	
	Sleep	
	Safety logic to minimize BRAM data corruption	
	✓ Enable Safety Circuit	
		OK Canc

Step 30 – Click on Validate the design

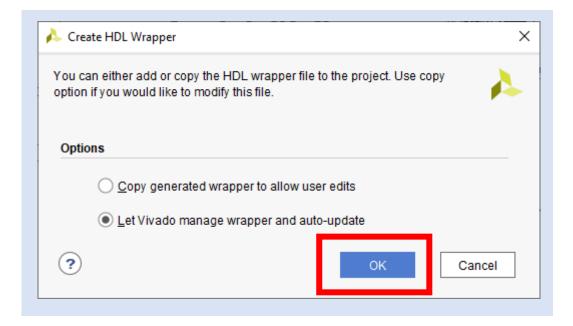
Step 31 – Click On OK the warning is due to the change from AXI BRAM control



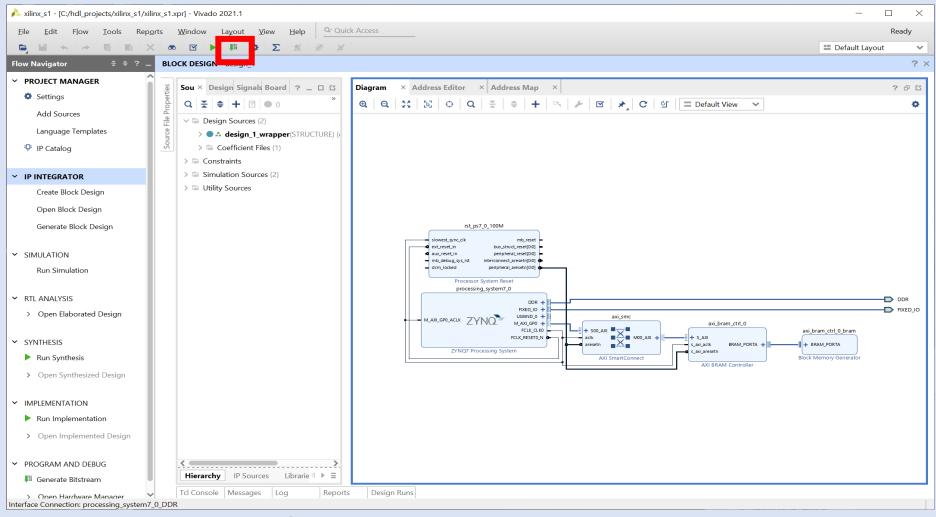
Step 32 – In the sources tab, right click on the block diagram and select create HDL Wrapper



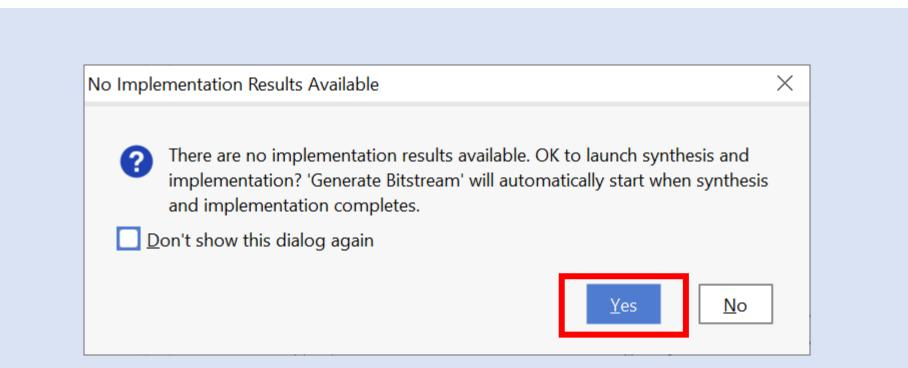
Step 33 – leave the options as set and let Vivado manage the wrapper, click OK



Step 34 – Click on Generate Bit Stream



Step 35 – Click yes



Step 36 – Click Ok

Launch Runs	×
Launch the selected synthesis or implementation runs and generate bitstream.	•
Launch <u>directory</u> :	~
Options	
Launch runs on local host: Number of jobs: 1	~
O <u>G</u> enerate scripts only	
Don't show this dialog again	
? ОК	Cancel

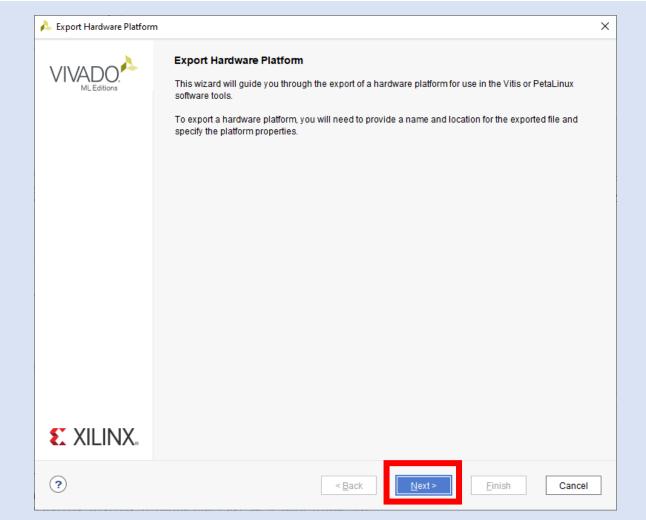
Step 37 – Wait until the bit stream is complete

kilinx_s1 - [C:/hdl_projects/xilinx_s1/		>
	ports <u>W</u> indow Layout <u>View H</u> elp <u>Q. Quick Access</u>	write_bitstream Complete
		Default Layout
ow Navigator	BLOCK DESIGN - design_1	?
PROJECT MANAGER Settings Add Sources Language Templates IP Catalog IP Catalog Den Block Design Open Block Design Open Block Design Generate Block Design Generate Block Design SIMULATION Run Simulation SYNTHESIS Run Synthesized Design IMPLEMENTATION Run Implementation Open Implemented Design PROGRAM AND DEBUG	Sou × Design Signals Board ? G Q × Design Sources (2) > 0 design_JurrapperSTRUCTURD () > Constraints S Simulation Sources (2) > 0 Lotifuent Files (1) > Constraints S Simulation Sources (2) > 0 Utility Sources Utility Sources	2 € DDR DDR FixED_1 withram_ctrl_0_bram FixED_1 Block Memory Generator

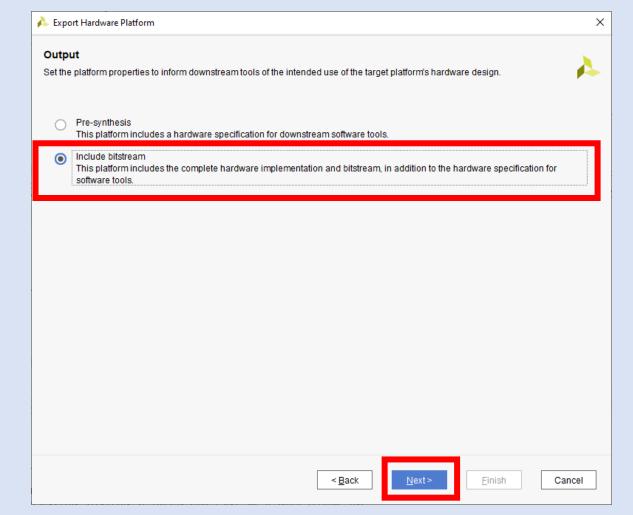
Step 38 – From the File Menu select Export->Export Hardware

ile	<u>E</u> dit F <u>l</u> ow <u>T</u> ool	ls Rep <u>o</u> rts	Window Layout View Help Q- Quick Access
_	Project	۰.	∞ ☑ ▶ ቑ ✿ Σ ∞ ∅ × € €
	Add So <u>u</u> rces	Alt+A	BLOCK DE SIGN - design_1
	<u>C</u> lose Project		Sources × Design Signals Board ? _ 🗆
	Save Block Design	Ctrl+S	
	Save Block Design As.		
	<u>C</u> lose Block Design		✓ ■ Design Sources (2) A design 1 uranner (STPLICTURE) (design 1 uranner ub)
	<u>C</u> onstraints	Þ	> design_1_wrapper(STRUCTURE) (design_1_wrapper.vh/ > Coefficient Files (1)
	Simulation Waveform	Þ	> 🗁 Constraints
	Chec <u>k</u> point		V Simulation Sources (2)
	<u>I</u> P	Þ	_ >
	Text E <u>d</u> itor	Þ	
	I <u>m</u> port	Þ	
	Export	•	Export <u>H</u> ardware ibraries Compile Order
	Print	Ctrl+P	Export block Design
	Exit		Export Bitstream File ? _ 🗆 🖸
RT	'L ANALYSIS		Export Simulation 🔶 🔺

Step 39 – Click on Next



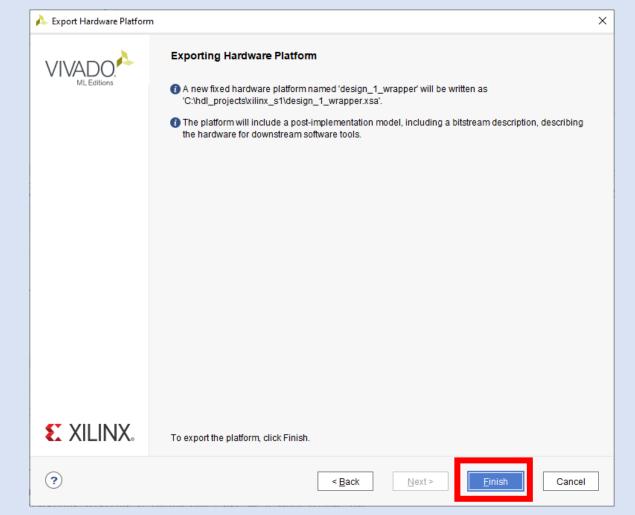
Step 40 – Ensure Include Bitstream is selected and click OK



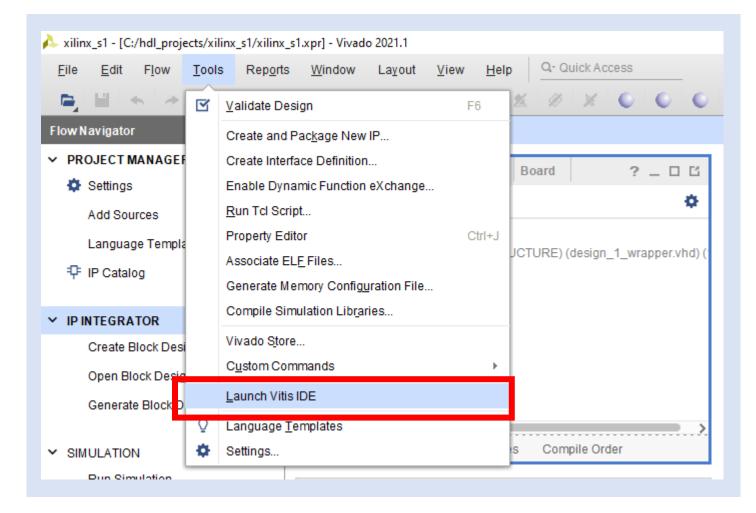
Step 41 – Leave the defaults as is and click on Next

	f your hardware platform file, and the directory where the XSA file will be stored.
XSA file name:	design_1_wrapper 😵
Export to:	C:/hdl_projects/xilinx_s1
	The XSA will be written to: C:\hdl_projects\xilinx_s1\design_1_wrapper.xsa

Step 42 – Click Finish



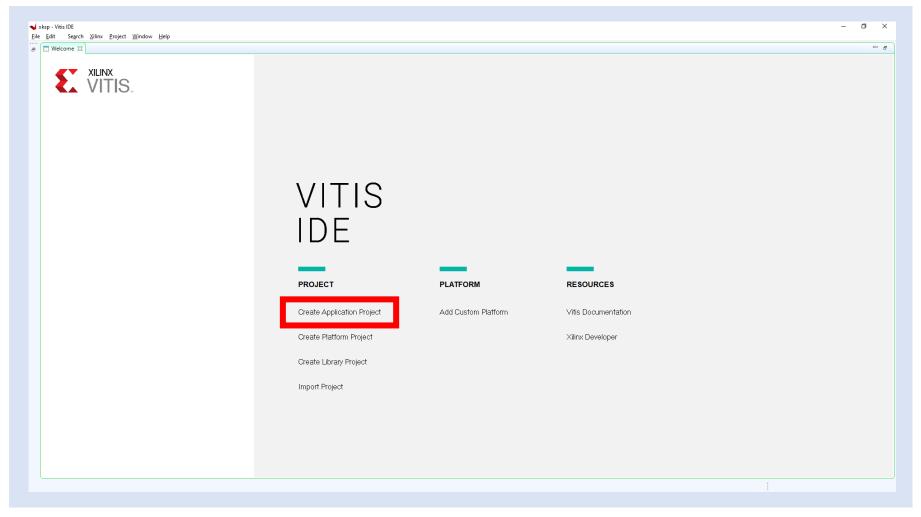
Step 43 – From the Tools menu select Launch Vitis IDE



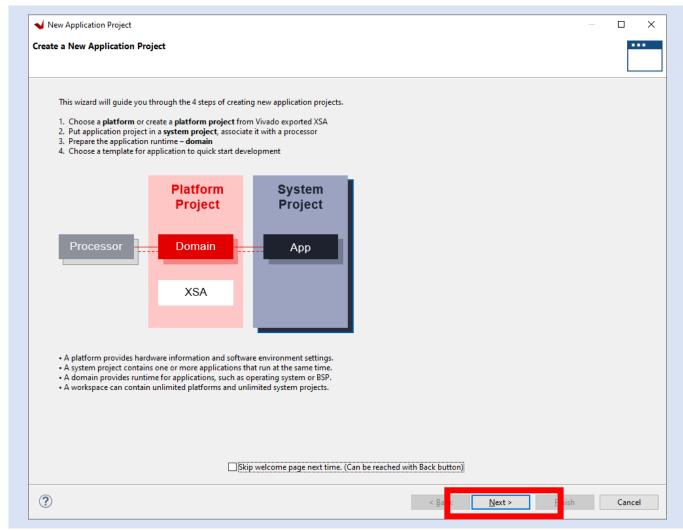
Step 44 – At the dialog, create a new folder in your project directory and select launch

lect a dire	ectory as workspace			
itis IDE use	s the workspace directory to stor	re its preferences and developme	ent artifacts.	
/orkspace:	C:\hdl_projects\xilinx_s1\xksp		~	<u>B</u> rowse
<u>U</u> se this a	s the default and do not ask agai	in		
	her Workspace			
<u>R</u> estore of	ner workspace			
<u>R</u> estore of <u>R</u> ecent We	•			
_	•			

Step 45 – Click on Create Application Project



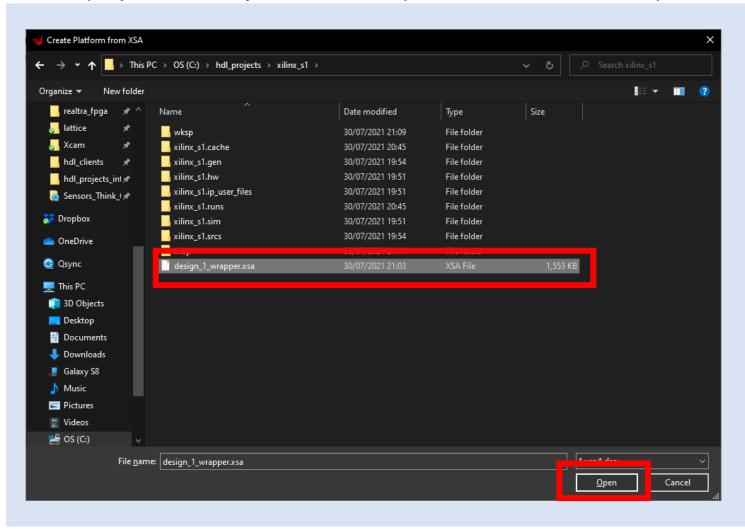
Step 46 – Click on next



Step 47 – Click on Create a New Platform from Hardware (XSA) and select browse

Please selec	t a platform to create the project	
		L
Selectau	platform from repository 🖳 Create a new platform from hardware (XSA)	
Hardware	e Specification Provide your XSA file or use a pre-built board description	
	vck190	
	vck190_es1	
	vmk180 vmk180_es1	
XSA File:	zc702 zc706	Browse
	zcu102	
	zcu106 zed	
Platform r	name:	

Step 48 – Browse to the project directory, select the exported XSA and Click Open



Step 49 – Click on OK

form		
te: A platfo	rm project will be generated automatically in workspace for the selected XSA. It can be customized later.	L
Select a	platform from repository 📳 Create a new platform from hardware (XSA)	
	e Specification	
	C:\hdl_projects\xilinx_s1\design_1_wrapper.xsa]
XSA File:	vck190 vck190_es1 vmk180 vmk180_es1 zc702	Browse
ASA FILE:	zc706 zcu102 zcu106 zed C:\hdl_projects\xilinx_s1\design_1_wrapper.xsa	DIOWSE
Gener	nponents ate boot components et processor to create FSBL:	
Platform	name: design_1_wrapper	

Step 50 – Enter a project name and select Next

New Application Project			_		>
pplication Project Details					
specify the application project nam	e and its system project propertie	25			
Application project name ArtyZ7					
System Project	the application or coloct on evictiv	a one from the worknesses	0		
Create a new system project for	the application or select an existin	ng one from the workpsace	U		
Select a system project	System project details				
		[
	System project name:	ArtyZ7_system			
	Target processor				
	Select target processor	for the Application project.			
	Processor	Associated applications			
	ps7_cortexa9_0	ArtyZ7			
	ps7_cortexa9_1				
	ps7_cortexa9 SMP				
	Show all processors in	the hardware specification 🔽	0		
?	< Back	Next >	Finish	Cance	el

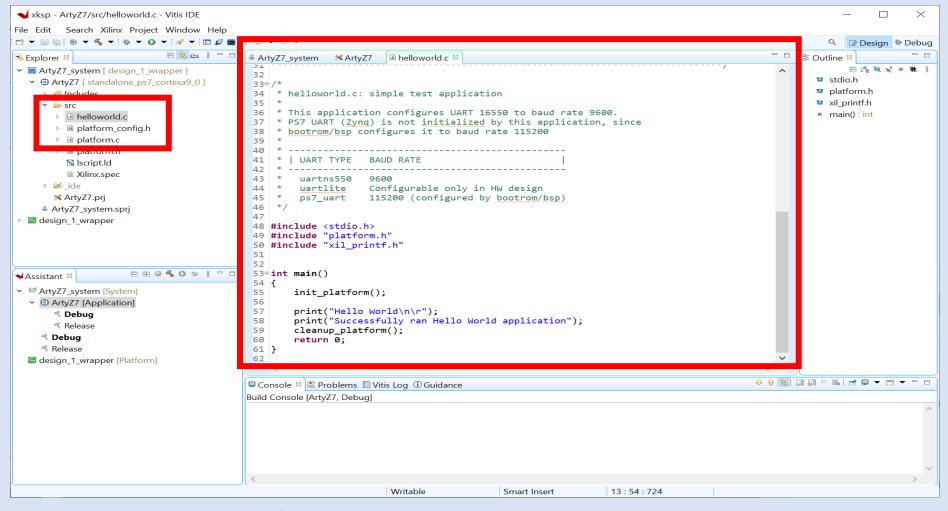
Step 51 – Click Next

Vew Application Project					×
Domain					•••
Select a domain for your project or	create a new domain				
Select the domain that the applicati Note: New domain created by this v			emplate selected	in the next st	en
Select a domain	Domain details				- F
	Name:	standalone_ps7_cortexa9_	0		
	Display Name:	standalone_ps7_cortexa9_	0		
	Operating System:	standalone	\sim		
	Processor:	ps7_cortexa9_0			
	Architecture:	32-bit	~		
(?)	< Bac	k Next >	Finish	Ca	ncel
	< Bac	ivext >	FINISH	Ca	icel

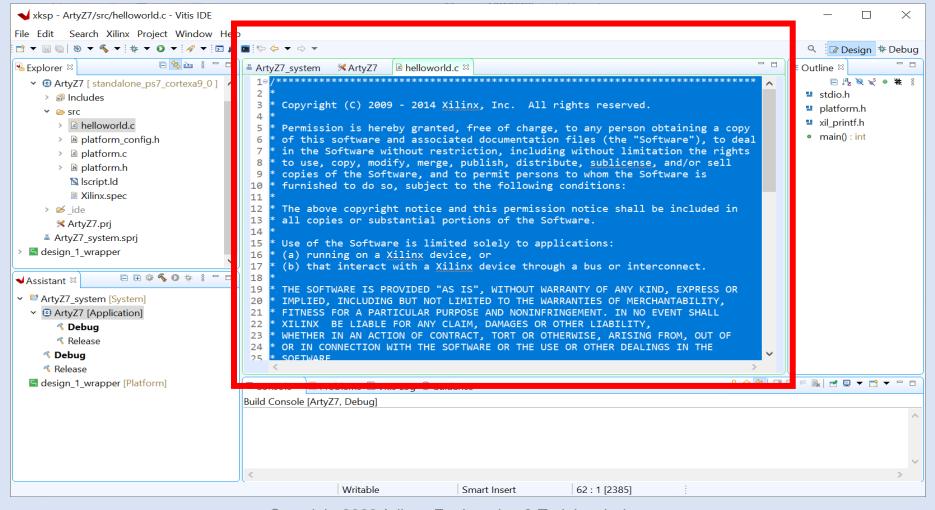
Step 52 - Select Hello World and click finish

✓ New Application Project			
emplates Select a template to create your project.			
Available Templates:			
Find:	Hello World		
✓ Embedded software development templates Dhrystone Empty Application (C++) Empty Application C) Hello World Image Recovery Image Selector Iw/P TCP Perf Client Iw/P TCP Perf Server Iw/P UDP Perf Server Iw/P UDP Perf Server Memory Tests Peripheral Tests Zynq MP DRAM tests Zynq MP FSBL	Let's say 'Hello World' in C.		
(?)	< <u>B</u> ack <u>N</u> ext > F	nish	Cancel

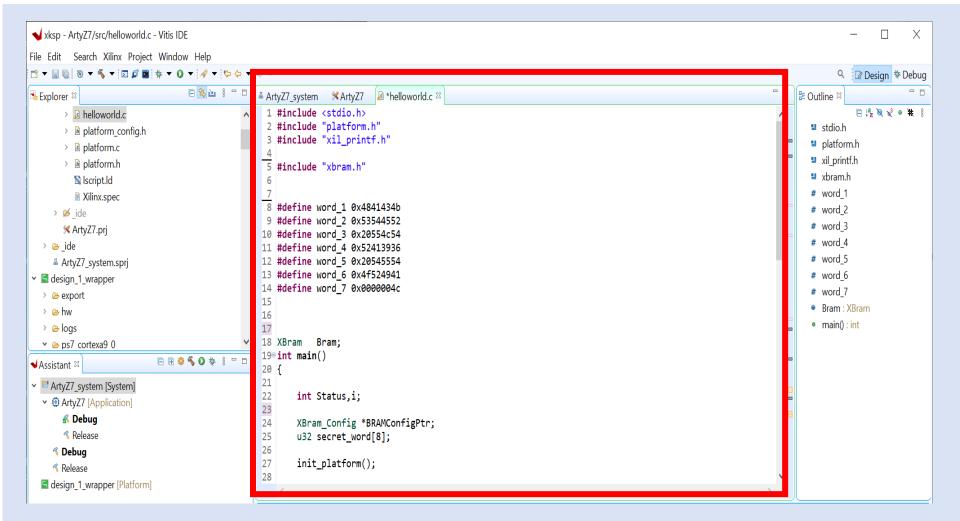
Step 53 - From the application / src folder double click and open the helloworld.c



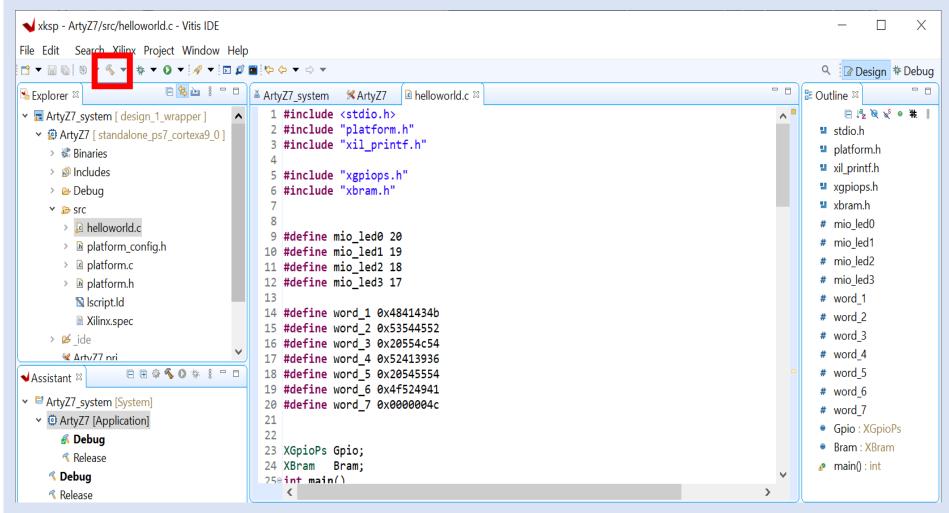
Step 54 - Click CNTRL-A to select all the code in the file and delete it



Step 55 - Copy and paste in the code from the Github repo session one lab



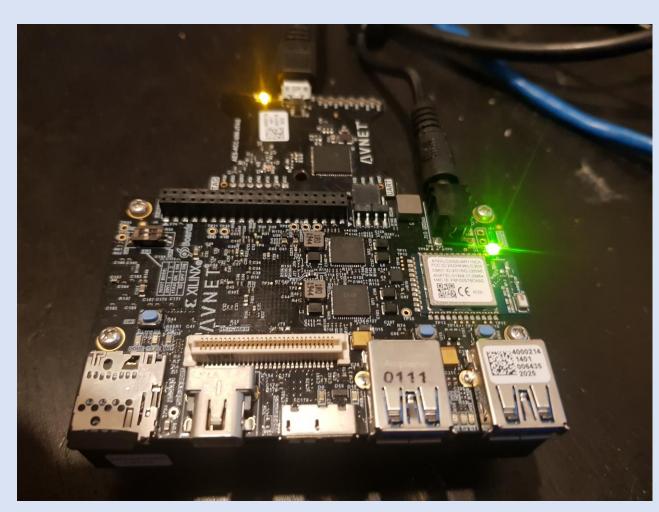
Step 56 - Click on the Hammer to Build the project



Step 57 - It will take a few minutes to compile. Successful completion will show as below

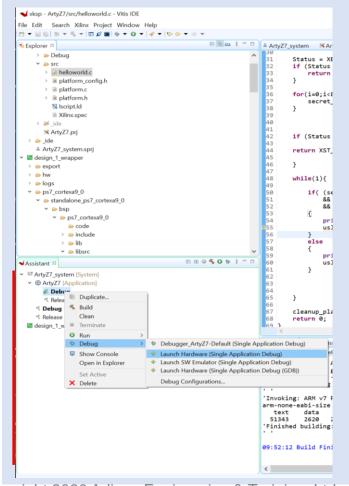
Sectors Disk T Addr. years Mail Disk T Sectors Disk Disk <th>xksp - ArtyZ7/src/helloworld.c - Vitis IDE</th> <th></th> <th>- 0</th>	xksp - ArtyZ7/src/helloworld.c - Vitis IDE		- 0
<pre>prove 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</pre>		A ★ 0 ★	Q 🔐 Design 🎋 De
<pre>b Box discussion of the set of the set</pre>	Explorer 🛙	🖻 🎕 🖮 📱 🗖 🔲 🔺 ArtyZ7, system 🛛 🛠 ArtyZ7 🗇 helloworld.c 🖄	- □ # Outline ≈
Build Console [Arty27, Debug] 'Building target: Arty27, elf' 'Invoking: ARM v7 gcc linker' arm=none-eabi-gcc =mcpu=cortex=a9 =mfpu=vfpv3 =mfloat=abi=hard =wl,=build=id=none =specs=Xilinx.spec =wl,=T =wl,/src/lscript.ld =LC:/hdl_projects/xilinx_s1/xksp/design_1_wrapper/export, 'Finished building target: Arty27.elf; 'Invoking: ARM v7 Prit Size' arm=none=eabi-size Arty27.elf tee "Arty27.elf.size" text data bs dec hex filename 51343 2620 22720 76683 128b8 Arty27.elf 'Finished building: Arty27.elf.size' ' 99:52:12 Build Finished (took 1s.265ms)	 > Debug > src > Debug > src > Debug > Belatorm_config.h > Be platform.c > Set platform.c > Be platfore	<pre>Status = XBram_ffgInitialize(&Bram, BRAMConfigPtr,BRAMConfigPtr->CtrlBaseAddress); if (Status != XST_SUCCESS) { return XST_FAILURE; } for(i=0;i<&;i++){ secrt_word[i] = XBram_ReadReg(XPAR_BRAM_0_BASEADDR, i*4); } if (Status != xST_SUCCESS) { return XST_FAILURE; } if (scatus != xST_SUCCESS) { return XST_FAILURE; } if((scatus != xST_SUCCESS) { return XST_FAIL</pre>	stich st
		<pre>'Building target: ArtyZ7.elf' 'Invoking: ARM v7 gcc linker' arm-none-eabi-gcc -mcpue-ucortex-a9 -mfpu=vfpv3 -mfloat-abi=hard -Wl,-build-id=none -specs=Xilinx.spec -Wl,-T -Wl,/src/ 'Finished building target: ArtyZ7.elf' 'Invoking: ARM v7 Print Size' arm-none-eabi-size ArtyZ7.elf tee "ArtyZ7.elf.size" text data bss dec hex filename 51343 2620 22720 76683 1208D ArtyZ7.elf 'Finished building: ArtyZ7.elf.size' 'Invoking: ArtyZ7.elf.size'</pre>	/lscript.ld -LC:/hdl_projects/xilinx_s1/xksp/design_1_wrapper/export/
		د	

Step 58 - Connect the USB to the ArtyZ7, Check the book Mode is JTAG. Power on the board.

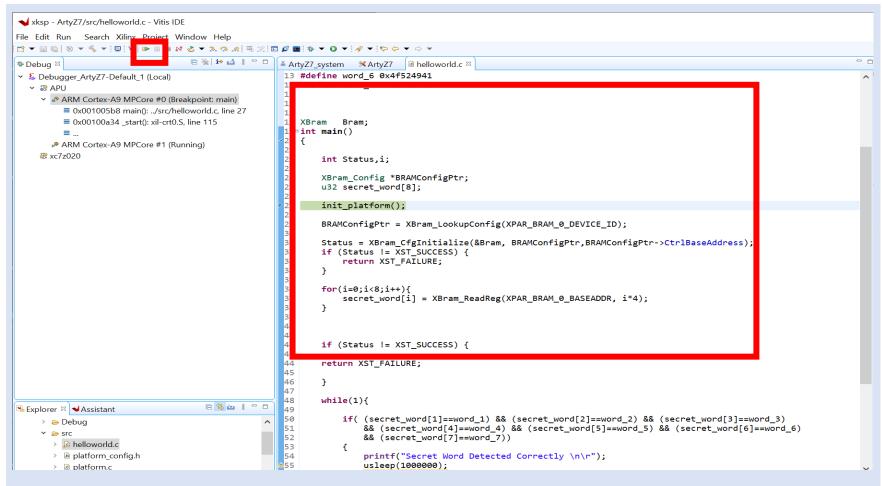


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Step 59 - From the assistant view, right click on debug and select debug-> launch on Hardware. This will configure the ArtyZ7, download the PL and the application.



Step 60 - The application will pause at the first instruction on the ArtyZ7. Click the Run Arrow



Step 61 – Project will run, Click on Vitis Serial Terminal and Click +

xksp - ArtyZ7/src/helloworld.c - Vitis IDE File Edit Run Search Xilinx Project Window	Help			-	٥	2
		\$ ▼ 0 ▼ <mark> </mark>		٩ [2 Design	‡ D€
† Debug ≅	E 🐩 🖬 🗧 🗖	≚ ArtyZ7_system	Vari 😫	⁰ Brea ⅔ Exp	r MReg	i '
Pebug ≓ Sebugger_ArtyZ7-Default (Local) Party PARM Cortex-A9 MPCore #0 (Running) PARM Cortex-A9 MPCore #1 (Running) xc7z020 Cortex-A9 MPCore #1 (Running) Cortex-A9 MPCore		<pre>1 #include <stdio.h> 1 #include <stdio.h> 2 #include <stdio.h> 2 #include "xli_printf.h" 4 5 #include "xli_printf.h" 6 7 8 #define word_1 0x4841434b 9 #define word_2 0x53544552 10 #define word_3 0x20554c54 11 #define word_6 0x4452413936 12 #define word_6 0x44524941 13 #define word_6 0x44524941 14 #define word_7 0x0000004c 15 16 17 17 18 XBram Bram; 19=int main() 20 { 21 11 tstatus,i; </stdio.h></stdio.h></stdio.h></pre>	Name \leftrightarrow Status \rightarrow is \rightarrow BRAM \Rightarrow # secret Mo \Rightarrow # #	Type int Con XBram_Con wou u32 [8]	Value 1051 30 ff {Dev [0xb	E3 C3
	@ % 0 	<pre>23 24 25 26 27 27 28 29 29 29 29 29 29 29 29 29 29 29 20 20 20 20 20 20 20 20 20 20 20 20 20</pre>		4000030 40000040 40000050 40000060 40000070 40000080 40000080	2054553	36 00 00 00 00 00 00
% Debug % Release ■ design_1_wrapper (Platform)		Conse Vitis Serial Terminal Conse Vitis Log Debug Shell Vitis Log Problems Debugger Consc Click on + button to add a port to the terminal.	MPCore #0 = #0 (targe ld.c: 27	t 2) Stopped	l at 0x1	.005t

Step 62 – Add the following settings to the pop up and click ok

Port:	COM7	~
Baud Rate:	115200	~
• Advance	Settings	
Data Bits:	8	\sim
Stop Bits:	1	~
Parity:	None	\sim
Flow Contro	ol: None	\sim
Timeout (se	c):	

Step 63 - Check the terminal window, secret word should be detected correctly

