Getting to Know Vivado

Course Workbook

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The contents of this workbook are created by Adiuvo Engineering & Training, Ltd.

If you have any questions about the contents, or need assistance, please contact Adam Taylor at <u>adam@adiuvoengineering.com</u>.

Pre-Lab Workshop Pre-requisites

Required Hardware

There is no required hardware for this course.

Pre-Lab

Pre-Lab

Downloads and Installations

Step 1 – Download and install the following at least one day prior to the workshop. This may take a significant amount of time and drive space.

Vitis 2021.1	Download
Source Project Files	Download

Step 1 – Open Vivado 2021.1.

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Quick Start Create Project > Open Example Project >	Ŷ
Tasks Manage IP > Open Hardware Manager > Vivado Store >	
Learning Center Documentation and Tutorials > Quick Take Videos > What's New in 2021.1 >	~

Step 2 – Click on Create Project – This will open the New Project Wizard – Click Next.



Step 3 – Enter the project name of "**01_Vivado**" and select the location you want to save the project. Click Next



Step 4 – Select RTL Project. Check Do not specify sources is unticked



Step 5 – Click **ADD FILES** and select the two files downloaded from Github. For the file average_tb.vhd, change the HDL source to **Simulation Only**. Click Next

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	Index	Name	Library	HDL Source For	Location	
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Lab 4

Step 6 – At this time we do not want to add any constraints files. Click Next.



Step 7 – Select the Arty Z7-20 and click Next.

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Step 8 – On the project summary tab, select Finish.



Step 9 – This will open Vivado in the project manager view.



Step 10 – Expand the Simulation Sources.



Step 11 – This will show the test bench and the design source to be simulated.



Step 12 – Double clicking on the VHDL files will open the source for inspection.



Step 13 – To run a simulation, click on Run Simulation and select Run Behavioral Simulation.



Step 14 – This will open the behavioral simulation view. Note the scope and objects.

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Step 15 – Click on the **Untitled* tab** to see the waveform of the simulation. Note this view shows the signals defined within the test bench only, not the Unit Under Test.

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Step 16 – At the moment, the results are in hexadecimal but they make more sense in decimal. Select all the signals, right click, and select **unsigned decimal** from the **radix**.

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Lab 4

Step 17 – This will change the results to decimal. Correct operation has result showing 118 then 96. This is the block average of 16 input values.

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Step 18 – Often we want to be able to see the signals in the UUT. To do this, first let's insert a divider. Right click on the **bottom signal** and select **New Divider**.

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Step 19 – When prompted, enter the name **UUT** and you will see the new divider in the waveform.

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Step 20 – To add in the UUT, right click on the **UUT** under the scope and select **Add to Wave Window**.



Step 21 – This will add in the UUT signals, however, some information may be missing as it was not saved during the simulation.



Step 22 – To add in the missing waveform, we need to restart the simulation. Select **Restart** from menu bar.



Step 23 – This will clear all waveform data and restart the simulation.

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Step 24 – To rerun the simulation, select the **Run button** on the menu. The simulation will stop automatically.

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Step 25 – When the simulation completes, you will see the highlighted line in the test bench.

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Open block Design	🛿 read 1	69 O wait until rising_edge(clk);	
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		76 end loop; 77 O wait until rising edge(valid);	
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			>
✓ PROGRAM AND DEBUG ▼ Type a Tcl command here			
			Sim Time: 625 ns

Step 26 – Selecting the waveform tab again will show all the signals for the UUT.

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Step 27 – If you make changes to the source code, you need to relaunch the simulation. This can be achieved using the relaunch button on the menu.

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Step 28 – With the simulation complete, we are now ready to implement the design. Close the **simulation view**.

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	🛆 \$finish called at time	: 625 ns : File "	C:/hdl_projects/01	_Vivado/	01_Vi	ivado.srcs/sim_1/imports/	′01_Vivado/a	verage_tb.vhd" Line 79	
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✓ PROGRAM AND DEBUG	Type a Tcl command here								

Step 29 – When asked to confirm, click OK. If a save waveform dialog pops up, select Discard.




Step 30 – To synthesize the design, click the green run arrow and select Run Synthesis.



Step 31 – On the Launch Runs dialog, select the number of jobs you want to run on your system and click **OK**.



Step 32 – When synthesis is complete, you will see a dialog box appear.

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Step 33 – Select Open Synthesized Design.



Step 34 – This will open the synthesis view. From the menu layout, select I/O Planning.



Step 35 – Expand the **Data_In, Result and Scalar Ports** and assign them to pins. All EXCEPT the clock pin can be assigned to any pin.

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Step 36 – Assign the clock pin to L16. Clocks have to be assigned to clock capable pins.

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> 🙋 result (12)	OUT							35	default (LVCMOS18)	•	1.800		12	~	
🗸 🗟 Scalar por	ts (5)														
🕑 clk	IN				L16	~		35	default (LVCMOS18)	٠	1.800				
🕑 empty	IN				H15	~	✓	35	default (LVCMOS18)	۳	1.800				
🕢 read	OUT				H16	~		35	default (LVCMOS18)	•	1.800		12	\checkmark	
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Step 37 – Ensure the **IO Standard** is set to **LVCMOS18.** Do not leave it as default because this will lead to a failure to implement and generate a bitstream.

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Q ¥ ♦ [K + N													\$
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🕢 read	OUT				H16	\checkmark		35	LVCMOS18	· 1.	300	2	~	
— .							C)							

Step 38 – Save the Constraints we just edited.

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Step 39 – This will present two new dialogs. Click **OK** on the first and enter a **file name** for the second.



Step 40 – Close the Synthesis View.

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	Name: data_in[7]	U								
V SYNTHESIS	Direction: IN	w			+000					
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Report Methodology	V 🍓 data_in (8) 🛛 IN			V	(Multi	ple) default (LVCMOS18)	÷ 1.800)		NONE
Report DBC	▷ data_in[7] IN		A16 💉	/ 🗸		35 default (LVCM0S18)	▼ 1.800)		NONE
Report Noise	data_in[6] IN		A17 N	/ 🖌		35 default (LVCMOS18)	• 1.800			NONE
Report Utilization	Adata in[4] IN		A10 A19			35 default (LVCM0S18)	 1.800 1.800)		NONE
	data_in[3] IN		A21			35 default (LVCM0S18)	• 1.800)		NONE
Keport Power	data_in[2] IN		A22	/ 🖌		35 default (LVCMOS18)	▼ 1.800)		NONE
🖪 Schematic	Auto (1973) (8)		401	~		10 Hofe (NON0010)	1.000			
•										

Step 41 – Confirm the decision to close by clicking **OK**. This will take us back to the project manager view.



Step 42 – We are now ready to Run Implementation.



Step 43 – Click Yes when the Synthesis Out-of-Date dialog pops up.



Lab 4

Step 44 – Select OK on the Lunch Runs dialog.

Launcl	n Runs 😣
Launch the selected synthesis or impl	ementation runs.
Launch <u>d</u> irectory: 🕞 <default laun<="" th=""><th>ch Directory> 🗸 🗸</th></default>	ch Directory> 🗸 🗸
Options	
• Launch runs on local host:	Number of jobs: 12 🗸
O Launch <u>r</u> uns on remote hosts	Configure <u>H</u> osts
◯ Launch run <u>s</u> on Cluster	lsf 🗸
◯ <u>G</u> enerate scripts only	
Don't show this dialog again	OK Cancel

Step 45 – When the implementation completes, you will see a dialog appear. Select **Generate Bitstream**.



Step 46 – A dialog box will appear when the bitstream generates. Congratulations you have completed your first Vivado FPGA implementation.



Step 1 – Open the project created in part one.



Step 2 – This will open in project management view. Click on Create Block Diagram.



Step 3 – Leave the predefined name and locations unchanged and click OK.

Сгеа	ate Block Design	8
Please specify name	of block design.	A
<u>D</u> esign name:	design_1	
D <u>i</u> rectory:	ፍ <local project="" to=""></local>	~
Specify source set:	🗅 Design Sources	~
?	ок	Cancel

Step 4 – Undock the block diagram window and maximize it.



Step 5 – We are going to add in new IP. Click on the **+ button**.



Lab 5

Step 6 – Select the FIFO Generator. This will add a FIFO to the block diagram.

~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~		
	[]	
	Search: O-I	
	# CIC Compiler	
	Clocking Wizerd	
	Clock Verification IP	
	Color Correction Matrix	
	Color Filter Array Interpolation	
	Complex Multiplier	
	* Concat	
	Constant	
	Convolution Encoder	
	* CORDIC	
	DDS Compiler	
	Debug Bridge	
	DFX AXI Shutdown Manager	
	DFX Bitstream Monitor	
	DFX Controller	
	DFX Decoupler	
	Discrete Fourier Transform This design is empty. Pres	s the 🕂 button to add IP
	Distributed Memory Generator	
	Divider Generator	
	DSP48 Macro	
	TE DUC/DDC Compiler	
	IF ECC	
	Fast Fourier Transform	
	FIFO Generator	
	EIR Compiler	
	Fixed Interval Timer	
	Floating-point	
	F Gamma Correction	
	👎 Gamma LUT	
	👎 Gmii to Ramii	
	₱ I2C Bus Master Controller	
	12S Receiver	
	🜻 I2S Transmitter	
	🜻 ILA (Integrated Logic Analyzer)	
	👎 Image Enhancement	
	ENTER to select, ESC to cancel, Ctrl+Q for IP details	

Step 7 – Double click on the FIFO Generator to customize it.



Step 8 – Leave the first page unchanged.

Documentation 🕒 IP Location							
] Show disabled ports	Component Name fifo_generator_0						
	Basic Native Ports Status Flags Data Co	ounts Summary					
	Interface Type						
	Native O AXI Memory Mapped O AXI Stream	am					
	Fifo Implementation Common Clock Block RAM	~					
	FIEO Implementation Options						
	Supported Features	Momony					
		Type	(1)	(2)	(3)	(4)	(5)
	Common Clock (CLK)	Block RAM	✓	. ✓		✓	✓
FIFO_WRITE	Common Clock (CLK)	Distributed RAM		√			
	Common Clock (CLK)	Shift Register					
	Common Clock (CLK)	Built-In FIFO		¥	4	4	4
	Independent Clocks (RD_CLK, WR_CLK)	Distributed RAM	V	4		Ý	Ý
	Independent Clocks (RD_CLK, WR_CLK)	Built-in FIEO		1	1	1	1
	(1) Non-symmetric aspect ratios (different read	and write data widths)					
or et	(2) First-Word Fall-Through	and write data watrisy					
SISC	(3) Uses Built-in EIEO primitives						
	(4) ECC support						
	(4) Ecc support (5) Dynamic Error Injection						
	(5) Dynamic Erfor Injection						

Step 9 – Change the Write and Read Width to be **8 bits**.

) Documentation 🛛 🖨 IP Location	
Show disabled ports	Component Name fifo_generator_0
	Basic Native Ports Status Flags Data Counts Summary
	Standard FIF0 First Word Fall Through
	Write Width 8 © 1,2,3 1024
	Write Depth: 1024
	Read Width 8 🗸
📕 🕂 FIFO WRITE	Read Depth 1024 Actual Read Depth: 1024
EIFO BEAD	ECC, Output Register and Power Gating Options
clk	ECC V Single Bit Error Injection Double Bit Error Injection
	ECC Pipeline Reg Dynamic Power Gating
	Output Registers
	Initialization
	Reset Pin
	Reset Type Synchronous Reset 🗸
	Full Flags Reset Value 0 V
	Dout Reset Value 0 0 (Hex)
	Read Latency : 1

Step 10 – Leave the third page unchanged.

Documentation 📄 IP Location									
Show disabled ports	Component Name [fifo_generator_0								
	Basic Native Ports Status Flags Data Counts Summary								
	Optional Flags								
	Almost Full Flag 🔲 Almost Empty Flag								
	Handshaking Options								
	Write Port Handshaking								
	□ Write Acknowledge Active High ✓ □ Overflow Active High ✓								
	Pead Port Handshaking								
📕 🕂 FIFO WRITE									
	Programmable Flags								
	Programmable Full Type No Programmable Full Threshold 🗸								
	Full Threshold Assert Value [4 - 1022]								
	Full Threshold Negate Value 1021 [3 - 1021]								
	Programmable Empty Type No Programmable Empty Threshold V								
	Empty Threshold Assert Value 2 [2 - 1020]								
	Empty Threshold Negate Value 3 [3 - 1021]								

64

Step 11 – Leave the fourth page unchanged.

cumentation 🛛 🕞 IP Location		
Show disabled ports	Component Name fifo_generator_0	
	Basic Native Ports Status Flags Data Counts Summary	
	Data Count Options	
	More Accurate Data Counts	
	Data Count	
	Data Count Width 10 [1 - 10]	
	Write Data Count (Synchronized with Write Clk)	
	Write Data Count Width 10 [1 - 10]	
	Read Data Count (Synchronized with Read Clk)	
+ FIFO_WRITE	Read Data Count Width [1 - 10]	
FIFO_READ		
clk		

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Step 12 – Leave the final page unchanged. Note that the FIFO OP are unregistered. Click OK.

ow disabled ports	<pre>w disabled ports Component Name ffg_generator_0 Basic Native Ports Status Flags Data Counts Summary Block RAM resource(s) (18K BRAMs): 1 Block RAM resource(s) (18K BRAMs): 0 Cocking Scheme Common Clock Model Generated Behavioral Model Write Width Behavioral Model Write Width Behavioral Model Programmable FullEmpty Flags Not Selected/Not Selected Programmable FullEmpty Flags Not Selected Not Selected Not Selected Read Mode / Reset Standard FIF/ Not Selected Read Note / Reset Standard FIF/ Not Select</pre>
Basic Native Ports Status Flags Data Counts Summary Biock RAM resource(s) (18K BRAMs): 1 Biock RAM resource(s) (36K BRAMs): 0 Common Clock Biock RAM Clocking Scheme Common Clock Biock RAM Biock RAM Model Generated Behavioral Model Behavioral Model Write Depth 1024 Bead Read Width 8 Bead Read Width 8 Not Selected/Not Selected Programable Full/Empty Flags Not Selected/Not Selected Read Latency (From Rising Edge of Read Clock) 1	Basic Native Ports Status Flags Data Counts Summary Block RAM resource(s) (16K BRAMs): 1 Block RAM resource(s) (36K BRAMs): 0
Block RAM resource(s) (18K BRAMs): 1 Block RAM resource(s) (36K BRAMs): 0 Clocking Scheme Common Clock Memory Type Block RAM Model Generated Behavioral Model Write Depth 1024 Read Writh 8 Read Depth 1024 Almost Full/Empty Flags Not Selected/Not Selected Programmable Full/Empty Flags Not Selected/INOT Selected Handshafug Not Selected M Read Mode / Reset Standard FIFO / Not Selected Handshafug Also Selected M Read Latency (From Rising Edge of Read Clock) 1 Herein Clock	Block RAM resource(s) (18K BRAMs): 1 Block RAM resource(s) (36K BRAMs): 0 Clocking scheme Common Clock Memory Type Block RAM Model Generated Behavioral Model Write Width 8 Memory Type Read Width 8 Read Depth 1024 Almost Full/Empty Flags Not Selected/Not Selected Programmable Full/Empty Flags Not Selected/Not Selected Data Count Outputs Not Selected Handshaking Not Selected Handshaking Not Selected Read Latency (From Rising Edge of Read Clock) 1 Hered Model Clock Clock 1 Clock RAM
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Model Generated Behavioral Model Write With With With Behavioral Model Write Udth Read With Read Udth Read Depth 1024 Read Depth 1024 Almost Full/Empty Flags Not Selected/Not Selected Programmable Full/Empty Flags Not Selected/Not Selected Data Count Outputs Not Selected Handshakug Read Mode / Reset Read Latency (From Rising Edge of Read Clock) 1	Model Generated Behavioral Model Write Width 9 Write Udth 9 Read Width 8 Read Depth 1024 Almost Full/Empty Flags Not Selected/Not Selected Programmable Full/Empty Flags Not Selected Mot Selected Data Count Outputs Not Selected Handshaking Not Selected Read Mode / Reset Standard FIFO / Not Selected Read Latency (From Rising Edge of Read Clock) 1
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White Depth 1024 Read Width 8 Read Depth 1024 Almost Full/Empty Flags Not Selected/Not Selected Data Court Outputs Not Selected Handshaking Not Selected Read Mode / Reset Standard FIFO / Not Selected Read Latency (From Rising Edge of Read Clock) 1	Image: Write Depth 1024 Read Width 8 Read Depth 1024 Almost FullEmpty Flags Not Selected/Not Selected Data Count Outputs Not Selected Handshaking Not Selected Read Mode / Reset Standard FIFO / Not Selected Read Mode / Reset Standard FIFO / Not Selected Read Latency (From Rising Edge of Read Clock) 1
Read Depth 1024 Read Depth 1024 Almost Full/Empty Flags Not Selected/Not Selected Programmable Full/Empty Flags Not Selected Data Court Outputs Not Selected Handshaking Not Selected Read Mode / Reset Standard FIFO / Not Selected Read Latency (From Rising Edge of Read Clock) 1 Clk	Image: Note Selected Note S
Almost Full/Empty Flags Not Selected/Not Selected Programmable Full/Empty Flags Not Selected Not Selected Data Court Outputs Not Selected Handshaking Not Selected Read Mode / Reset Read Latency (From Rising Edge of Read Clock) 1 I	Almost Full/Empty Flags Not Selected/Not Selected Programmable Full/Empty Flags Not Selected/Not Selected Data Count Outputs Not Selected Handshaking Not Selected Read Modey Asset Read Modey Asset Read Latency (From Rising Edge of Read Clock) 1
Programmable Full/Empty Flags Not Selected Data Court Dyuts Not Selected Handshaking Not Selected Read Mode / Reset Standard FIFO / Not Selected Read Mode / Reset Standard FIFO / Not Selected Read Latency (From Rising Edge of Read Clock) 1	Image: Programmable Full/Empty Flags Not Selected/Not Selected Data Count Outputs Not Selected Handshaking Not Selected Read Mode / Reset Standard FIFO / Not Selected Read Latency (From Rising Edge of Read Clock) 1
Data Court Outputs Not Selected Handshaking Not Selected Read Mode / Reset Standard FIFO / Not Selected Read Mode / Reset Standard FIFO / Not Selected Read Latency (From Rising Edge of Read Clock) 1	Data Count Outputs Not Selected Handshaking Not Selected Read Mode / Reset Standard FIFO / Not Selected Read Latency (From Rising Edge of Read Clock) 1
Handshaking Not Selected Read Mode / Reset Head Mode / Reset Read Mode / Reset Read Latency (From Rising Edge of Read Clock) 1 Not Selected Read Mode / Reset Read Latency (From Rising Edge of Read Clock) 1	Handshaking Not Selected Read Mader (Reset) Read Mader (Reset) Read Latency (From Rising Edge of Read Clock) I Not Selected Standard FIFO / Not Selected Read Latency (From Rising Edge of Read Clock) I
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+ FIFO_READ clk	+ FIFO_READ - clk
	clk

Lab 5

Lab 5: Intermediate Vivado

Step 13 – Click back on the Vivado Project Management view you will see the block diagram under the design sources.



Step 14 – Right click on the average RTL block and select Add Module to Block Design.



Step 15 – This will add the average block to the block diagram.



Lab 5

Step 16 – Expand the FIFO Write and Read Interfaces.



Step 17 – Make the Clk, Reset, Result, Valid and FIFO Write interfaces external by right-clicking on each pin and selecting **Make External**. Connect the remaining interfaces as below.



Step 18 – Click on Validate Design.



Lab 5
Step 19 – The validated design should result in no error or critical warnings. Click OK.



Step 20 – Re-dock the block diagram window into the Vivado Project Manager.



Lab 5

Lab 5: Intermediate Vivado

Step 21 – Click on the Zoom Fit button to fit the design to the window.



Lab 5: Intermediate Vivado

Step 22 – Right click on the block diagram design under the Design Sources tab and select **Create HDL Wrapper**.



Step 23 – Allow Vivado to manage the wrapper and click OK.



Step 24 – Expand the newly created wrapper and you will see the entire design.



Step 25 – Run the Synthesis.



Step 26 – On both resultant dialogs click OK and wait for synthesis to complete.



Step 27 – When synthesis completes, Open the Synthesized Design.



Step 28 – If any critical warnings pop up, select **OK.** This is due to out of data constraints which we are about to address.



Lab 5: Intermediate Vivado

Step 29 – Change the I/O standard from default to LVCMOS18.

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	🗁 0.75V			E				C					
IP INTEGRATOR	🗁 0.9V		~	бн		8		+ + +					
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Open Block Design	VREF.			K L			• • •	SS					
Generate Block Design	I/O Port Interface Properties ×	Clock Regions ?	_ 🗆 🖾	M N P				+ + + +					
	B FIFO_WRITE_0_54576	+	⇒ 🗘	T									
Run Simulation	Name: FIFO_WRITE_0_5	4576 🛞	^	v w									
✓ RTL ANALYSIS	General I/O Ports								HSTL_I	~			
> Open Elaborated Design	Tcl Console Messages Log	Reports Design Runs	Package Pi	ins I/O Ports ×					HSTL_II				? _ □ □
	Q <u>∓</u> ≑ <u>∎</u> + <u></u>							г	HSTL_I_18				0
✓ SYNTHESIS	Name	Direction B	loard Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	ank	HSUL_12	Vce	Vref	Drive Strength	Slew
Run Synthesis	✓ ➡ All ports (25)								LVCMOS12				
 Open Synthesized Design 	> Tai CLK.CLK_0_54576 (1)	IN							LVCMOS15	- 1.8	0		
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Step 30 – Assign the clock input to pin L16. Assign all other IO to pins of your choice.

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Step 31 – Click on Save Constraints.

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Lab 5

Step 32 – If an out-of-date warning appears, click OK.



Step 33 – From the sources tab, open the **IO constraints.** You will see the old pin out for the previous project and your new project. This is because we have evolved the original project.

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Step 34 – Select the old constraints (at the top of the file) and delete them. Save the file.

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Step 35 – Run the Implementation, Re run synthesis if you get an out of date warning

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 > Open Elaborated Design SYNTHESIS > Run Synthesis > Open Synthesized Design Constraints Wizard Edit Timing Constraints Edit Timing Constraints 	Tcl Console Messages Log Q X Image: Console Messages Log Name Image: Console Messages Image: Console Messages Image: Console Messages Image: Console Messages Log Image: Console Messages Image: Console Messages Log Messages Messages Log Messages Messages Log Log Log Log Log Log Log Log <thlog< th=""> Log<!--</td--><td>Reports Design Ri Direction IN IN (Multiple)</td><td>Board Part Pin</td><td>Board Part Interface</td><td>Neg Diff Pair</td><td>Package Pin L16 V</td><td>Fixed v</td><td>Bank 35 35 35</td><td>I/O Std LVCMOS18 LVCMOS18 LVCMOS18</td><td>•</td><td>Vcco Vret 1.800 - 1.800 - 1.800 -</td><td>f Drive Strength</td><td>Sle</td></thlog<>	Reports Design Ri Direction IN IN (Multiple)	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin L16 V	Fixed v	Bank 35 35 35	I/O Std LVCMOS18 LVCMOS18 LVCMOS18	•	Vcco Vret 1.800 - 1.800 - 1.800 -	f Drive Strength	Sle
 > Open Elaborated Design SYNTHESIS Run Synthesis Open Synthesized Design Constraints Wizard Edit Timing Constraints & Set Up Debug 	Tcl Console Messages Log Q X Image: Console Messages Log Name Image: Console Image: Co	Reports Design Ri	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin L16 V	Fixed V V V	Bank 35 35 35 35	I/O Std LVCMOS18 LVCMOS18 LVCMOS18 LVCMOS18	•	Vcco Vret 1.800 1.800 1.800 1.800	f Drive Strength	Sle
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Step 36 – Click **OK** to run the implementation.

Launc	h Runs 😣
Launch the selected synthesis or impl	ementation runs.
Launch <u>d</u> irectory: 📮 <default laun<="" th=""><th>ch Directory></th></default>	ch Directory>
Options	
<u>Launch runs on local host:</u>	Number of jobs: 12 🗸 🗸
O Launch <u>r</u> uns on remote hosts	Configure <u>H</u> osts
O Launch run <u>s</u> on Cluster	lsf 🗸 🗸
◯ <u>G</u> enerate scripts only	
Don't show this dialog again	OK Cancel

Step 37 – Open the Block Design when design has built.



Step 38 – Select Constraints under Design Sources.



Step 39 – Click on the Add Source button.



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Step 40 – Select Add or Create Constraints. Then Create File, enter the name "timing" for the file, and click Finish.

	Add Sources 🛛 🛞	Add Sources ×
	Add Sources	Add or Create Constraints
HLx Editions	This guides you through the process of adding and creating sources for your project	Specify or create constraint files for physical and timing constraint to add to your project.
	Add or <u>c</u> reate constraints	Specify constraint set: 🕞 constrs_1 (active)
	O Add or create simulation sources	+ - +
		Constraint File Location
		io.xdc C:\hdl_projects\01_Vivado\01_Vivado.srcs\constrs_1\new
		Add Files
XILINX.		С саду солониятся ниса ребуссе
?	< Back Next > Einish Cancel	? < Back
		Add Sources X
6		Add or Create Constraints
ci		Specify or create constraint files for physical and timing constraint to add to your project.
Create a new	constraints file and add	
it to your pro		Specify constraint set: Constraint (active)
		Constraint File Location
<u>F</u> ile type:	▶ XDC V	Constraint File Location io.xdc C\hdlptrojects\01_Vivado\01_Vivado.srcs\constrs_1\new theirs de Deirate Deirate
<u>F</u> ile type: F <u>i</u> le name:	timing ⊗	Constraint File Location io.xdc C\hdl_prrojects\01_Vivado\01_Vivado.srcs\constrs_1\new timing.xdc <local project="" to=""></local>
<u>F</u> ile type: F <u>i</u> le name:	Image Image	Constraint File Location io.xdc C:\hdl_projects\01_Vivado\01_Vivado.srcs\constrs_1\new timing.xdc <local project="" to=""></local>
<u>File type:</u> F <u>i</u> le name: Fil <u>e</u> location	Iming timing Cocar to Project>	Constraint File Location ioxdc C:\hdl_projects\01_Vivado\01_Vivado.srcs\constrs_1\new timing.xdc <local project="" to=""></local>
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Eile type: File name: Fil <u>e</u> location ?	XDC timing Cancel	Constraint File Location io.xdc C\hdl_projects\01_Vivado\01_Vivado.srcs\constrs_1\new timing.xdc <local project="" to=""> Add Files Create File</local>
<u>F</u> ile type: File name: Fil <u>e</u> location ?	Iming timing Cancel	Constraints File Location io.xdc C/hdl_projects/01_Vivado.urcs/constrs_1/new timing.xdc <local project="" to=""> Add Files Create File Copy constraints files into project Create File</local>
Eile type: File name: Fil <u>e</u> location	Iming Iming Iming	Constraint File Location Locat

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Step 41 – Right click on the newly created constraint file and select Set as Target Constraints File.



Step 42 – Open the implemented design. If you see the warning below click OK.



Lab 5: Intermediate Vivado

Step 43 – From the Tools menu, select Timing -> Constraints Wizard.



Lab 5: Intermediate Vivado

Step 44 – On the welcome screen, click Next and then enter 200 MHz for the clock frequency. Once done, select Skip to Finish.

	Timing Constraints Wizard	Timing Constraints Wizard 🛛 🚳
	Identify and Recommend Missing Timing Constraints The Timing Constraints Wzard guides you through creating timing constraints per Xilinx design methodology. It analyzes your design for missing timing constraints and makes recommendations. You need to review and understand all of the recommendations to ensure they are appropriate for your design.	Primary Clocks Primary clocks usually enter the design though input ports. Specify the period and optionally a name and waveform (rising and falling degree times) to describe the duty cycle if not 50%. More info
	Clocks: • Primary Clocks • Generated Clocks • Forwarded Clocks • External Feedback Delays Input and Output Ports: • Input Delays • Output Delays	Q tba 2 tba 1 1 tba 1 </td
	Combinational Delays Combinational Delays Clock Domain Crossings: Physically Exclusive Clock Groups with No Interaction Logically Exclusive Clock Groups with Interaction Logically Exclusive Clock Groups with Interaction Asynchronous Clock Domain Crossings Clicking 'Next' on a page applies the constraints to the design in memory, so that missing constraints on subsequent pages can be identified. Each page may require considerable runtime to discover missing constraints. The Clock Networks report is available on every page to help you review the constraints. Schematics and timing nath remote are available on the Asymchronous Clock Domain Crossing page	Constraints for Pulse Width Check Only Q 100 Object 100 Period (ns) Rise At (ns) Fall At (ns) Jitter (ns)
	To leave the Wizard and automatically save the new constraints to the target XDC file, click Finish. To discard the new constraints click Cancel.	Tcl Command Preview (1) Existing Create Clock Constraints (0) Q
E XILINX.	Next > Skip to Finish >> Cancel	(?) (Skip to Finish >>) Cancel

Lab 5: Intermediate Vivado

Step 45 – On the final page, check that only one constraints is being created, check the View Timing Constraints, and click Finish.



Step 46 – Close the implementation view and rerun the implementation. Run synthesis if you get out of date pop up. Click OK on any dialogs which pop up prior to implementation starting.



Lab 5

Lab 5: Intermediate Vivado

Step 47 – Once the implementation completes, Timing will fail. Open the Implemented Design.



Step 48 – In the implemented design, select the failing Intra-Clock Paths.

<u>File Edit Flow Tools Re</u>	ep <u>o</u> rts <u>W</u> indow La <u>y</u> out <u>V</u> iew <u>H</u> elp
	X 💩 🕨 👭 🙀 🖄 🖉 🗴 X
Flow Navigator 😤 🗘 ?	- IMPLEMENTED DESIGN - xc7z020clg400-1
 KIL ANALYSIS 	^
> Open Elaborated Design	Sources Netlist ×
	중 뇌
✓ SYNTHESIS	
Run Synthesis	0].ram.r (design_1_fifo_generator_0_0_blk_mem_
 Open Synthesized Design 	(40)
Constraints Wizard	_noinit.ram (design_1_fifo_generator_0_0_blk_me
Edit Timing Constraints	Vets (41)
Zuit Inning Constituints	eat Cells (2)
🕷 Set Up Debug	CENTER SINCEMINI INFO.SDP.SIMPL
Ӧ Report Timing Summary	
Report Clock Networks	Path Properties
Report Clock Interaction	Ъ Path 1
Report Methodology	Summarv
Penort DPC	
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Report Noise	
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🗯 Report Power	Q ± ₹ ♥
Schematic	Design Timing Summary
	Clock Summary (1)
MPLEMENTATION	> The Check Timing (20)
Run Implementation	✓ G Intra-Clock Paths
 Open Implemented Design 	 GK_0 Sature -0.221 pc (10)
o pen implementen Design	• Setup -0.321 ns (10)

Step 49 – Select **Path 1** and zoom in. You will see that the FIFO output data passes through LUTs before finally being registered. This path is too long for timing at 200 MHz.



Step 50 – To fix this, we need to register the output of the FIFO. Close the implementation view and reopen the block diagram. Double click on the **FIFO** to customize.

Documentation 📮 IP Location	
Show disabled ports	Component Name fifo_generator_0
	Basic Native Ports Status Flags Data Counts Summary Read Mode • Standard EED • Eirst Word Sall Through
	Data Port Parameters Write Width 8 0 1.2.31024
	Write Depth 1024 ✓ Actual Write Depth: 1024 Read Wridth 8 ✓ Read Depth 1024 Actual Read Depth: 1024
+ FIFO_WRITE	ECC, Output Register and Power Gating Options ECC Hard ECC Single Bit Error Injection
Cik	✓ Output Registers Embedded Registers
	Reset Pin Image: Constraint of the section of the s
	Full Flags Reset Value 0 v Dout Reset Value Previous dout Value Read Latency : 2

Lab 5

Step 51 – Note the latency has changed from 1 to 2 clocks. We would need to correct for this in the average block, however, we proceed assuming that we have.

	Re-customize IP	
FO Generator (13.2)		
Documentation 🚡 IP Location		
Show disabled ports	Component Name [fifo_generator_0	
	Basic Native Ports Status Flags Data Counts Summary	
	Block RAM resource(s) (18K BRAMs): 1 Block RAM resource(s) (36K BRAMs): 0	
	Clocking Scheme Memory Type	Common Clock Block RAM
	Model Generated Write Width	Behavioral Model 8
	Write Depth Read Width	1024 8
	Read Depth Almost Full/Empty Flags	1024 Not Selected/Not Selected
	Programmable Full/Empty Flags	Not Selected/Not Selected
	Read Mode / Reset	Standard FIFO / Not Selected
	Read Latency (From Kising Edge of Read Clock)	2
H + FIFO_READ		
		OK Cance

Step 52 – Reimplement the design. When the timing is completed, you should see that the implementation is correct and the timing is met.

