Getting to Know Vivado

Course Workbook

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About this Workbook

This workbook is designed to be used in conjunction with the Getting to Know Vivado course.

The contents of this workbook are created by Adiuvo Engineering & Training, Ltd.

If you have any questions about the contents, or need assistance, please contact Adam Taylor at adam@adiuvoengineering.com.

Pre-Lab

Workshop Pre-requisites

Required Hardware

There is no required hardware for this course.

Downloads and Installations

Step 1 – Download and install the following at least one day prior to the workshop. This may take a significant amount of time and drive space.

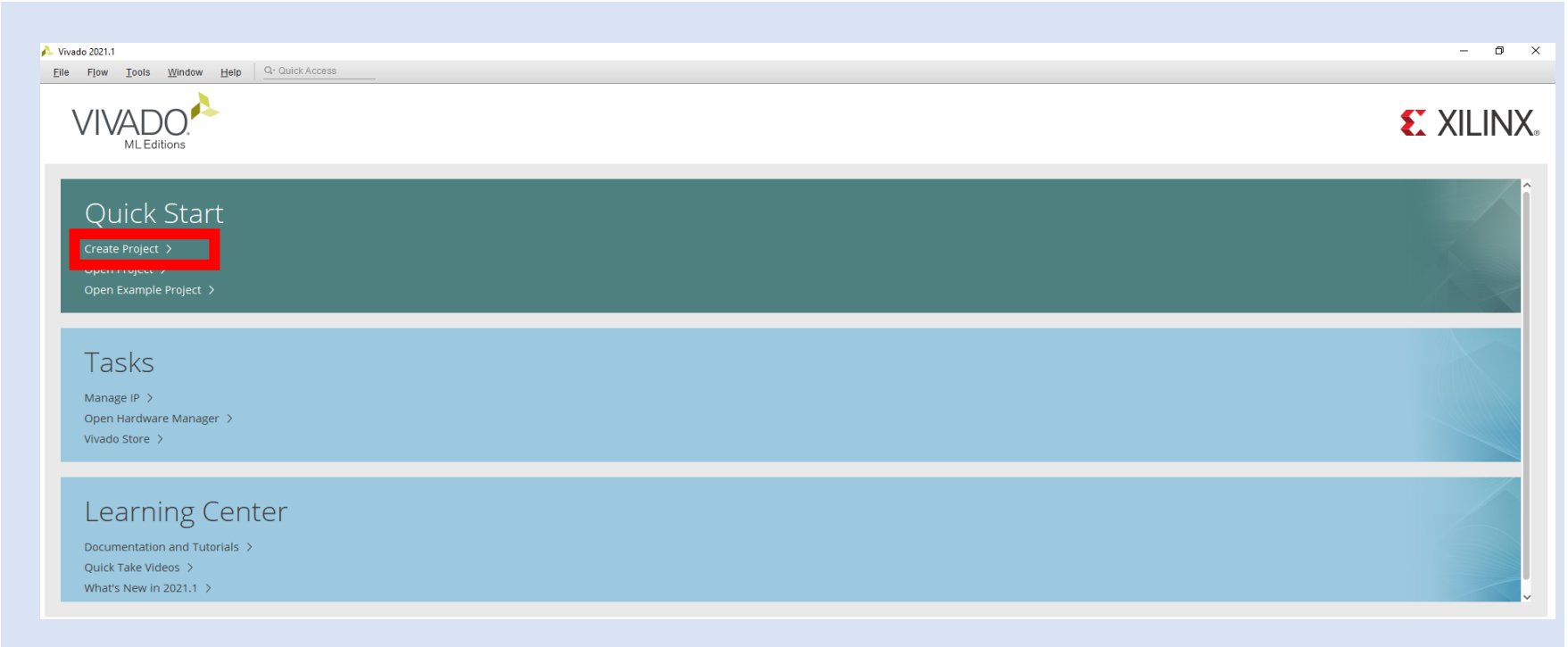
Vitis 2021.1	Download
Source Project Files	Download

Lab 4

Overview and Introduction to Vivado

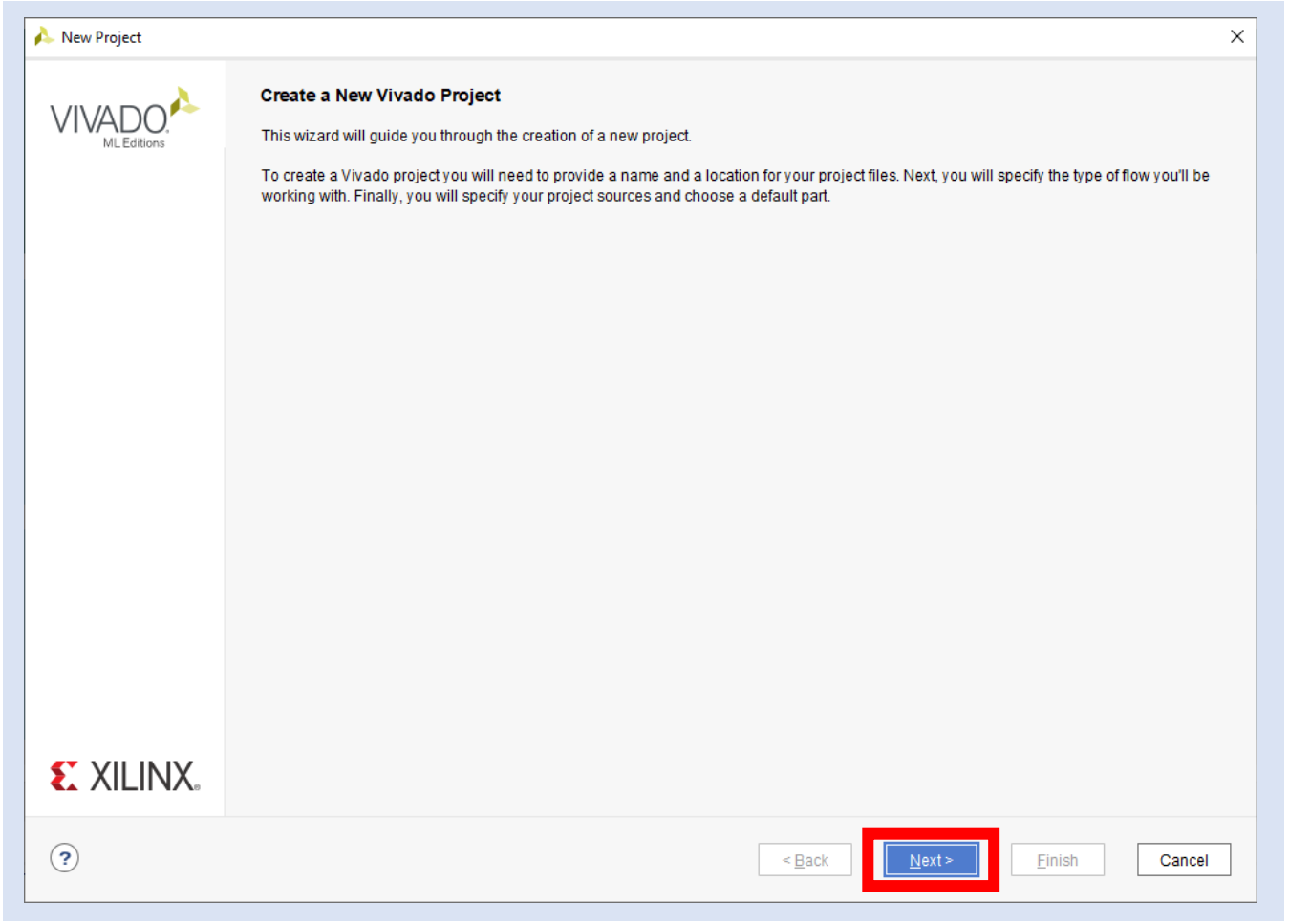
Lab 4: Overview and Introduction to Vivado

Step 1 – Open Vivado 2021.1.



Lab 4: Overview and Introduction to Vivado

Step 2 – Click on **Create Project** – This will open the New Project Wizard – Click **Next**.



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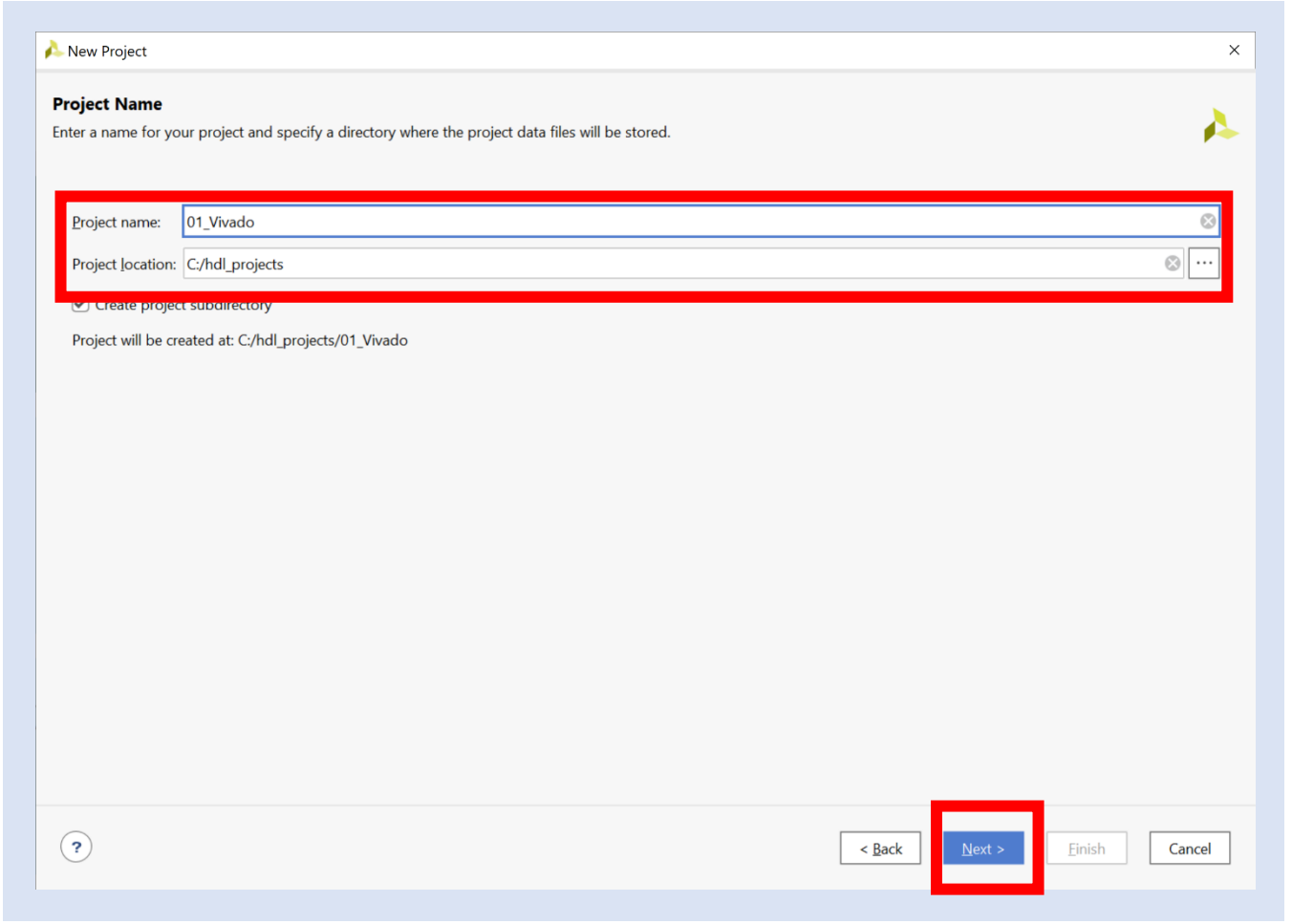
Step 3 – Enter the project name of "**01_Vivado**" and select the location you want to save the project. Click Next



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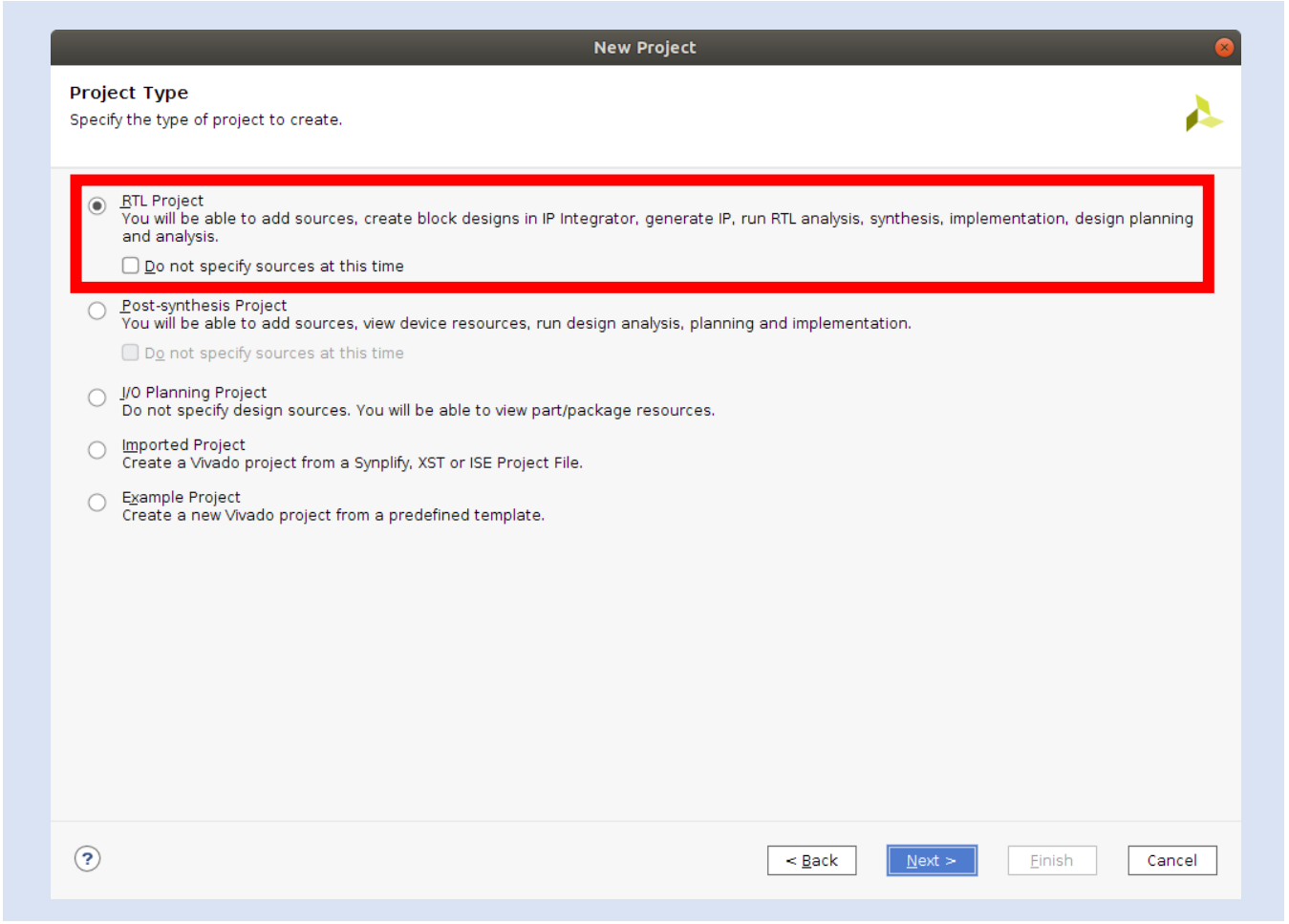
Step 4 – Select **RTL Project**. Check Do not specify sources is unticked



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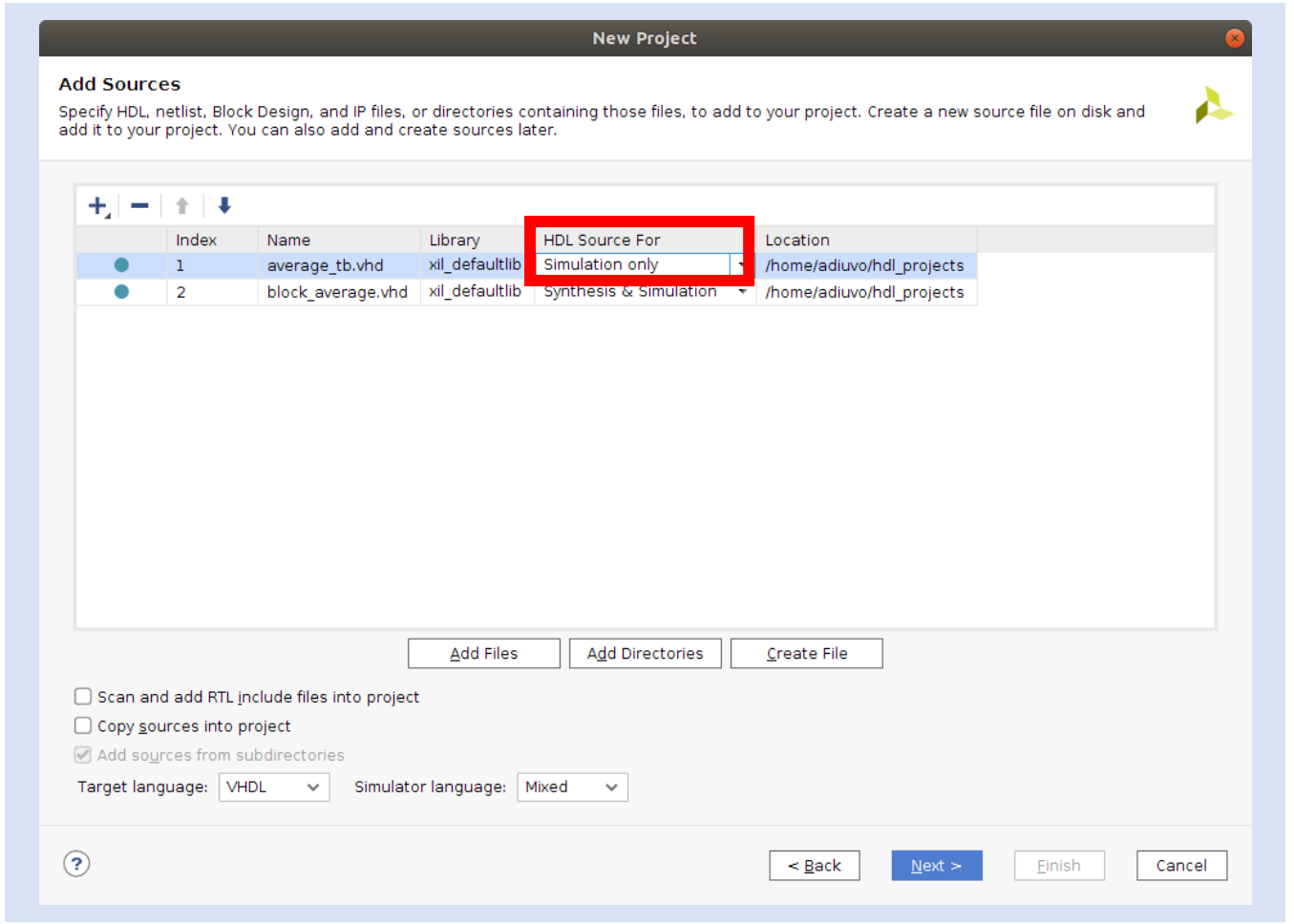
Step 5 – Click **ADD FILES** and select the two files downloaded from Github. For the file average_tb.vhd, change the HDL source to **Simulation Only**. Click Next



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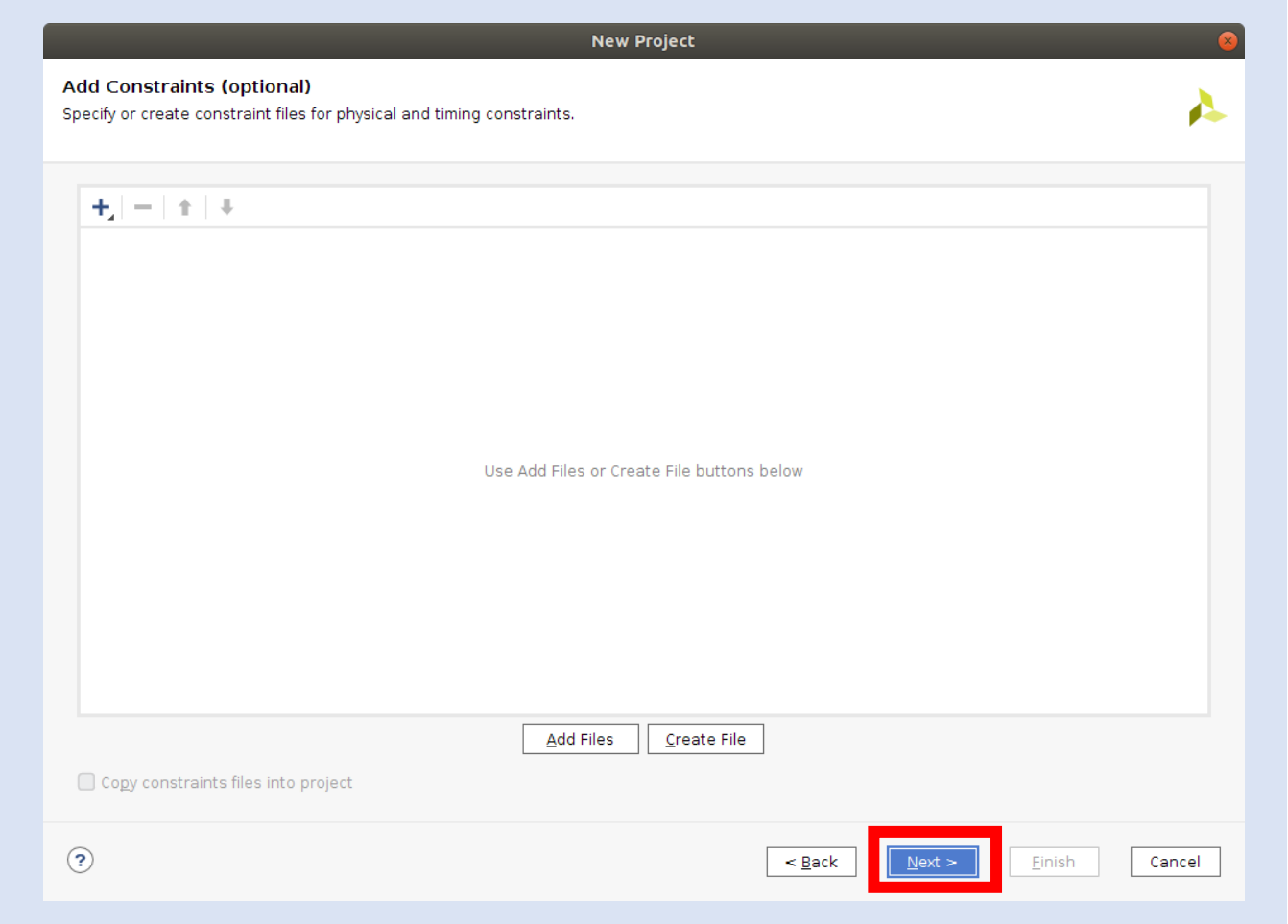
Step 6 – At this time we do not want to add any constraints files. Click **Next**.



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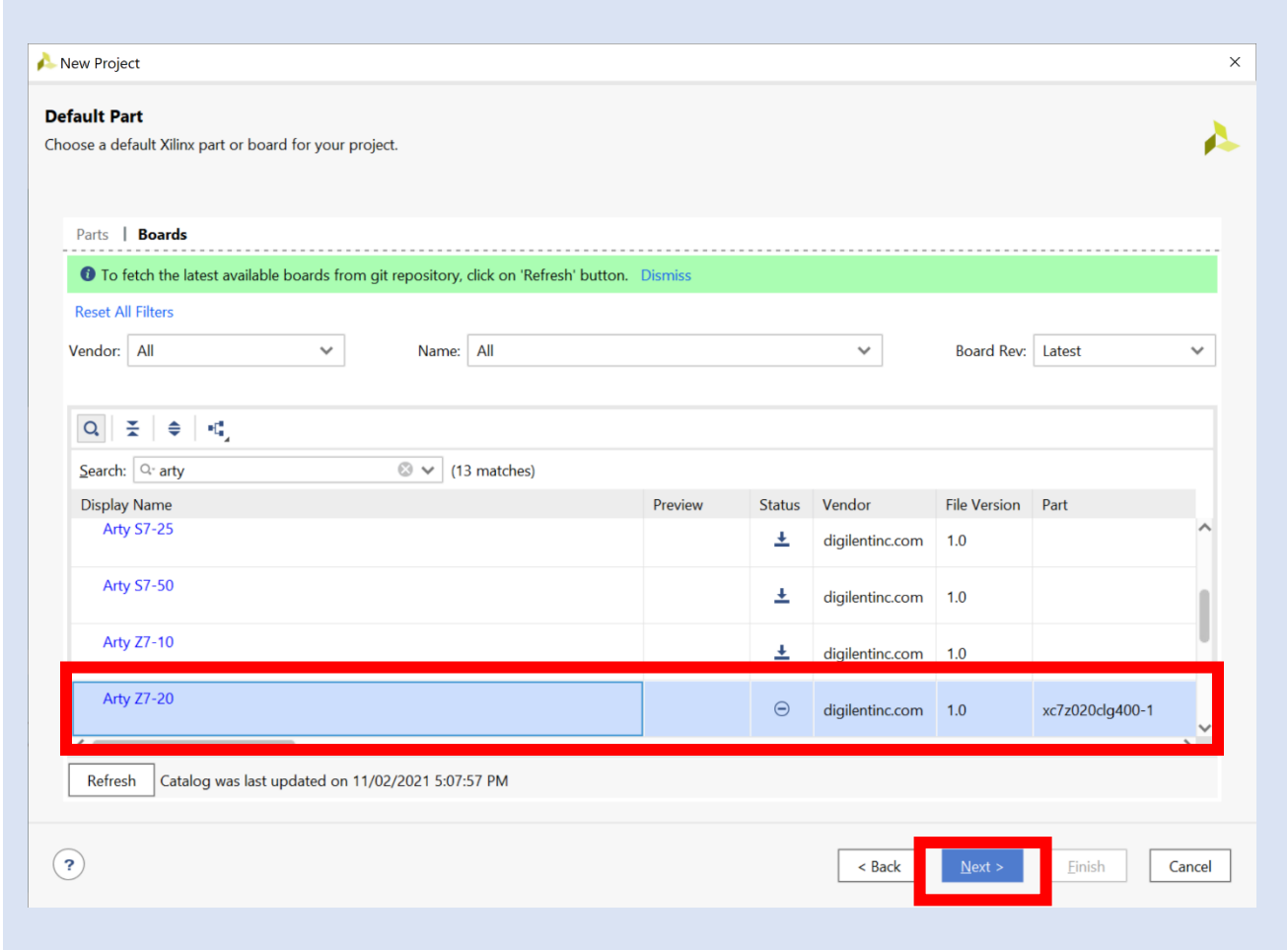
Step 7 – Select the **Arty Z7-20** and click **Next**.



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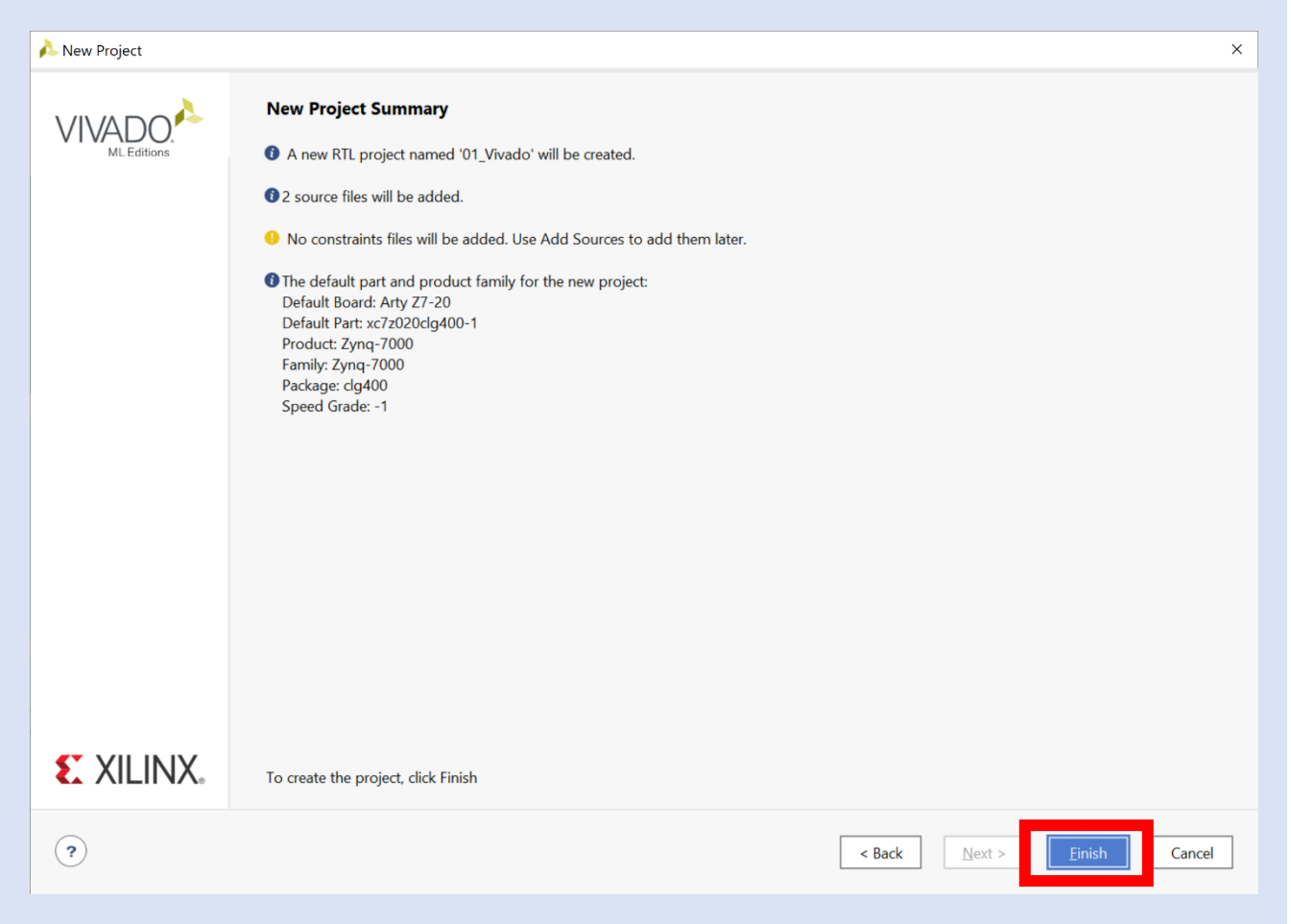
Step 8 – On the project summary tab, select **Finish**.



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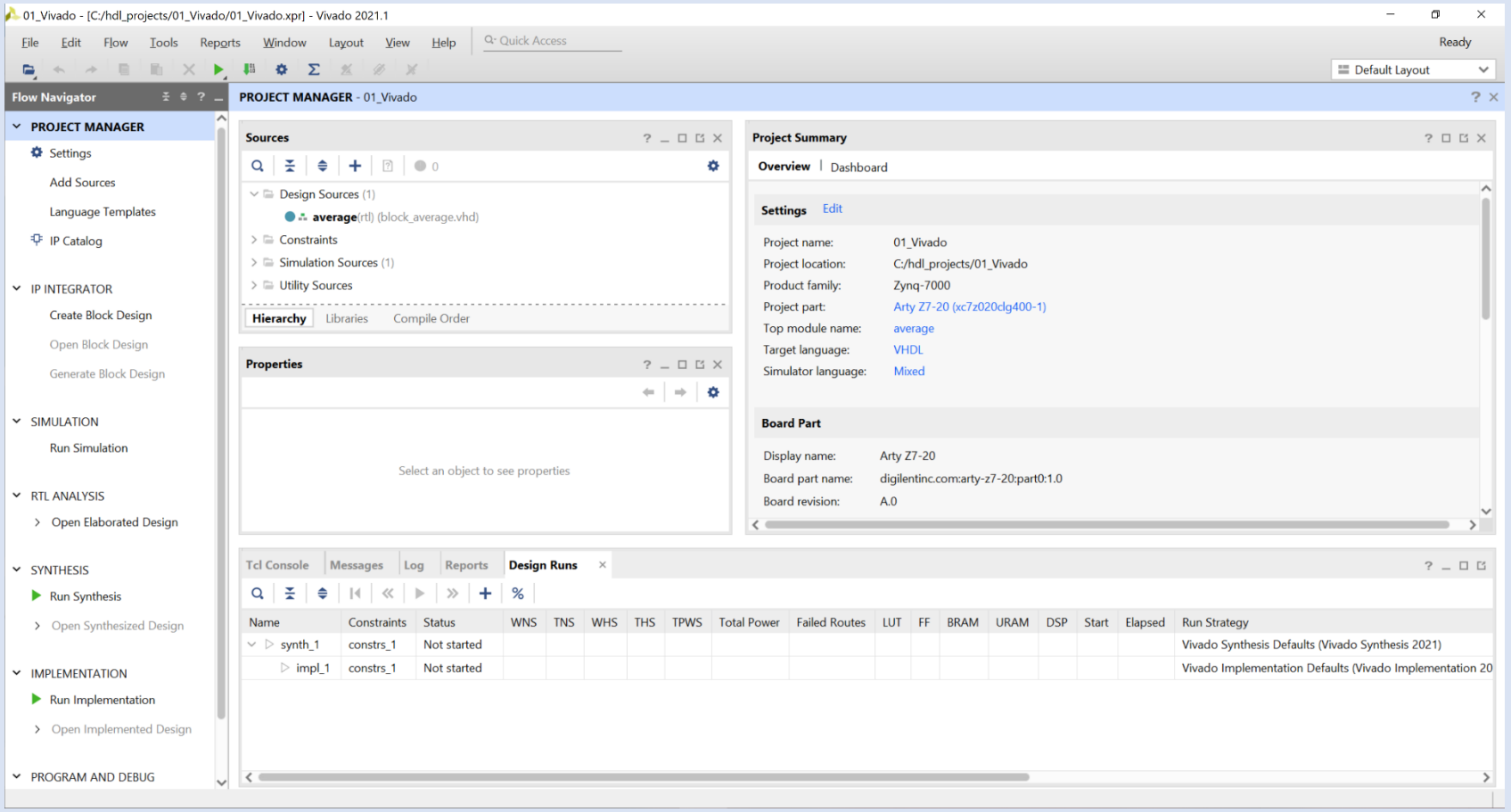
Step 9 – This will open Vivado in the project manager view.



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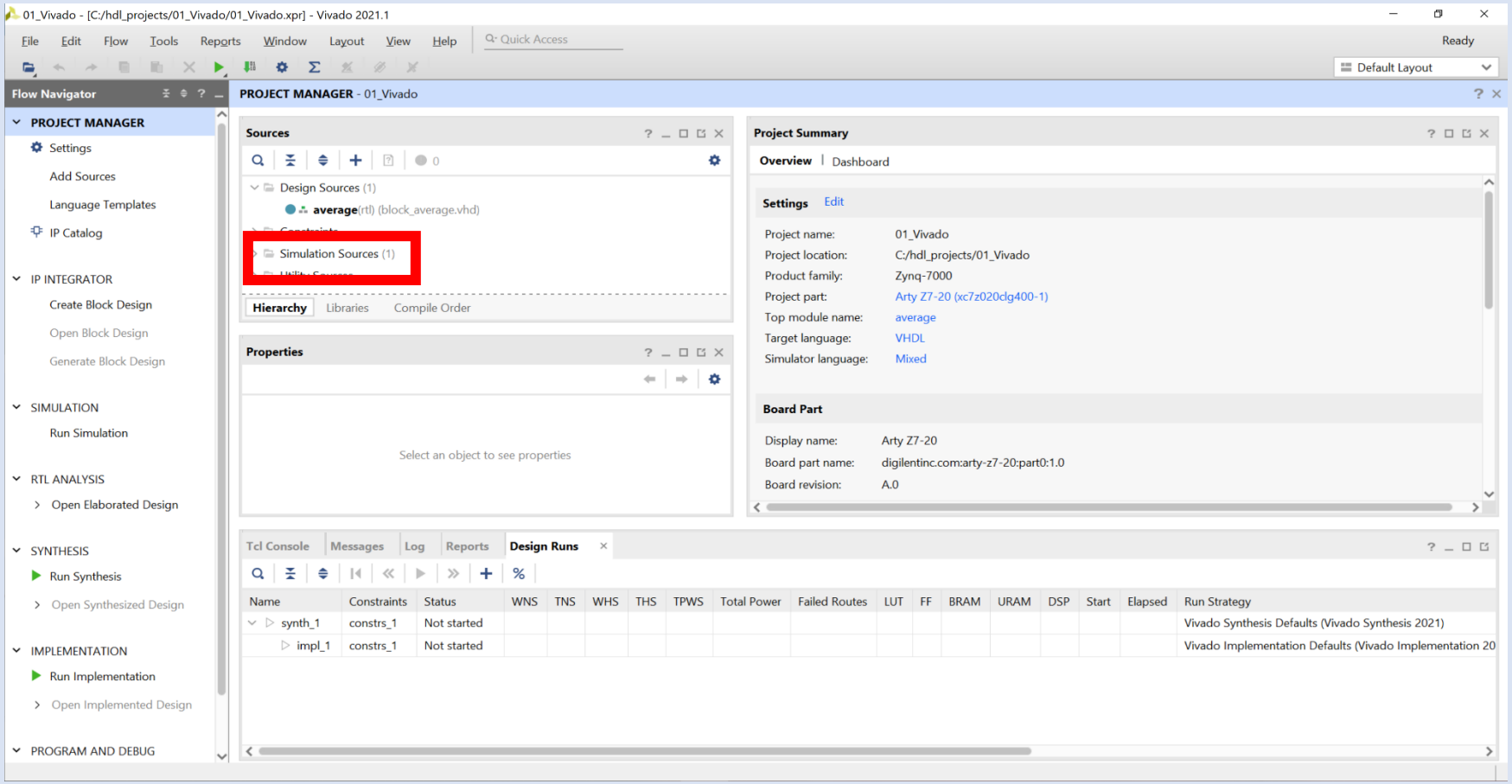
Step 10 – Expand the **Simulation Sources**.



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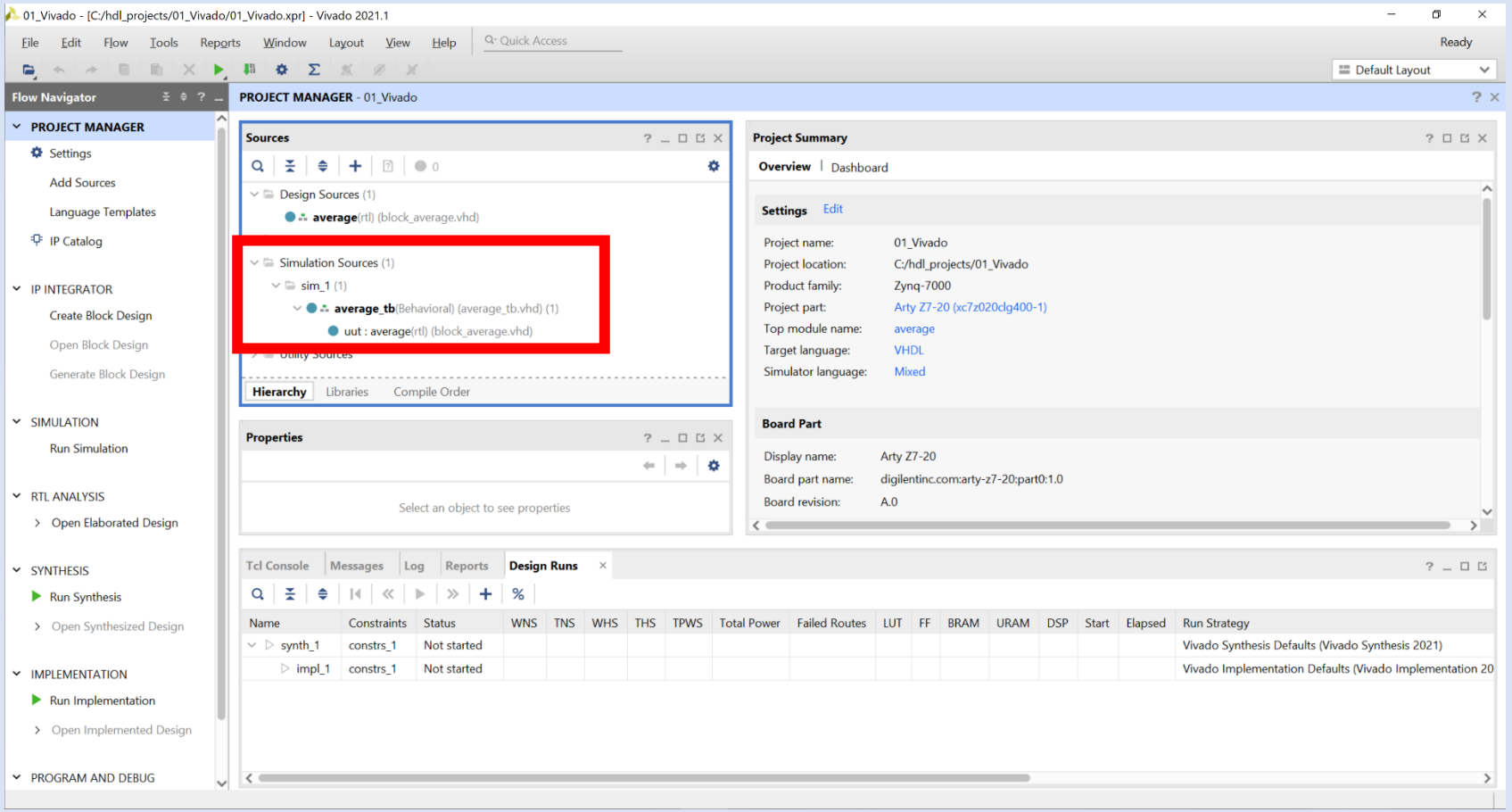
Step 11 – This will show the test bench and the design source to be simulated.



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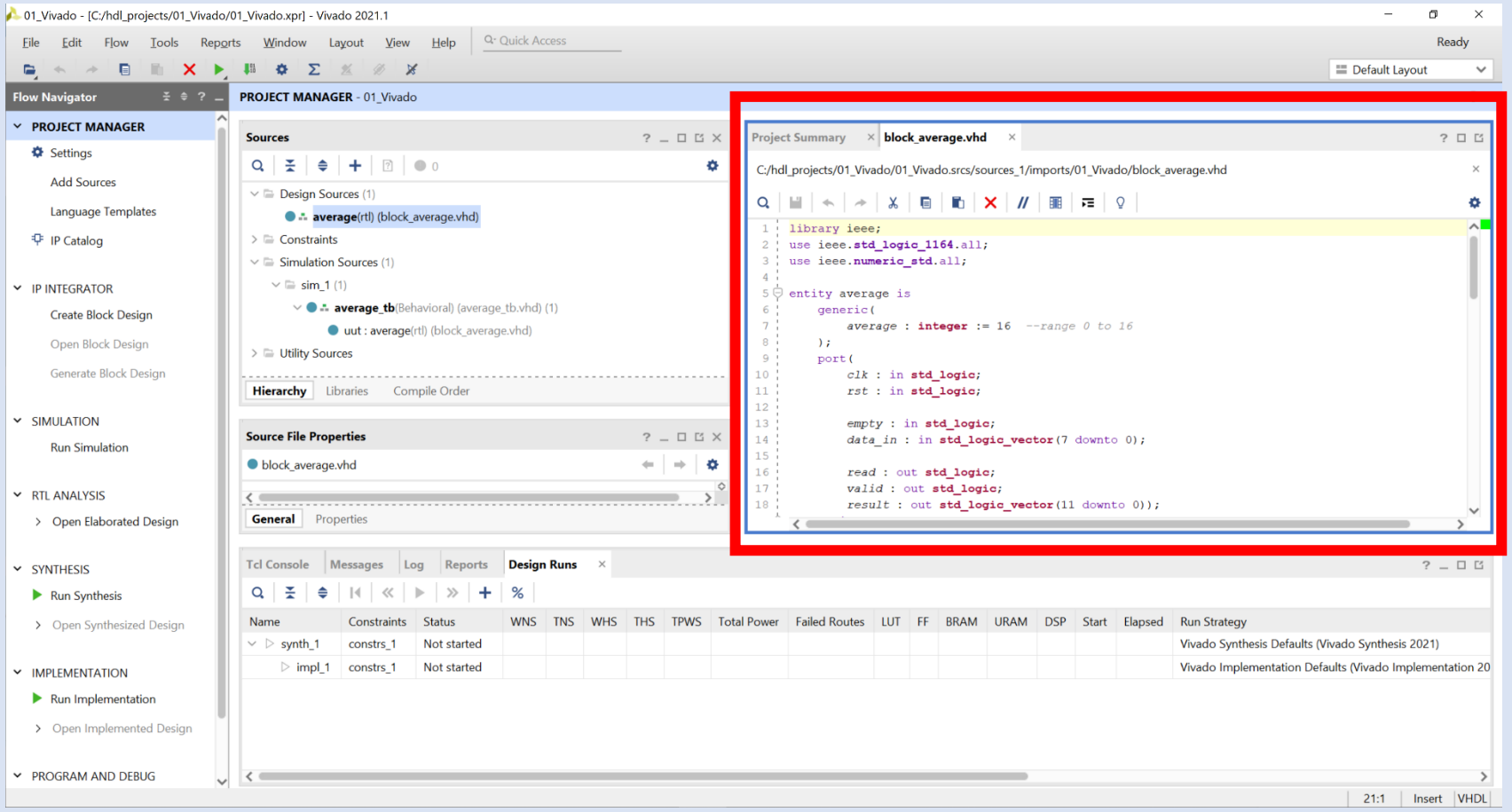
Step 12 – Double clicking on the VHDL files will open the source for inspection.



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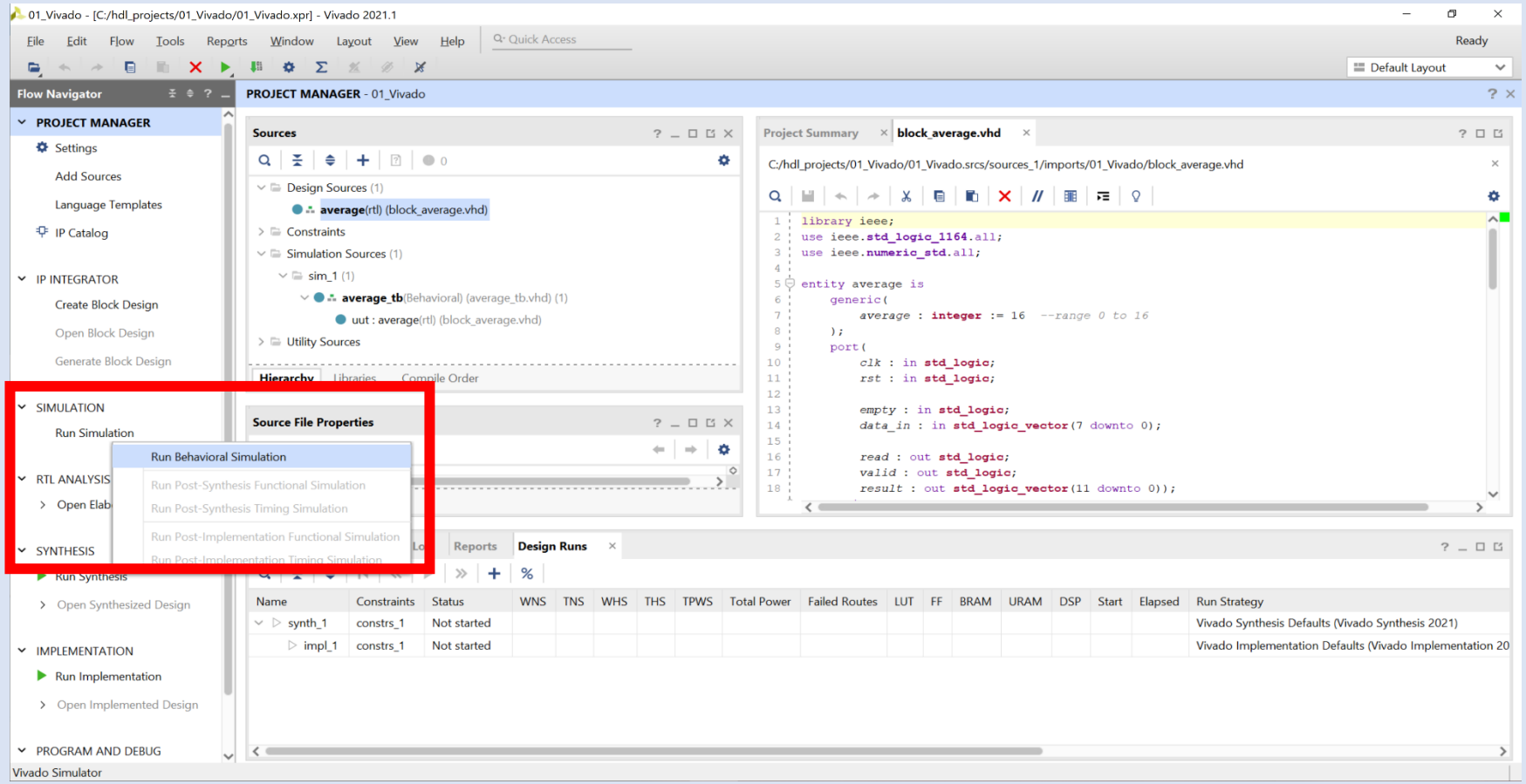
Step 13 – To run a simulation, click on **Run Simulation** and select **Run Behavioral Simulation**.



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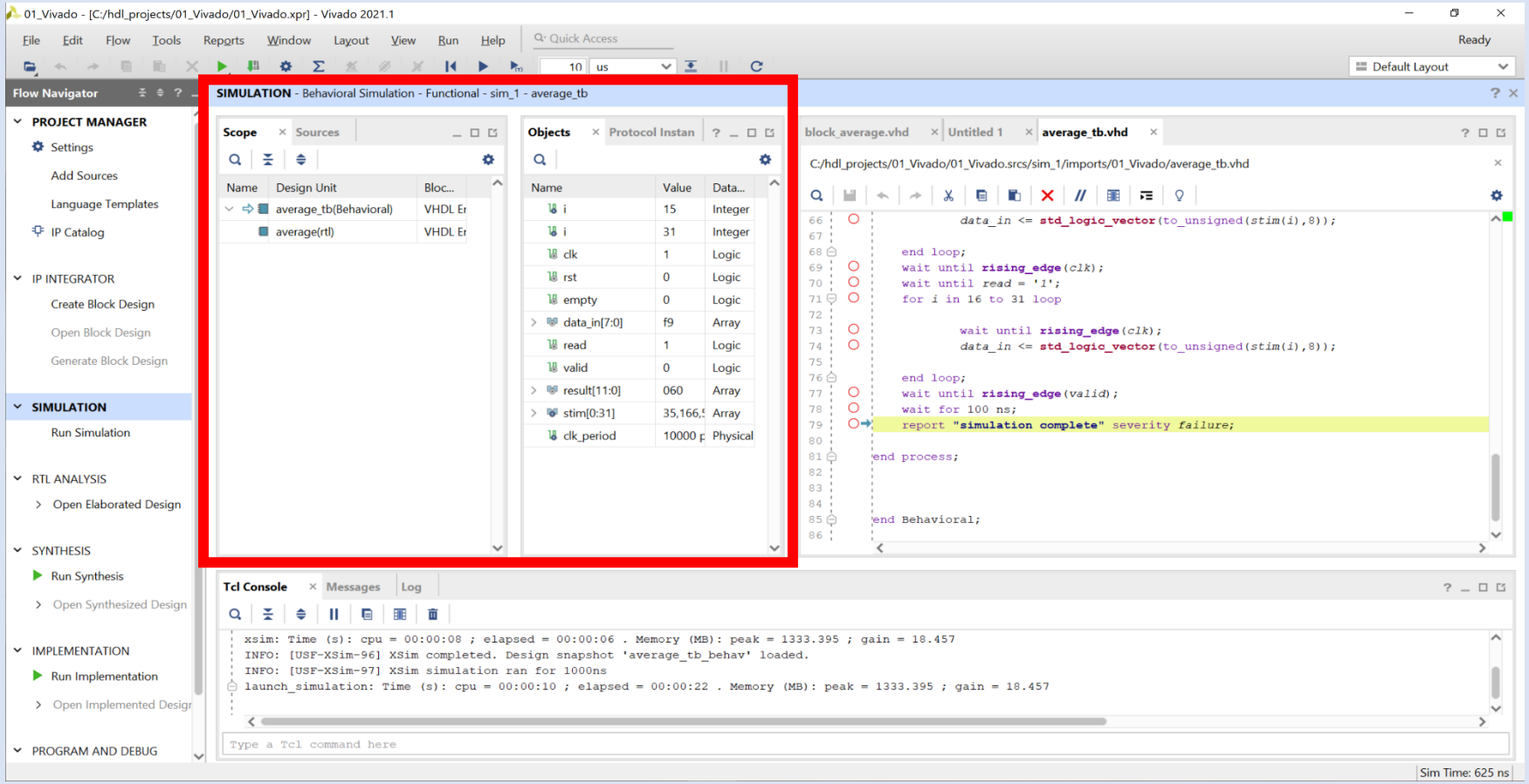
Step 14 – This will open the behavioral simulation view. Note the scope and objects.



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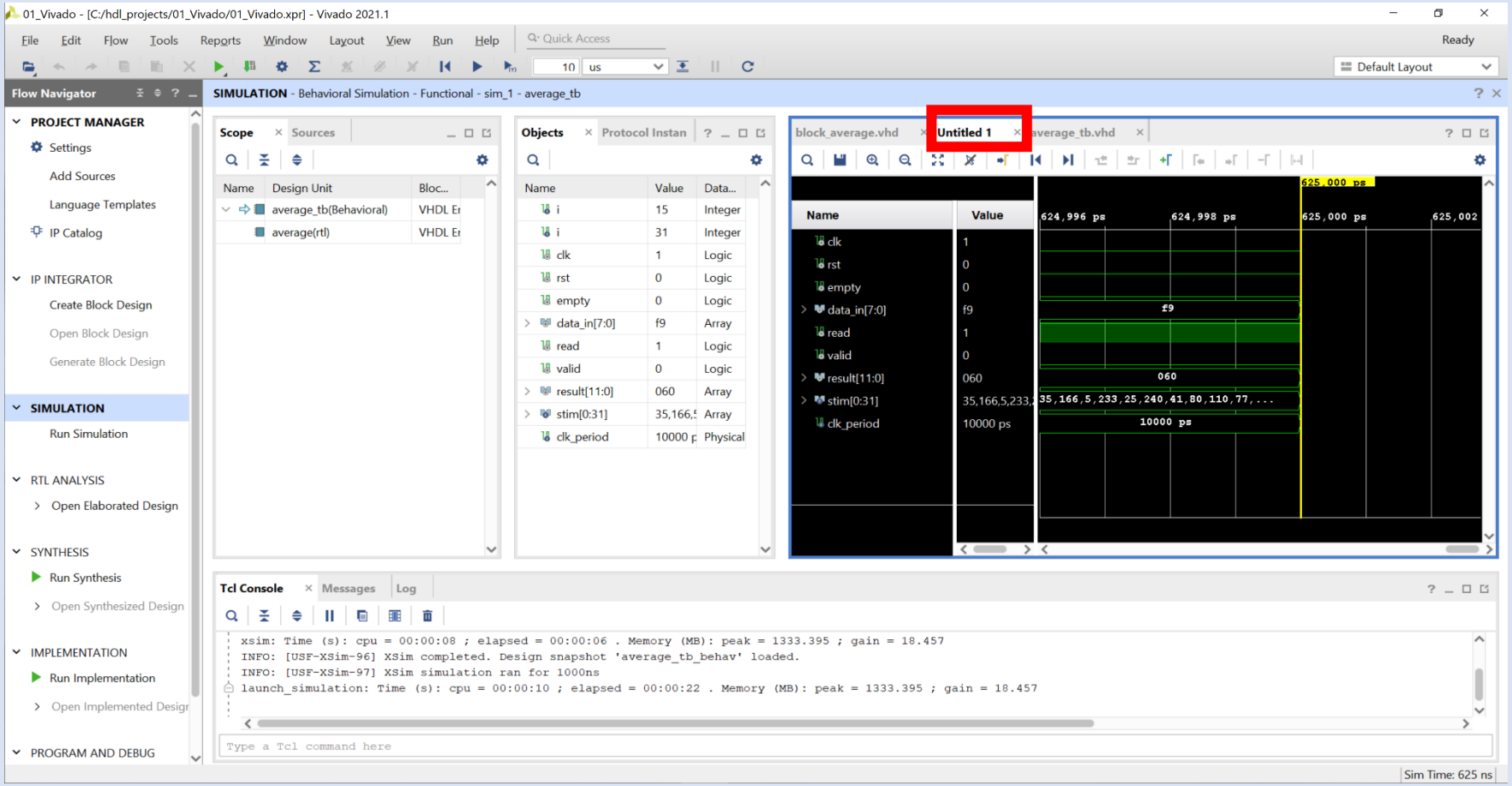
Step 15 – Click on the **Untitled* tab** to see the waveform of the simulation. Note this view shows the signals defined within the test bench only, not the Unit Under Test.



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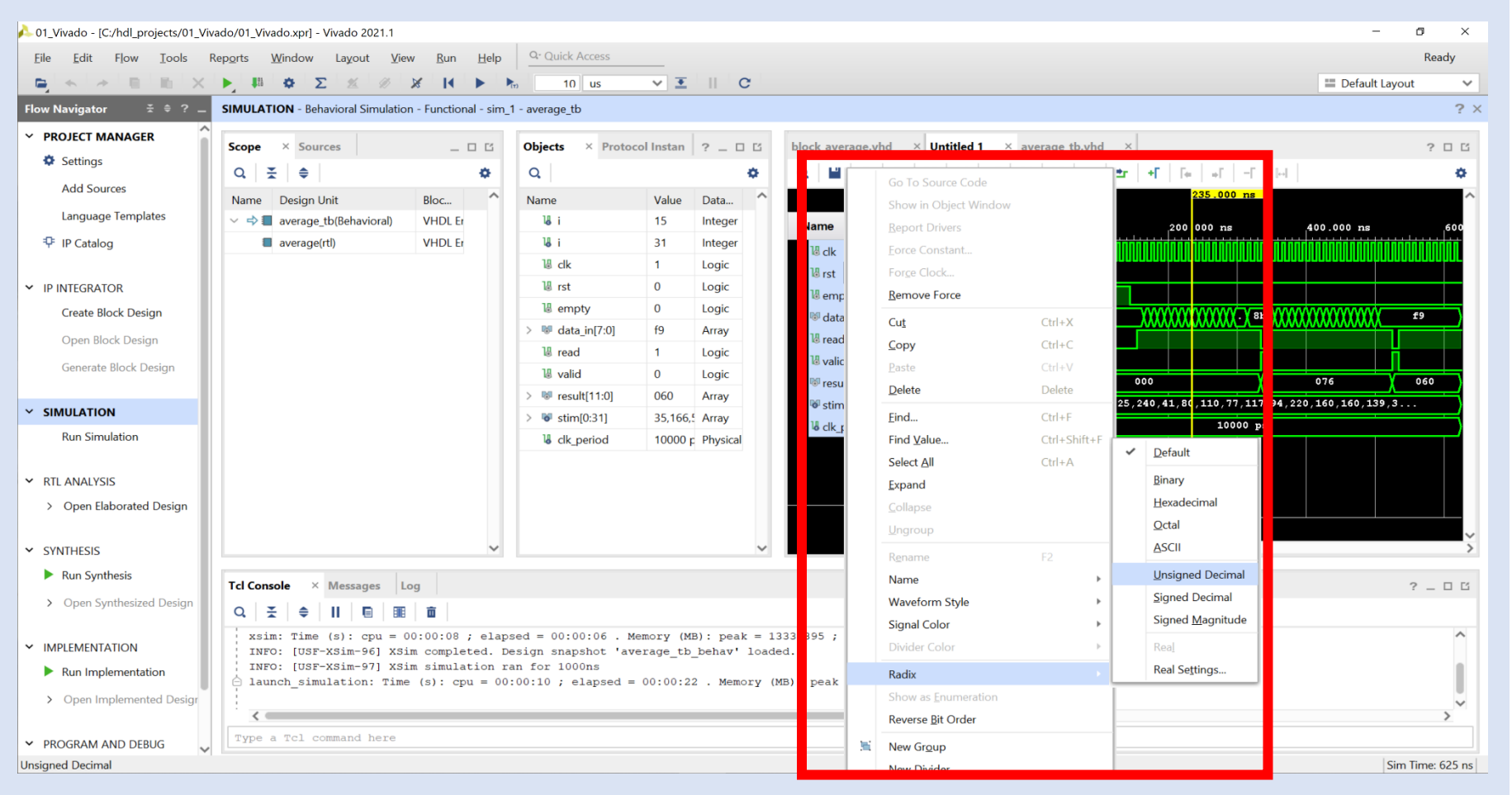
Step 16 – At the moment, the results are in hexadecimal but they make more sense in decimal. Select all the signals, right click, and select **unsigned decimal** from the **radix**.



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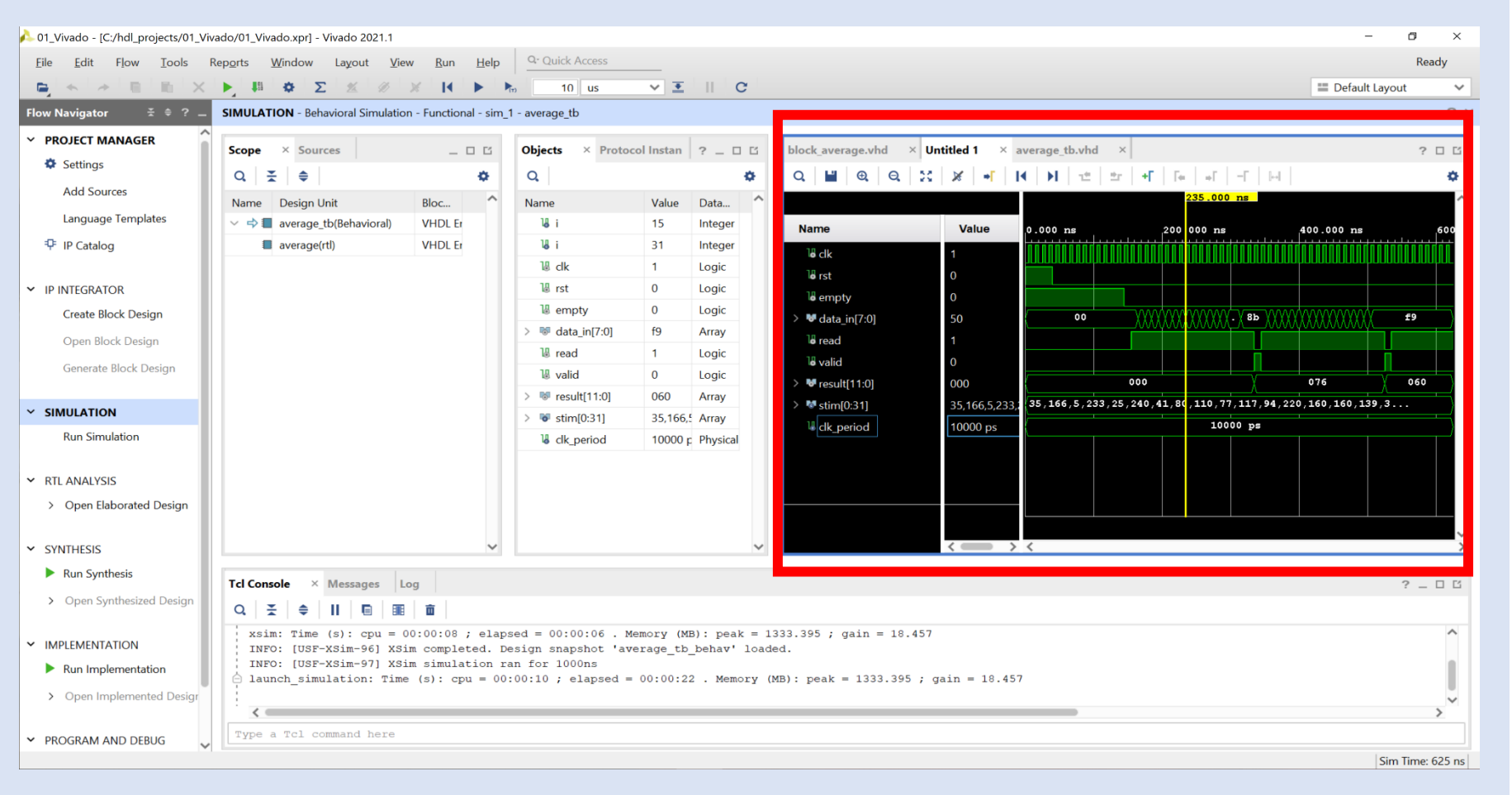
Step 17 – This will change the results to decimal. Correct operation has result showing 118 then 96. This is the block average of 16 input values.



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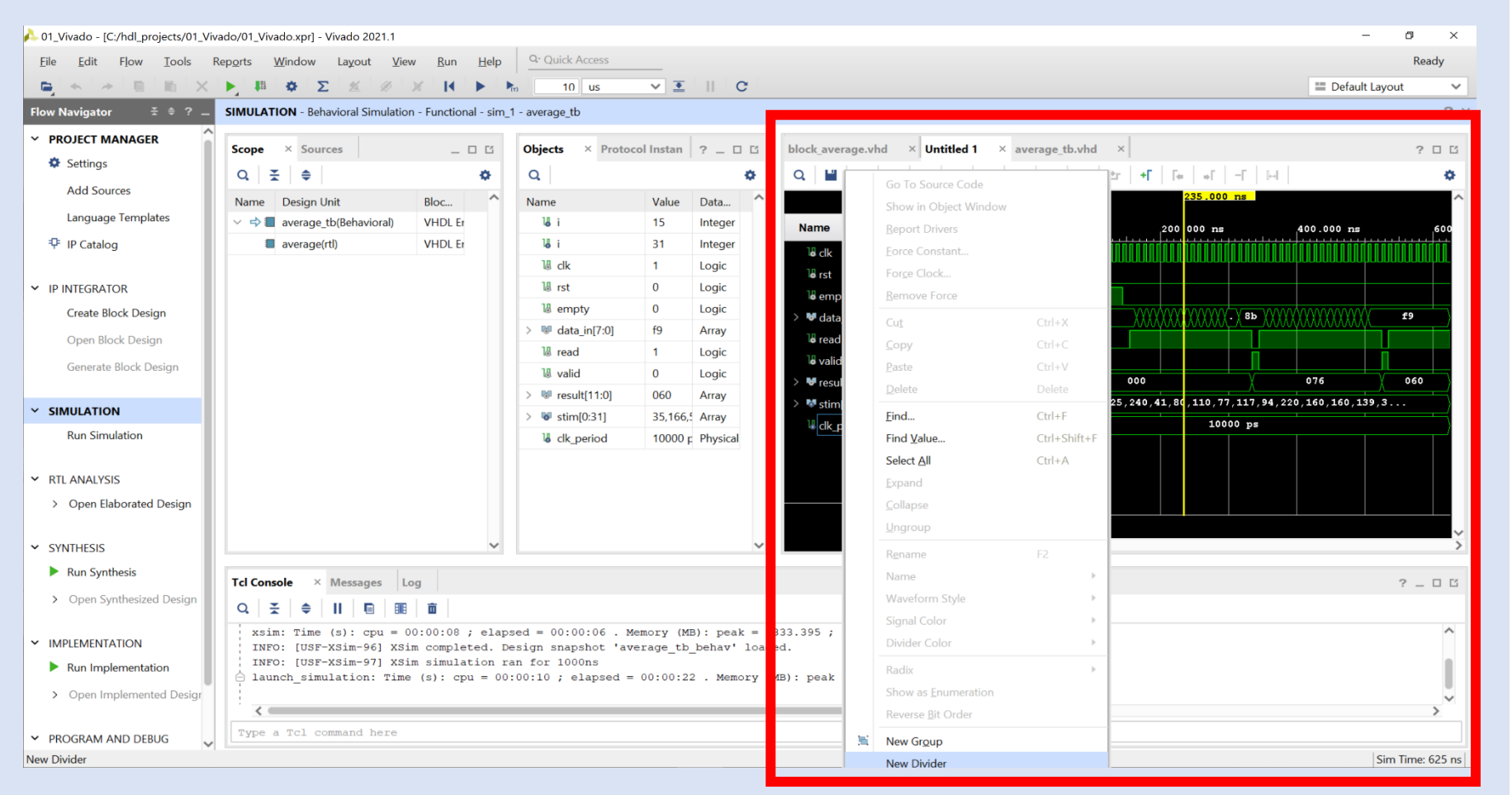
Step 18 – Often we want to be able to see the signals in the UUT. To do this, first let's insert a divider. Right click on the **bottom signal** and select **New Divider**.



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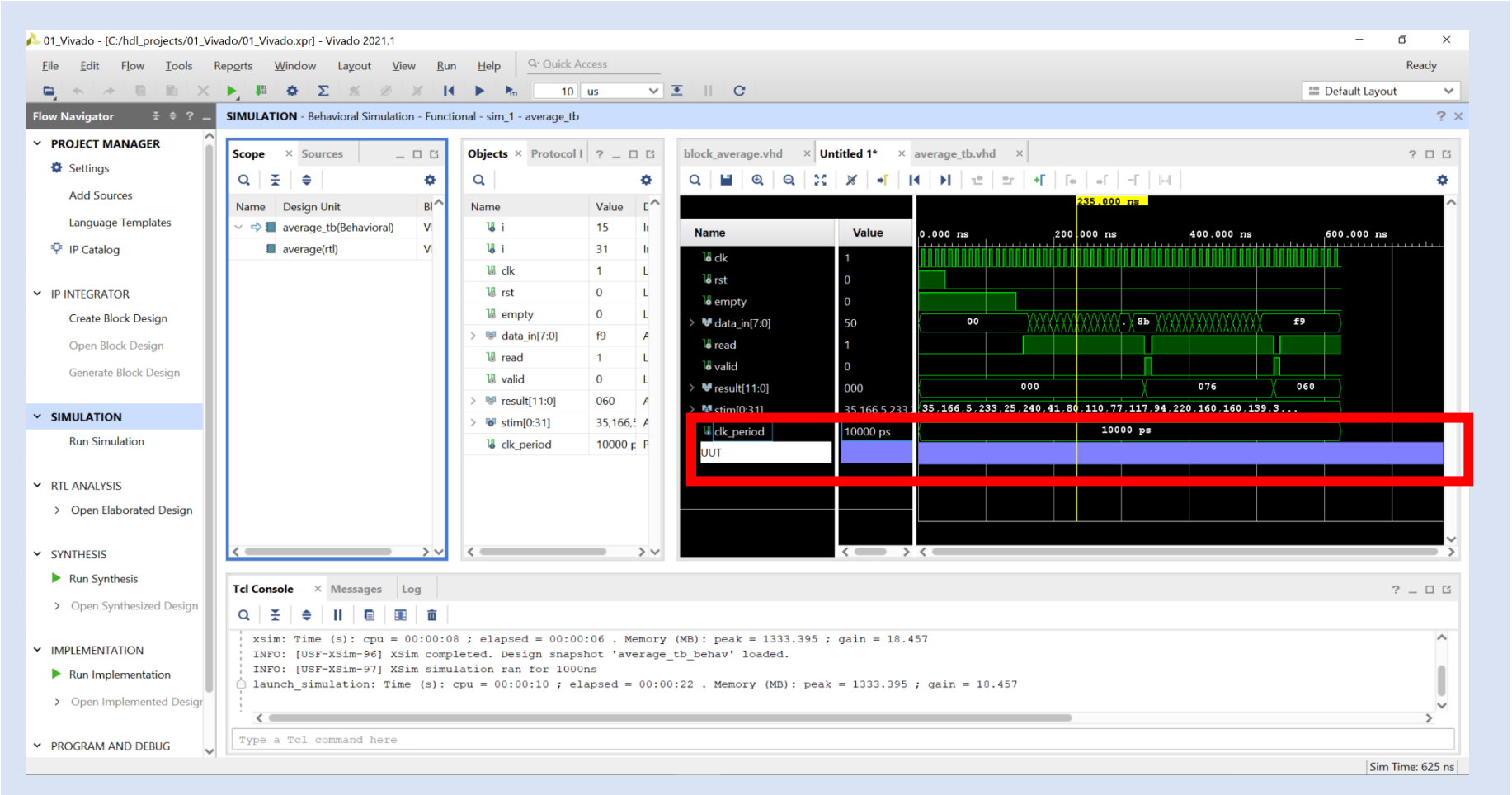
Step 19 – When prompted, enter the name **UUT** and you will see the new divider in the waveform.



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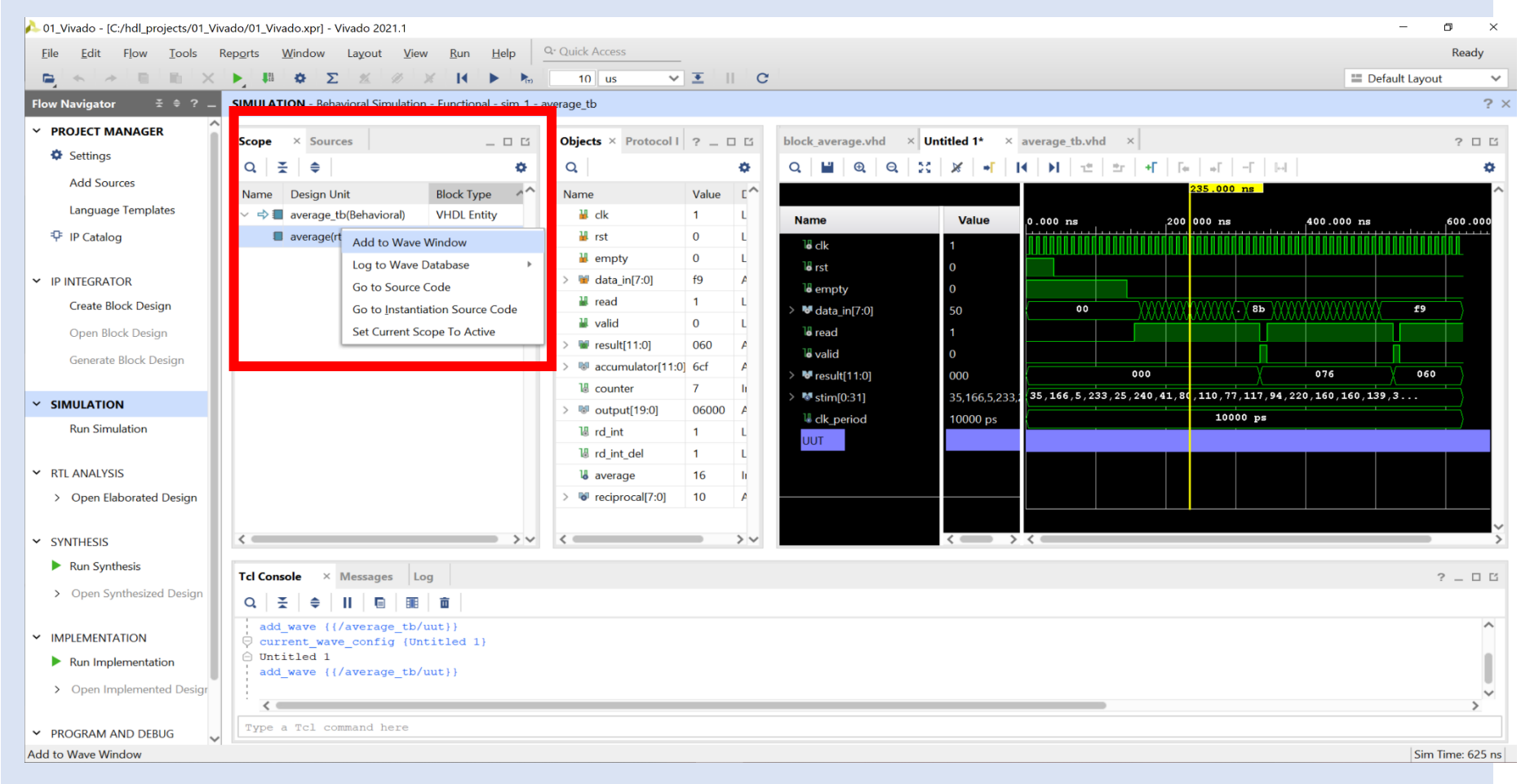
Step 20 – To add in the UUT, right click on the **UUT** under the scope and select **Add to Wave Window**.



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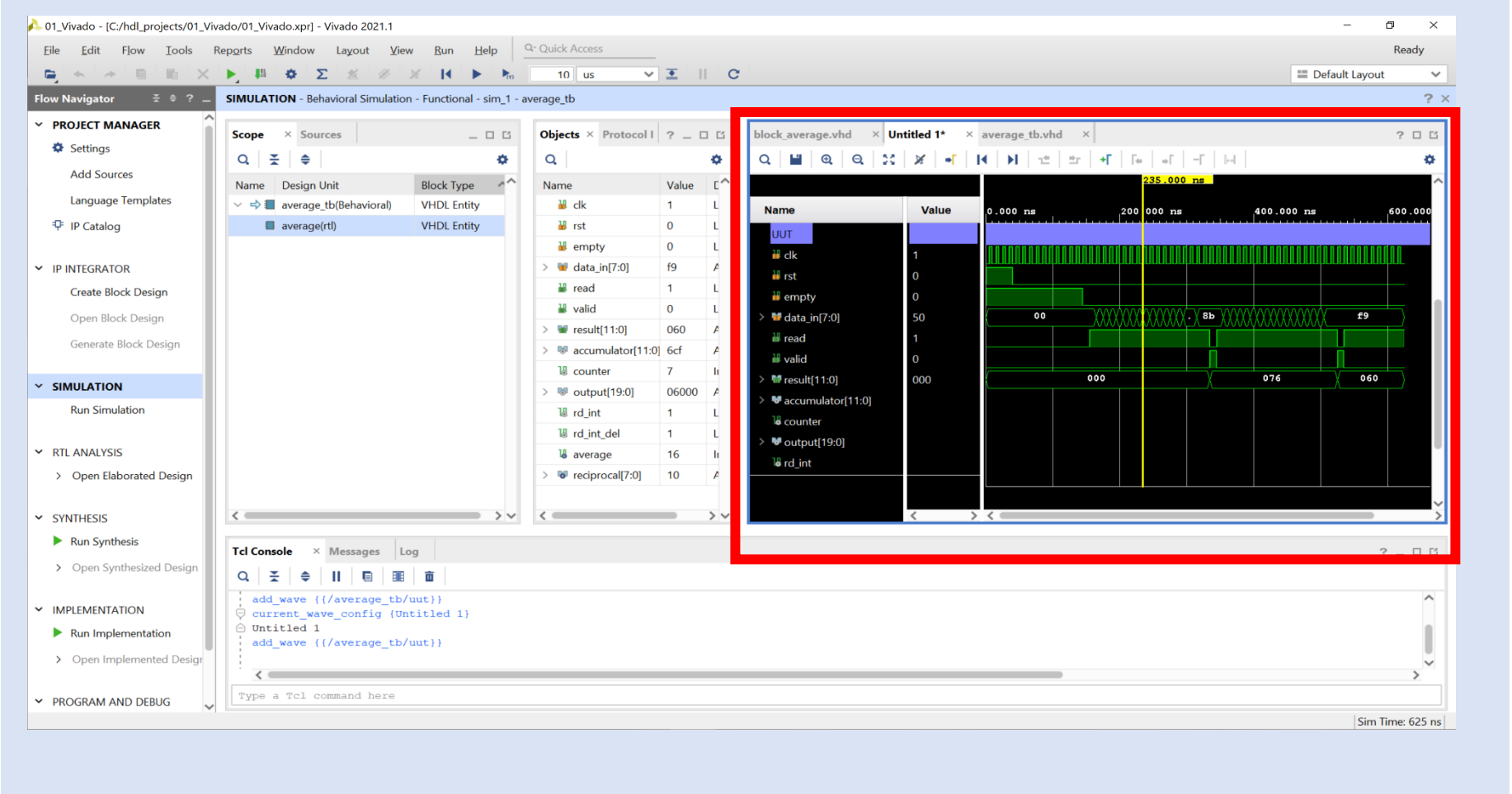
Step 21 – This will add in the UUT signals, however, some information may be missing as it was not saved during the simulation.



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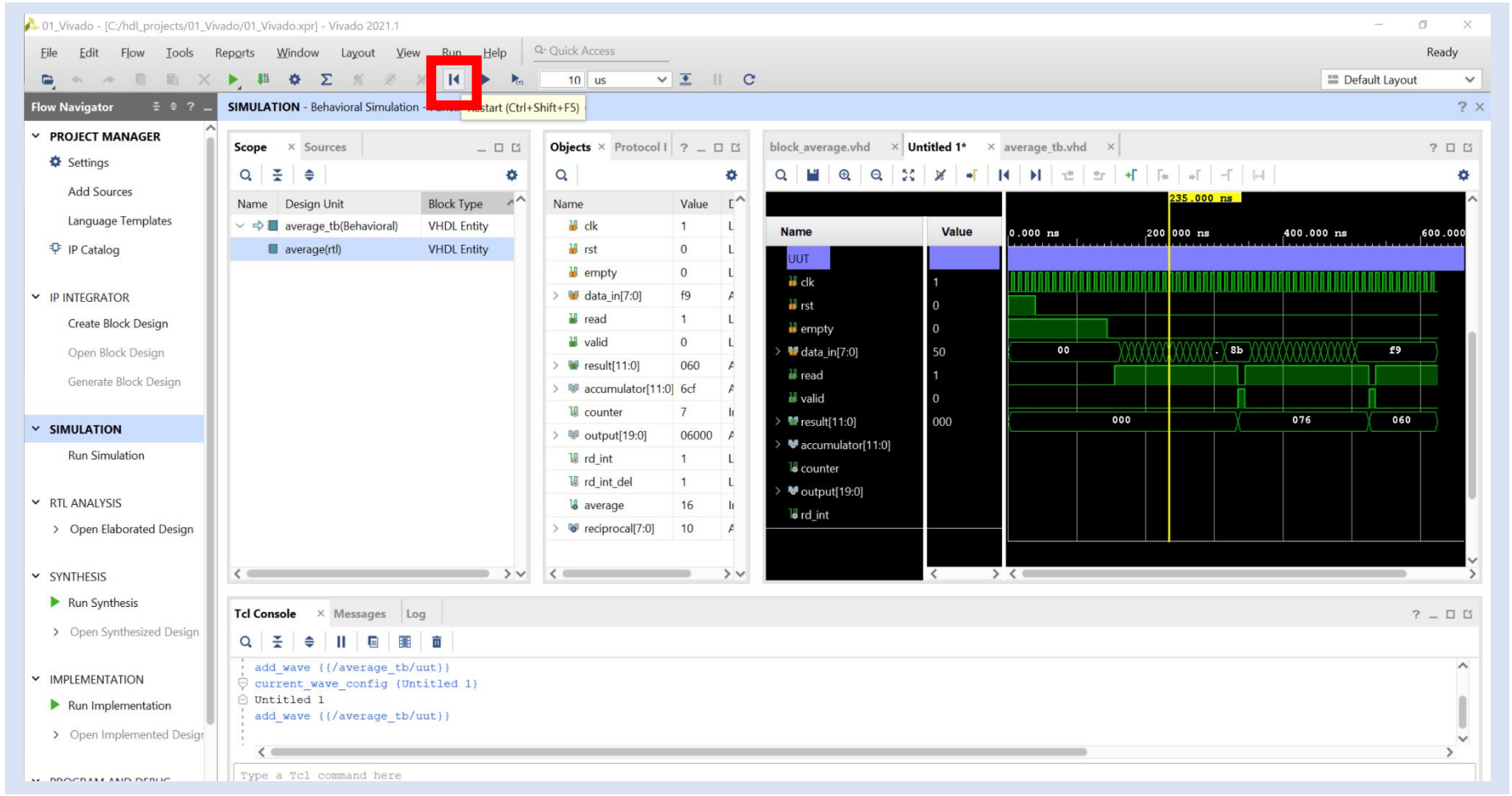
Step 22 – To add in the missing waveform, we need to restart the simulation. Select **Restart** from menu bar.



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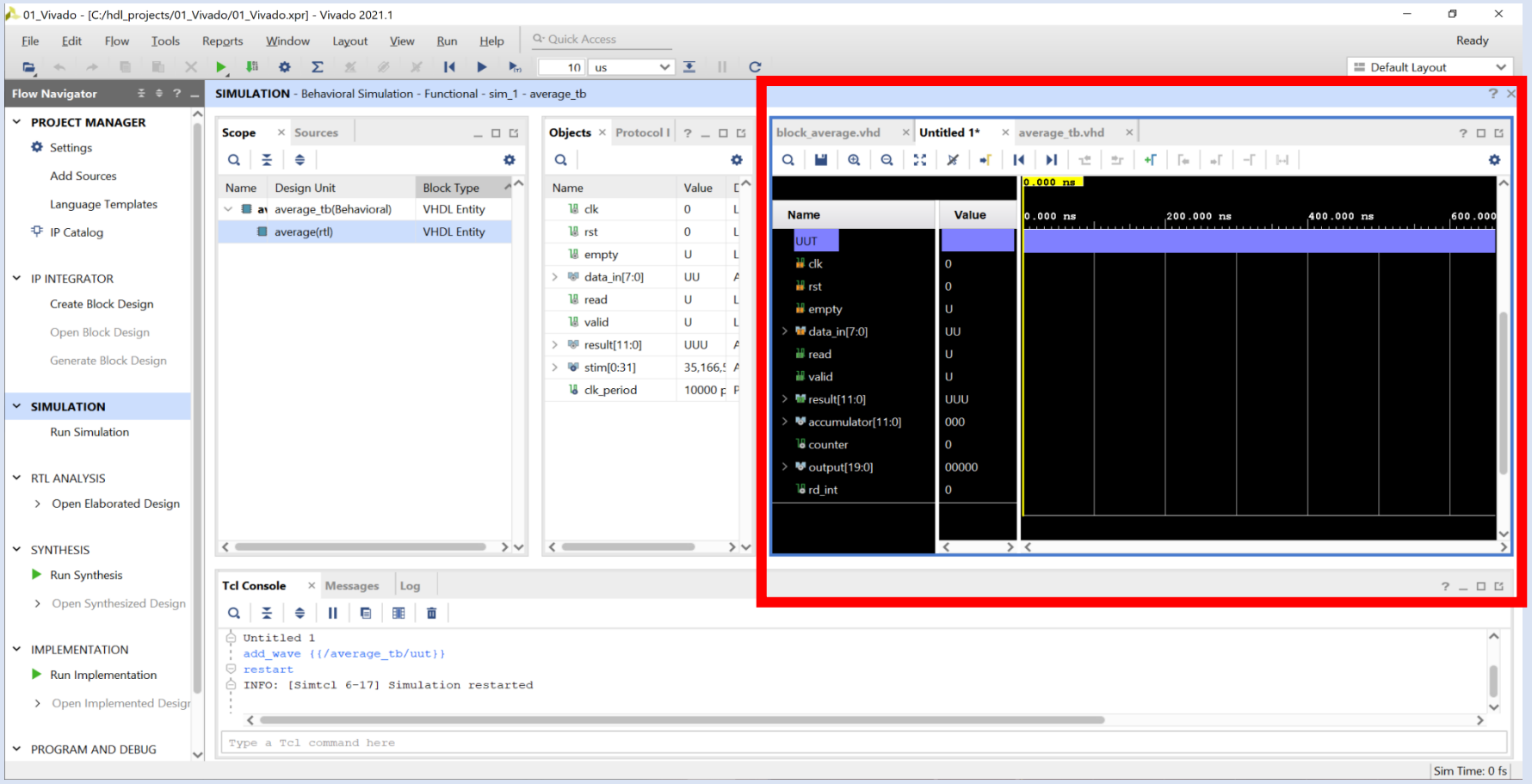
Step 23 – This will clear all waveform data and restart the simulation**.**



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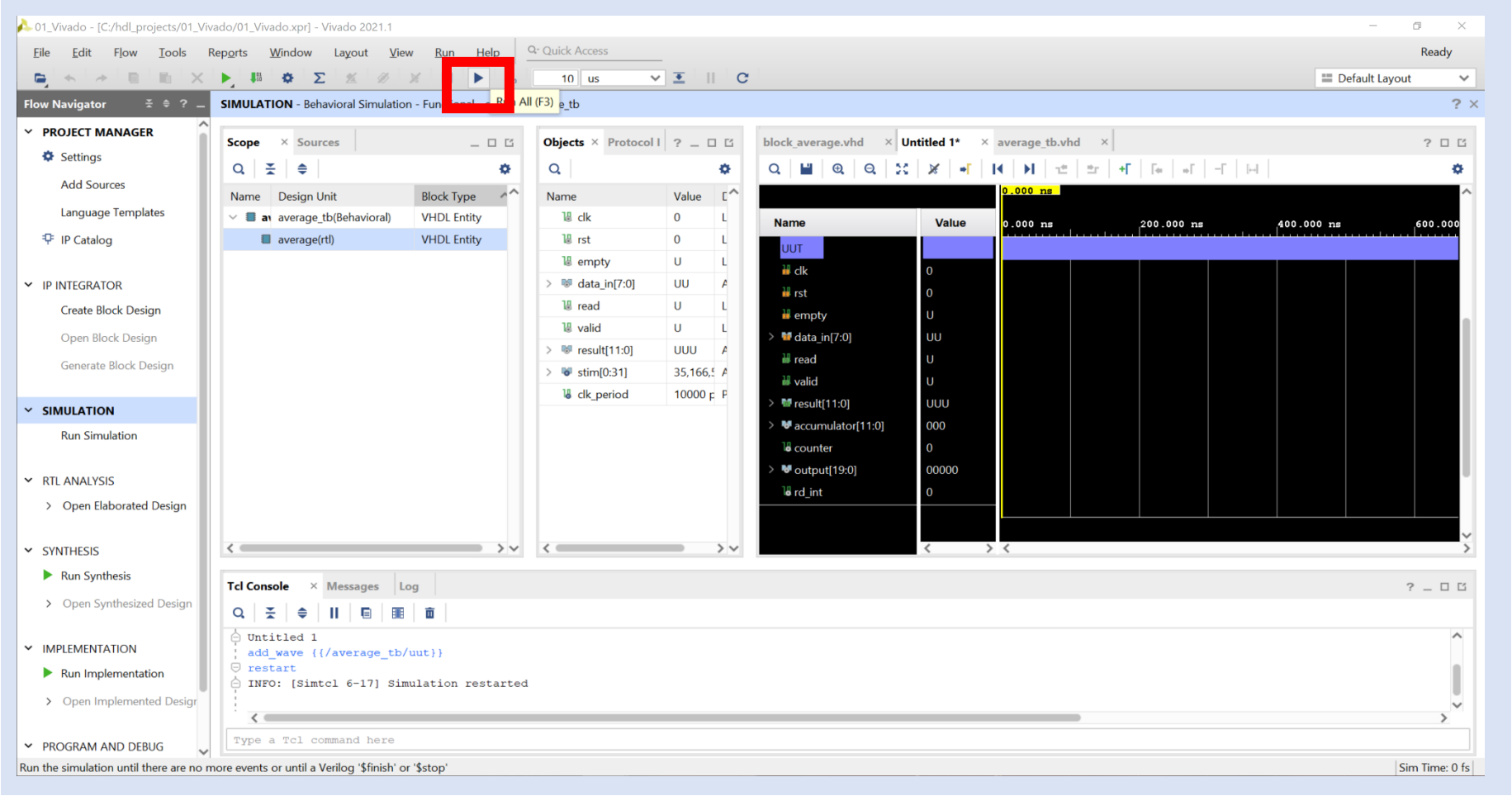
Step 24 – To rerun the simulation, select the **Run button** on the menu. The simulation will stop automatically.



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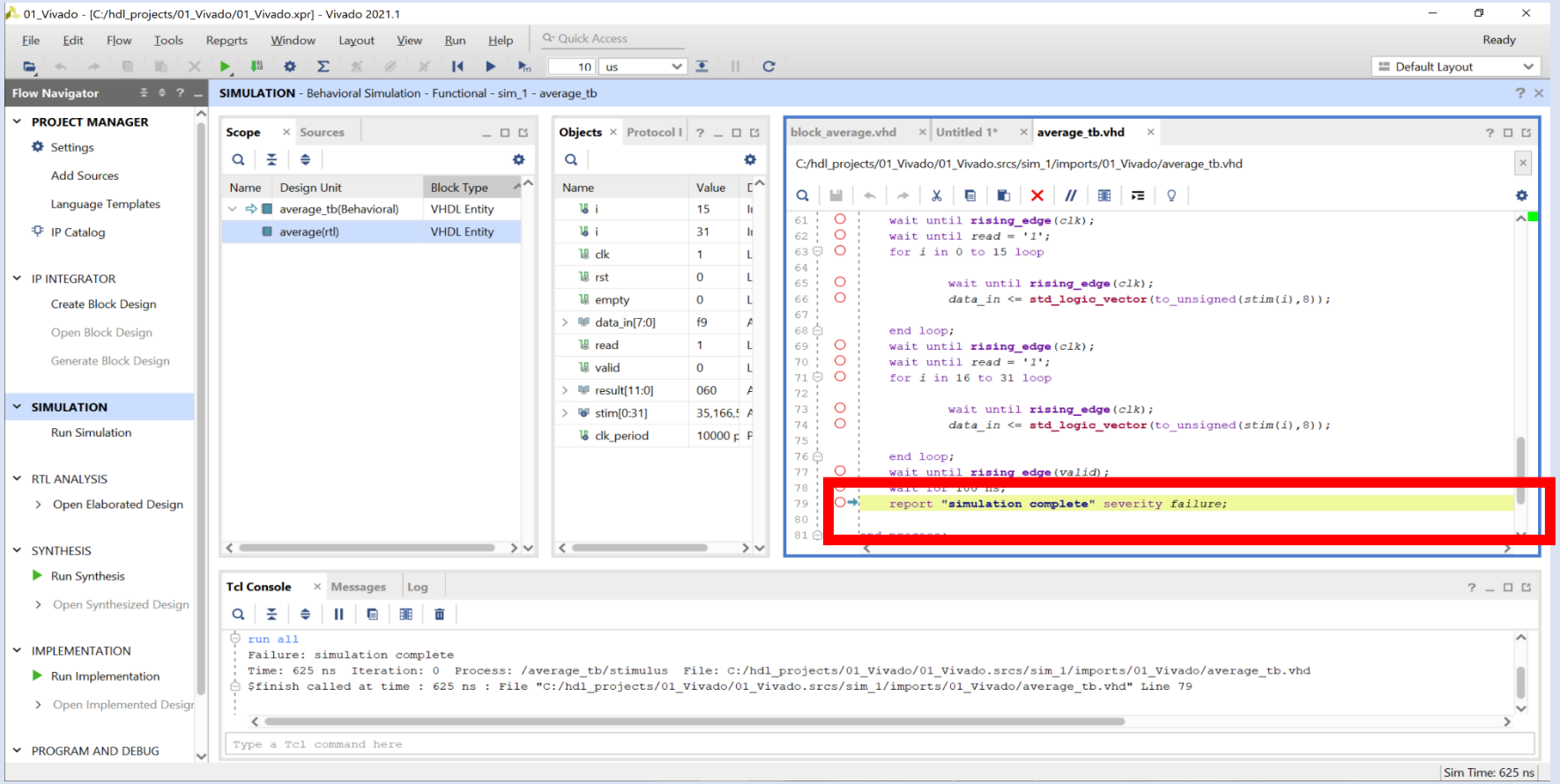
Step 25 – When the simulation completes, you will see the highlighted line in the test bench.



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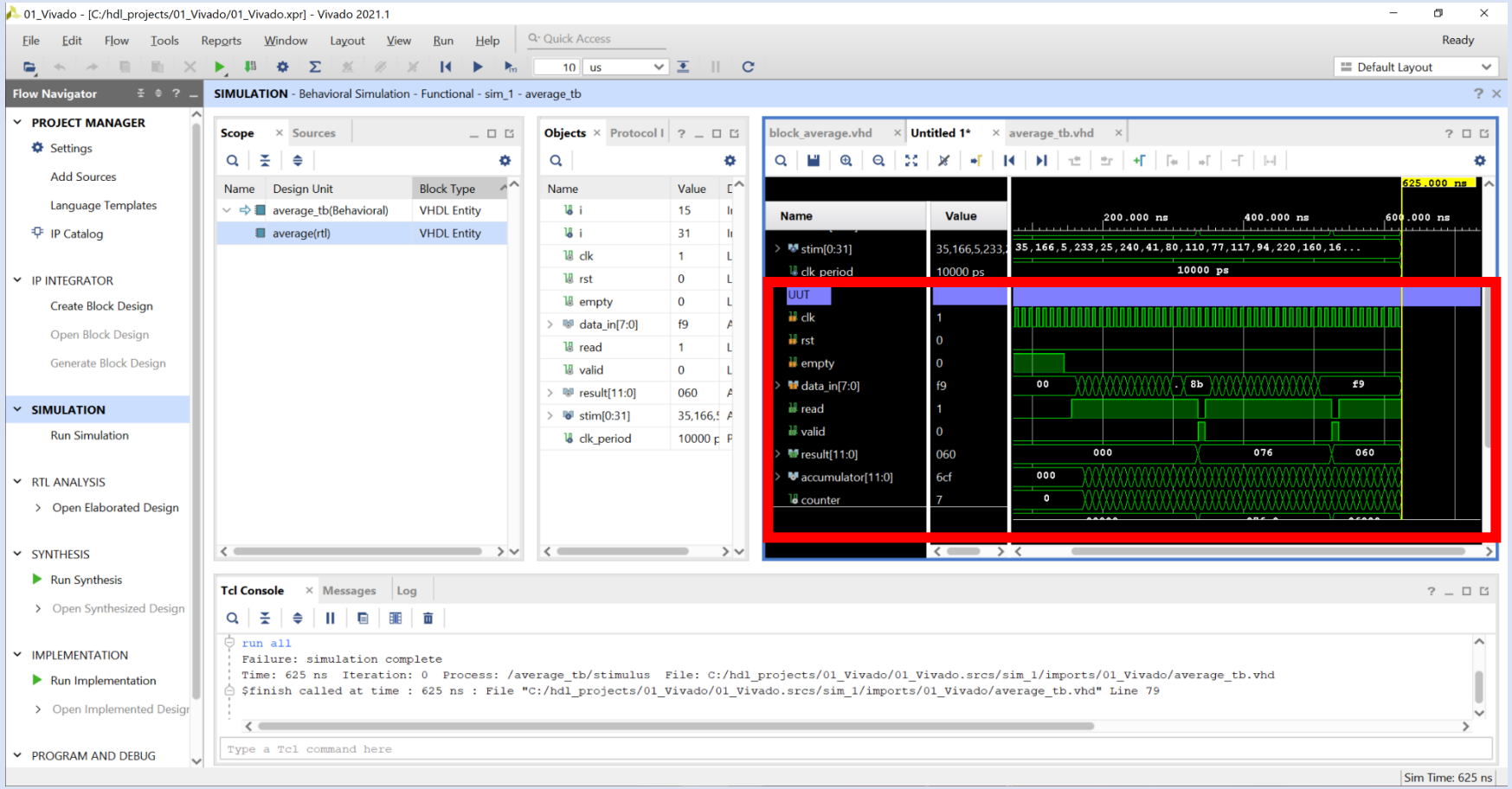
Step 26 – Selecting the **waveform tab** again will show all the signals for the UUT.



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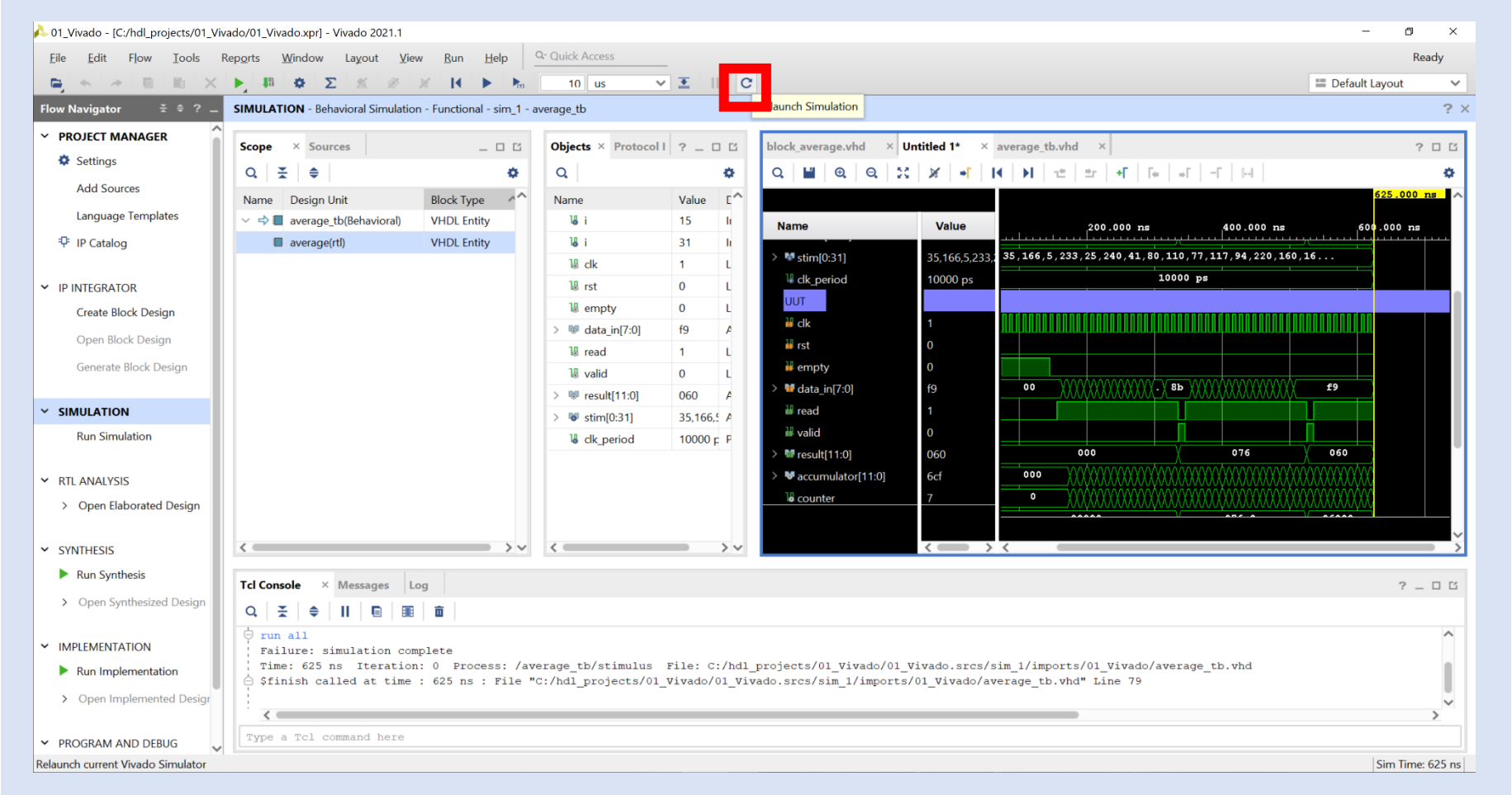
Step 27 – If you make changes to the source code, you need to relaunch the simulation. This can be achieved using the relaunch button on the menu.



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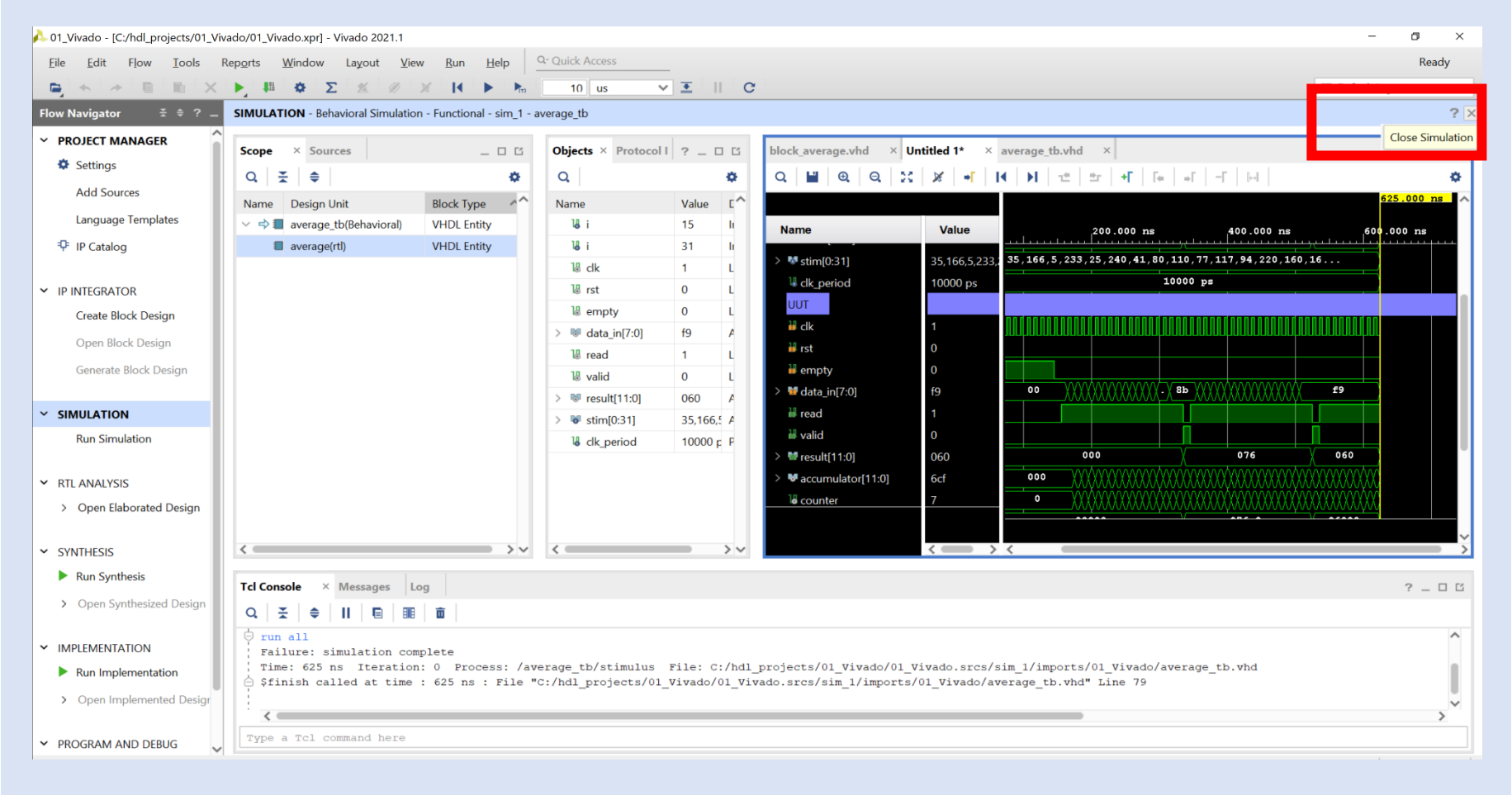
Step 28 – With the simulation complete, we are now ready to implement the design. Close the **simulation view**.



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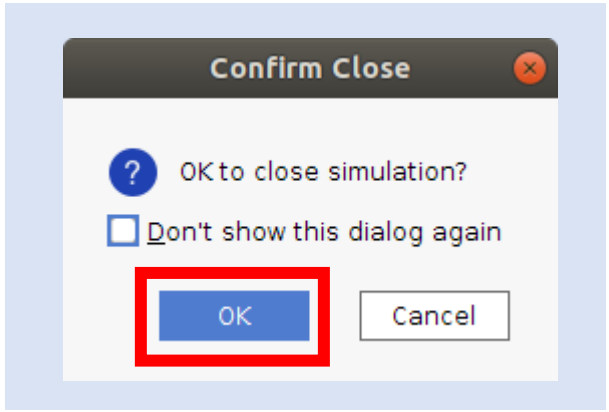
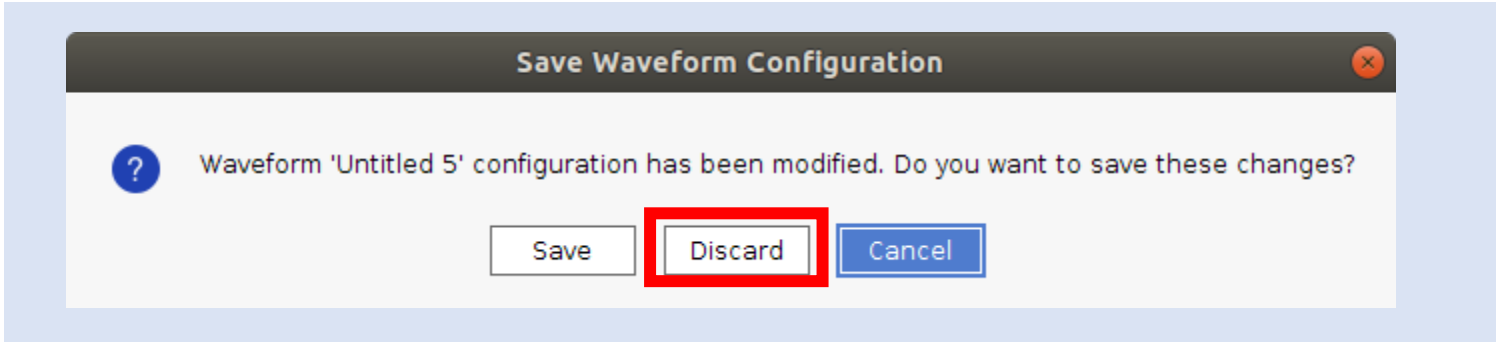
Step 29 – When asked to confirm, click **OK**. If a save waveform dialog pops up, select **Discard**.





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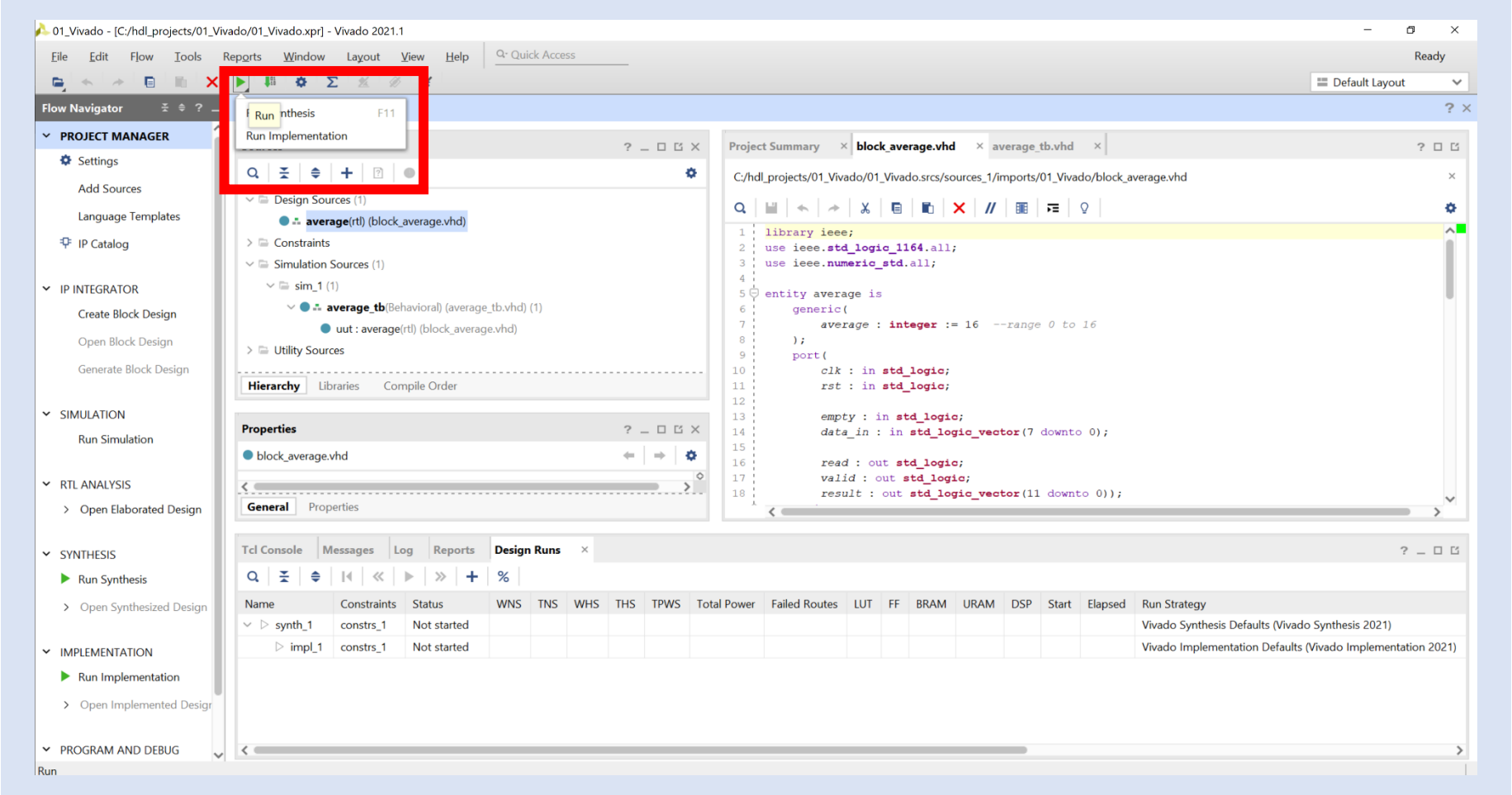
Step 30 – To synthesize the design, click the **green run arrow** and select **Run Synthesis**.



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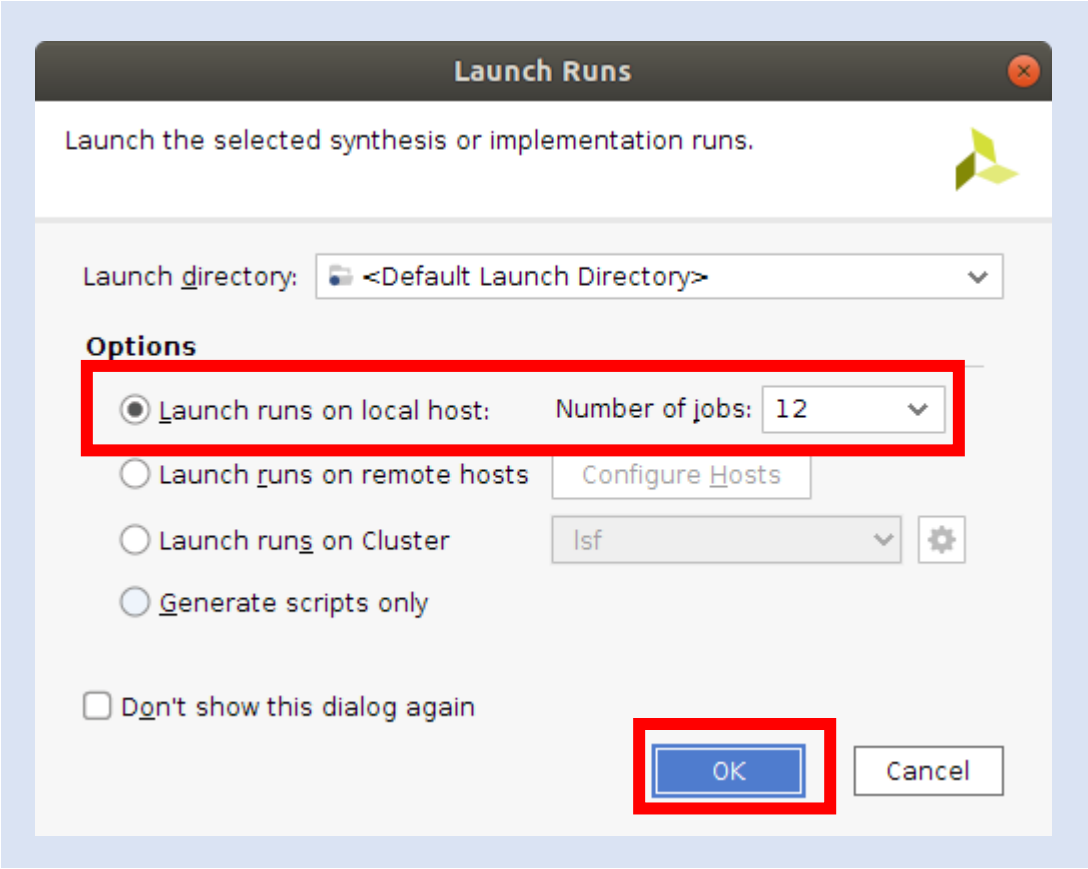
Step 31 – On the Launch Runs dialog, select the number of jobs you want to run on your system and click **OK**.



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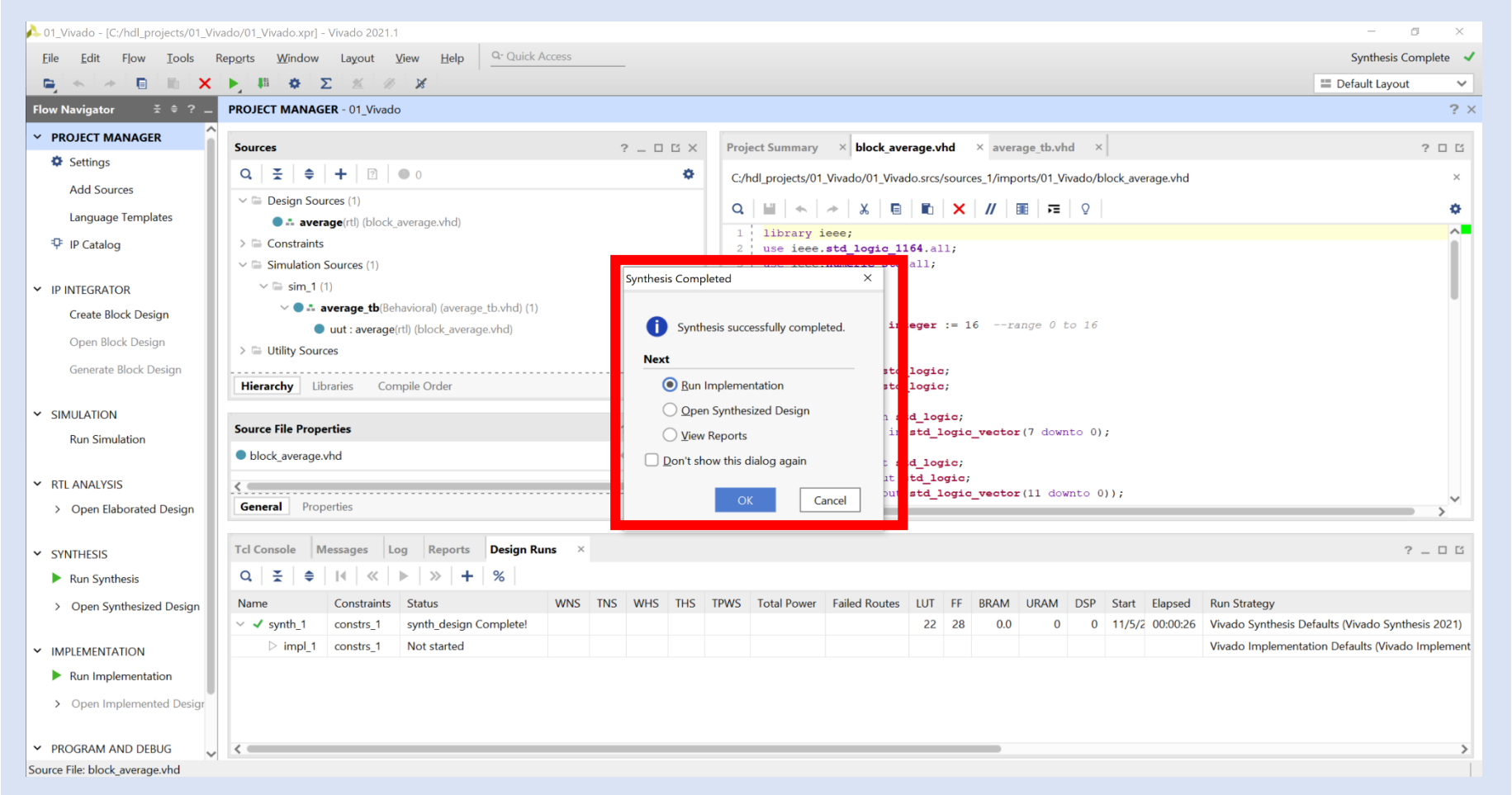
Step 32 – When synthesis is complete, you will see a dialog box appear.



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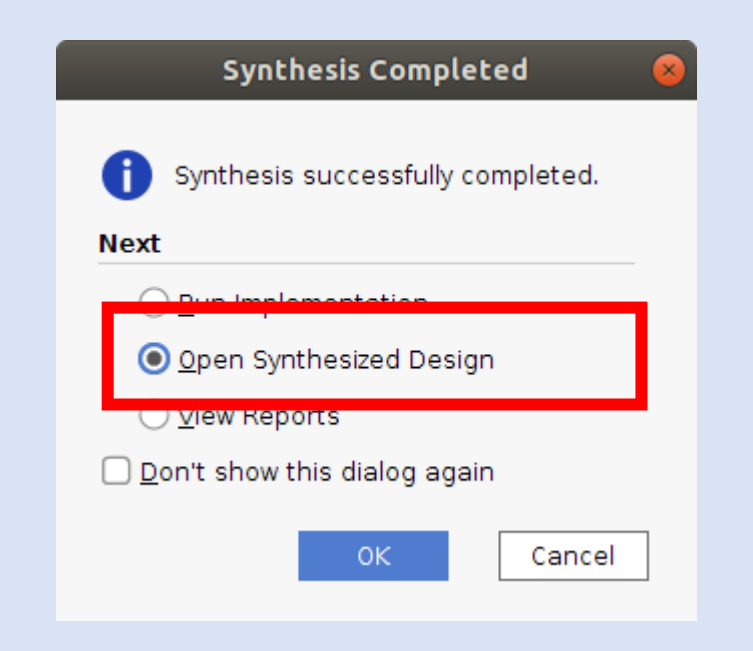
Step 33 – Select **Open Synthesized Design**.



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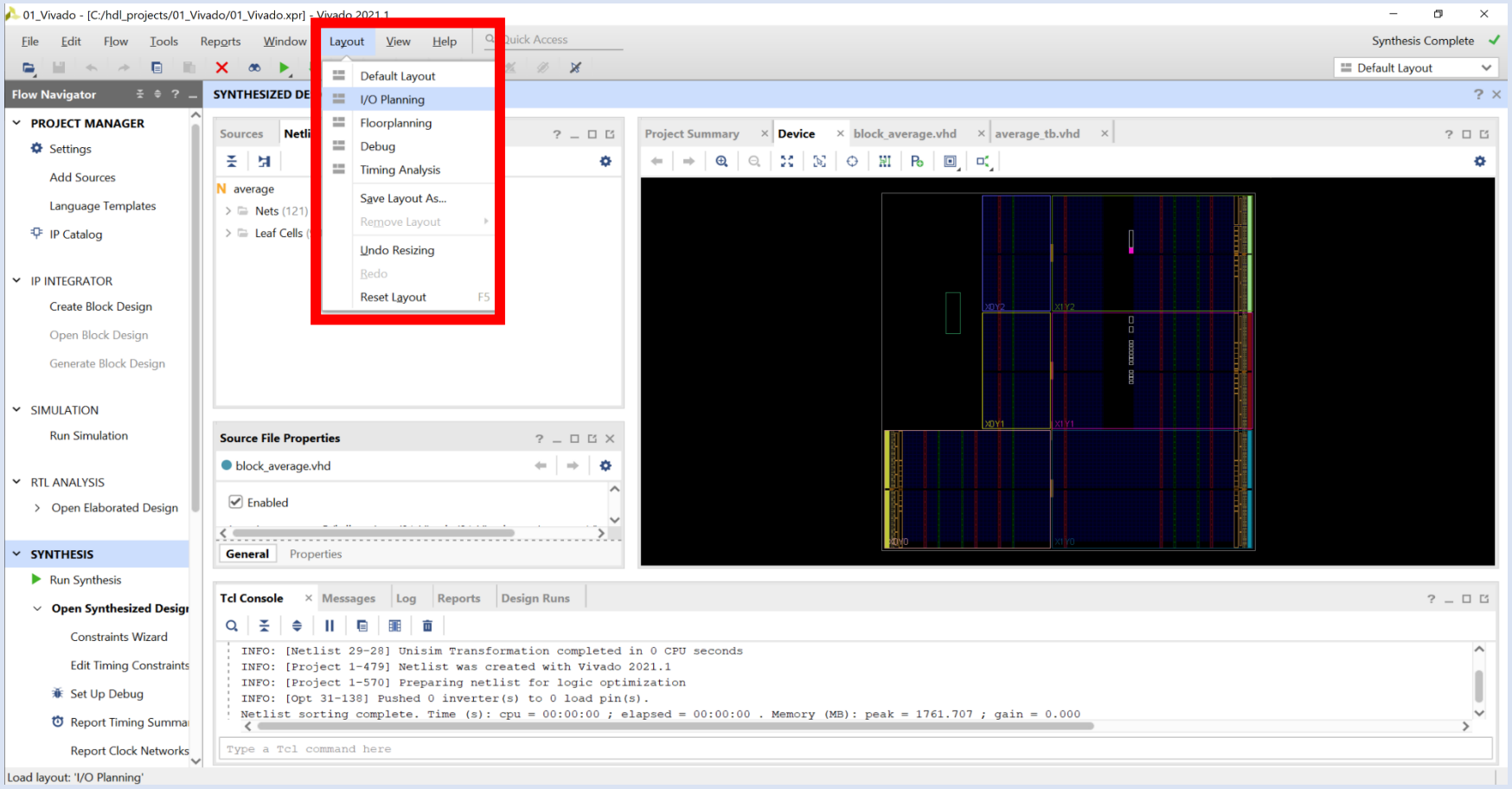
Step 34 – This will open the synthesis view. From the menu layout, select **I/O Planning**.



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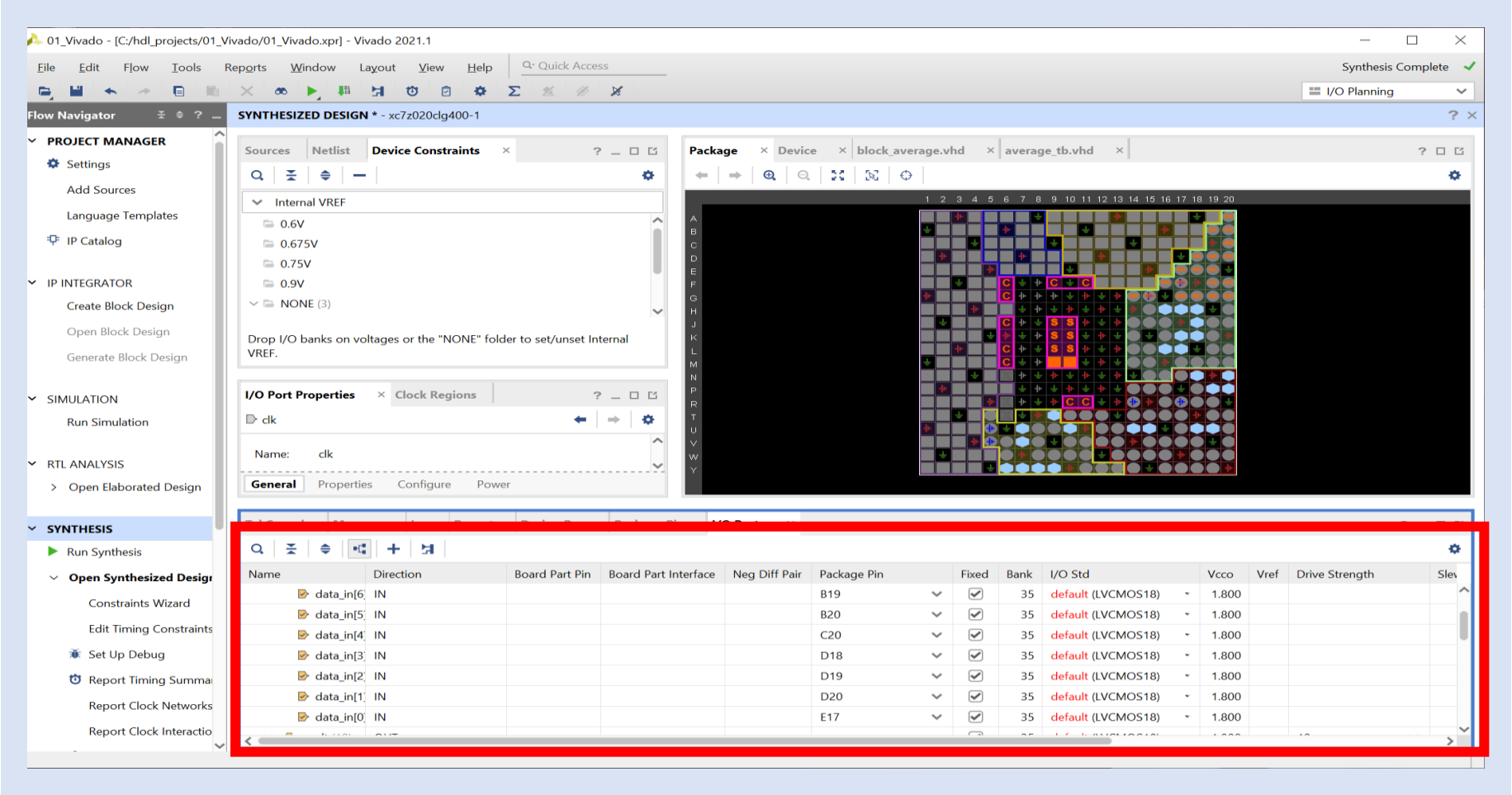
Step 35 – Expand the **Data_In, Result and Scalar Ports** and assign them to pins. All EXCEPT the clock pin can be assigned to any pin.



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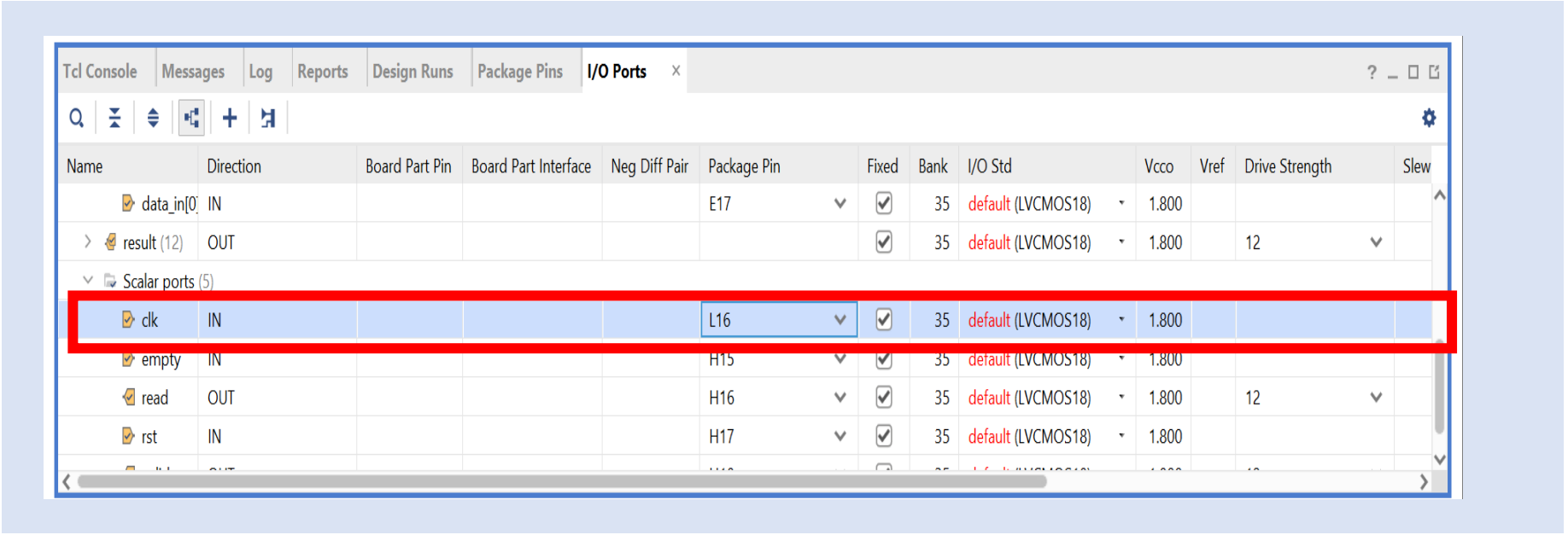
Step 36 – Assign the **clock pin to L16.** Clocks have to be assigned to clock capable pins.



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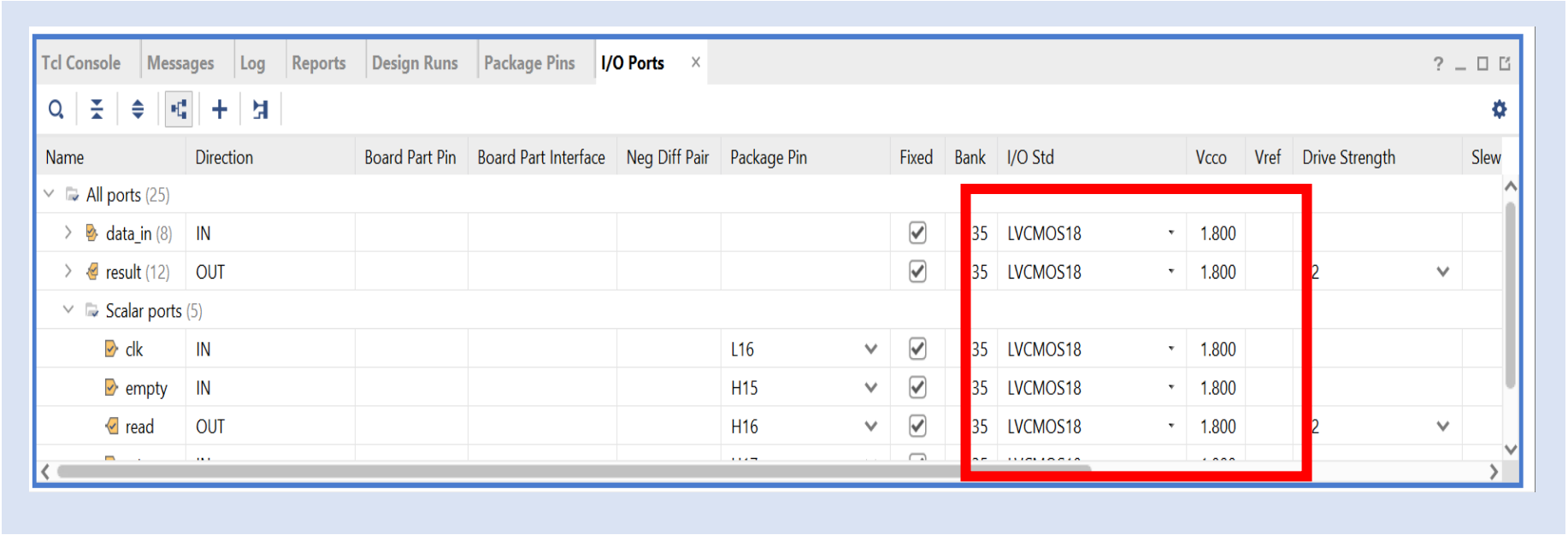
Step 37 – Ensure the **IO Standard** is set to **LVCMOS18.** Do not leave it as default because this will lead to a failure to implement and generate a bitstream.



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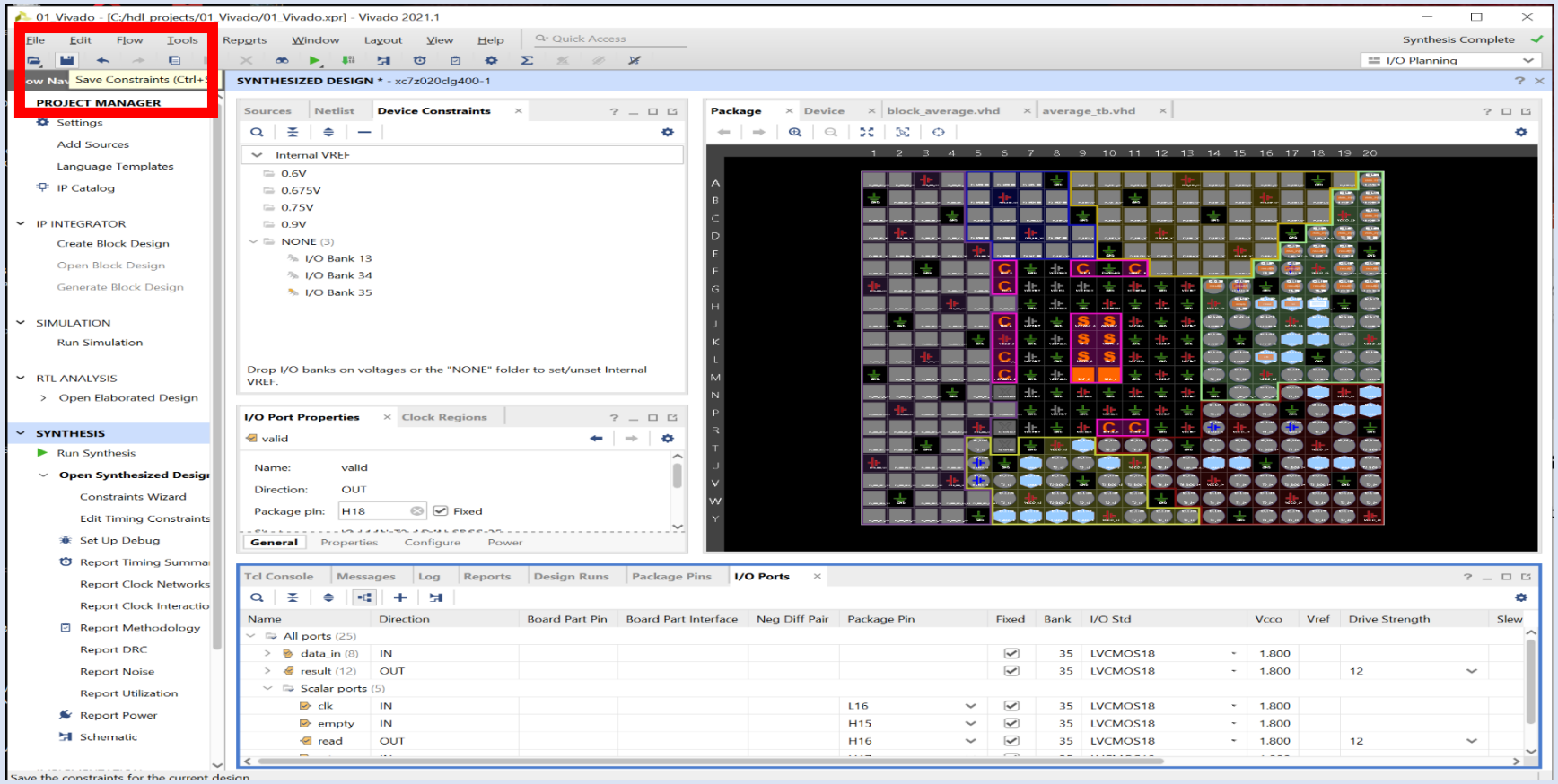
Step 38 – Save the **Constraints** we just edited.



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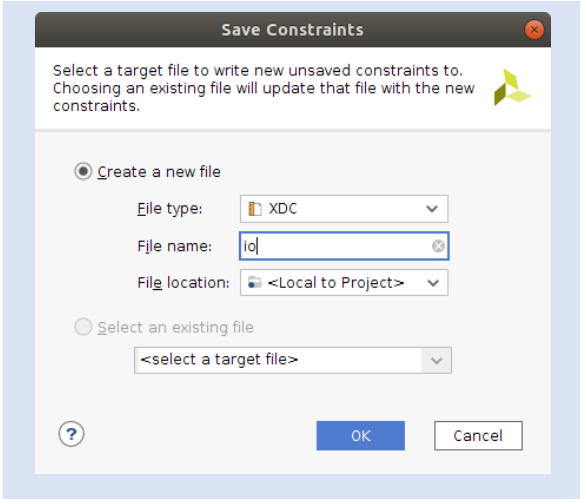
Step 39 – This will present two new dialogs. Click **OK** on the first and enter a **file name** for the second.



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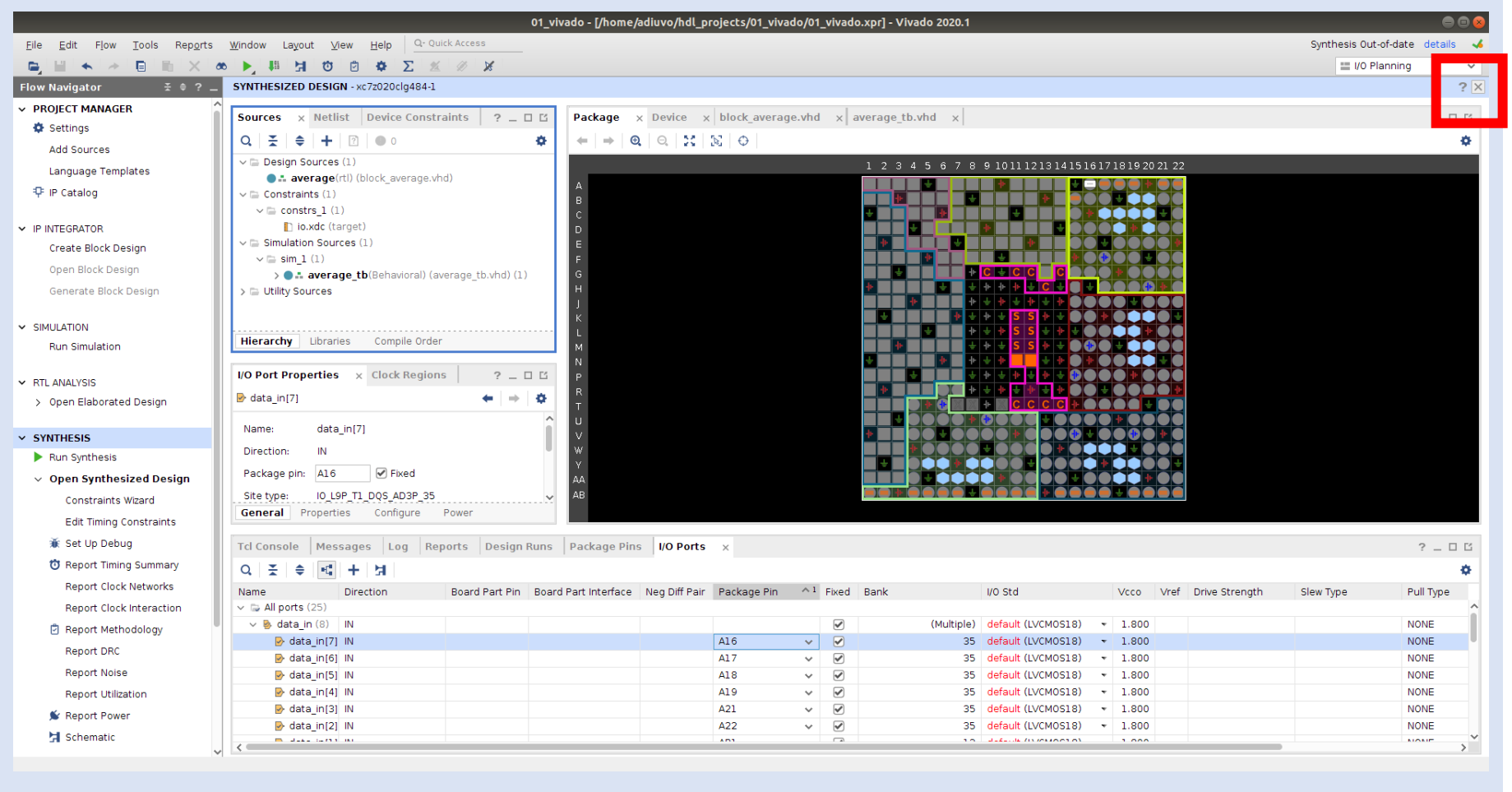
Step 40 – Close the **Synthesis View**.



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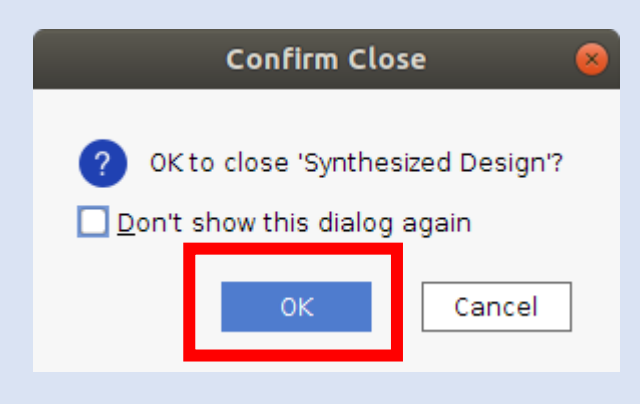
Step 41 – Confirm the decision to close by clicking **OK**. This will take us back to the project manager view.



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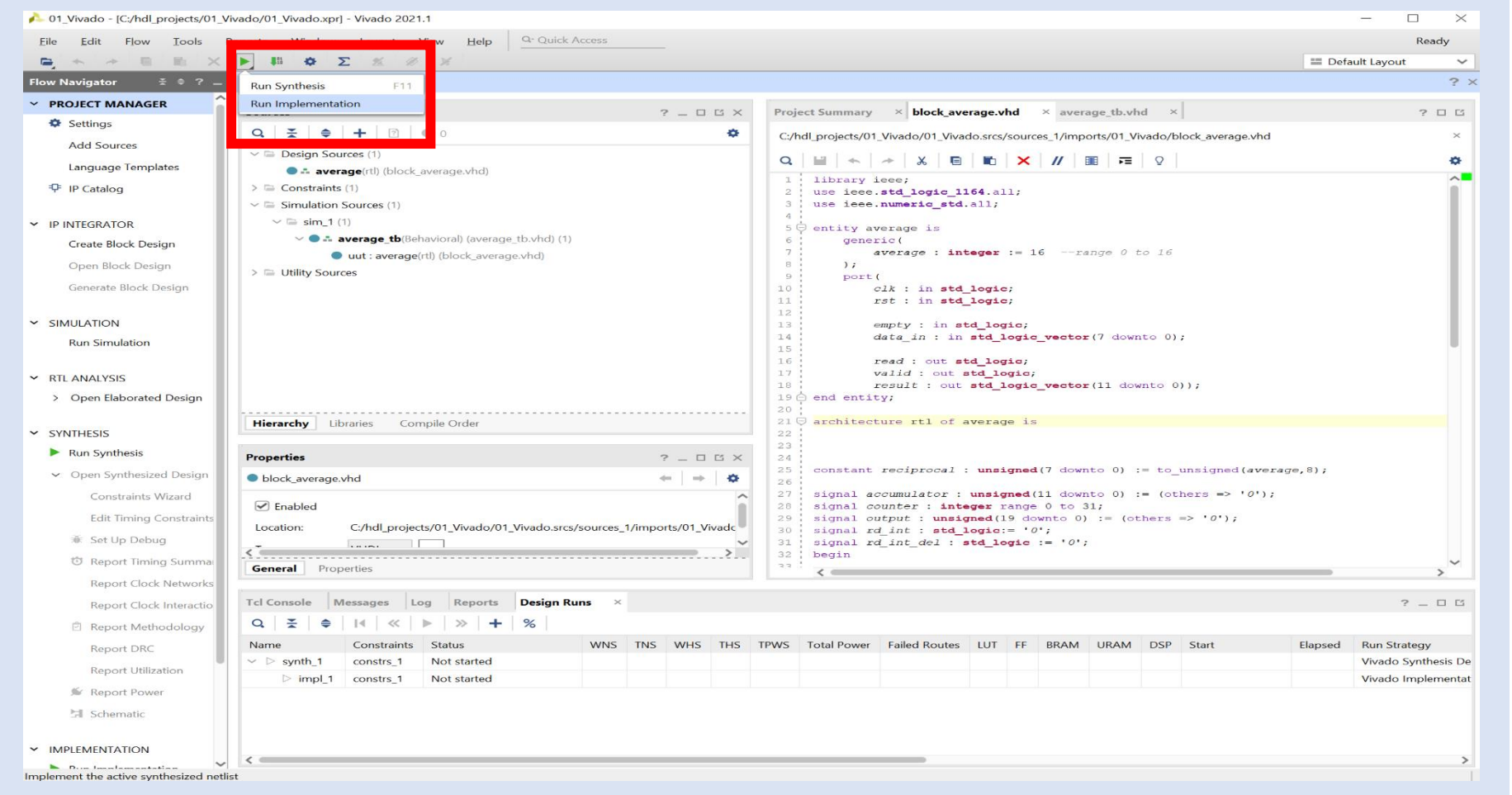
Step 42 – We are now ready to **Run Implementation**.



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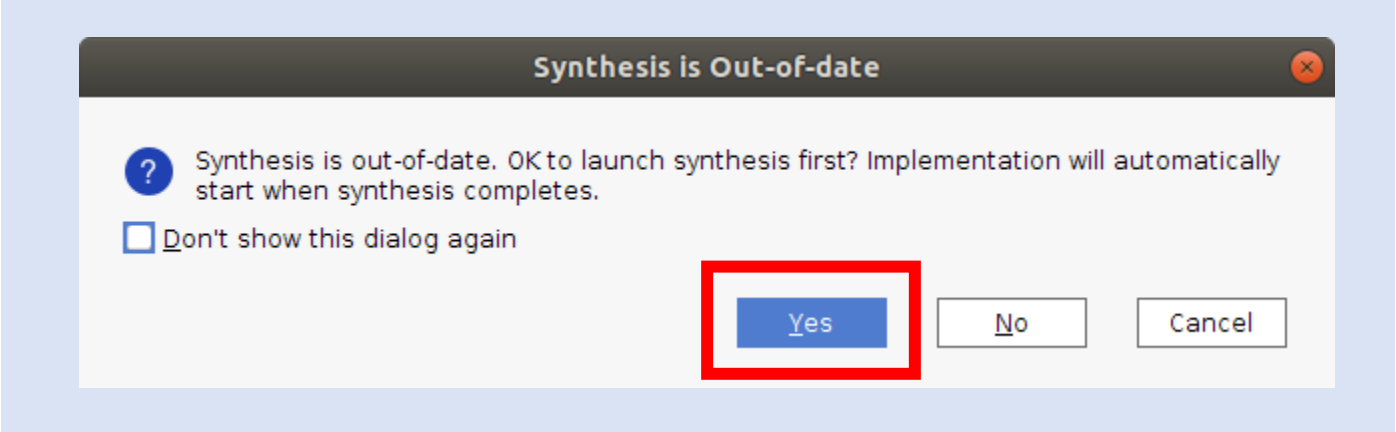
Step 43 – Click **Yes** when the Synthesis Out-of-Date dialog pops up.



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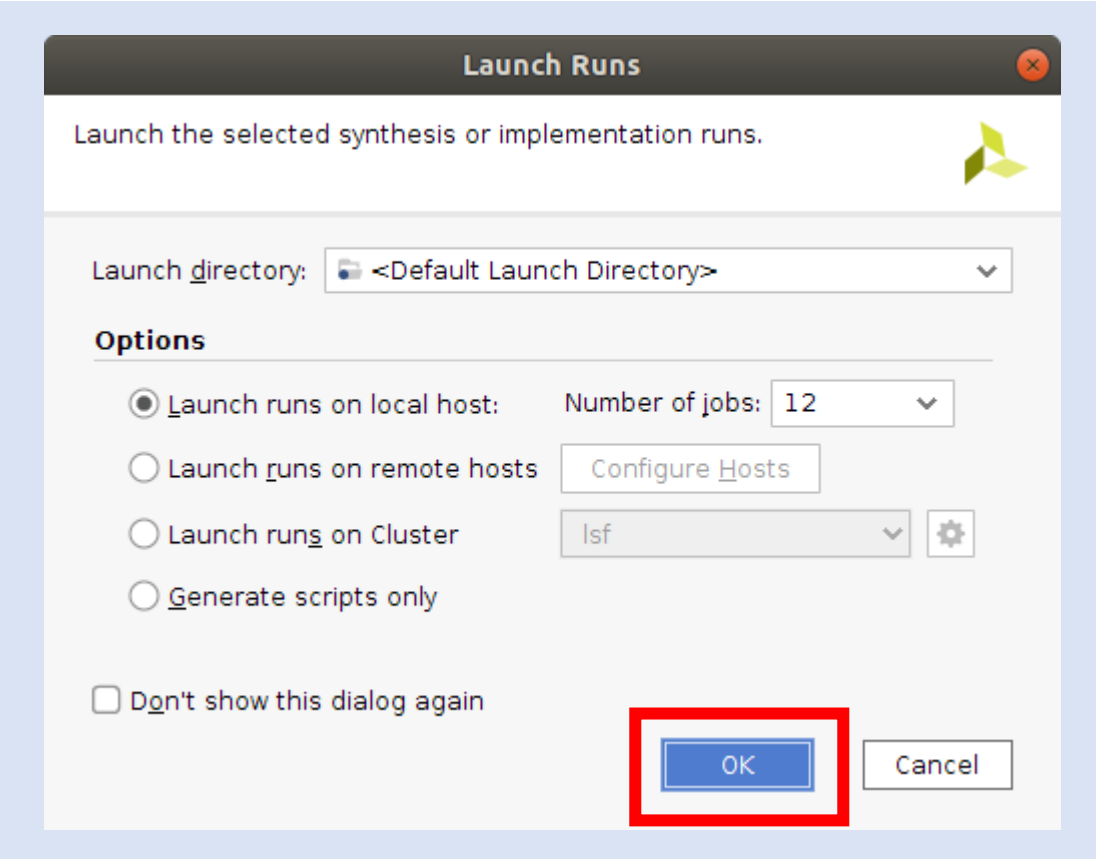
Step 44 – Select **OK** on the Lunch Runs dialog.



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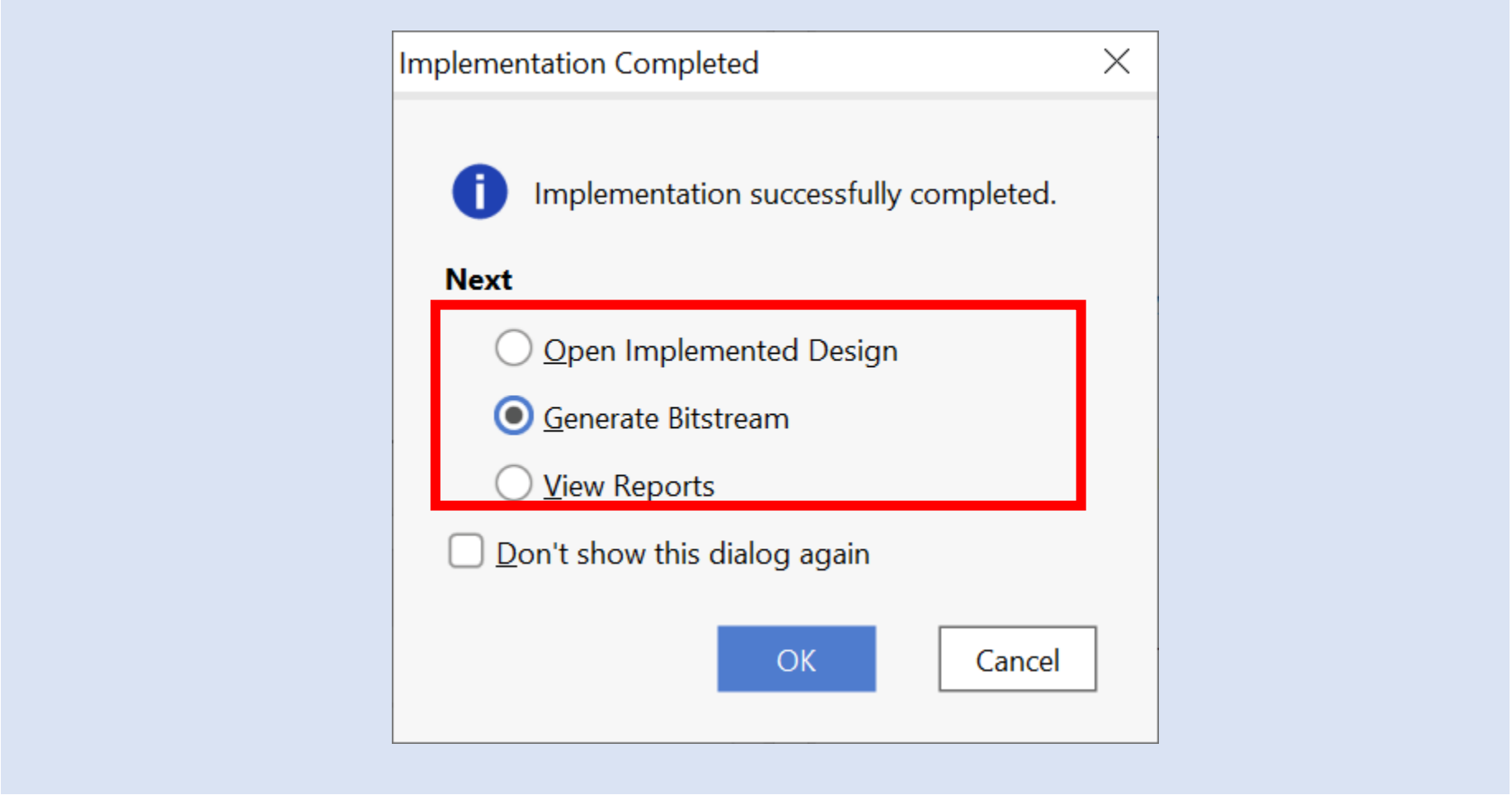
Step 45 – When the implementation completes, you will see a dialog appear. Select **Generate Bitstream**.



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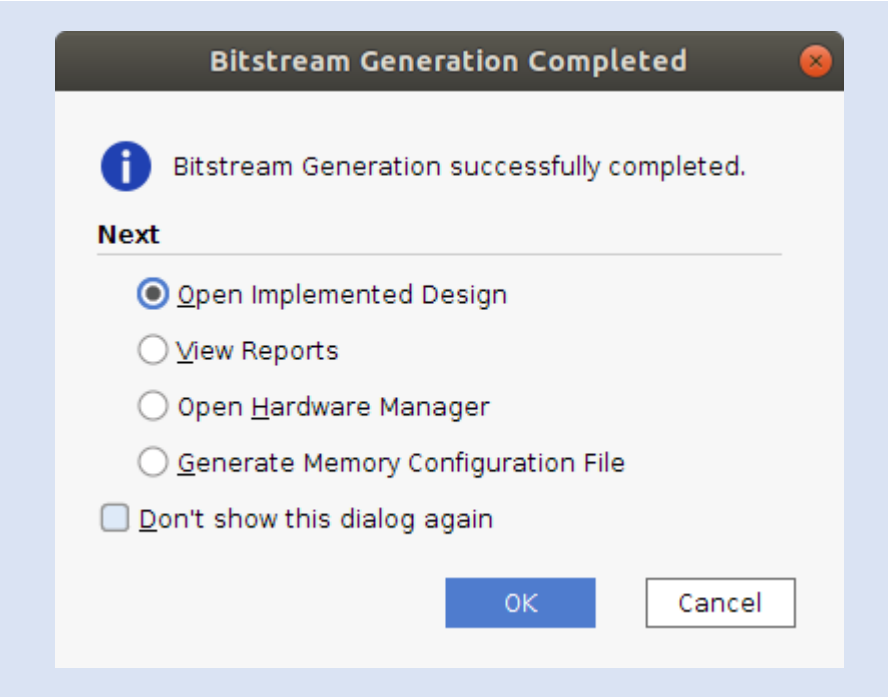
Step 46 – A dialog box will appear when the bitstream generates. Congratulations you have completed your first Vivado FPGA implementation.

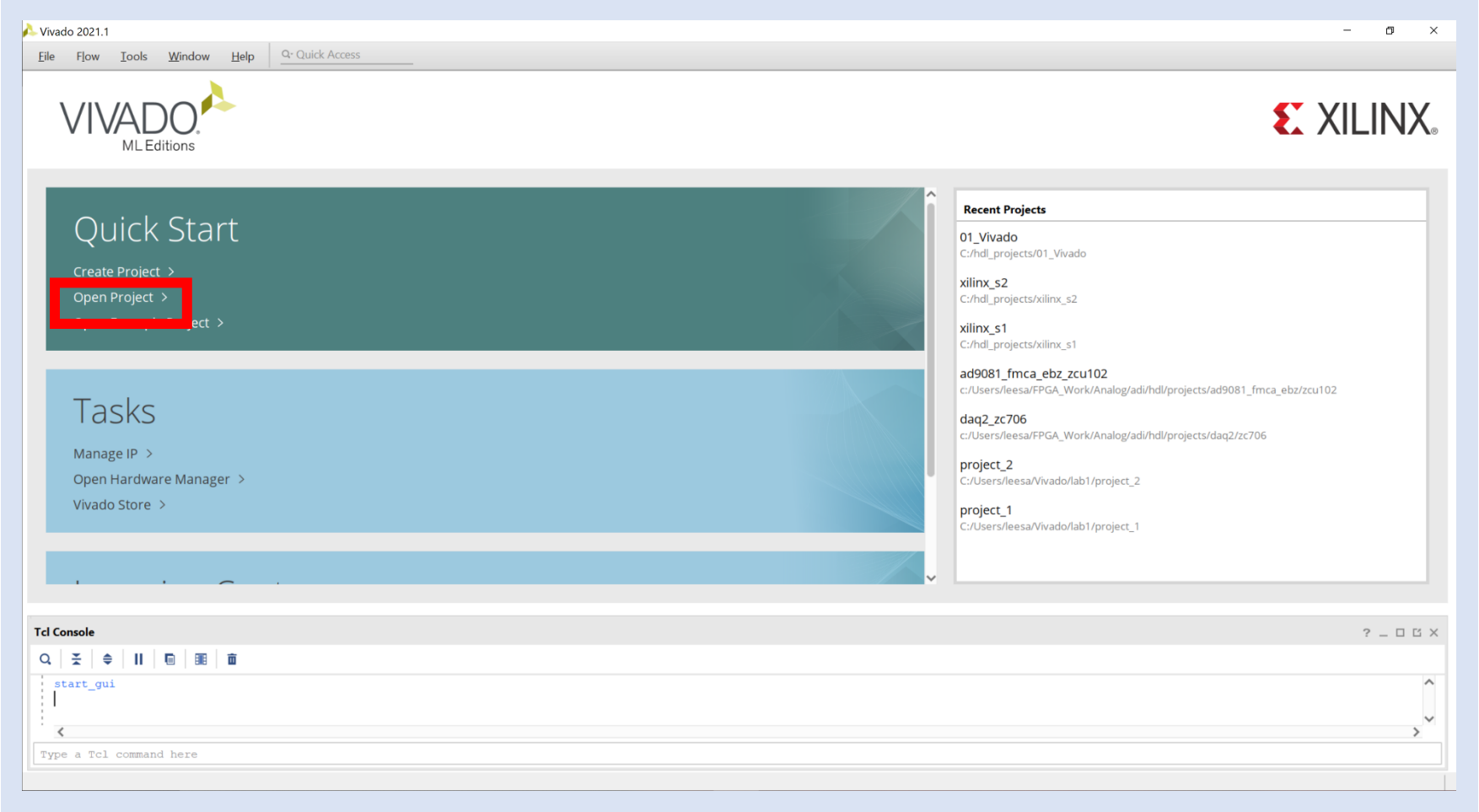


Lab 5

Intermediate Vivado

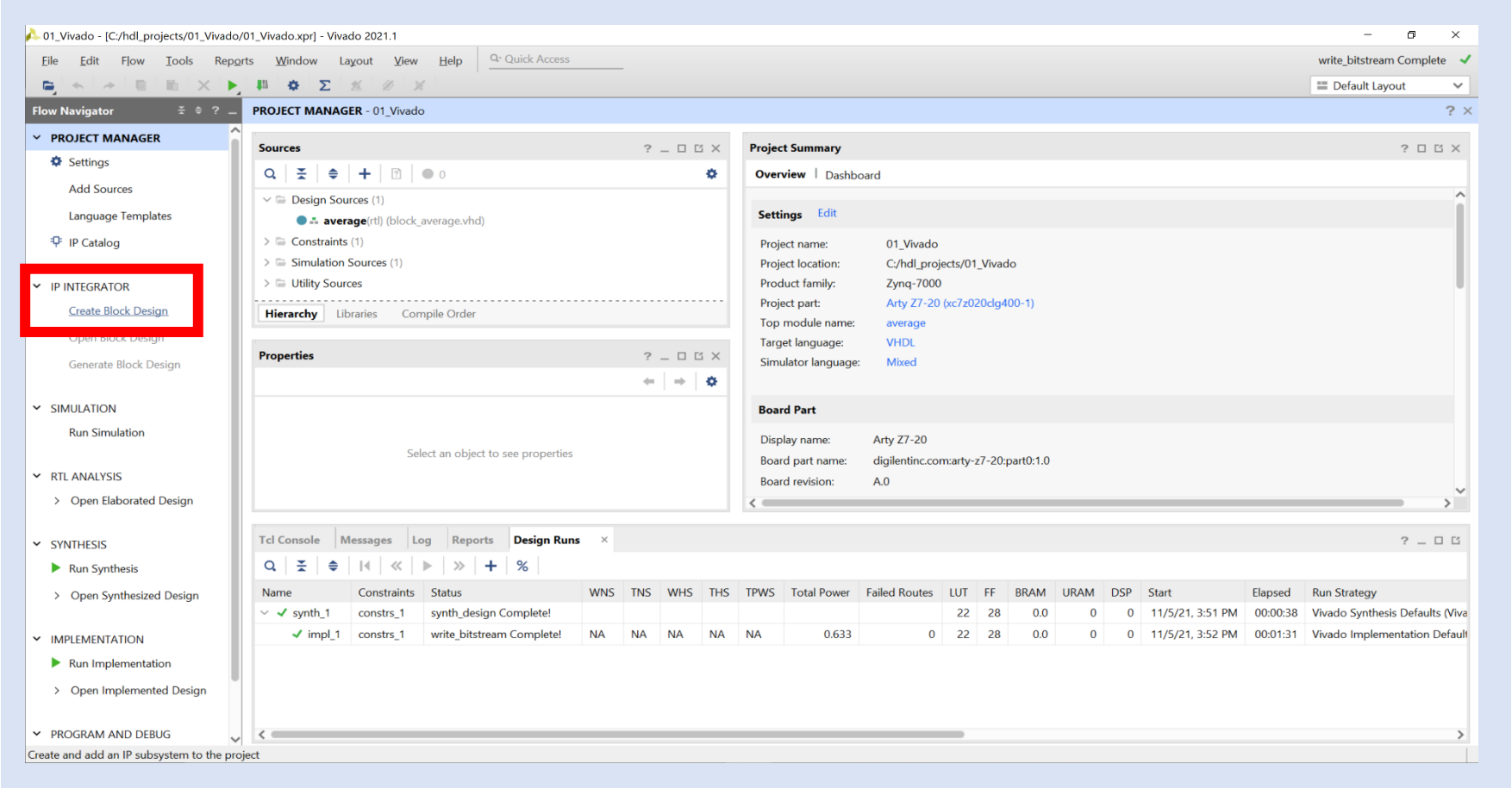
Lab 5: Intermediate Vivado

Step 1 – Open the project created in part one.



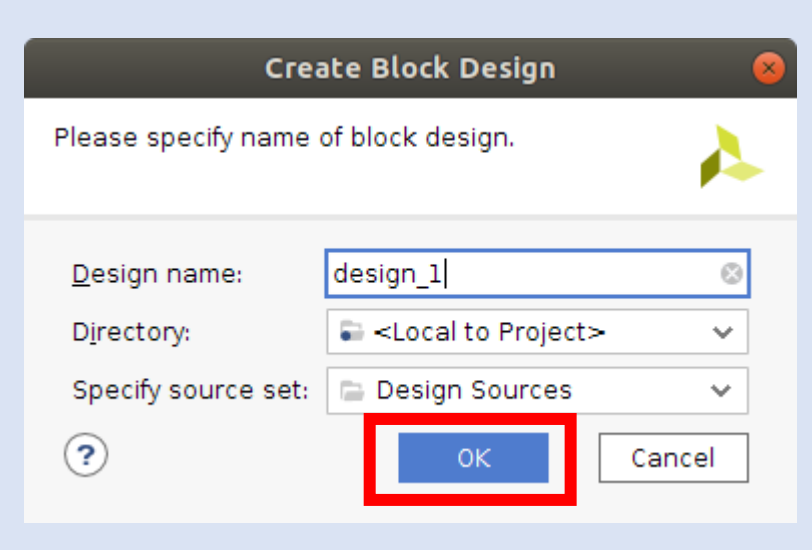
Lab 5: Intermediate Vivado

Step 2 – This will open in project management view. Click on **Create Block Diagram**.



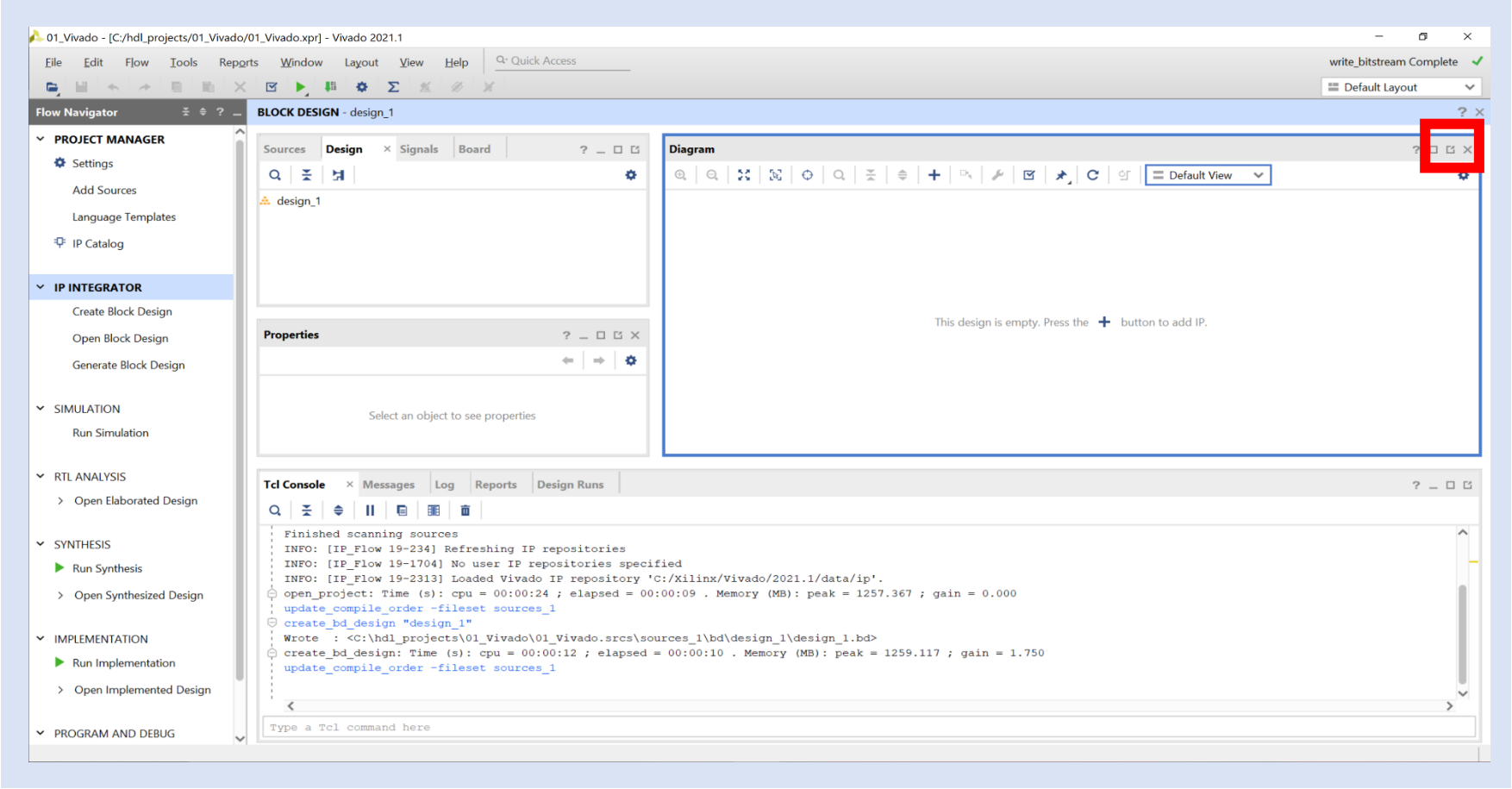
Lab 5: Intermediate Vivado

Step 3 – Leave the predefined name and locations unchanged and click **OK**.



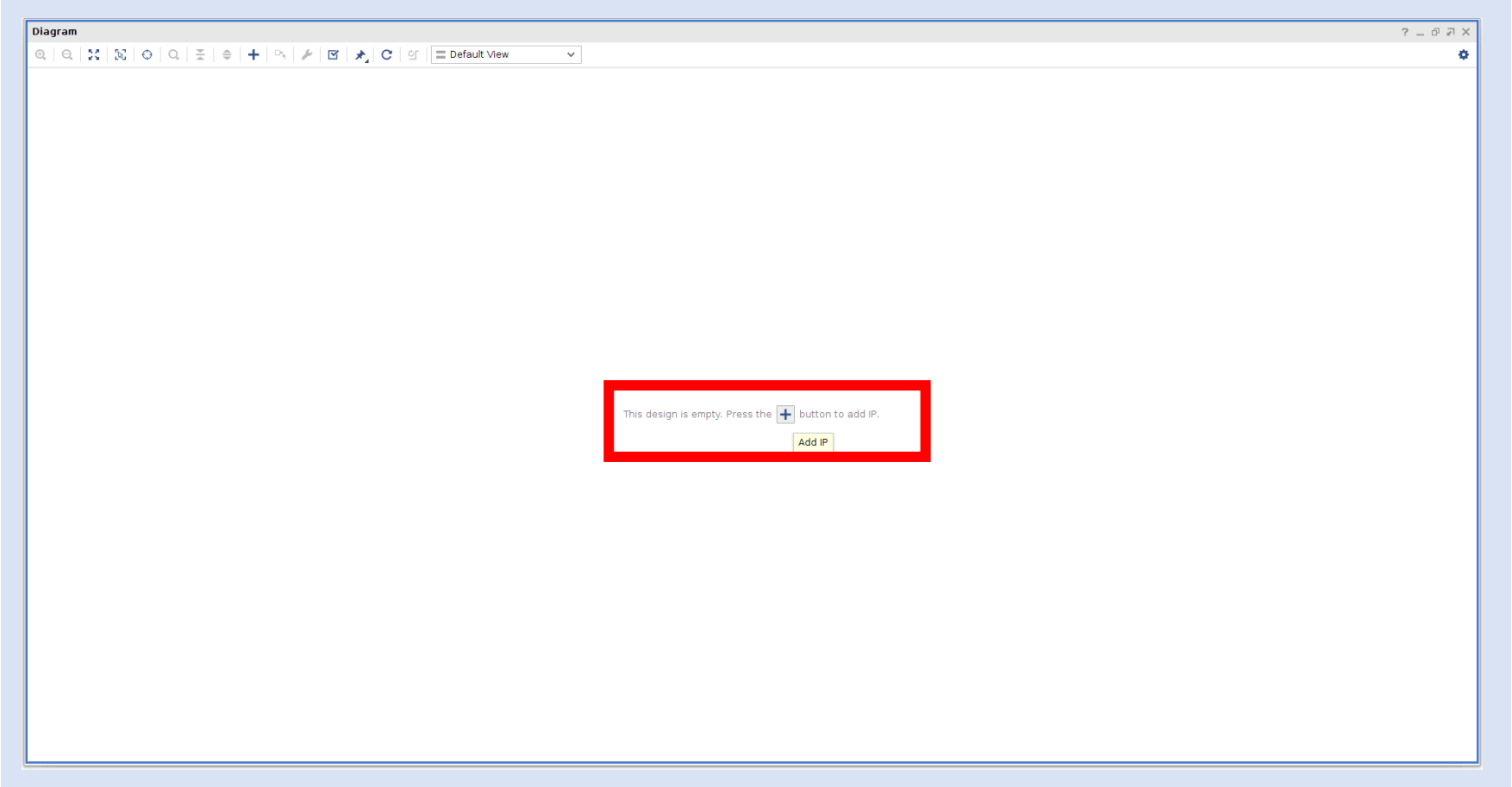
Lab 5: Intermediate Vivado

Step 4 – Undock the block diagram window and maximize it.



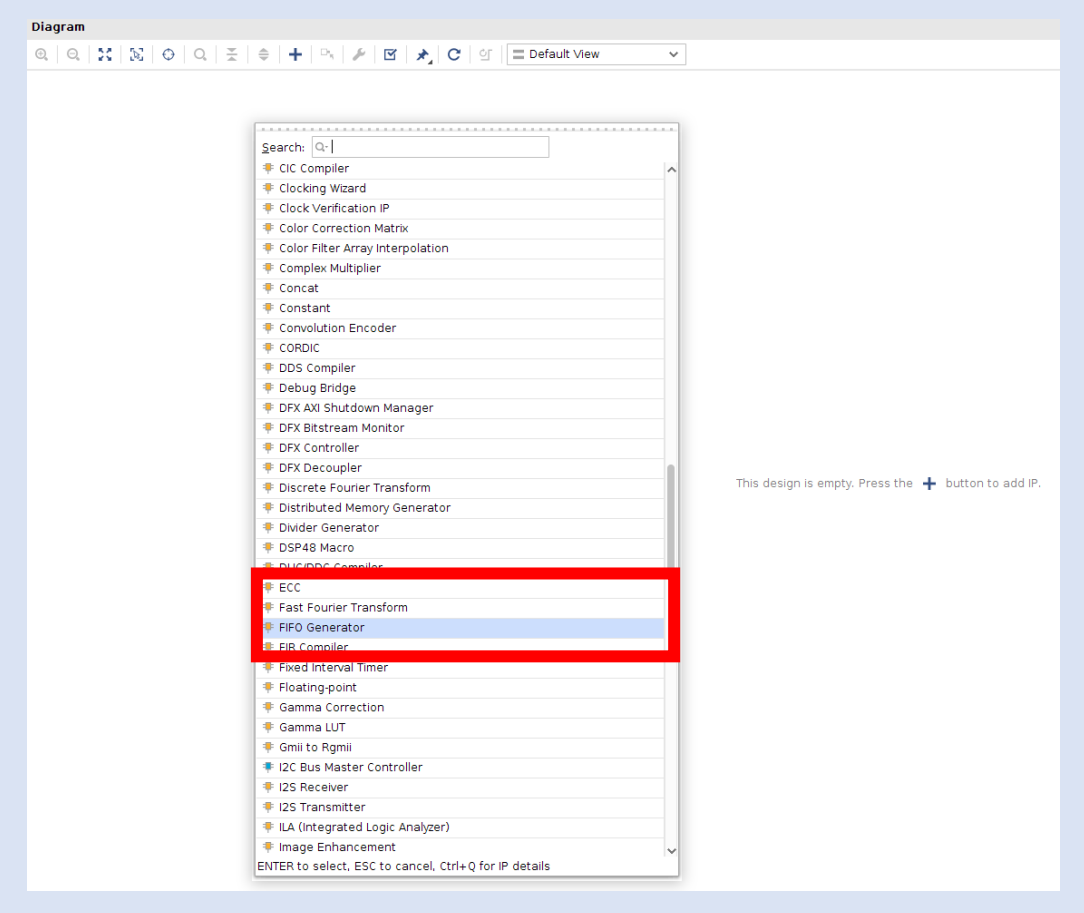
Lab 5: Intermediate Vivado

Step 5 – We are going to add in new IP. Click on the **+ button**.



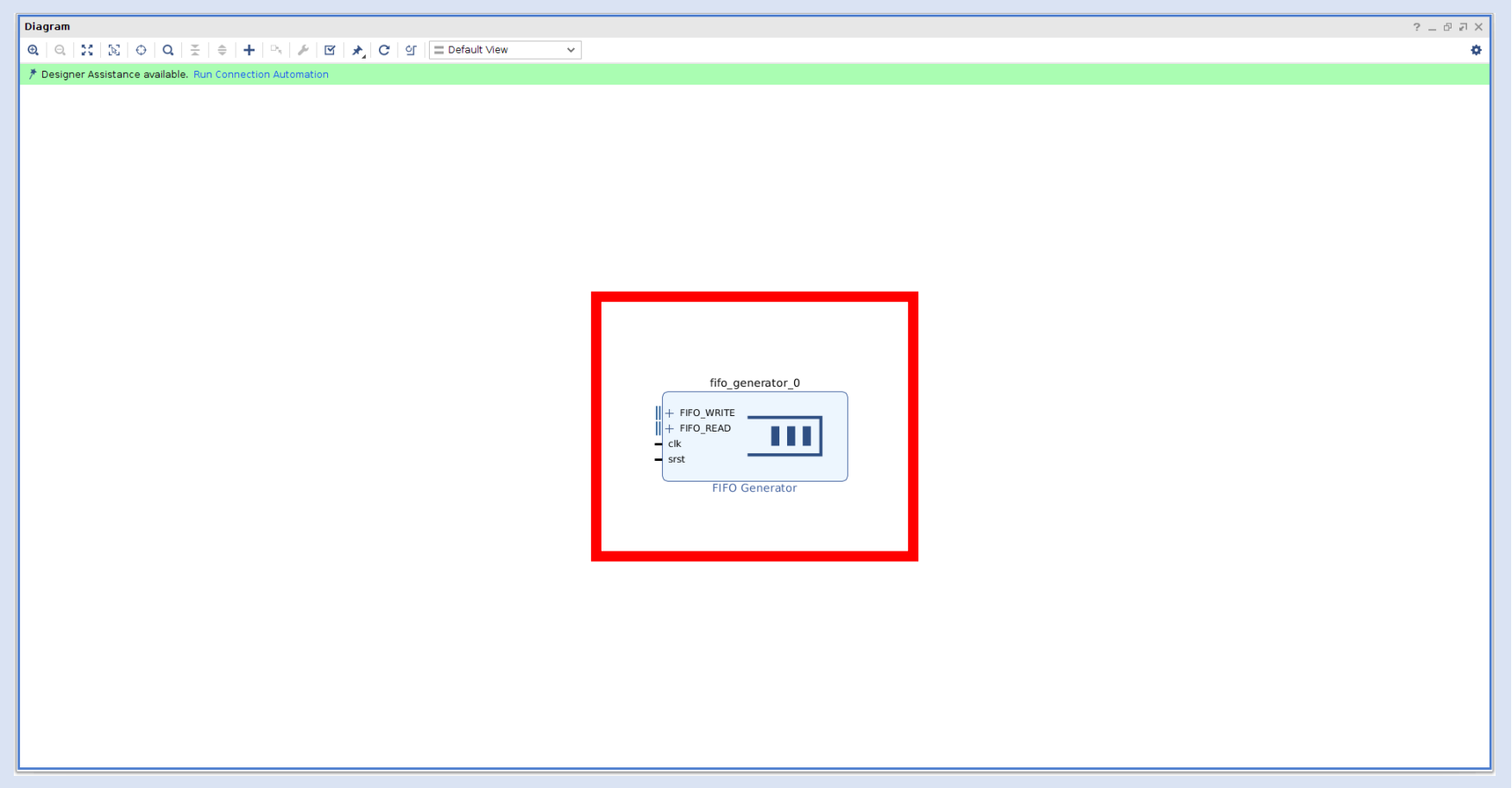
Lab 5: Intermediate Vivado

Step 6 – Select the **FIFO Generator**. This will add a FIFO to the block diagram.



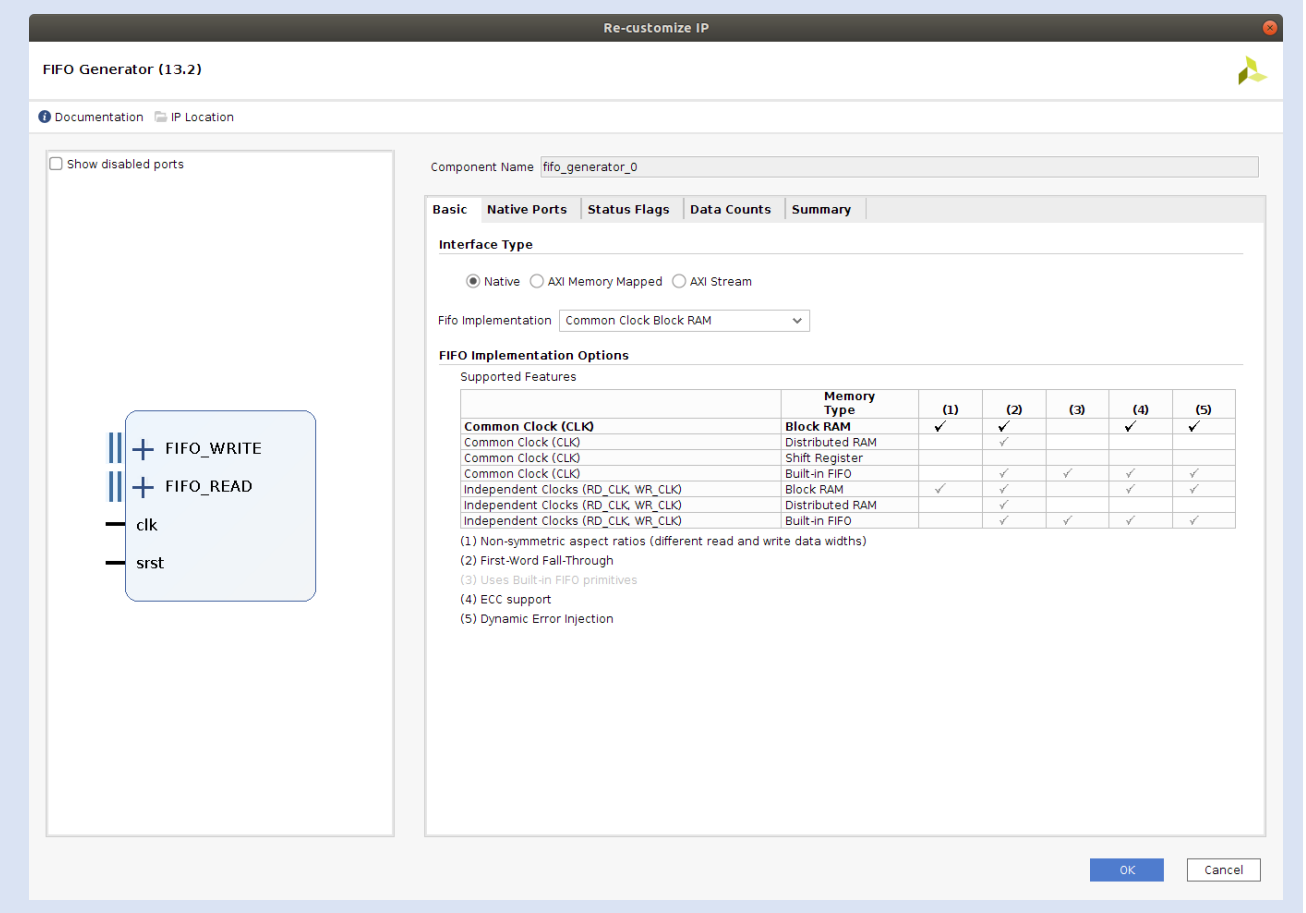
Lab 5: Intermediate Vivado

Step 7 – Double click on the **FIFO Generator** to customize it.



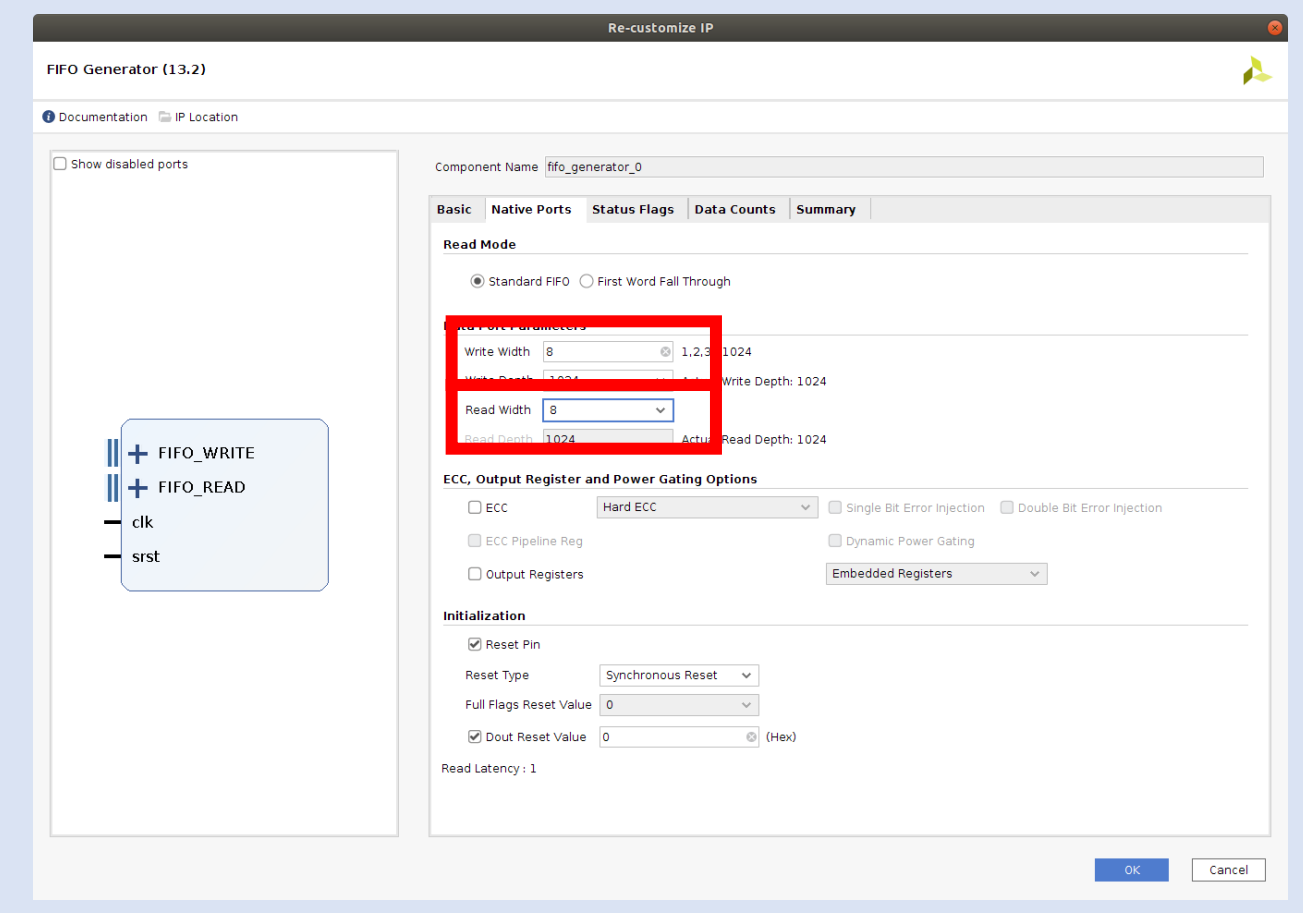
Lab 5: Intermediate Vivado

Step 8 – Leave the first page unchanged.



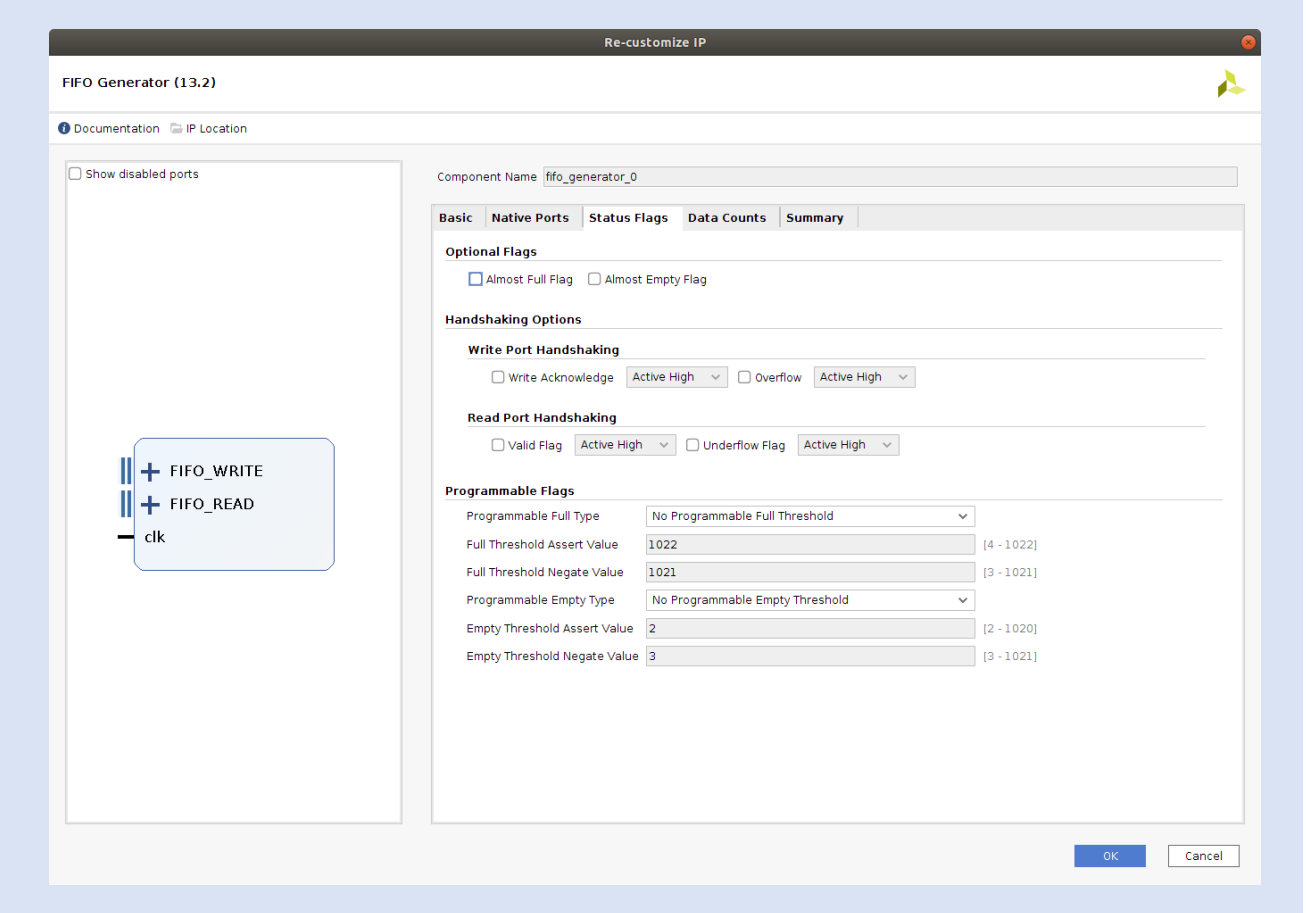
Lab 5: Intermediate Vivado

Step 9 – Change the Write and Read Width to be **8 bits**.



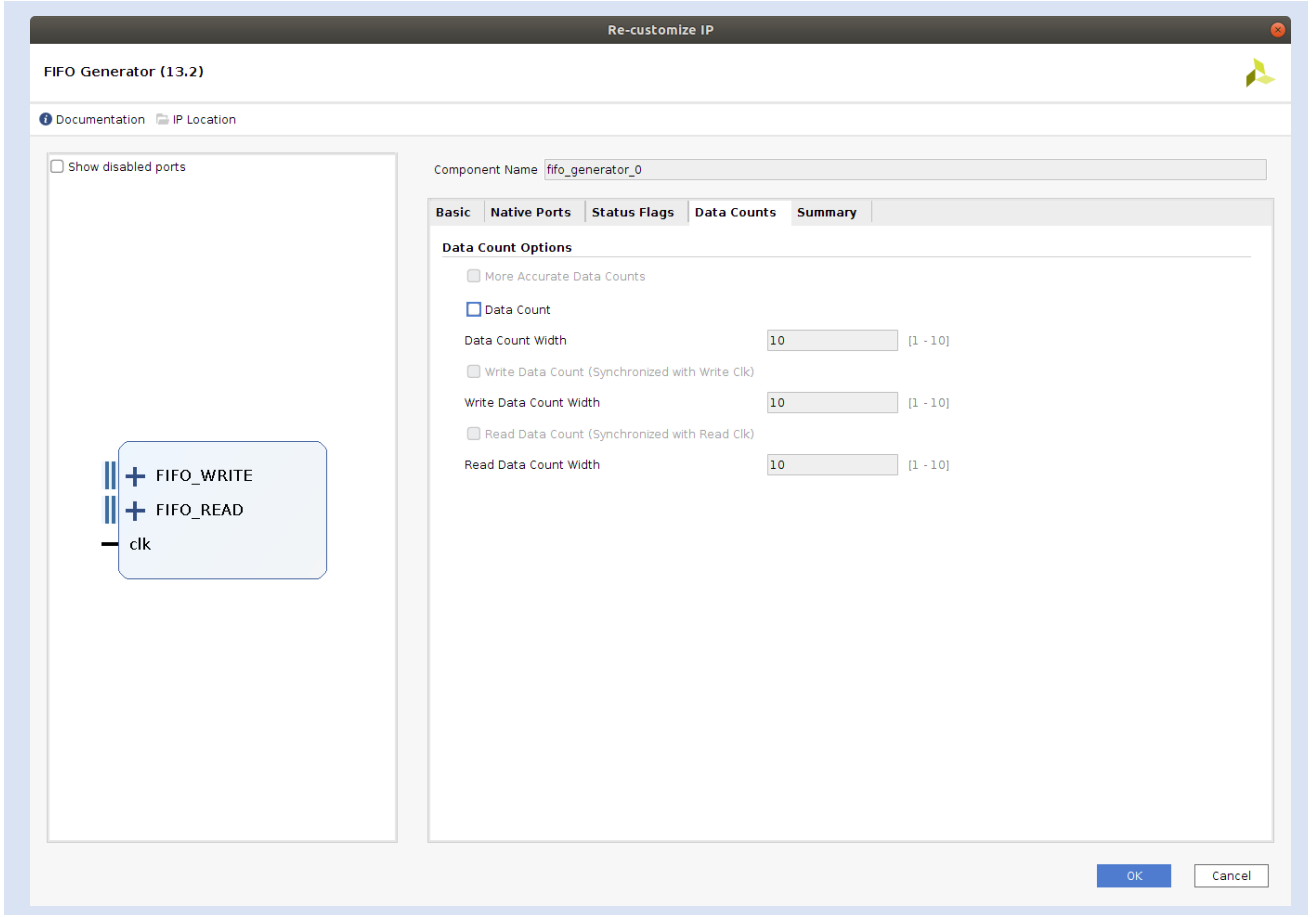
Lab 5: Intermediate Vivado

Step 10 – Leave the third page unchanged.



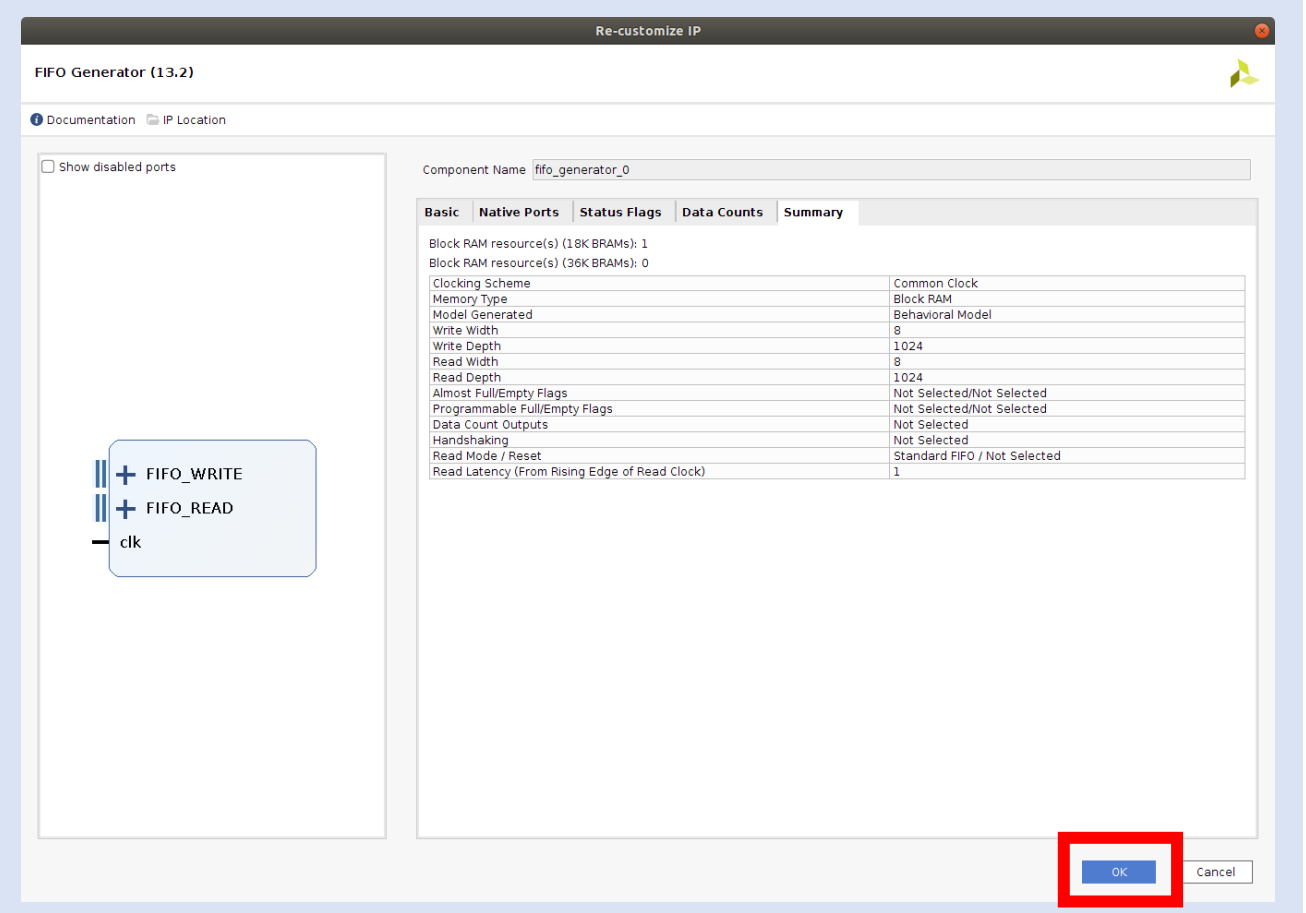
Lab 5: Intermediate Vivado

Step 11 – Leave the fourth page unchanged.



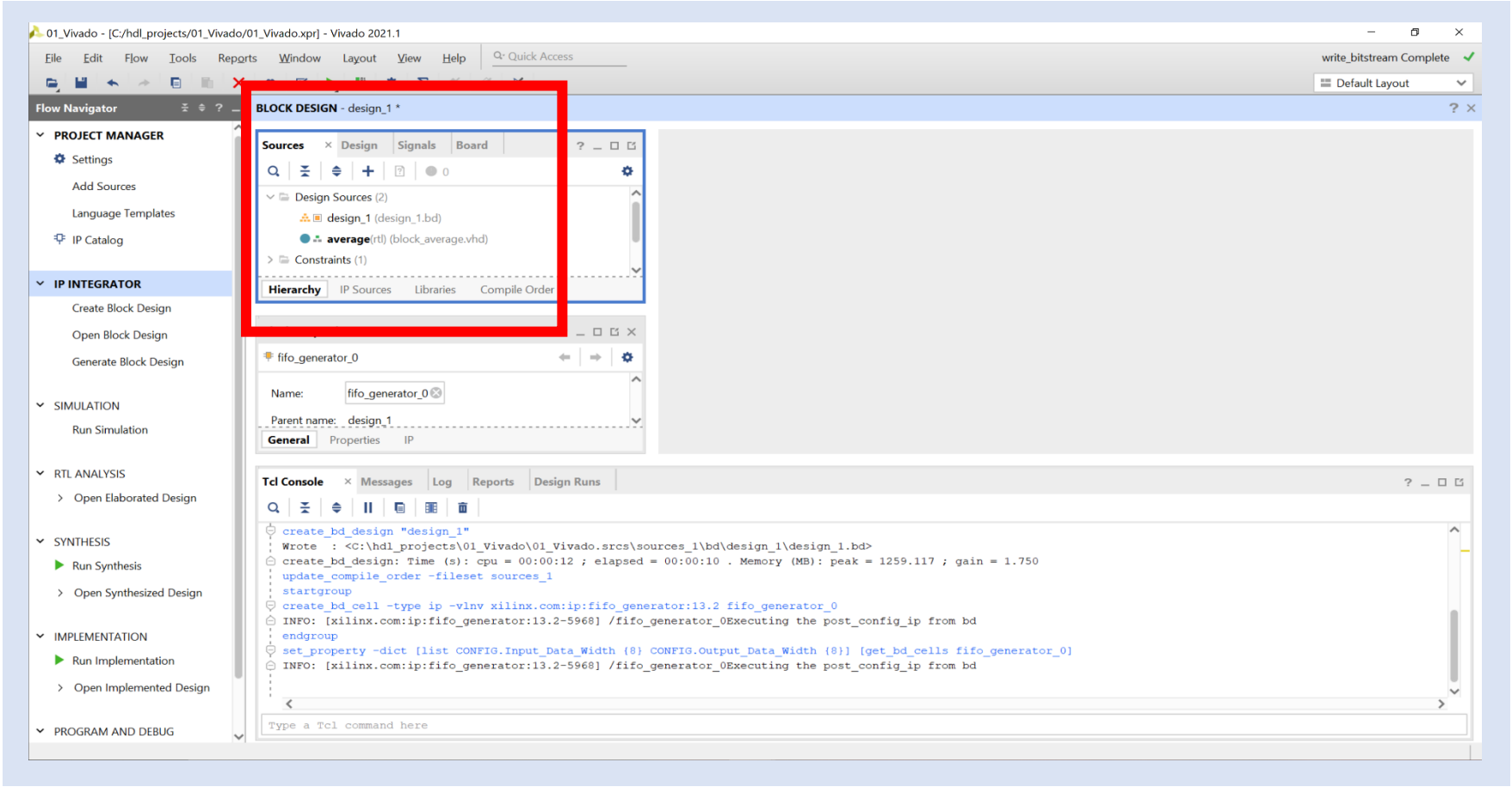
Lab 5: Intermediate Vivado

Step 12 – Leave the final page unchanged. Note that the FIFO OP are unregistered. Click **OK**.



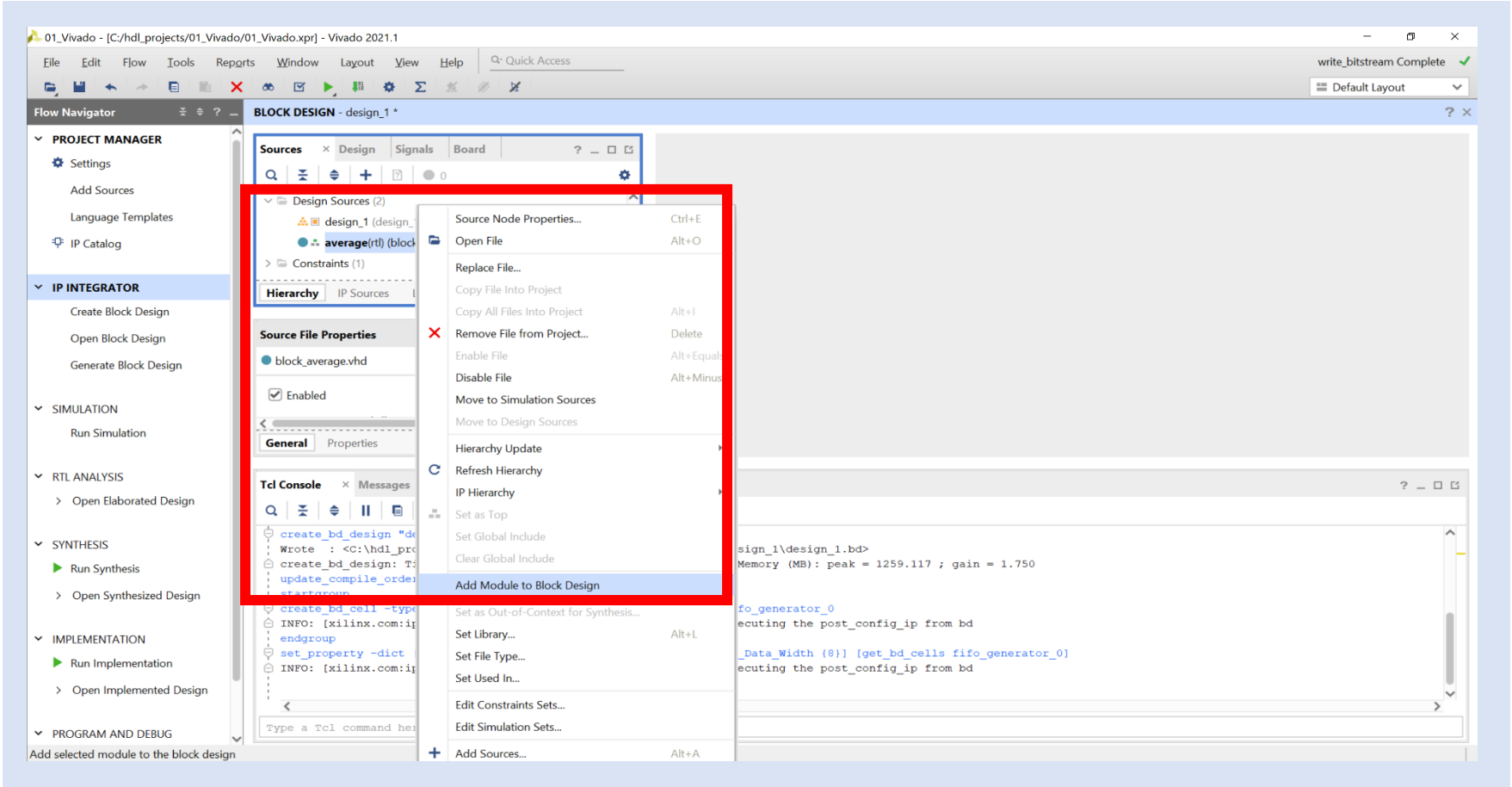
Lab 5: Intermediate Vivado

Step 13 – Click back on the Vivado Project Management view you will see the block diagram under the design sources.



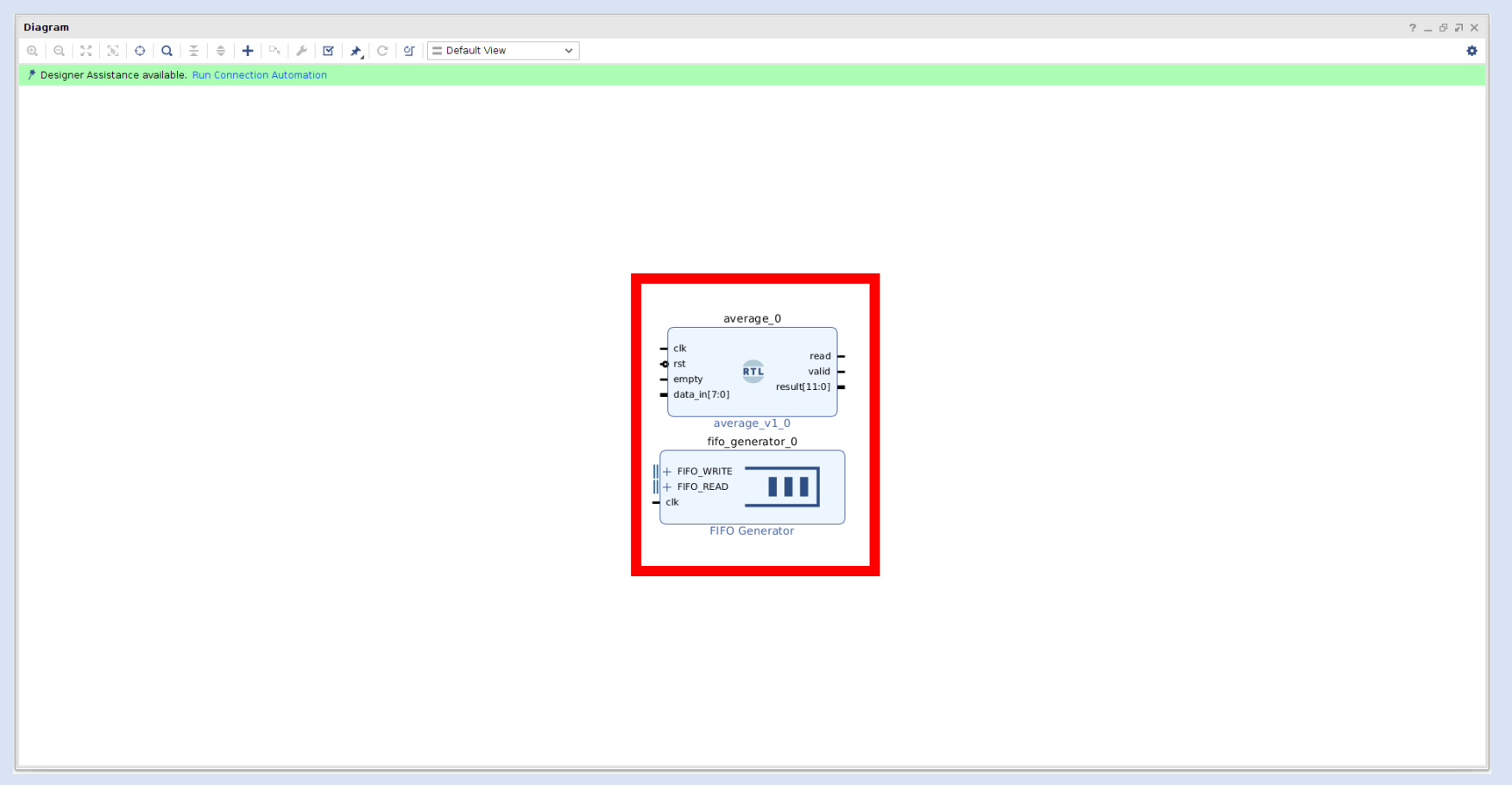
Lab 5: Intermediate Vivado

Step 14 – Right click on the average RTL block and select **Add Module to Block Design**.



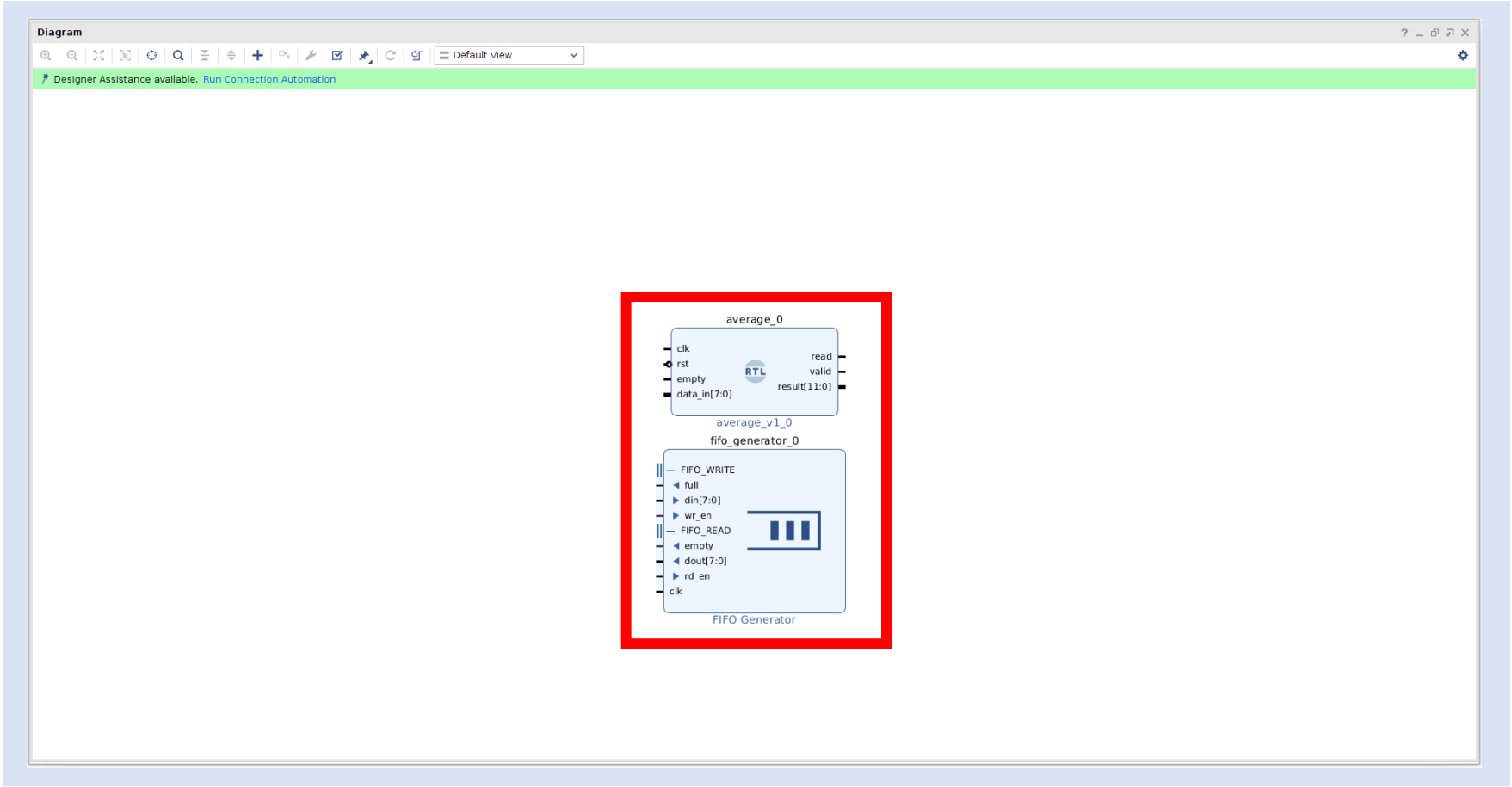
Lab 5: Intermediate Vivado

Step 15 – This will add the average block to the block diagram.



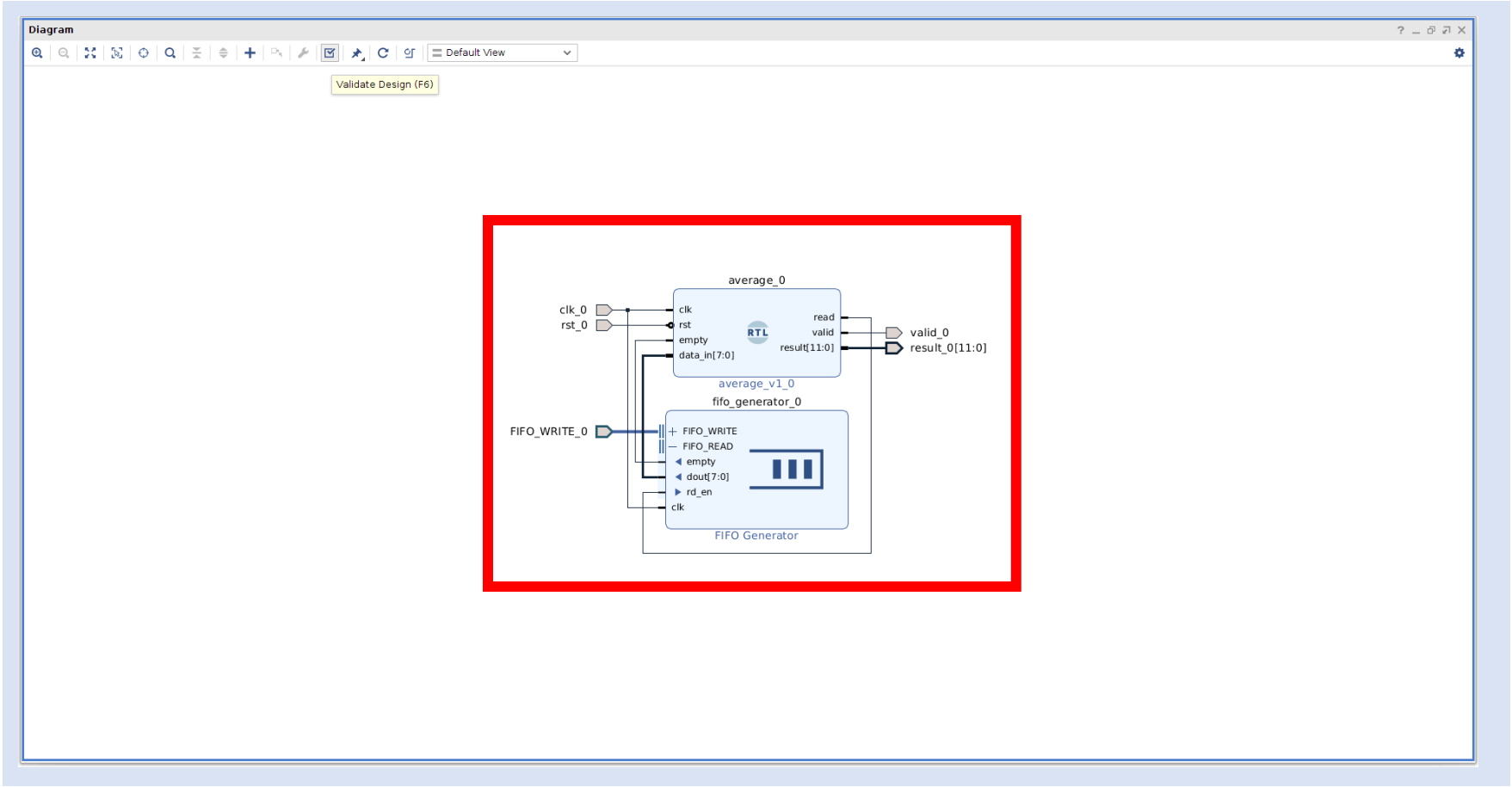
Lab 5: Intermediate Vivado

Step 16 – Expand the FIFO Write and Read Interfaces.



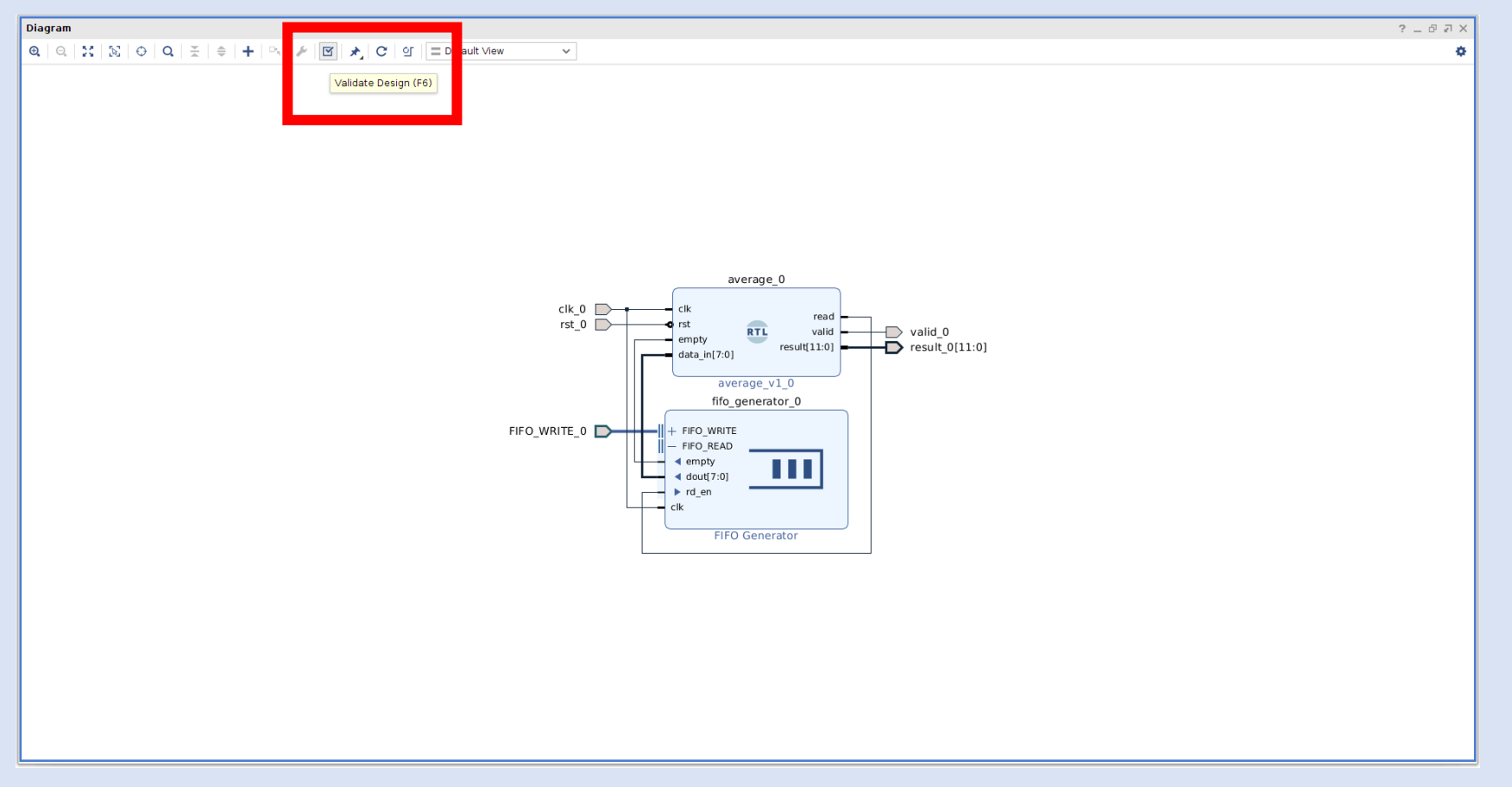
Lab 5: Intermediate Vivado

Step 17 – Make the Clk, Reset, Result, Valid and FIFO Write interfaces external by right-clicking on each pin and selecting **Make External**. Connect the remaining interfaces as below.



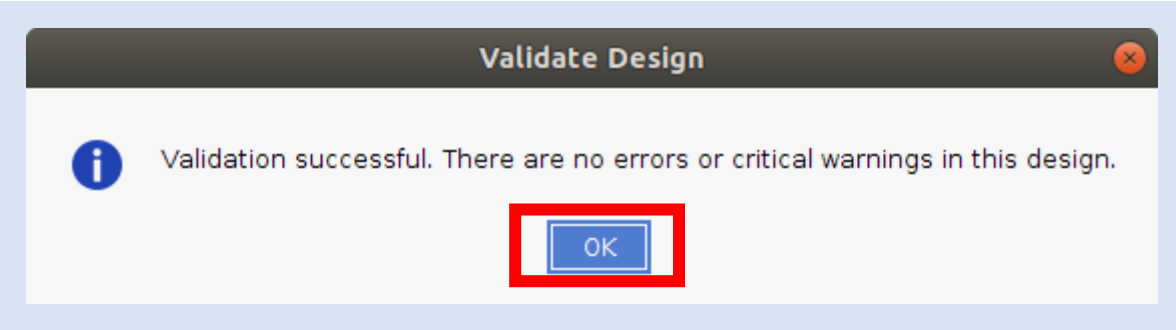
Lab 5: Intermediate Vivado

Step 18 – Click on **Validate Design**.



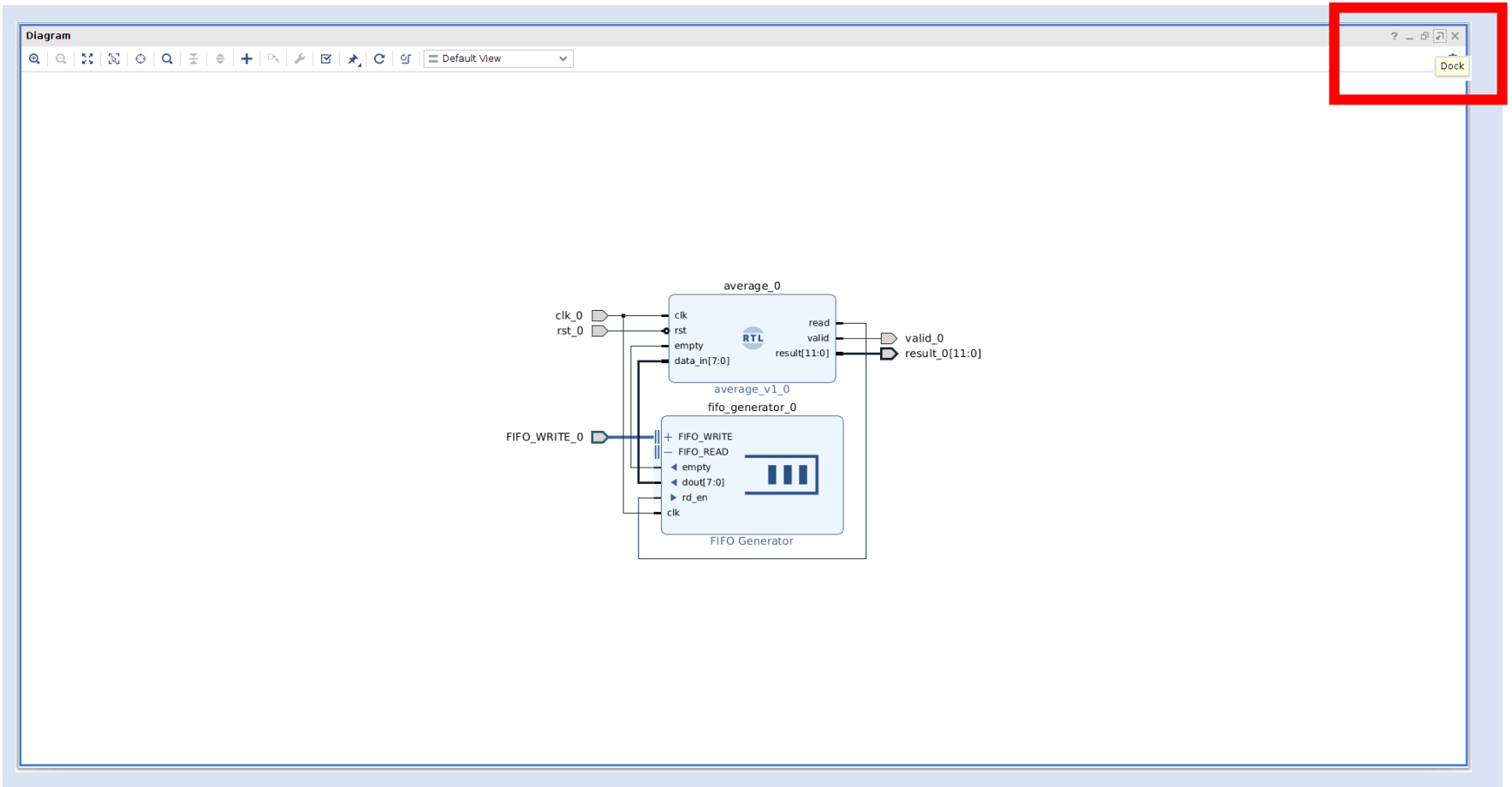
Lab 5: Intermediate Vivado

Step 19 – The validated design should result in no error or critical warnings. Click **OK**.



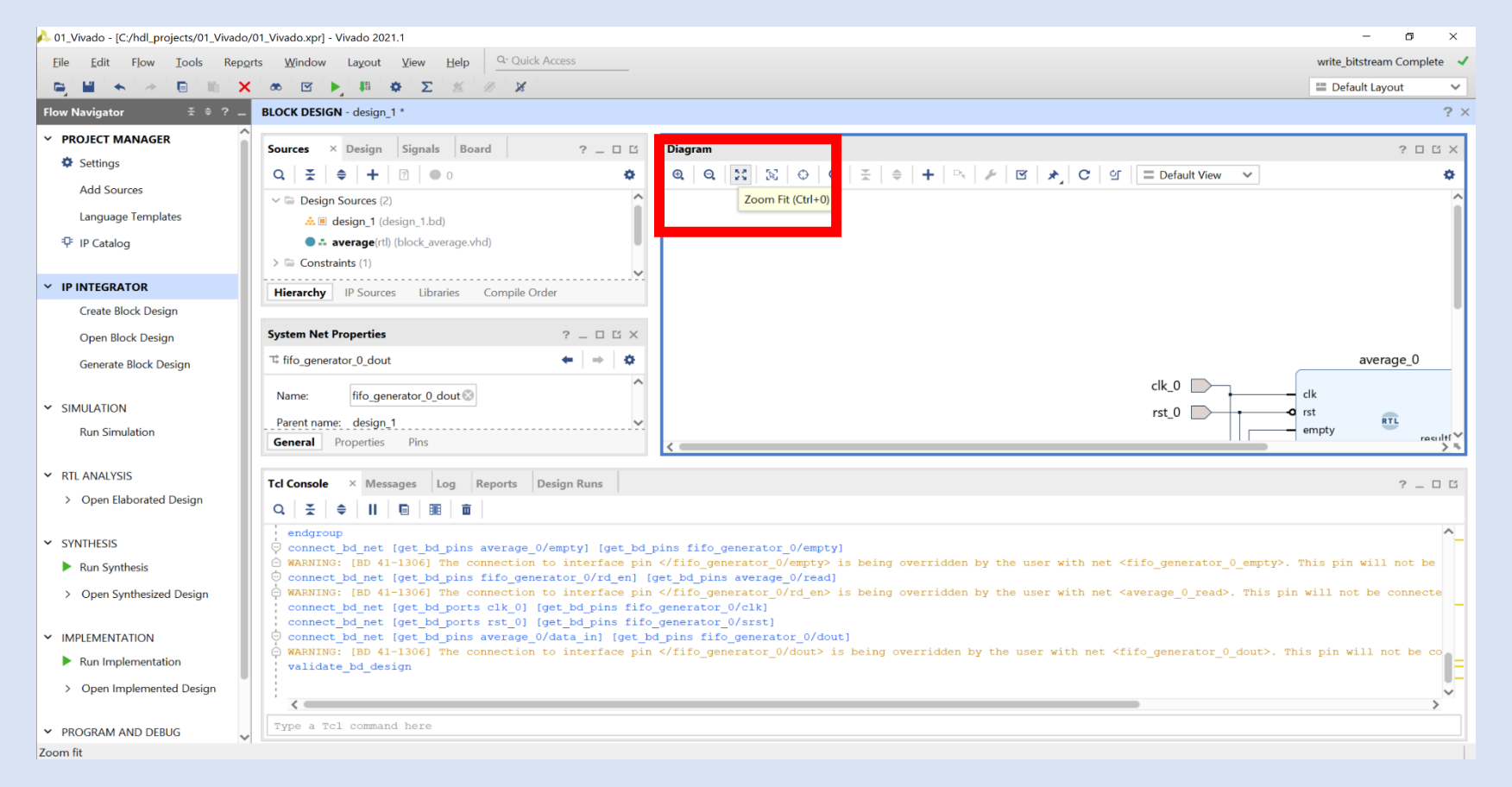
Lab 5: Intermediate Vivado

Step 20 – Re-dock the block diagram window into the Vivado Project Manager.



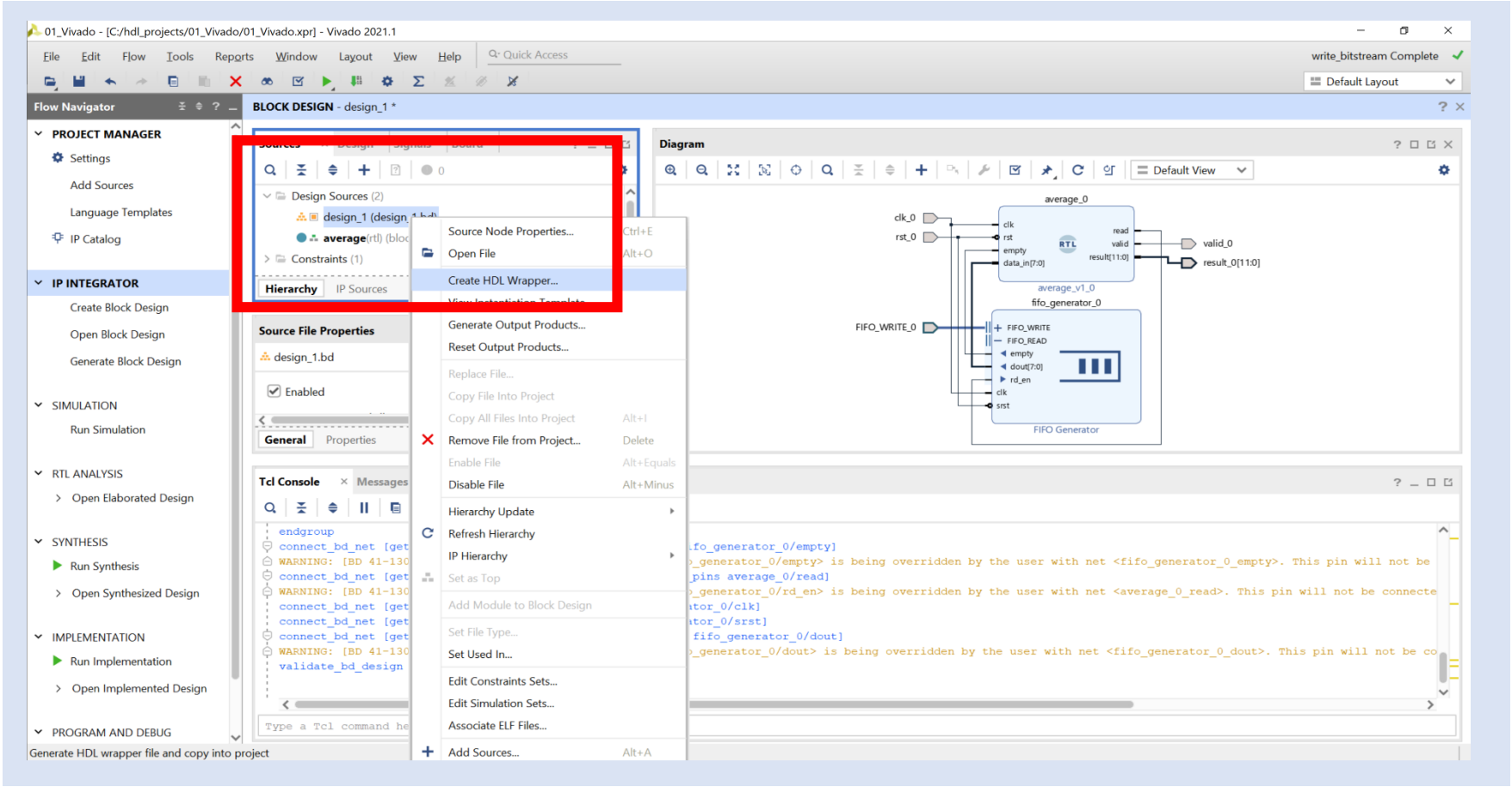
Lab 5: Intermediate Vivado

Step 21 – Click on the **Zoom Fit** button to fit the design to the window.



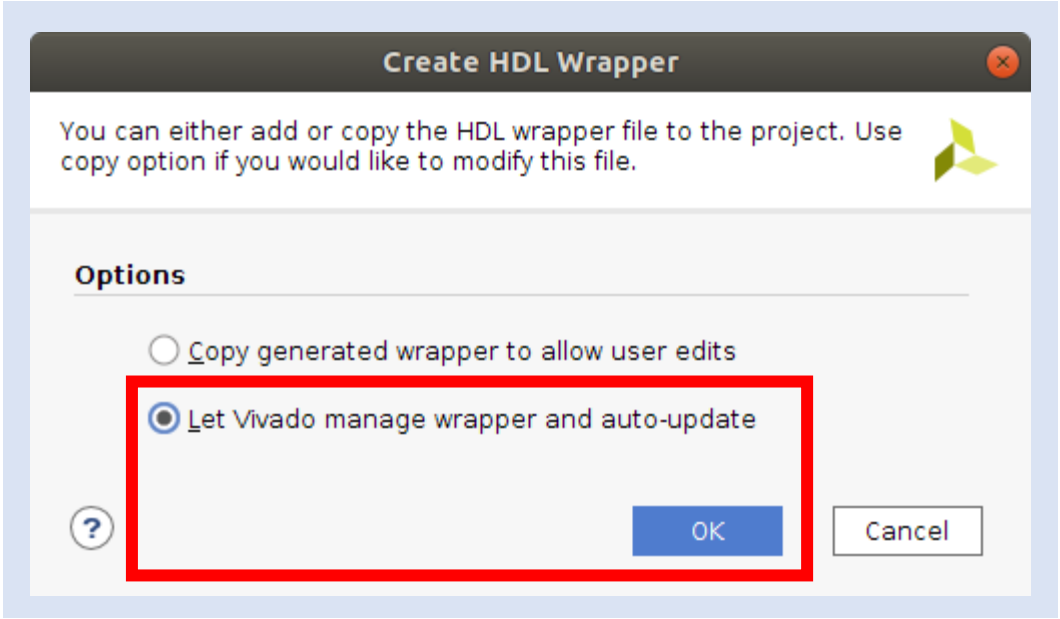
Lab 5: Intermediate Vivado

Step 22 – Right click on the block diagram design under the Design Sources tab and select **Create HDL Wrapper**.



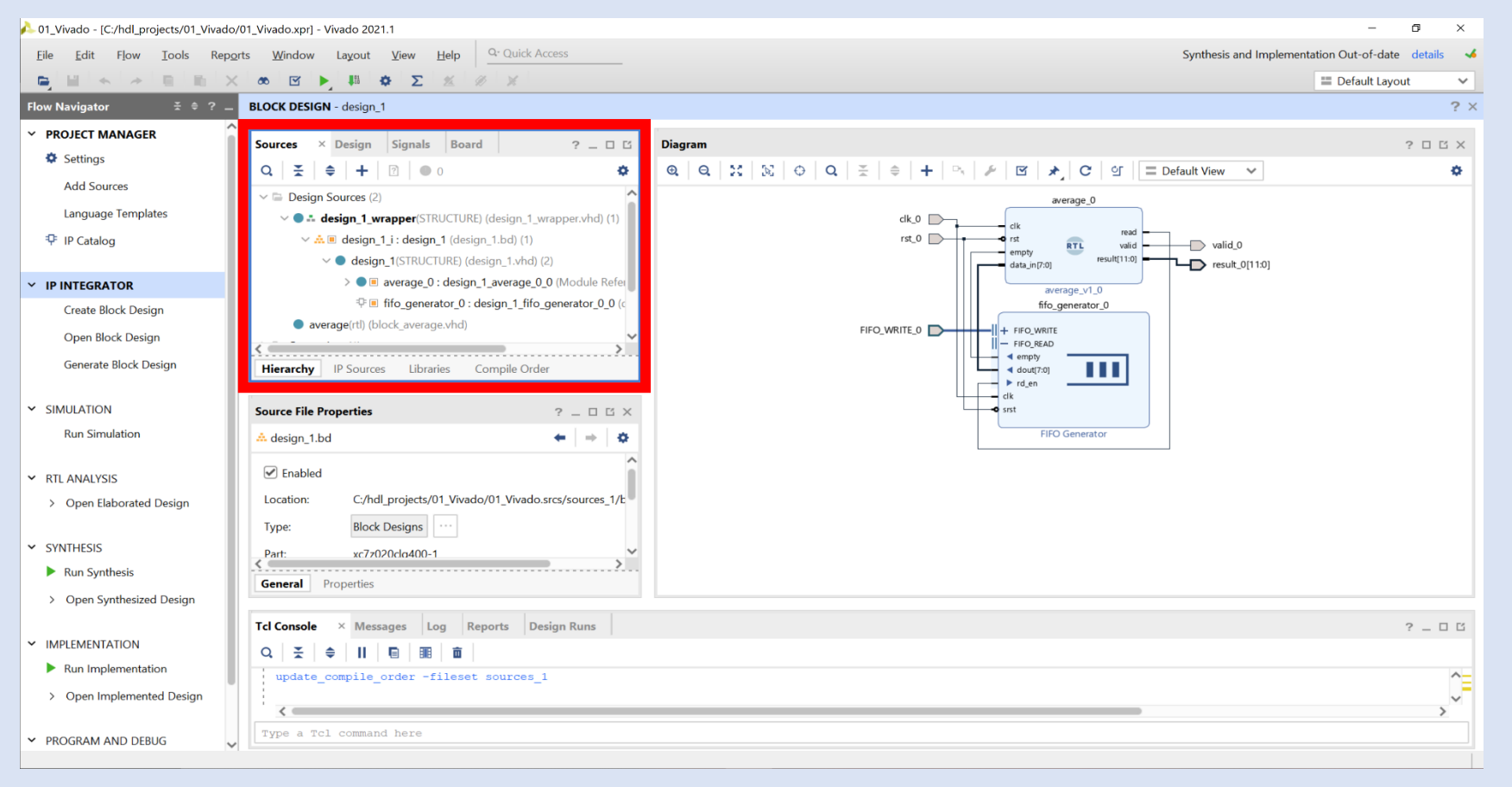
Lab 5: Intermediate Vivado

Step 23 – Allow Vivado to manage the wrapper and click **OK**.



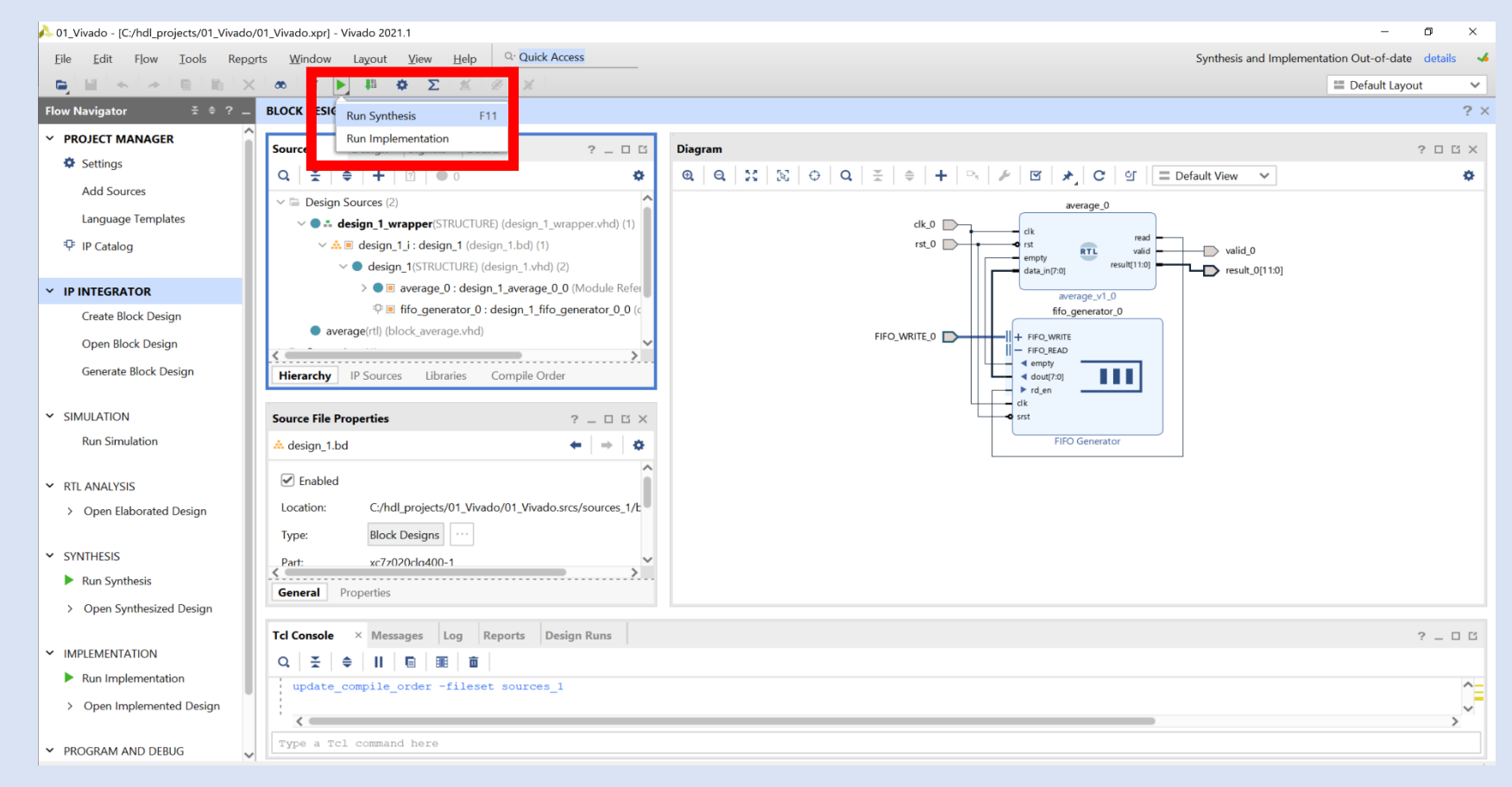
Lab 5: Intermediate Vivado

Step 24 – Expand the newly created wrapper and you will see the entire design.



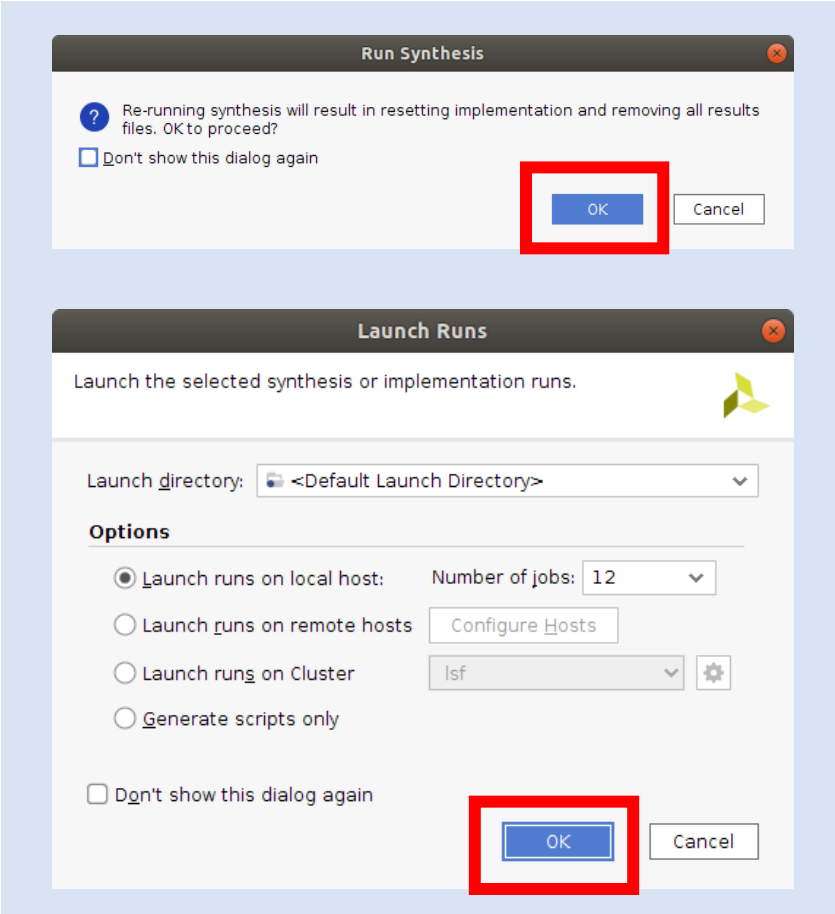
Lab 5: Intermediate Vivado

Step 25 – Run the Synthesis.



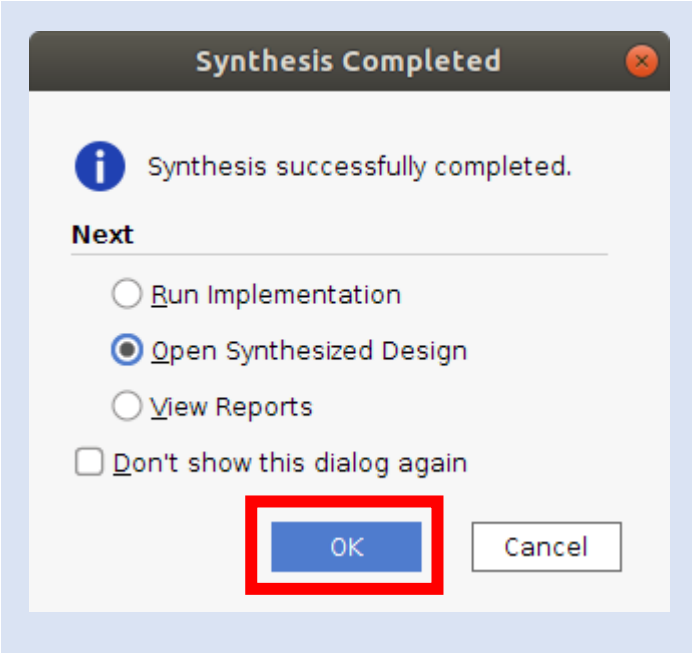
Lab 5: Intermediate Vivado

Step 26 – On both resultant dialogs click **OK** and wait for synthesis to complete.



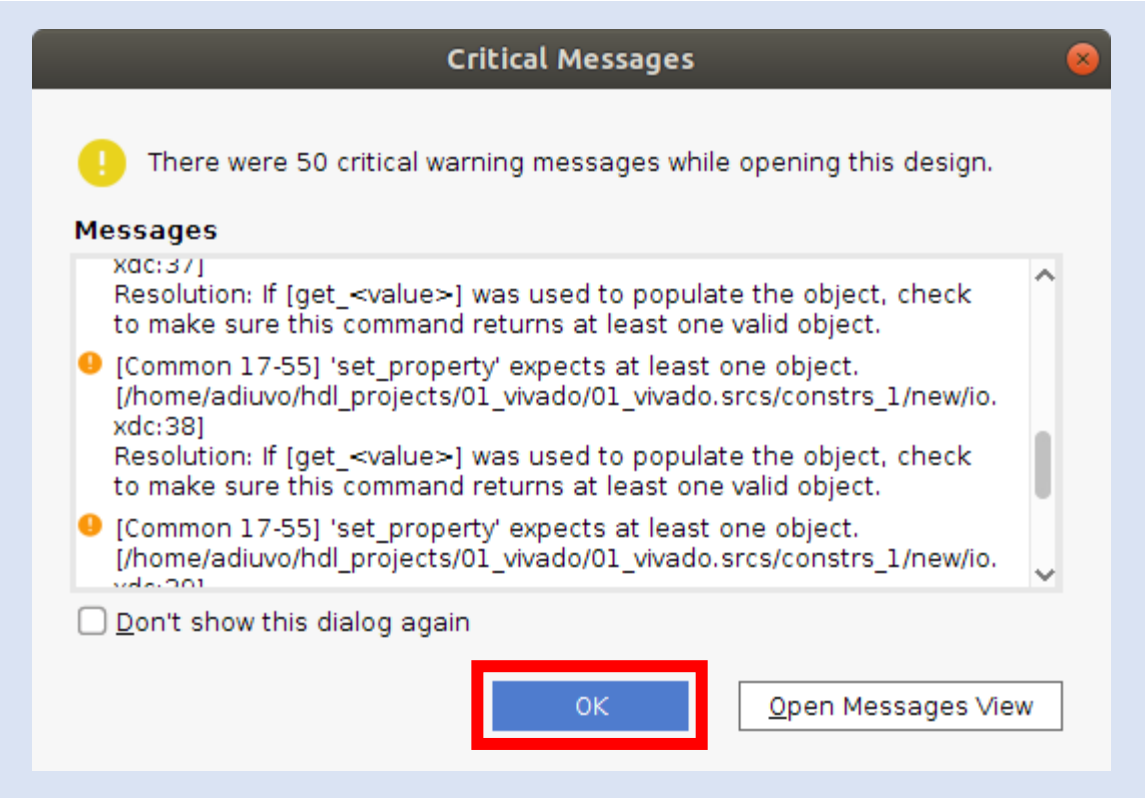
Lab 5: Intermediate Vivado

Step 27 – When synthesis completes, **Open the Synthesized Design.**



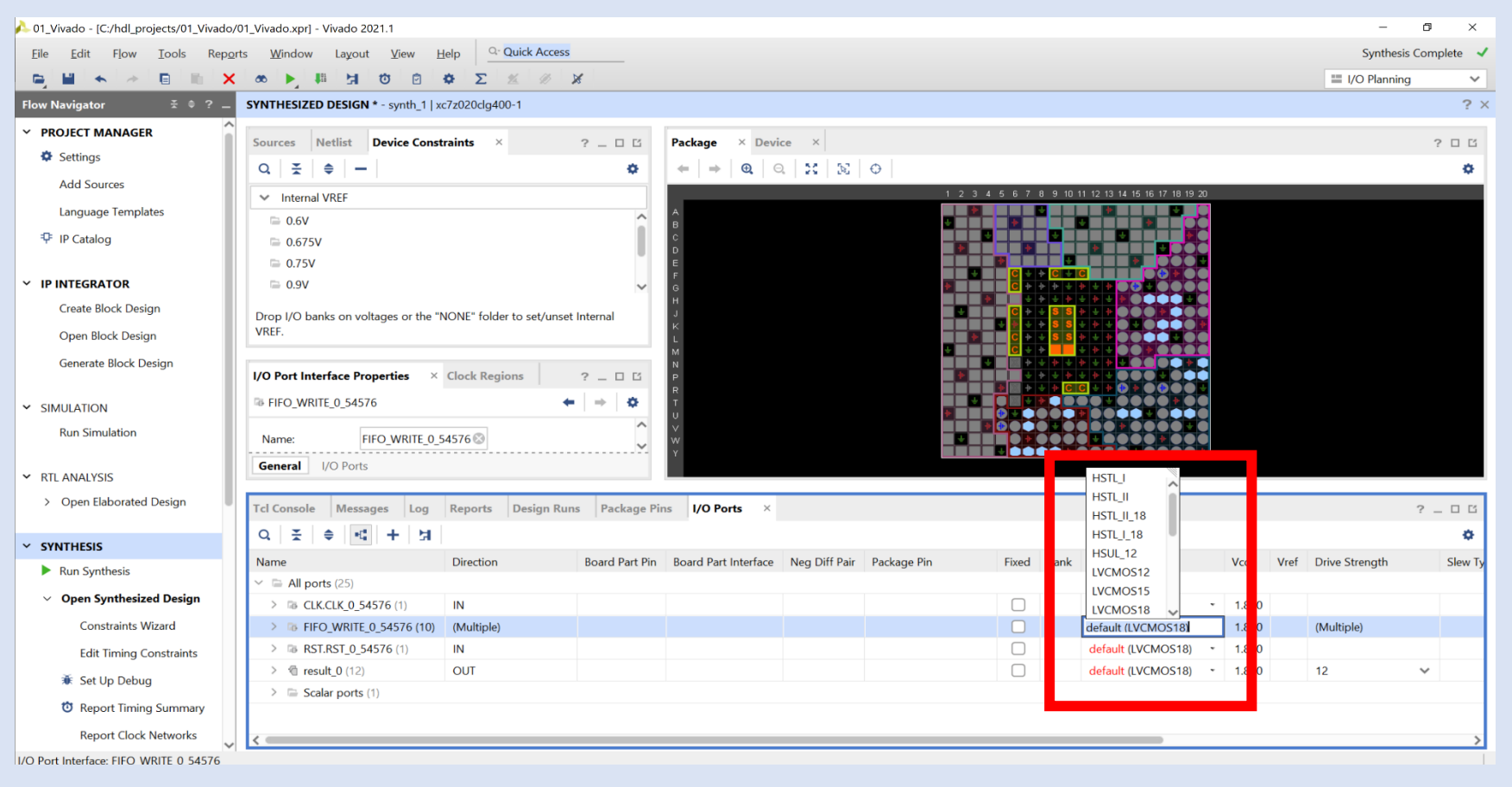
Lab 5: Intermediate Vivado

Step 28 – If any critical warnings pop up, select **OK.** This is due to out of data constraints which we are about to address.



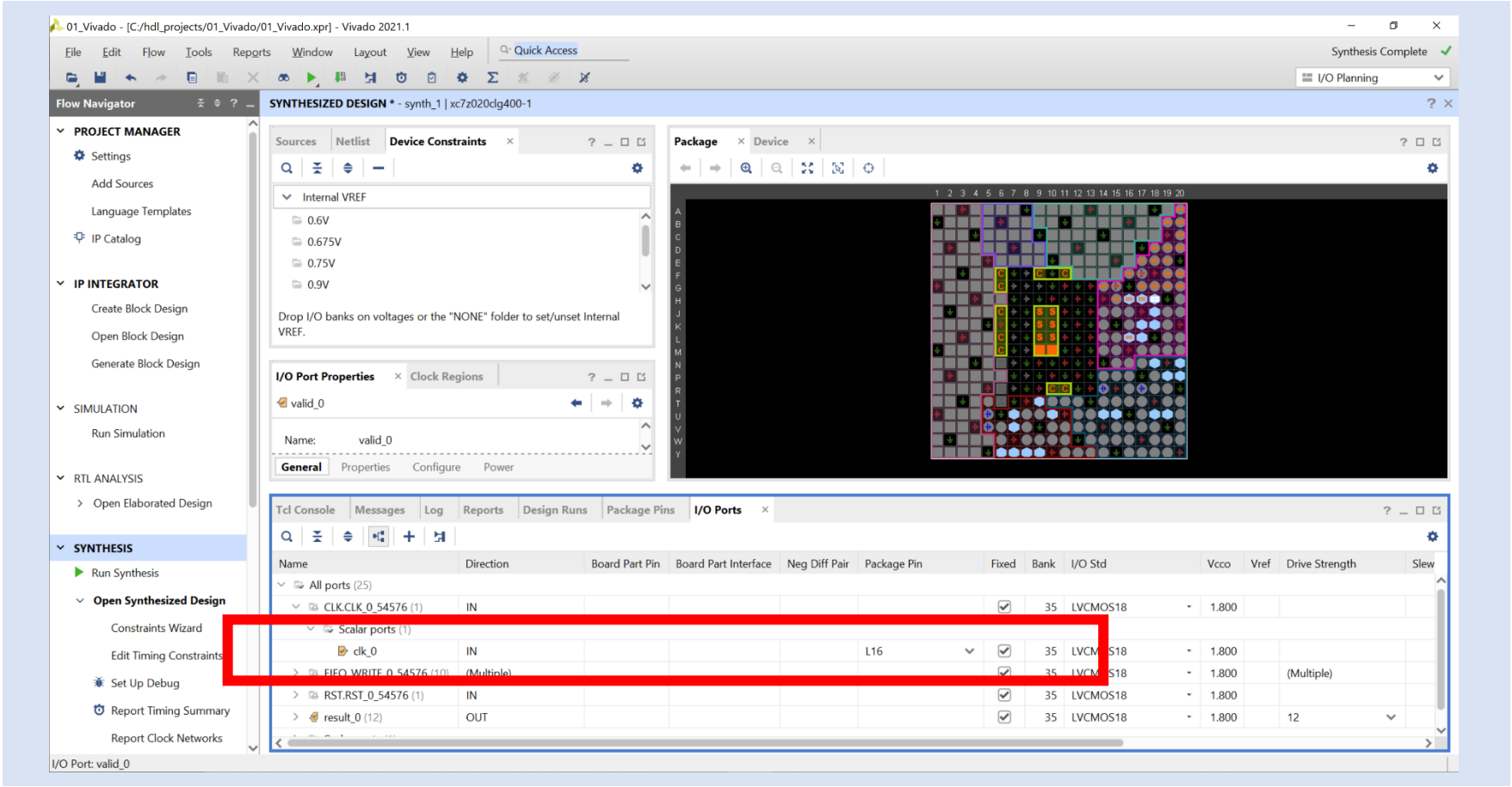
Lab 5: Intermediate Vivado

Step 29 – Change the I/O standard from default to **LVCMOS18**.



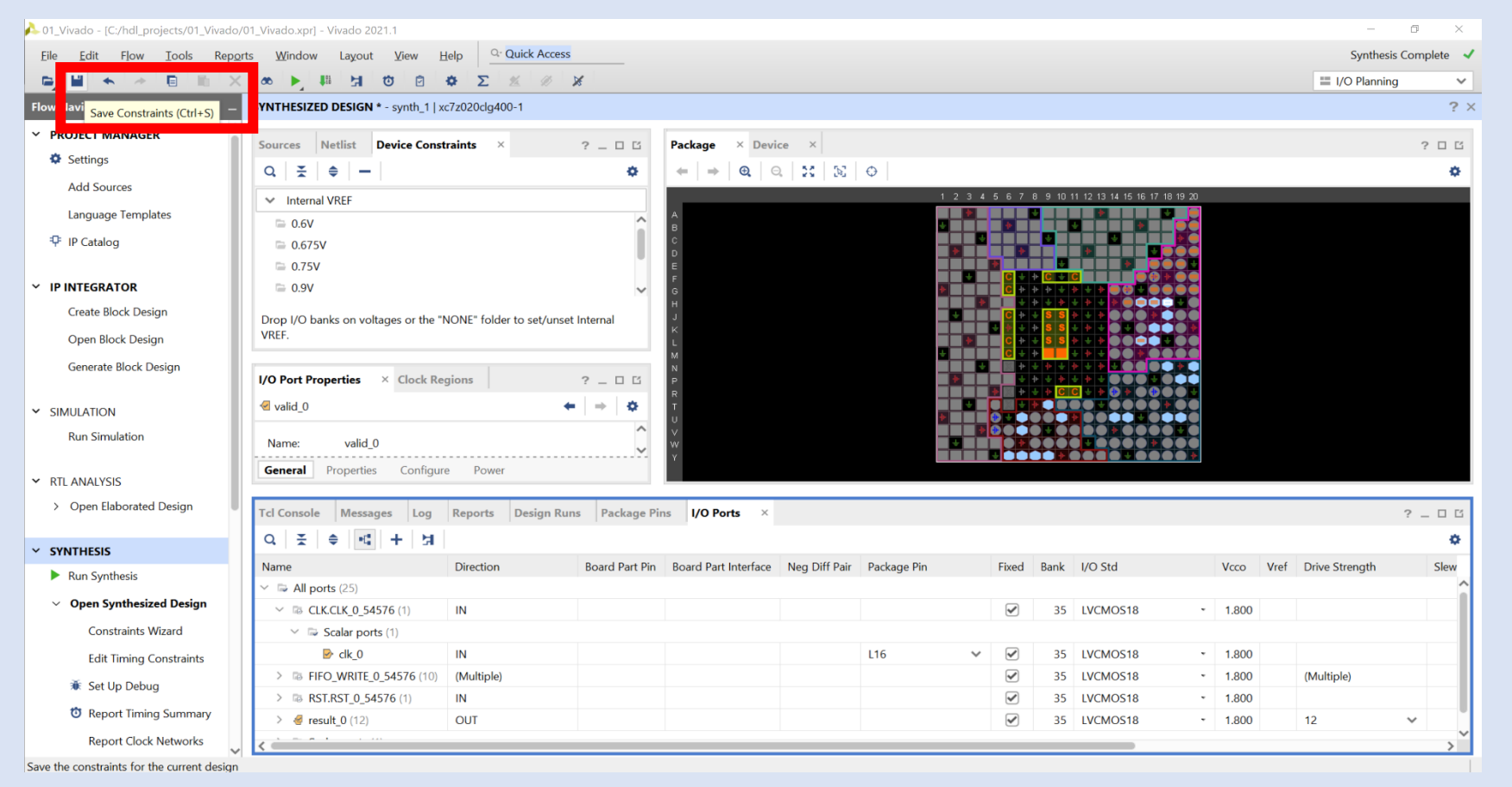
Lab 5: Intermediate Vivado

Step 30 – Assign the clock input to pin **L16.** Assign all other IO to pins of your choice.



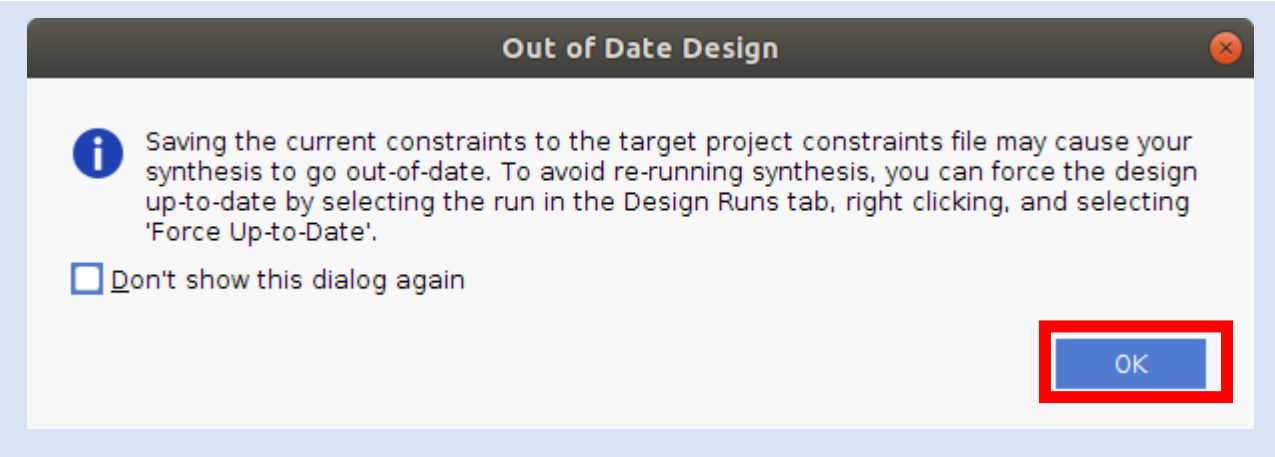
Lab 5: Intermediate Vivado

Step 31 – Click on **Save Constraints**.



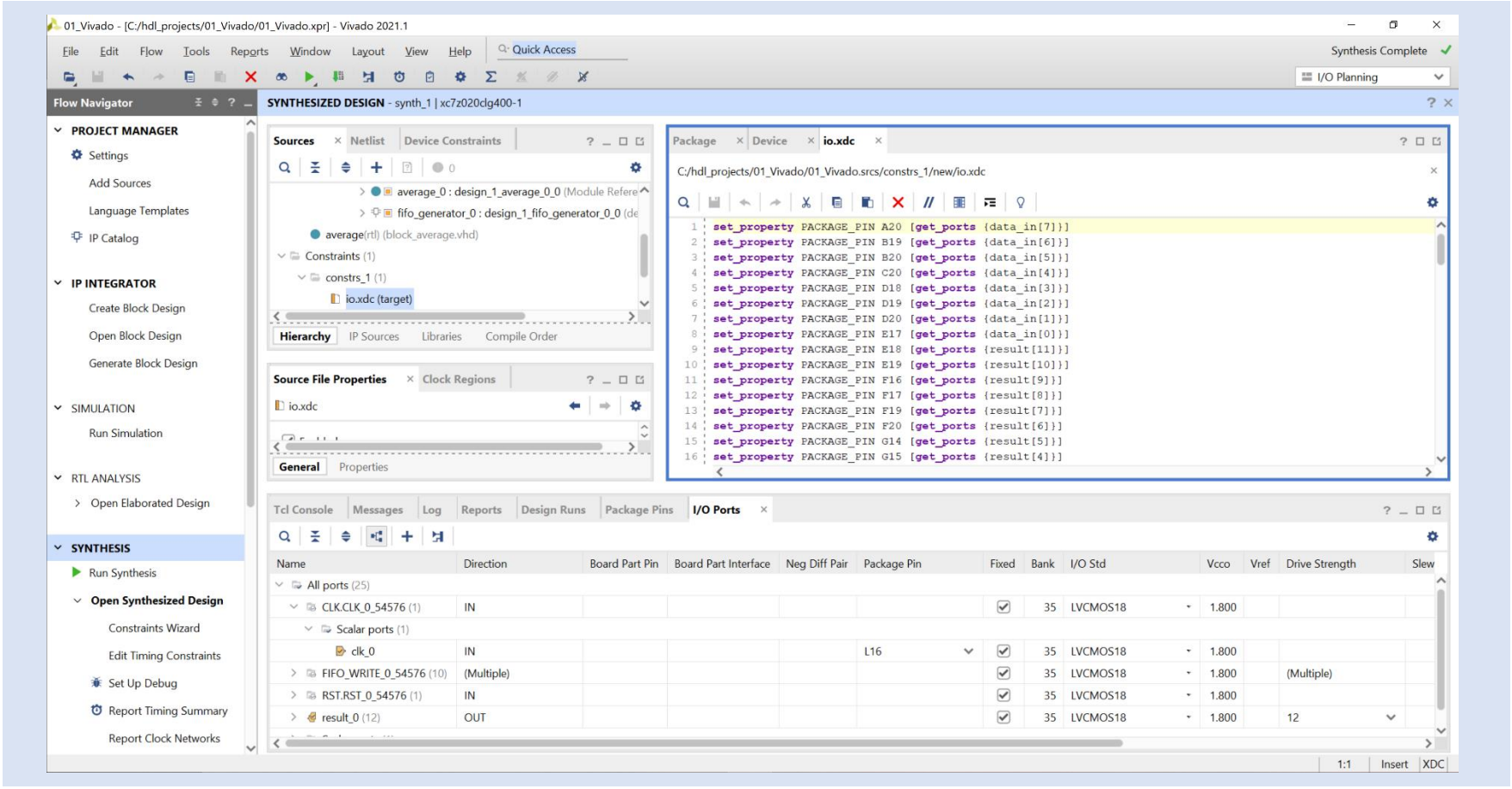
Lab 5: Intermediate Vivado

Step 32 – If an out-of-date warning appears, click **OK**.



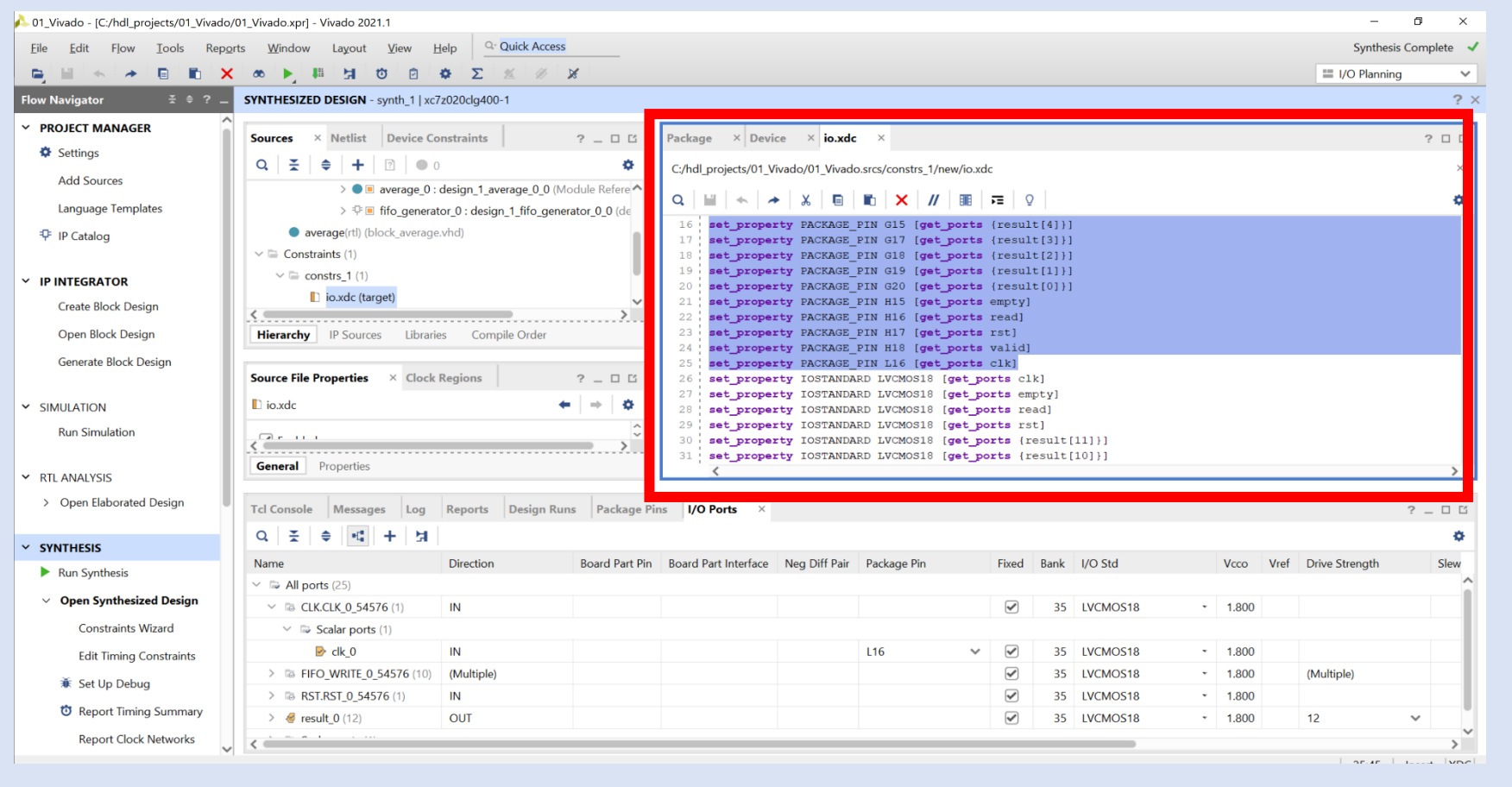
Lab 5: Intermediate Vivado

Step 33 – From the sources tab, open the **IO constraints.** You will see the old pin out for the previous project and your new project. This is because we have evolved the original project.



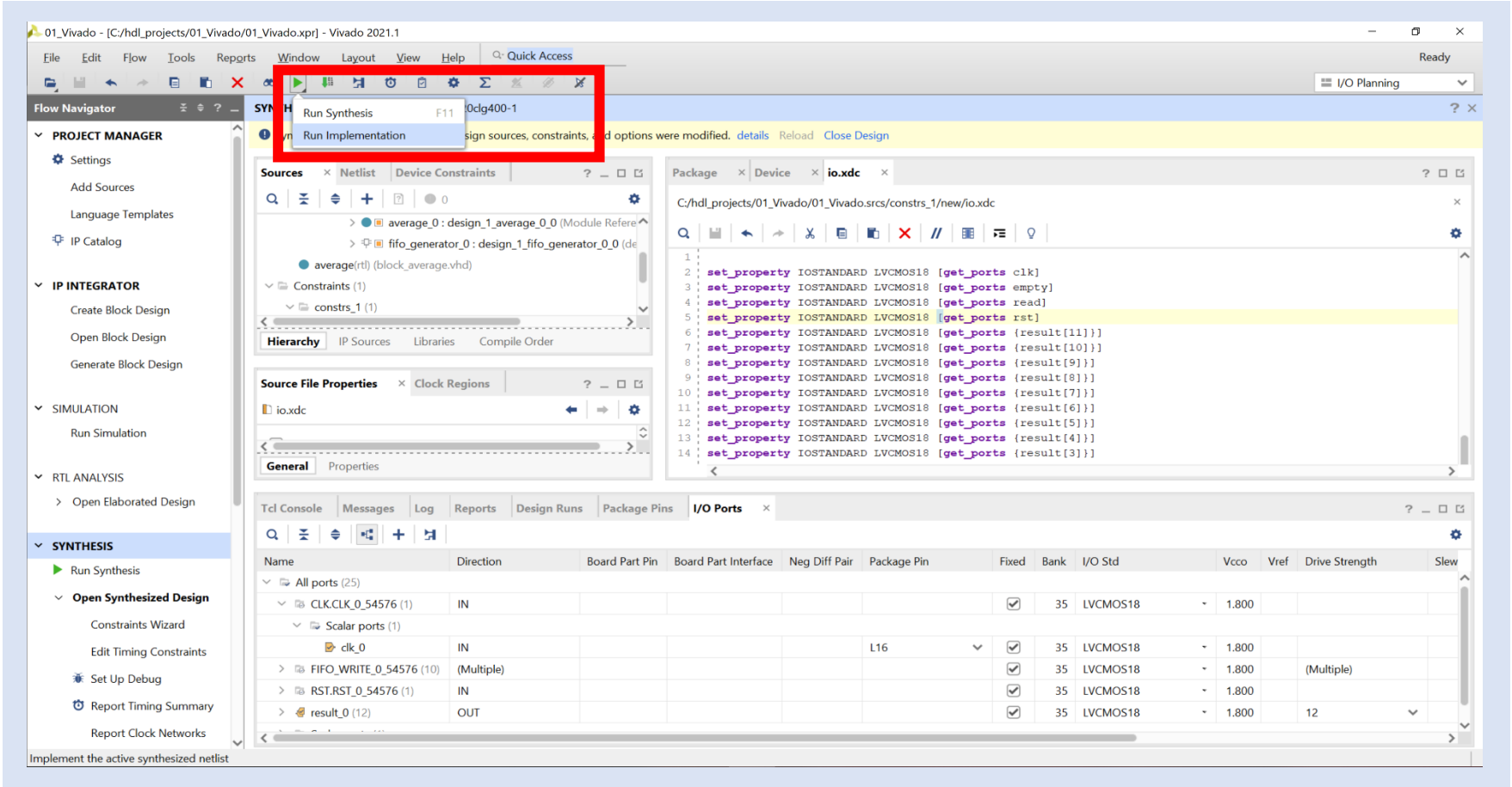
Lab 5: Intermediate Vivado

Step 34 – Select the old constraints (at the top of the file) and delete them. Save the file.



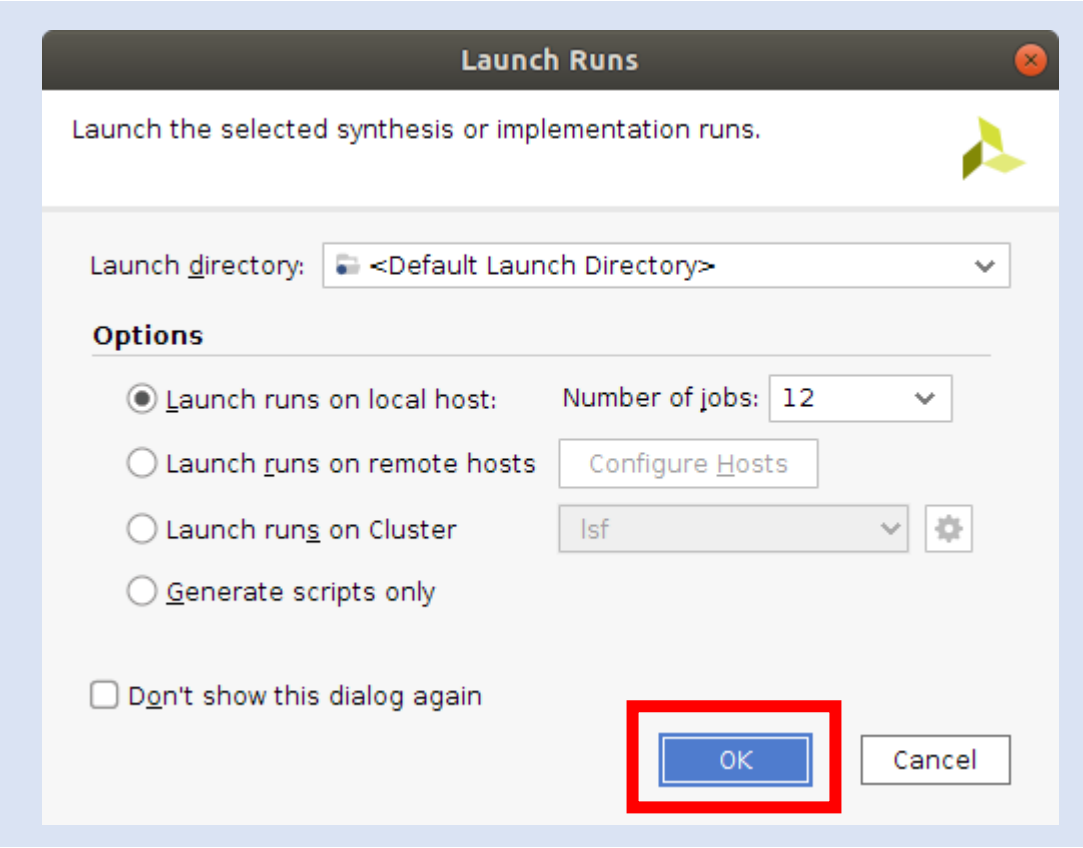
Lab 5: Intermediate Vivado

Step 35 –Run the Implementation, Re run synthesis if you get an out of date warning



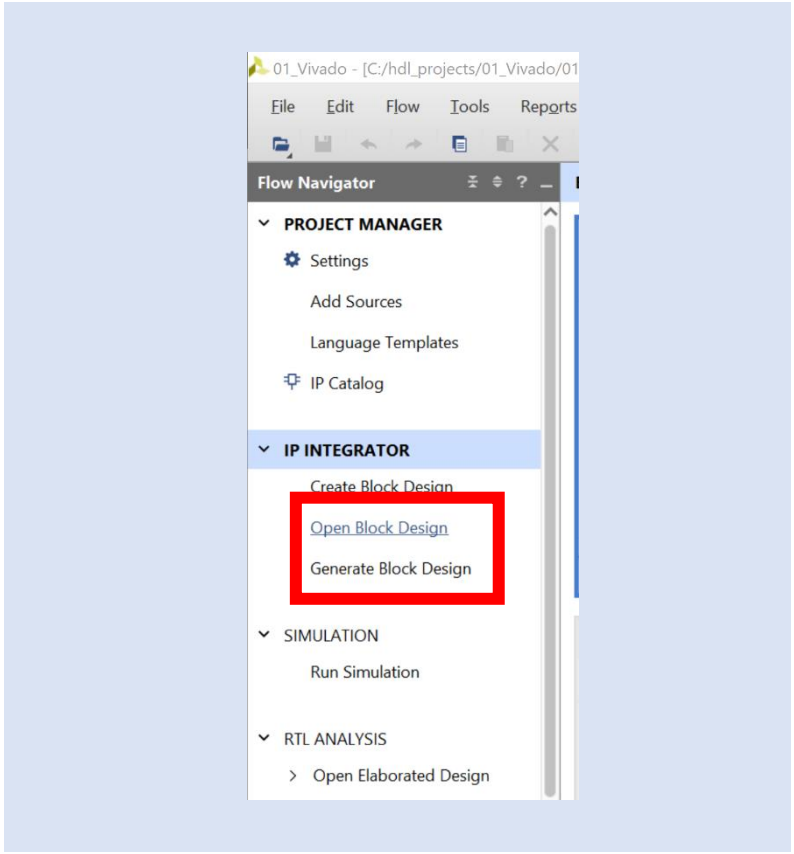
Lab 5: Intermediate Vivado

Step 36 – Click **OK** to run the implementation.



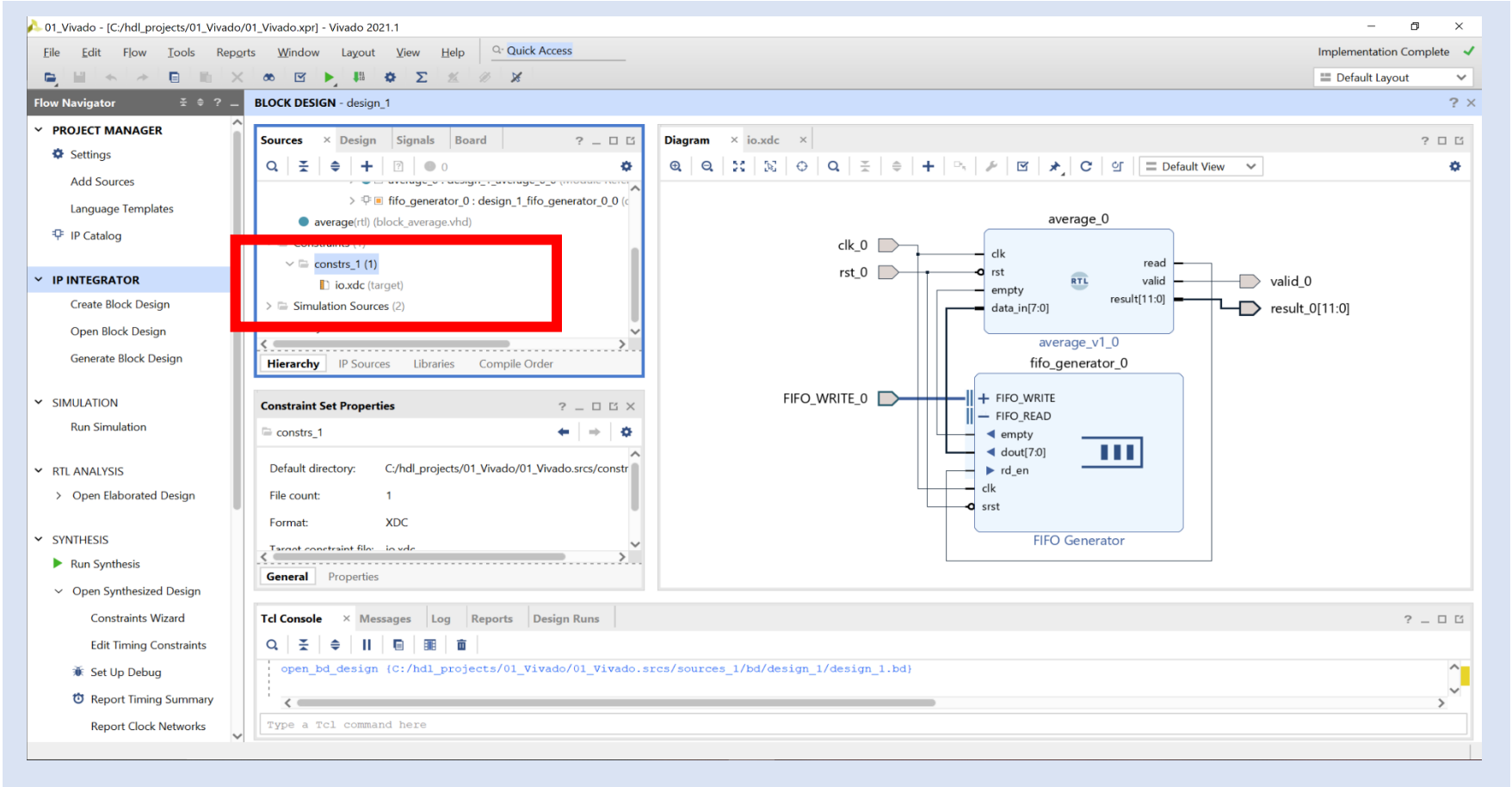
Lab 5: Intermediate Vivado

Step 37 – Open the Block Design when design has built.



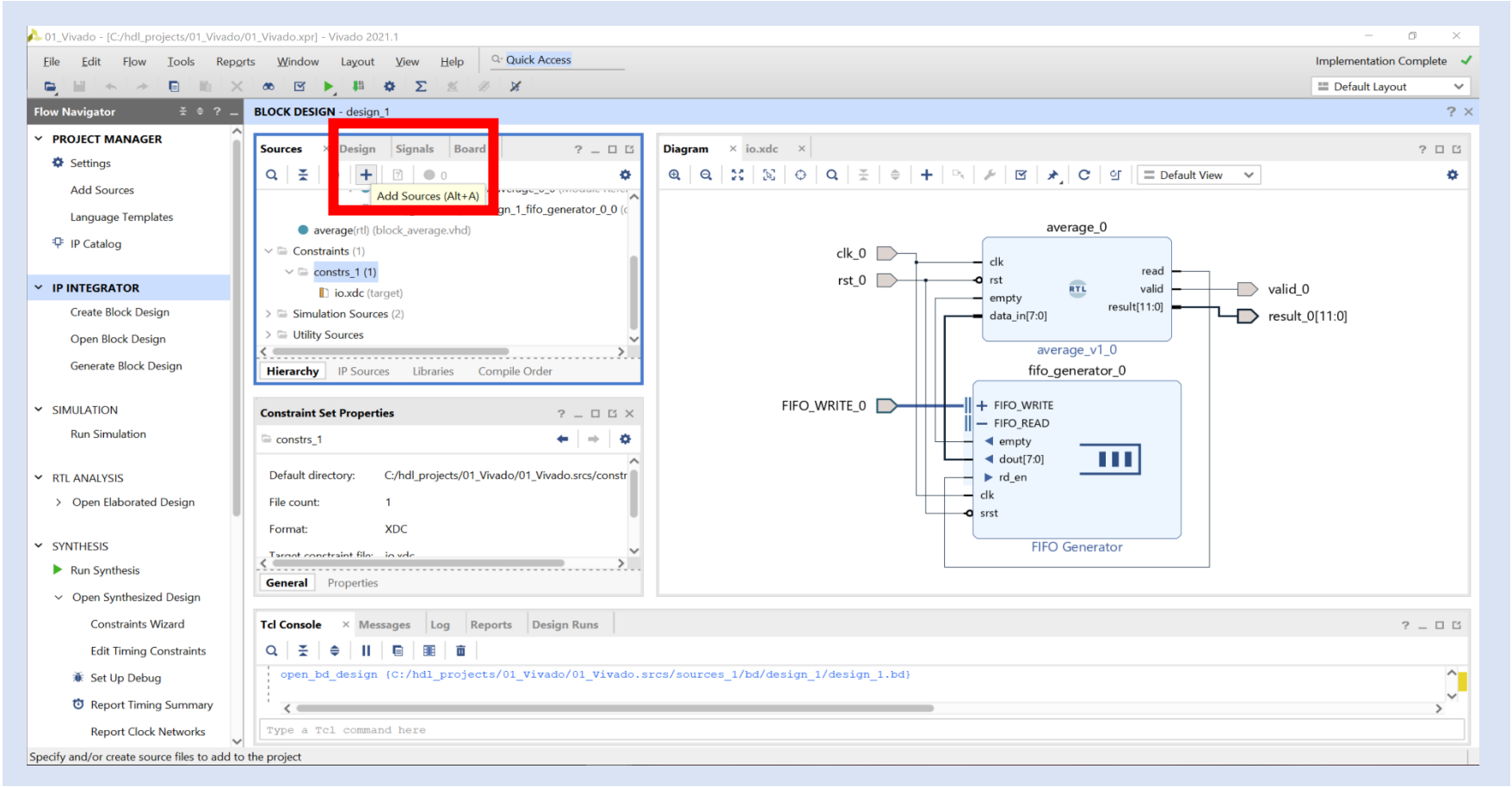
Lab 5: Intermediate Vivado

Step 38 – Select **Constraints** under Design Sources.



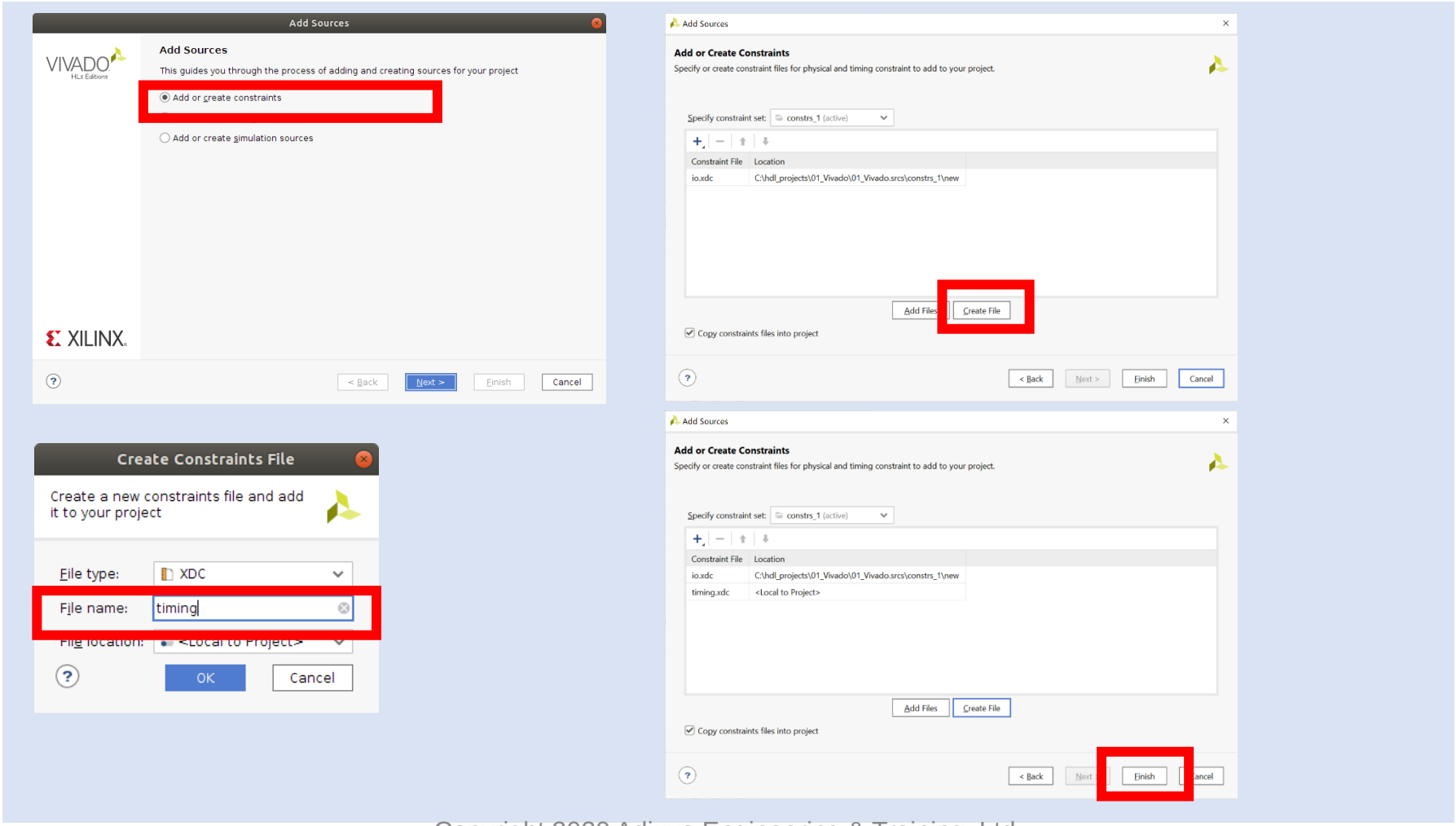
Lab 5: Intermediate Vivado

Step 39 – Click on the **Add Source** button.



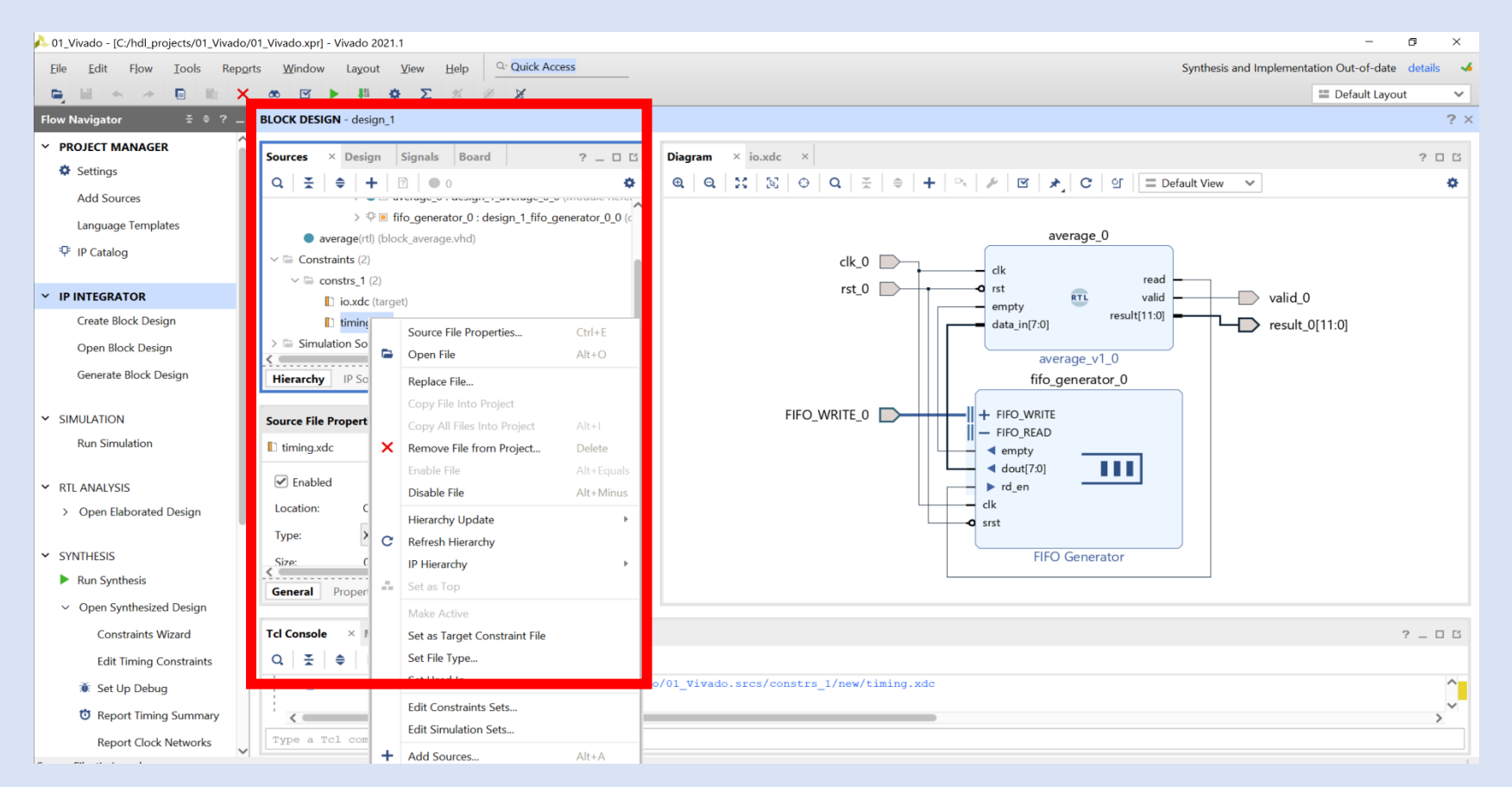
Lab 5: Intermediate Vivado

Step 40 – Select **Add or Create Constraints.** Then **Create File**, enter the name **“timing”** for the file, and click **Finish**.



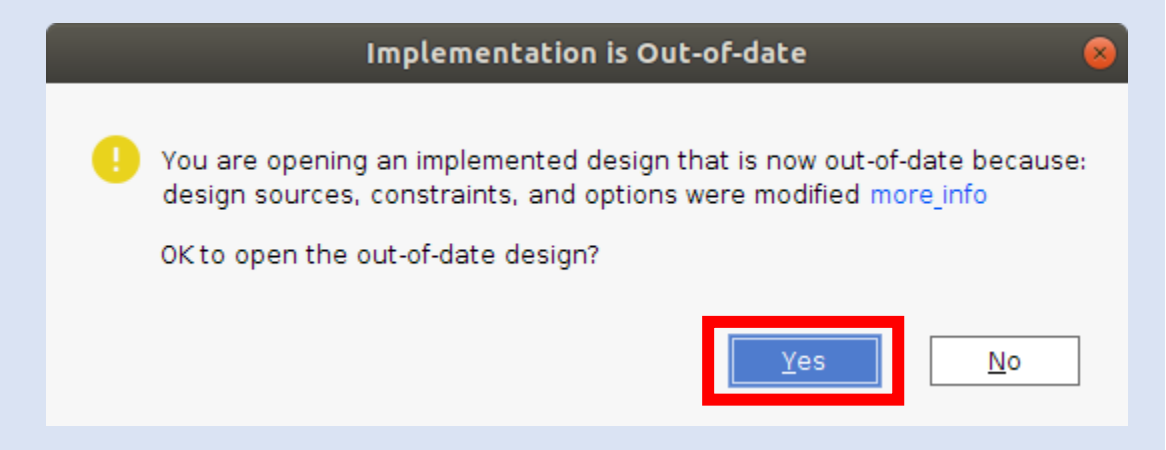
Lab 5: Intermediate Vivado

Step 41 – Right click on the newly created constraint file and select **Set as Target Constraints File**.



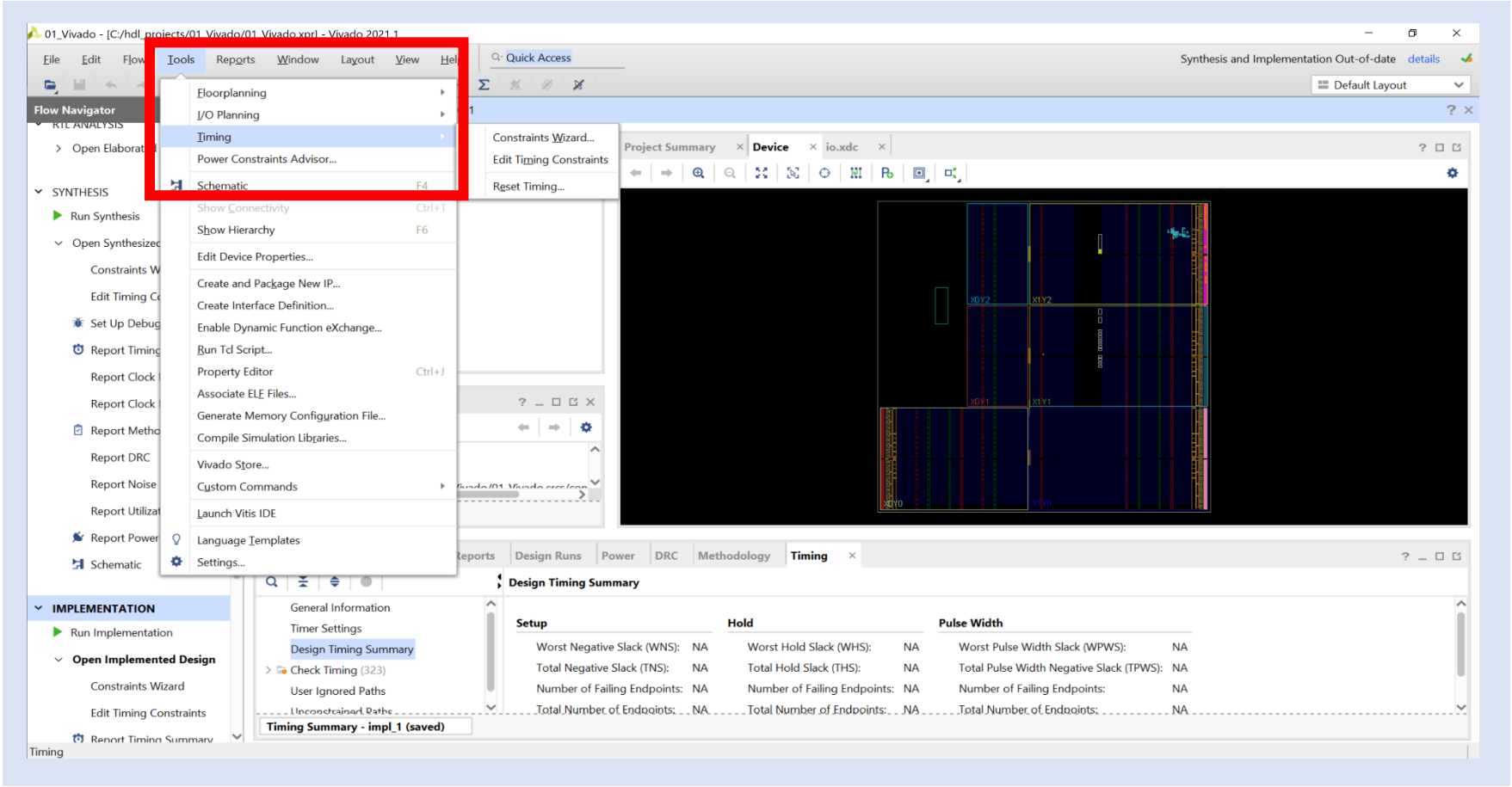
Lab 5: Intermediate Vivado

Step 42 – Open the implemented design. If you see the warning below click **OK**.



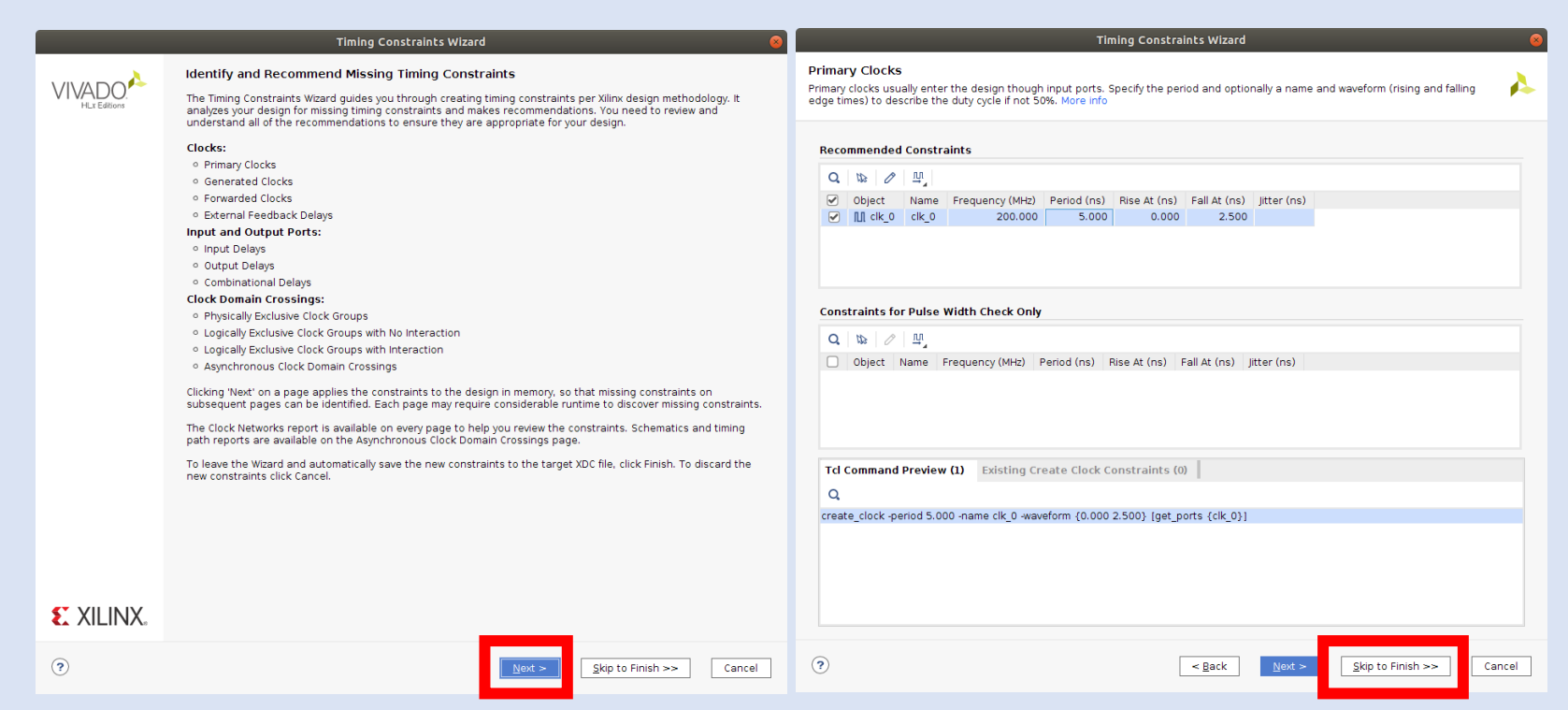
Lab 5: Intermediate Vivado

Step 43 – From the Tools menu, select **Timing** -> **Constraints Wizard**.



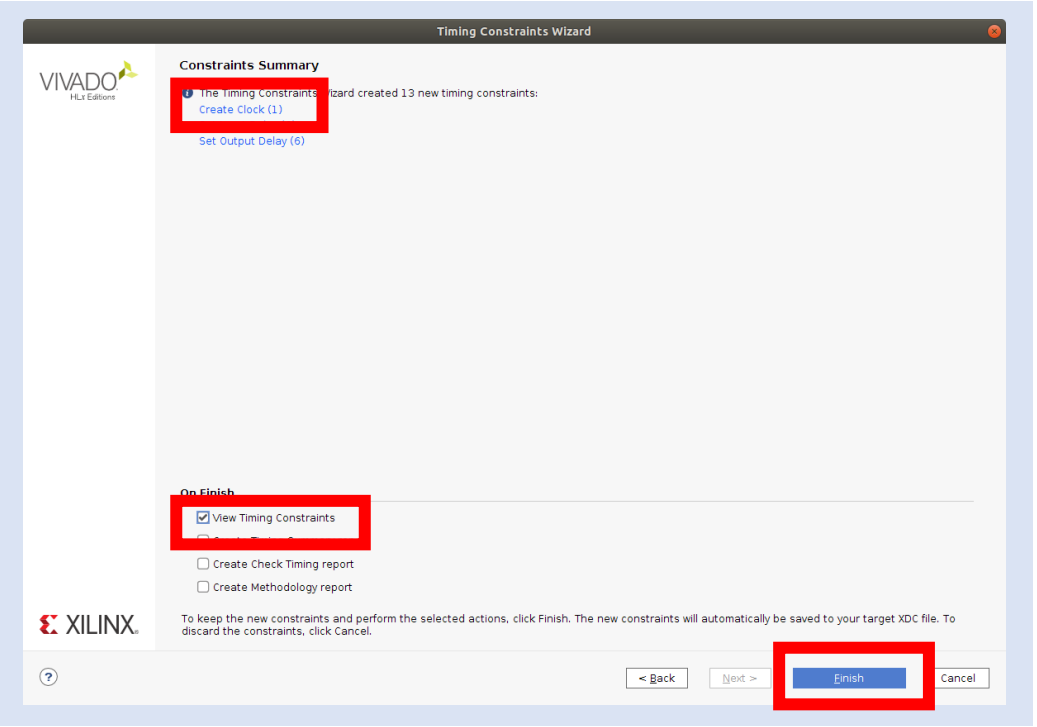
Lab 5: Intermediate Vivado

Step 44 – On the welcome screen, click **Next** and then enter **200 MHz** for the clock frequency. Once done, select **Skip to Finish**.



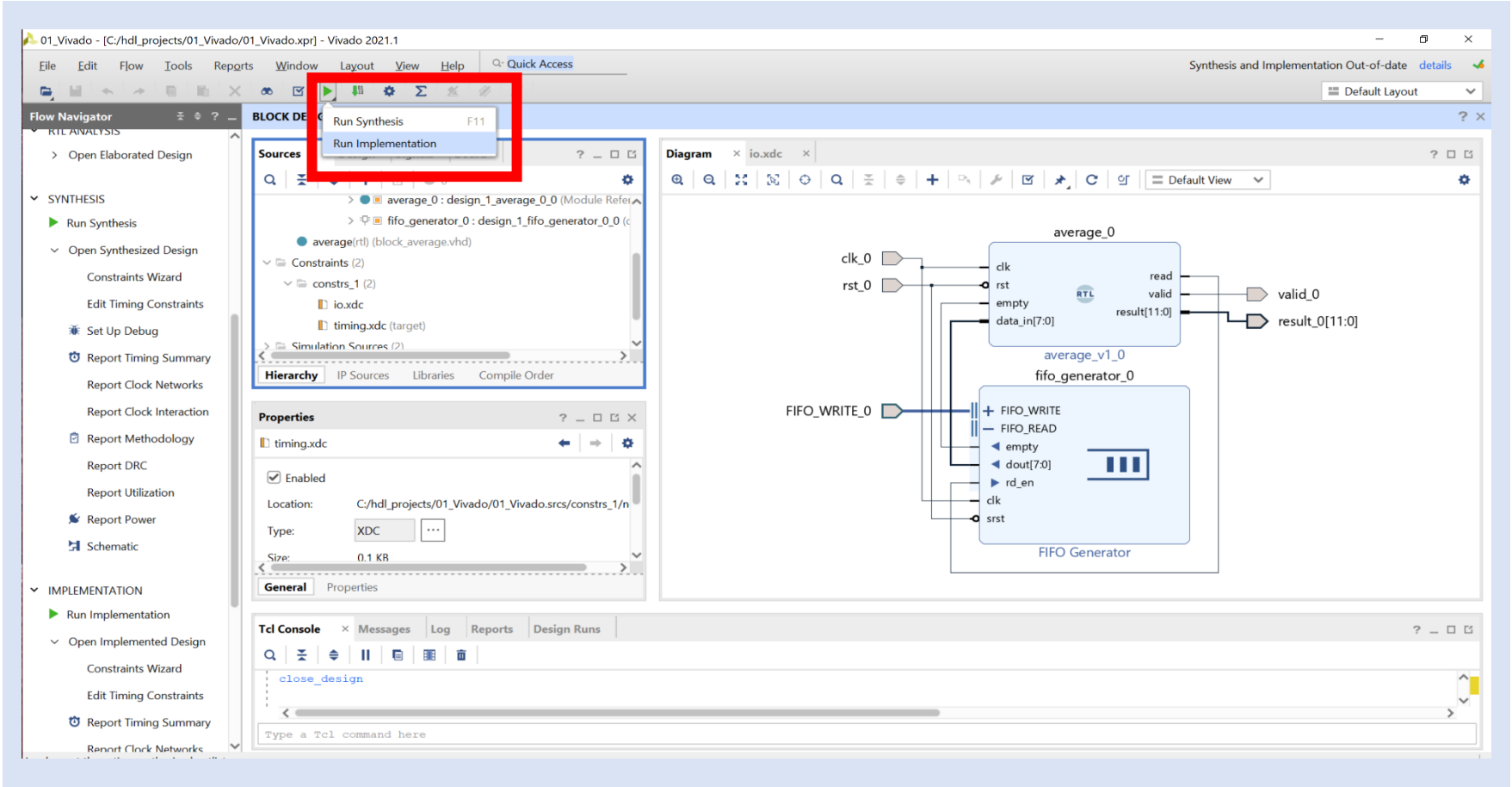
Lab 5: Intermediate Vivado

Step 45 – On the final page, check that only one constraints is being created, check the **View Timing Constraints,** and click **Finish**.



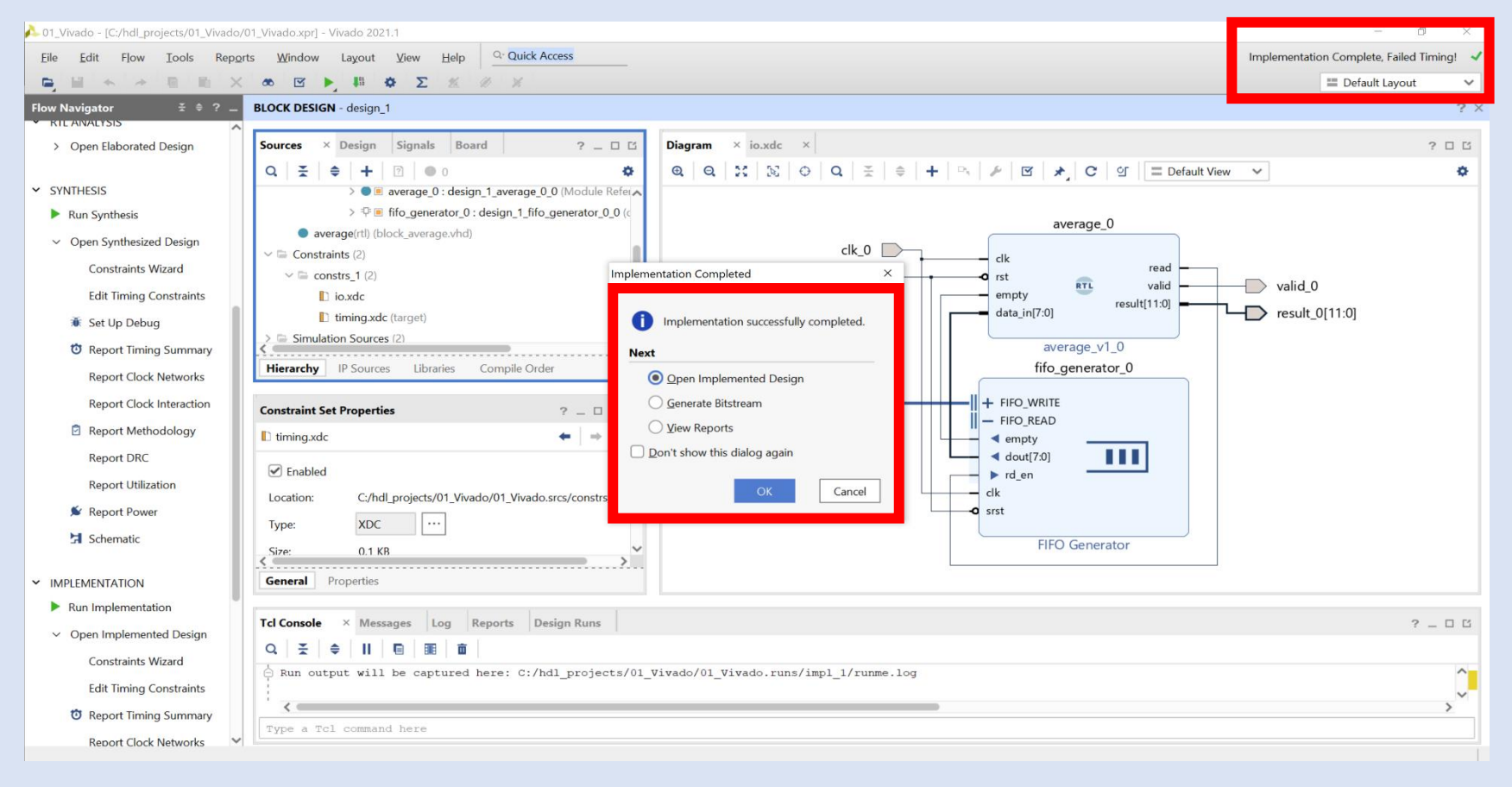
Lab 5: Intermediate Vivado

Step 46 – Close the implementation view and **rerun the implementation. Run synthesis if you get out of date pop up**. Click **OK** on any dialogs which pop up prior to implementation starting.



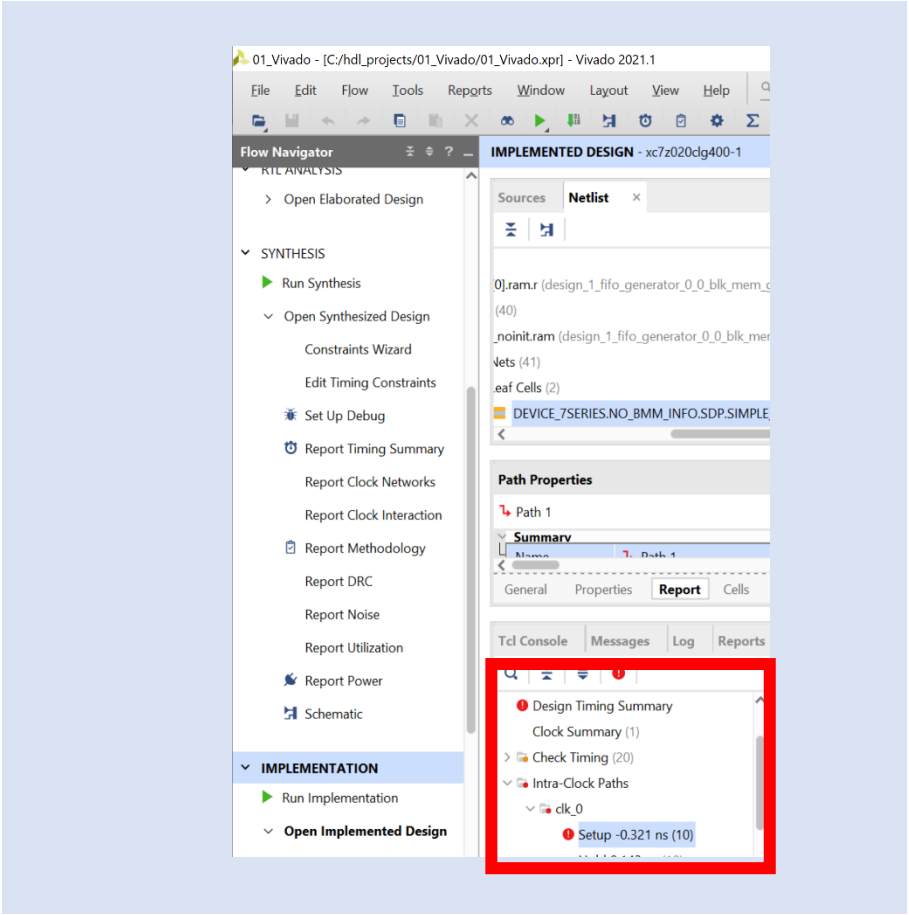
Lab 5: Intermediate Vivado

Step 47 – Once the implementation completes, Timing will fail. Open the **Implemented Design**.



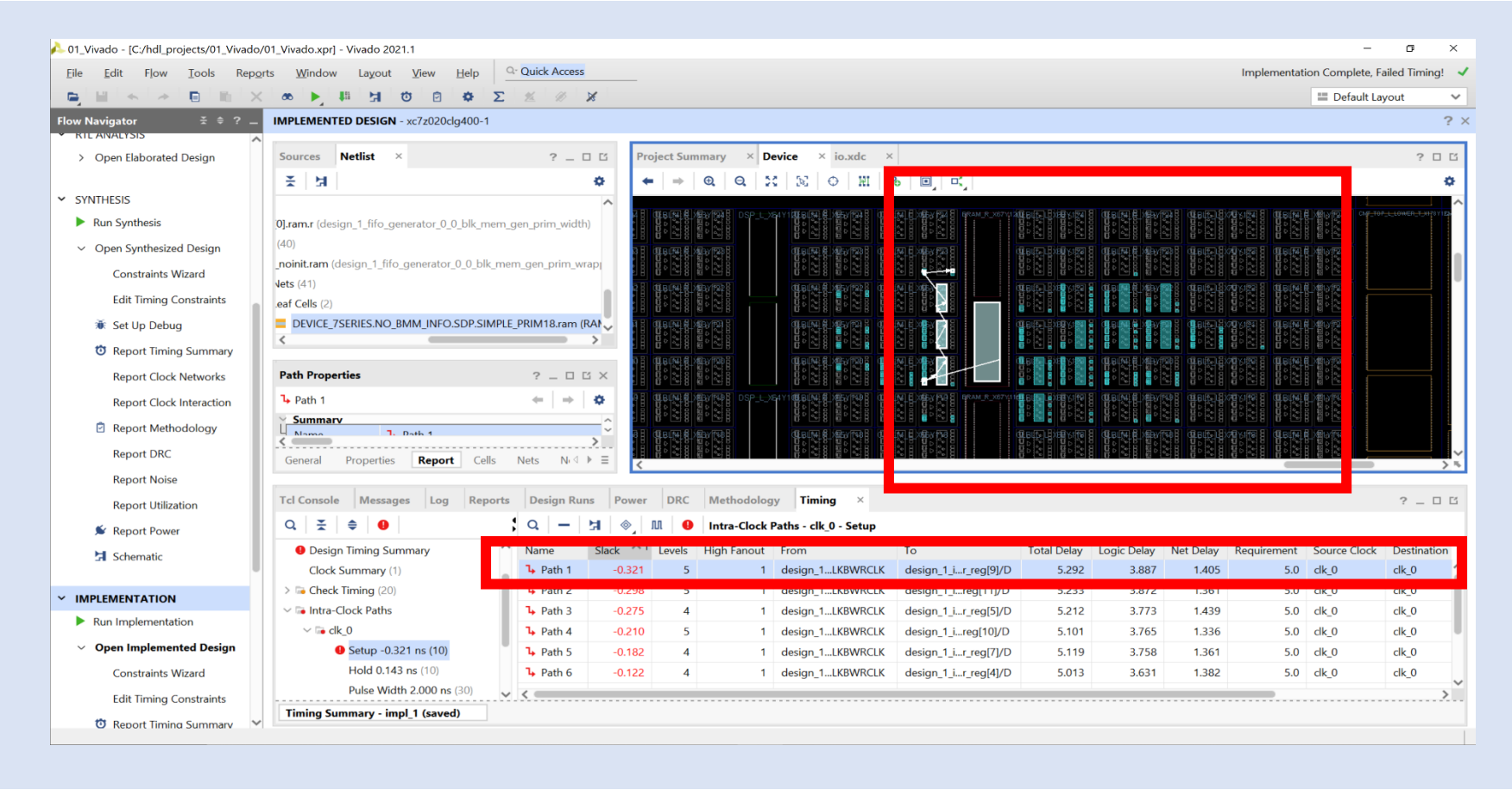
Lab 5: Intermediate Vivado

Step 48 – In the implemented design, select the failing **Intra-Clock Paths**.



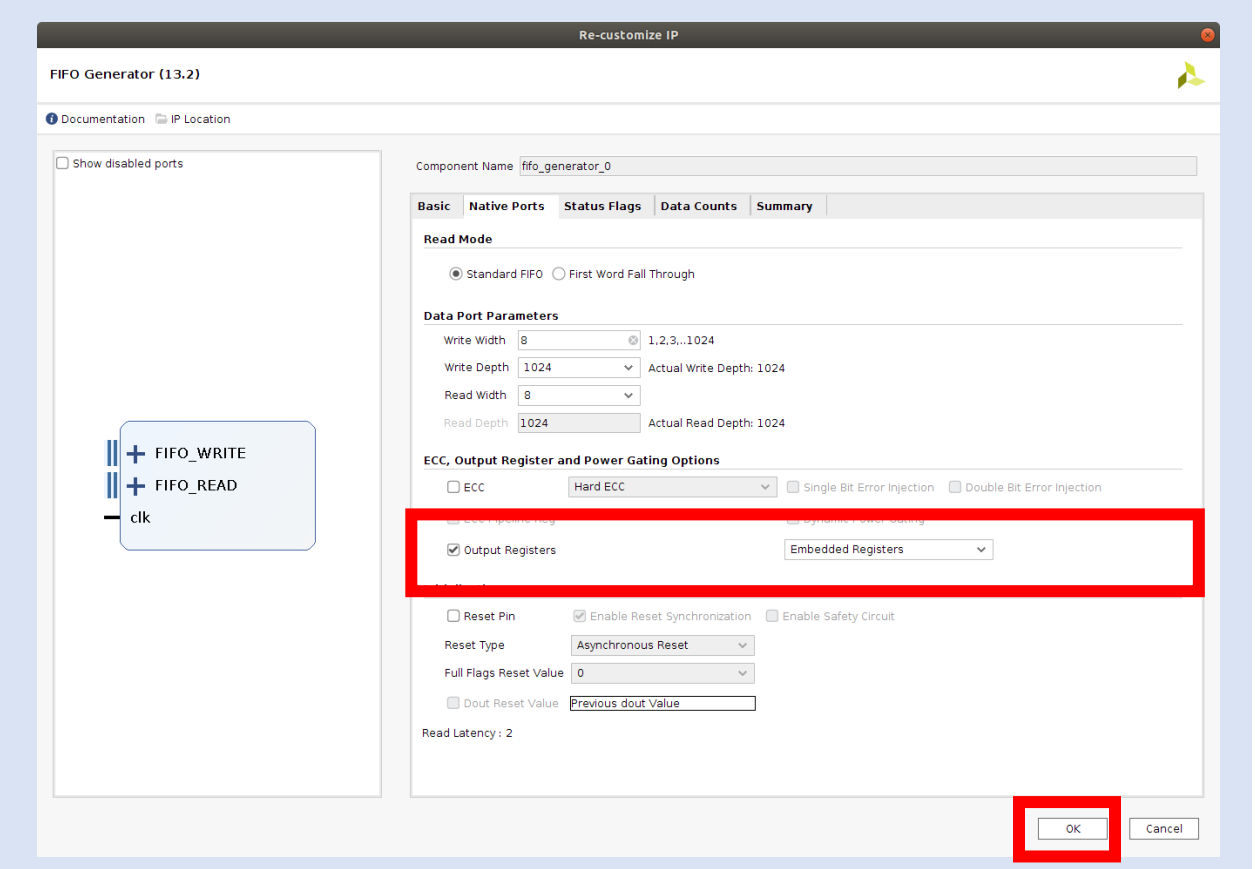
Lab 5: Intermediate Vivado

Step 49 – Select **Path 1** and zoom in. You will see that the FIFO output data passes through LUTs before finally being registered. This path is too long for timing at 200 MHz.



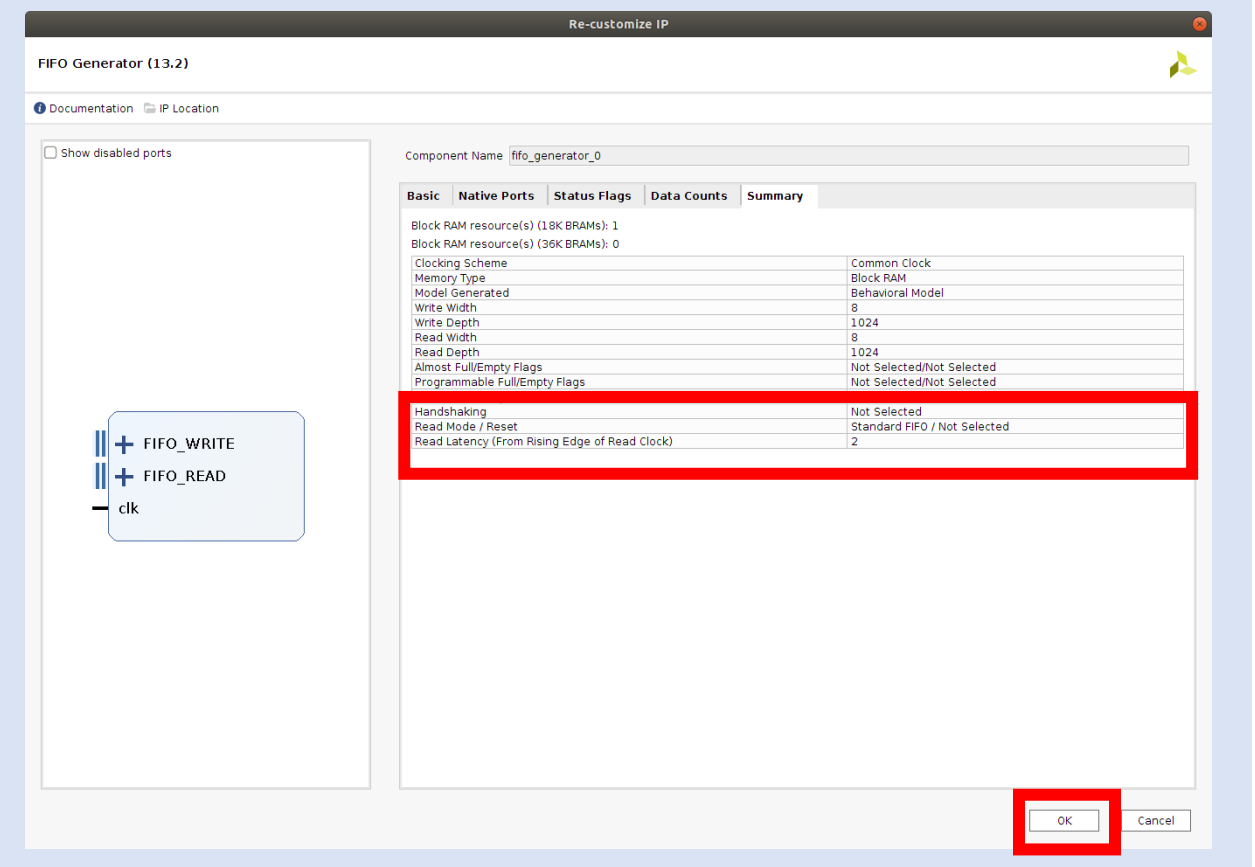
Lab 5: Intermediate Vivado

Step 50 – To fix this, we need to register the output of the FIFO. Close the implementation view and reopen the block diagram. Double click on the **FIFO** to customize.



Lab 5: Intermediate Vivado

Step 51 – Note the latency has changed from 1 to 2 clocks. We would need to correct for this in the average block, however, we proceed assuming that we have.



Lab 5: Intermediate Vivado

Step 52 – Reimplement the design. When the timing is completed, you should see that the implementation is correct and the timing is met.