

Getting to Know Vivado

Course Workbook

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About this Workbook

This workbook is designed to be used in conjunction with the Getting to Know Vivado course.

The contents of this workbook are created by Aduvo Engineering & Training, Ltd.

If you have any questions about the contents, or need assistance, please contact Adam Taylor at adam@aduvoengineering.com.

Pre-Lab

Workshop Pre-requisites

Required Hardware

There is no required hardware for this course.

Downloads and Installations

Step 1 – Download and install the following at least one day prior to the workshop. This may take a significant amount of time and drive space.

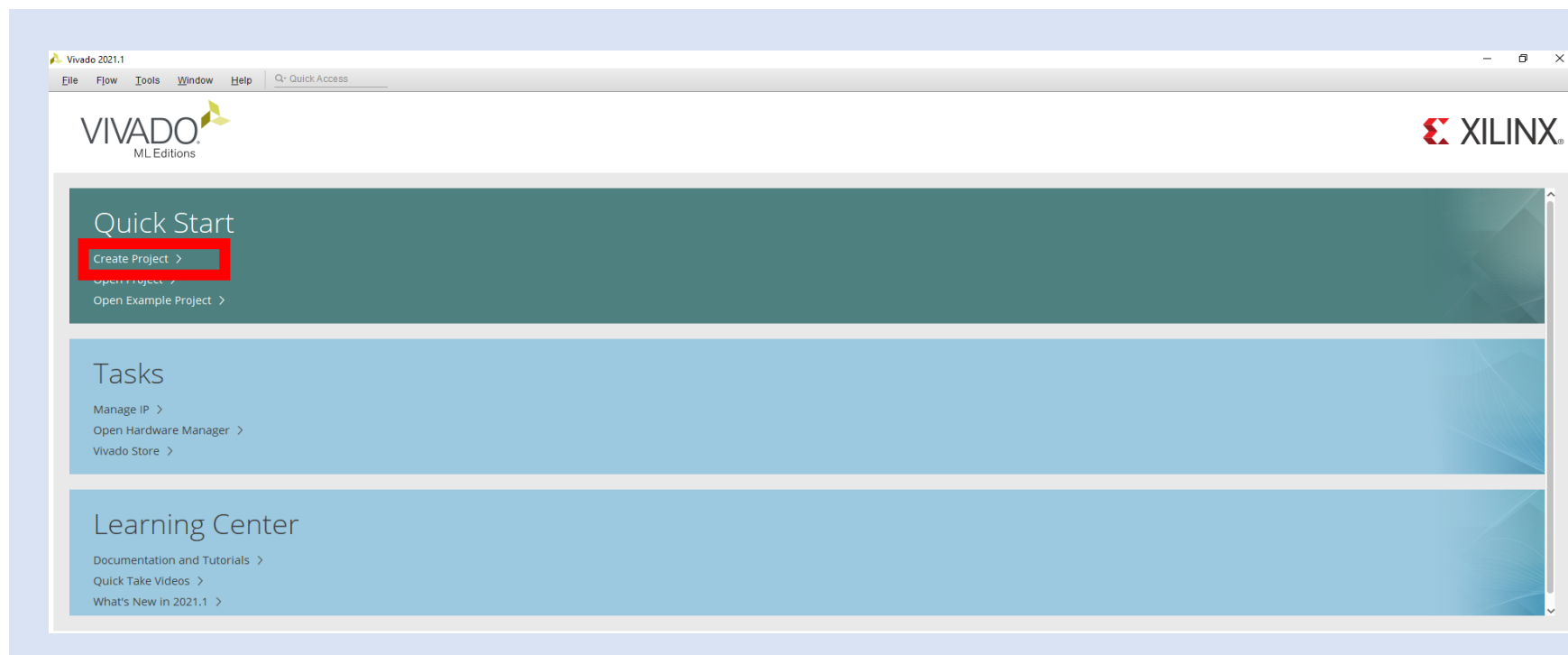
Vitis 2021.1	Download
Source Project Files	Download

Lab 4

Overview and Introduction to Vivado

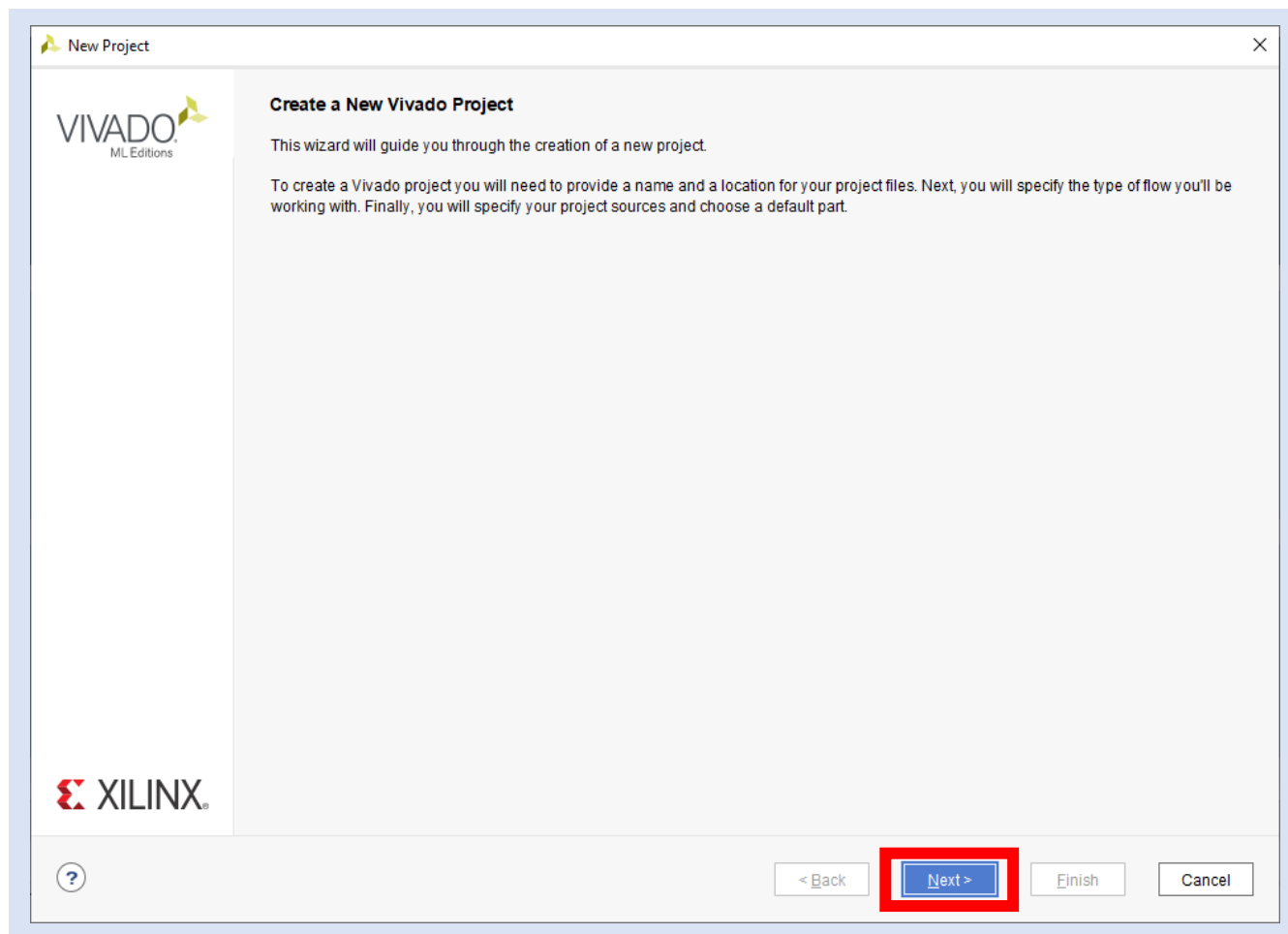
Lab 4: Overview and Introduction to Vivado

Step 1 – Open Vivado 2021.1.



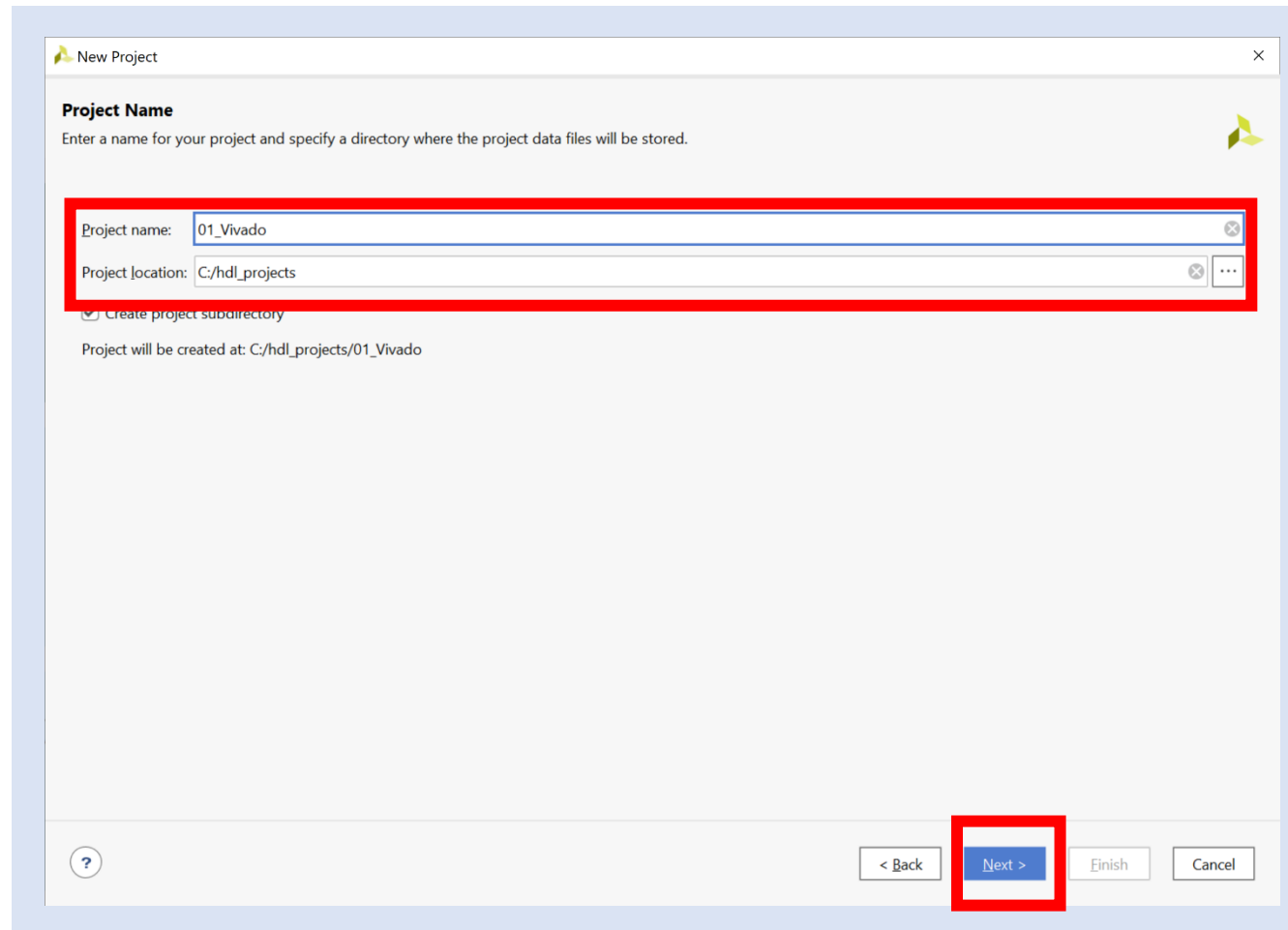
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Step 2 – Click on Create Project – This will open the New Project Wizard – Click Next.



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Step 3 – Enter the project name of “**01_Vivado**” and select the location you want to save the project.
Click Next



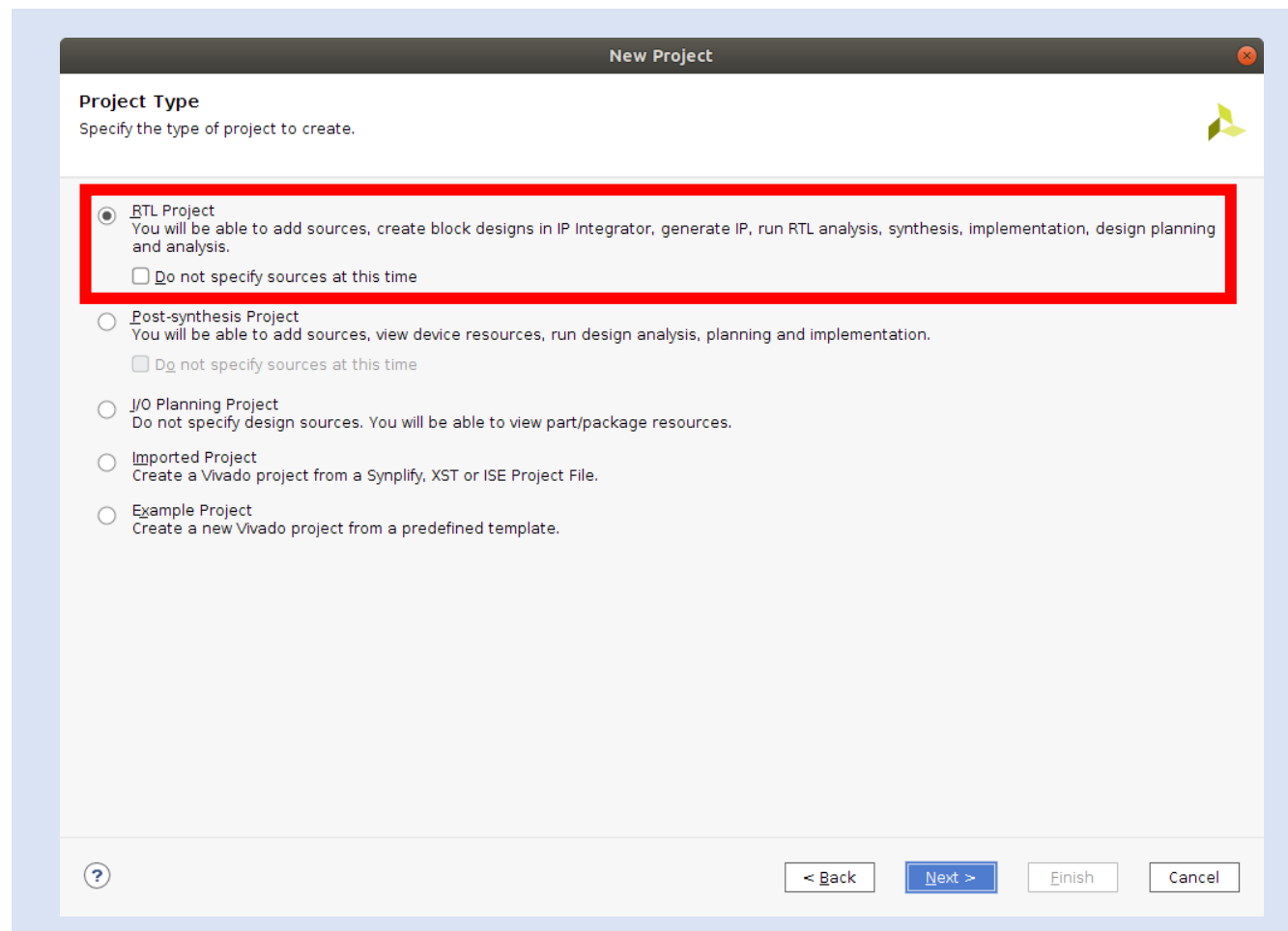
The screenshot shows the 'New Project' dialog box in Vivado. The 'Project Name' section is active, with the following fields and options:

- Project name:** 01_Vivado
- Project location:** C:/hdl_projects
- Create project subdirectory
- Project will be created at: C:/hdl_projects/01_Vivado

At the bottom of the dialog, the 'Next >' button is highlighted with a red box, indicating the next step in the process. Other buttons visible include '< Back', 'Finish', and 'Cancel'.

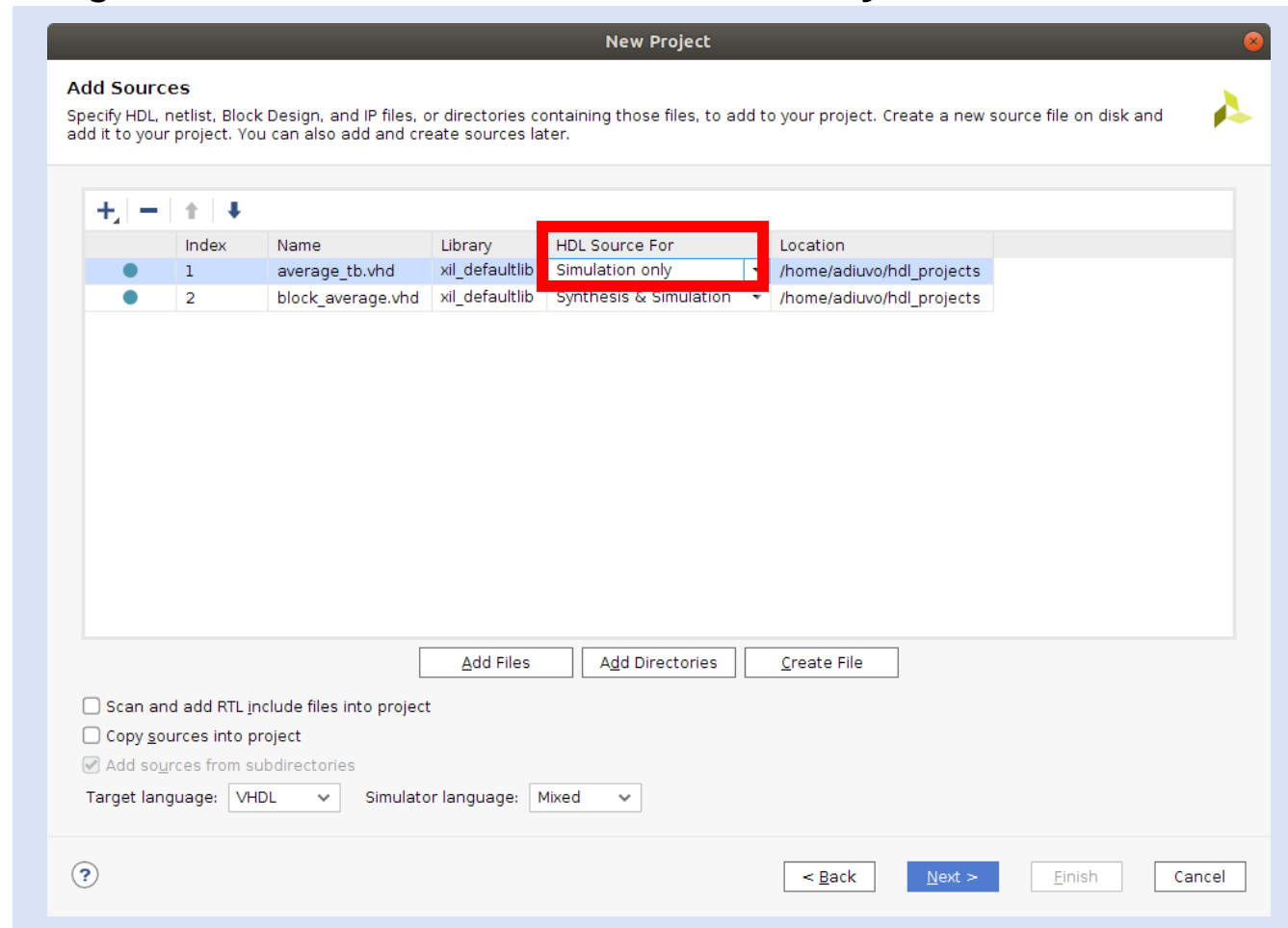
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Step 4 – Select RTL Project. Check Do not specify sources is unticked



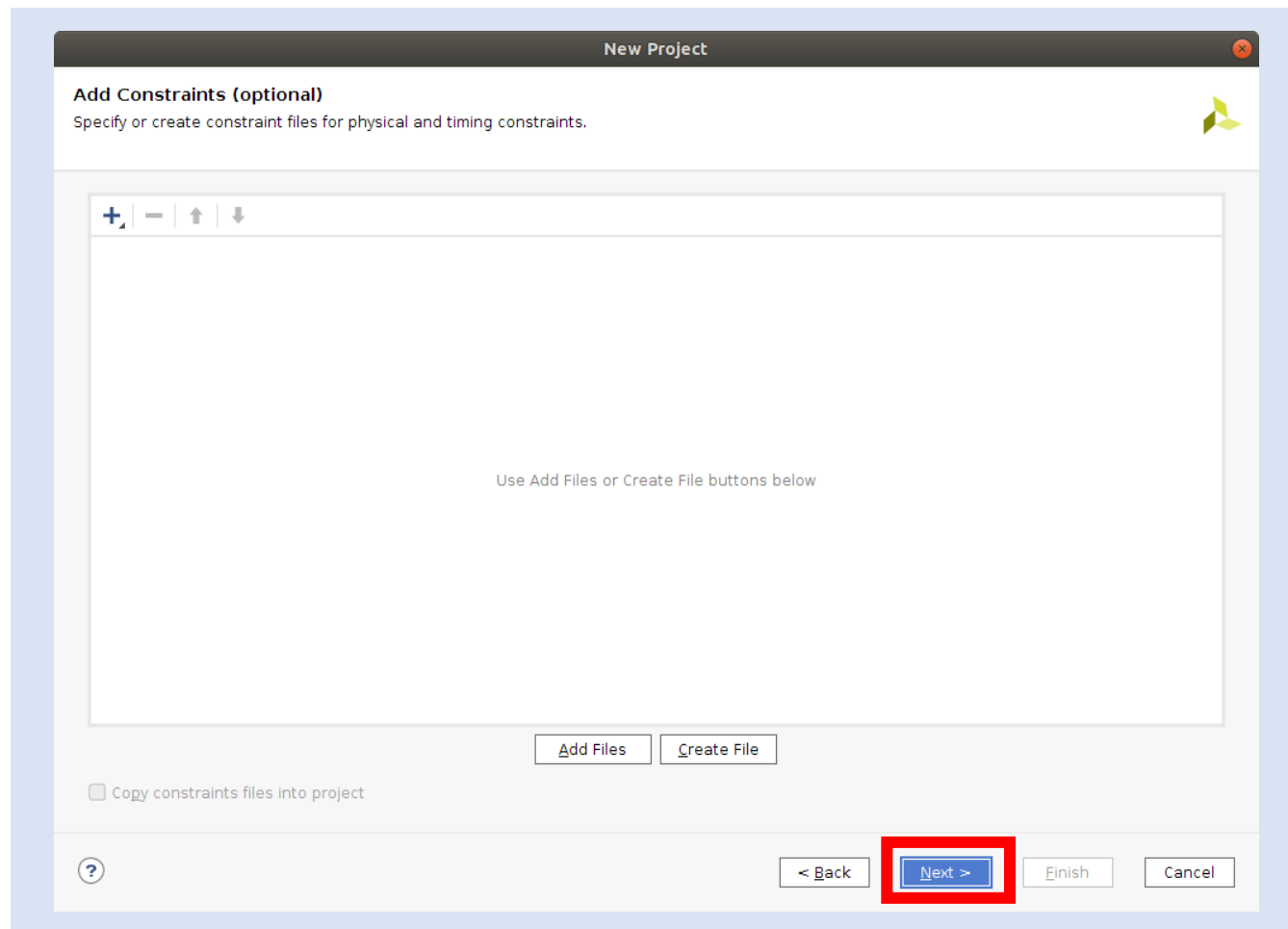
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Step 5 – Click **ADD FILES** and select the two files downloaded from Github. For the file `average_tb.vhd`, change the HDL source to **Simulation Only**. Click Next



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Step 6 – At this time we do not want to add any constraints files. Click **Next**.



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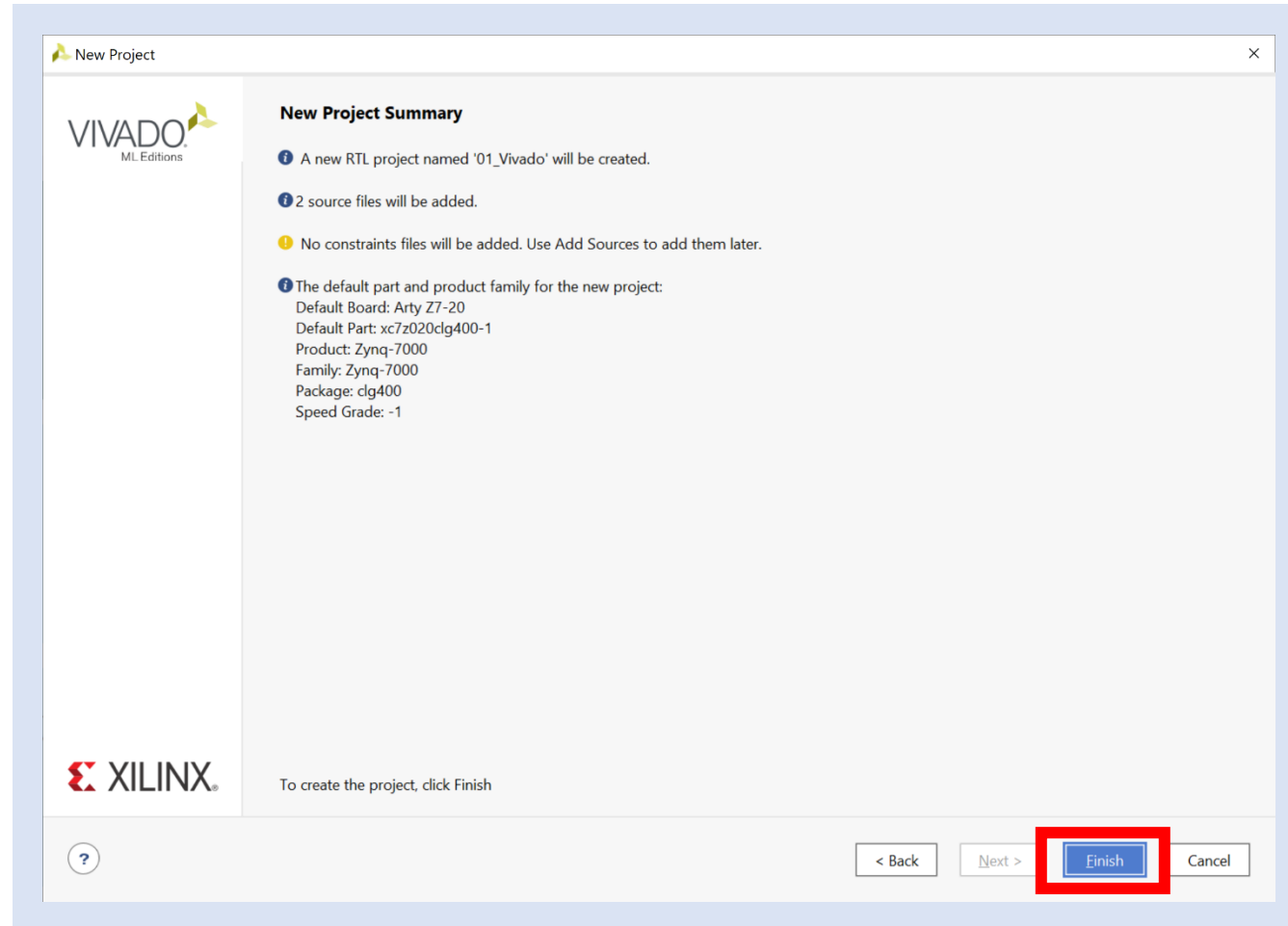
Step 7 – Select the Arty Z7-20 and click Next.

The screenshot shows the 'New Project' dialog box in Vivado, specifically the 'Default Part' section. The 'Boards' tab is selected, and a search for 'arty' has been performed, resulting in 13 matches. The 'Arty Z7-20' board is highlighted in blue and enclosed in a red box. The 'Next >' button at the bottom right is also highlighted with a red box.

Display Name	Preview	Status	Vendor	File Version	Part
Arty S7-25		↓	digilentinc.com	1.0	
Arty S7-50		↓	digilentinc.com	1.0	
Arty Z7-10		↓	digilentinc.com	1.0	
Arty Z7-20		⊖	digilentinc.com	1.0	xc7z020clg400-1

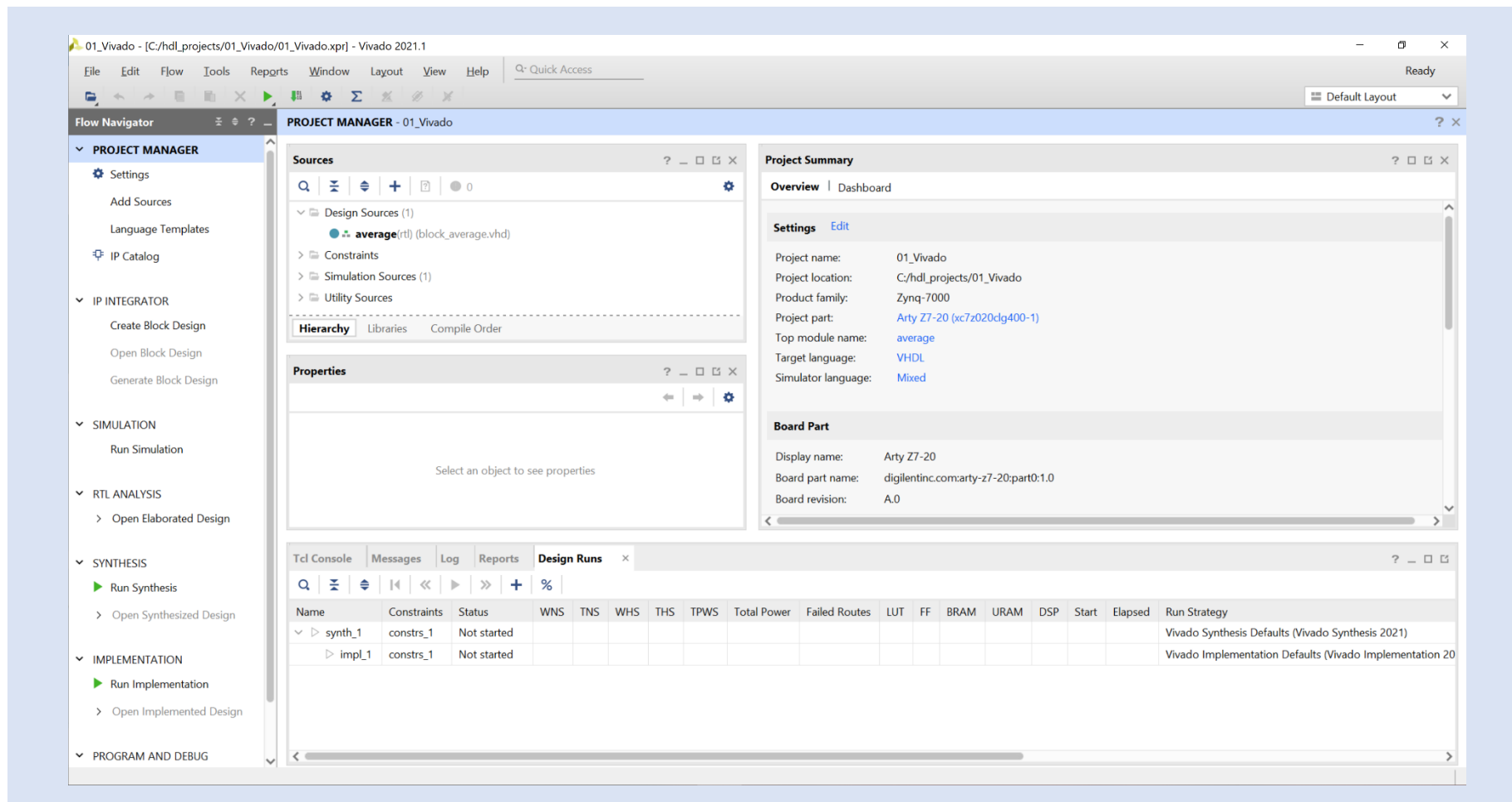
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Step 8 – On the project summary tab, select **Finish**.



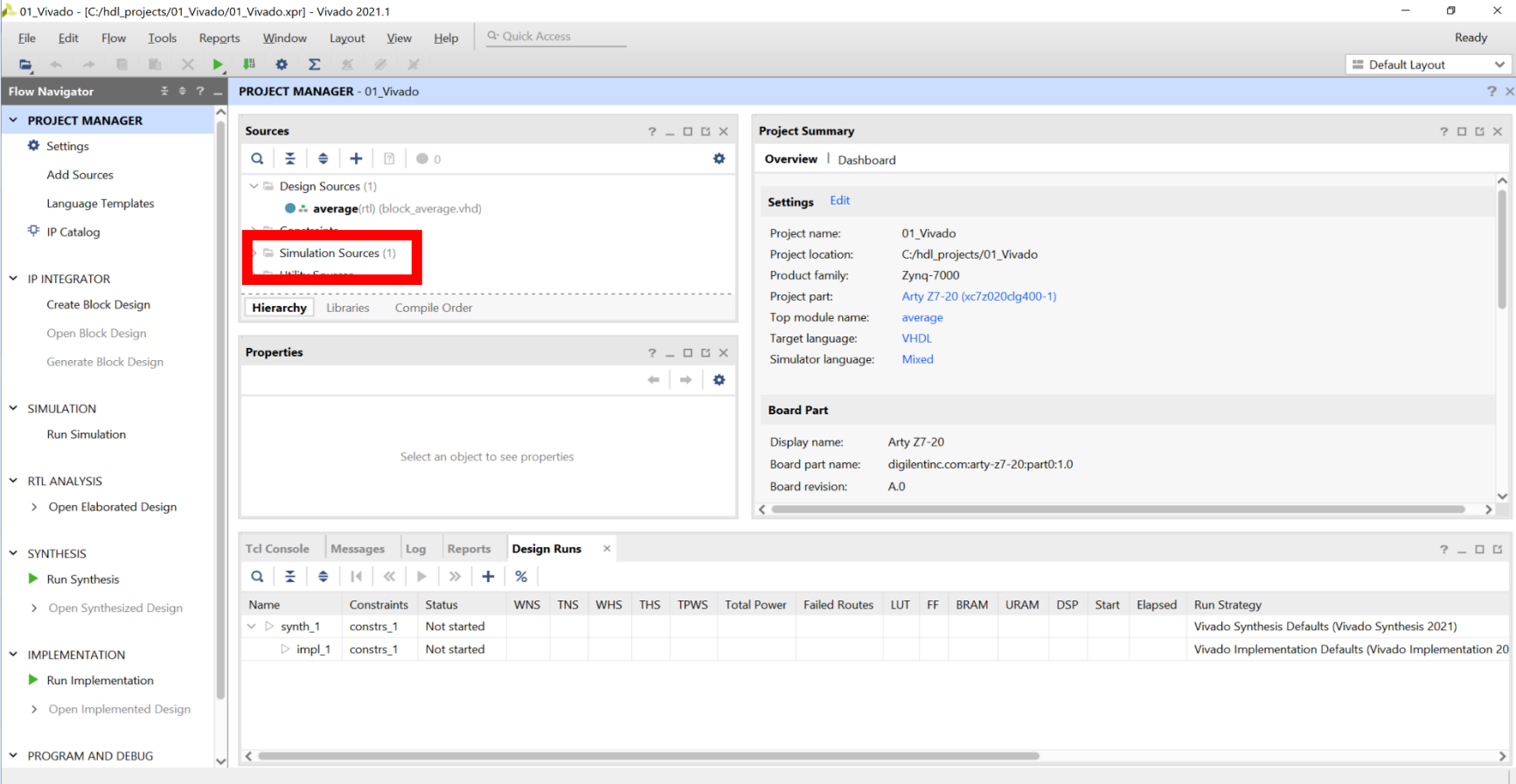
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Step 9 – This will open Vivado in the project manager view.



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Step 10 – Expand the Simulation Sources.



The screenshot displays the Vivado Project Manager interface for a project named '01_Vivado'. The 'Simulation Sources (1)' folder is highlighted with a red box, indicating it is expanded. The 'Sources' pane shows a design source 'average(rt1) (block_average.vhd)' and the expanded simulation source. The 'Project Summary' pane on the right provides details about the project, including the name, location, product family (Zynq-7000), project part (Arty Z7-20), top module name (average), target language (VHDL), and simulator language (Mixed). The 'Board Part' section shows the display name (Arty Z7-20), board part name (digilentinc.com:arty-z7-20:part0:1.0), and board revision (A.0). The 'Design Runs' table at the bottom shows the status of synthesis and implementation runs.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2021)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 20)

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Step 11 – This will show the test bench and the design source to be simulated.

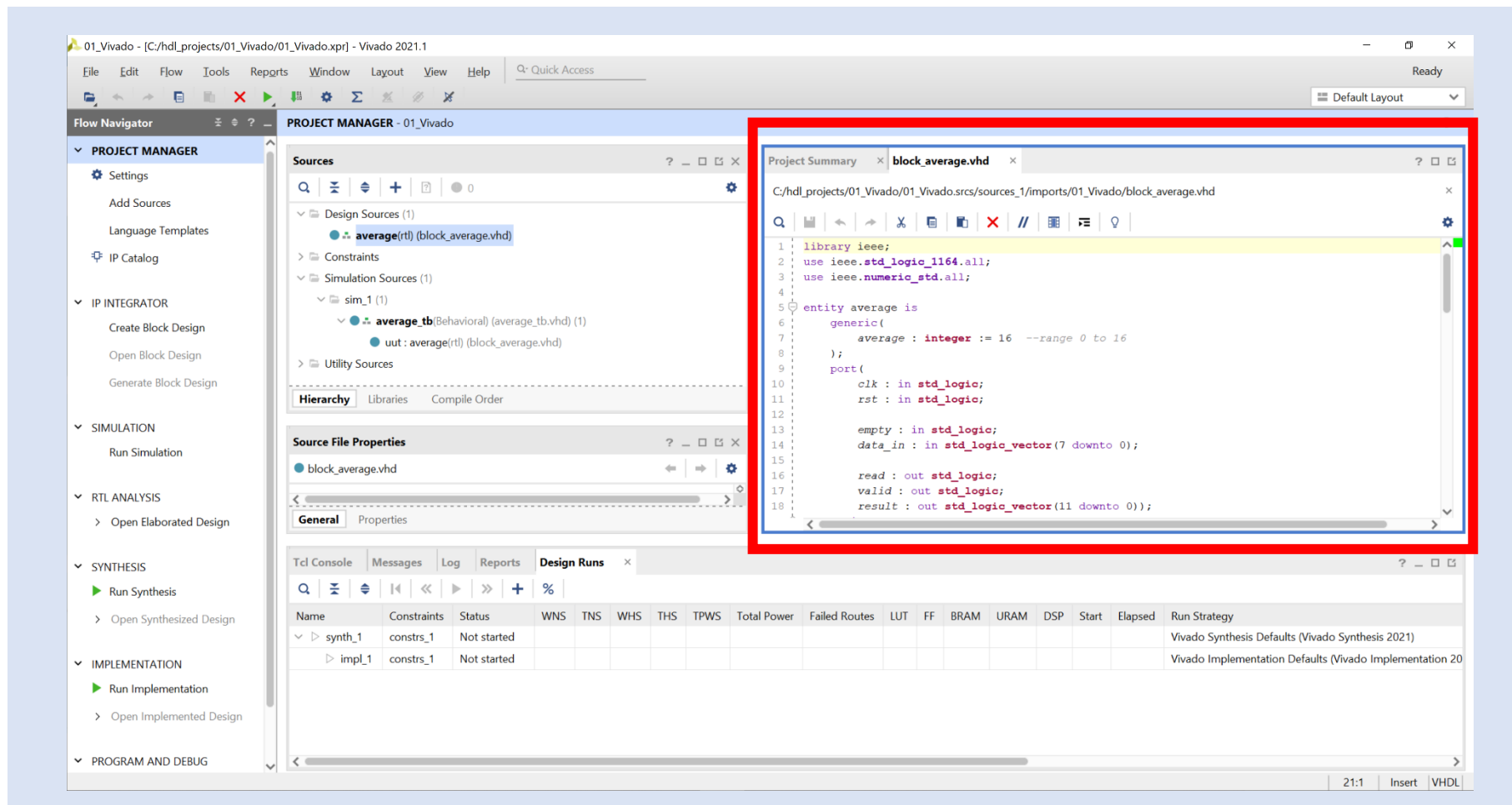
The screenshot displays the Vivado 2021.1 Project Manager interface. The left sidebar shows the Project Manager tree with sections for Settings, IP Integrator, Simulation, RTL Analysis, Synthesis, Implementation, and Program and Debug. The main area is divided into several panels:

- Sources:** Shows Design Sources (1) and Simulation Sources (1). The Simulation Sources section is highlighted with a red box, containing a sub-section 'sim_1 (1)' with a source 'average_tb(Behavioral) (average_tb.vhd) (1)' and a unit under test 'uut: average(rtl) (block_average.vhd)'.
- Project Summary:** Provides an overview of the project, including settings like Project name (01_Vivado), Project location (C:/hdl_projects/01_Vivado), Product family (Zynq-7000), Project part (Arty Z7-20), Top module name (average), Target language (VHDL), and Simulator language (Mixed).
- Board Part:** Shows board details such as Display name (Arty Z7-20), Board part name (digilentinc.com:arty-z7-20:part0:1.0), and Board revision (A.0).
- Design Runs:** A table at the bottom showing the status of synthesis and implementation runs.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2021)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 20)

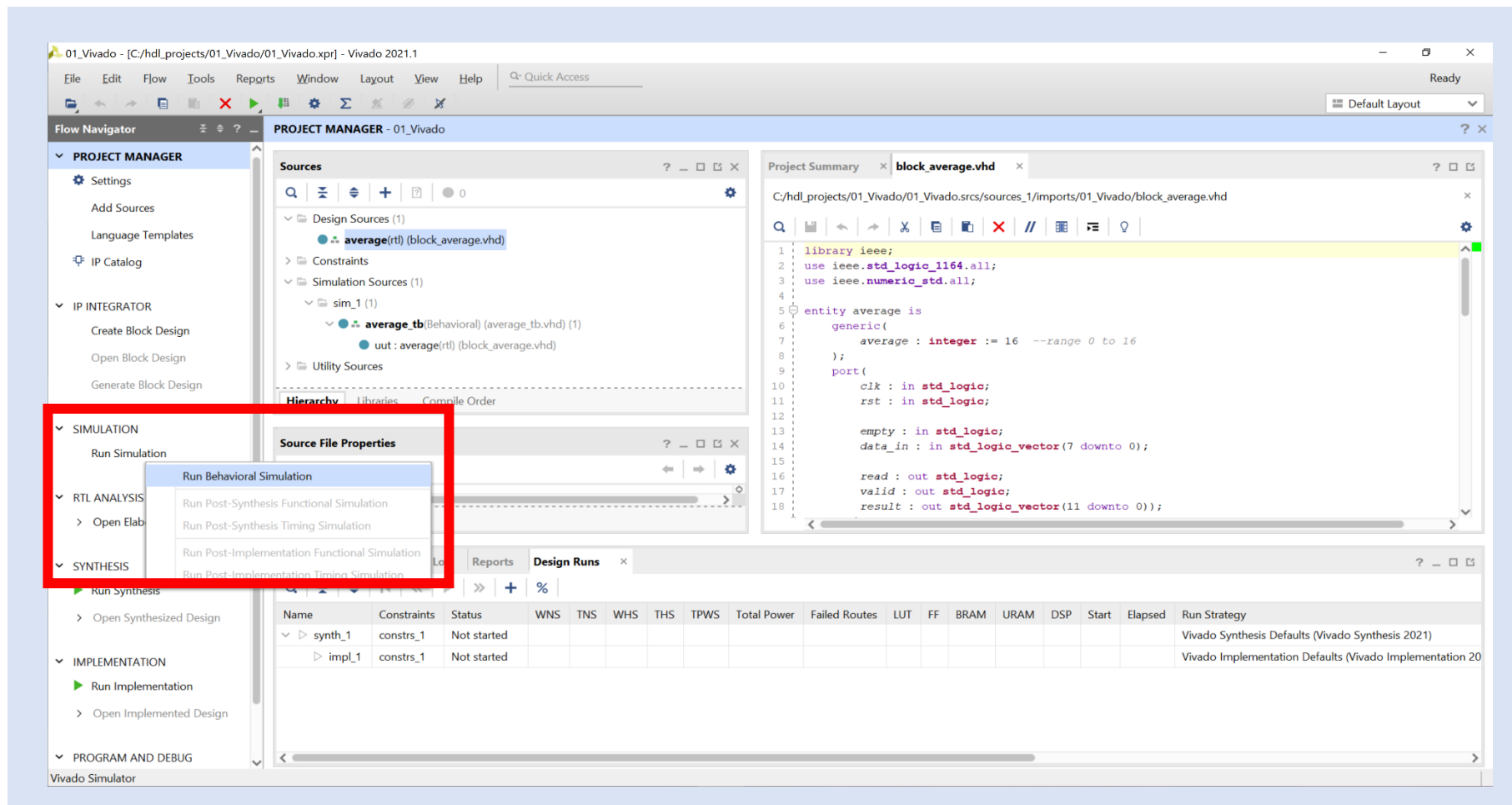
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Step 12 – Double clicking on the VHDL files will open the source for inspection.



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Step 13 – To run a simulation, click on **Run Simulation** and select **Run Behavioral Simulation**.



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Step 14 – This will open the behavioral simulation view. Note the scope and objects.

The screenshot displays the Vivado 2021.1 interface during a behavioral simulation. The main window is titled "SIMULATION - Behavioral Simulation - Functional - sim_1 - average_tb". The left sidebar shows the "PROJECT MANAGER" and "SIMULATION" sections. The "Scope" panel (highlighted with a red box) lists the design units: "average_tb(Behavioral)" and "average(rtl)". The "Objects" panel (also highlighted with a red box) lists the simulation objects and their values:

Name	Value	Data...
i	15	Integer
i	31	Integer
clk	1	Logic
rst	0	Logic
empty	0	Logic
data_in[7:0]	f9	Array
read	1	Logic
valid	0	Logic
result[11:0]	060	Array
stim[0:31]	35,166.5	Array
clk_period	10000 p	Physical

The main editor shows the VHDL code for "average_tb.vhd". The code includes a process that reads data from a stimulus and reports the simulation completion. The following code snippet is highlighted in yellow:

```
report "simulation complete" severity failure;
```

The Tcl Console at the bottom shows the simulation completion messages:

```
xsim: Time (s): cpu = 00:00:08 ; elapsed = 00:00:06 . Memory (MB): peak = 1333.395 ; gain = 18.457
INFO: [USF-XSim-96] XSim completed. Design snapshot 'average_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:10 ; elapsed = 00:00:22 . Memory (MB): peak = 1333.395 ; gain = 18.457
```

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Step 15 – Click on the **Untitled*** tab to see the waveform of the simulation. Note this view shows the signals defined within the test bench only, not the Unit Under Test.

The screenshot displays the Vivado 2021.1 interface during a behavioral simulation. The 'Scope' pane shows the design units 'average_tb(Behavioral)' and 'average(rt1)'. The 'Objects' pane lists various signals and their values, including 'i' (Integer), 'clk' (Logic), 'rst' (Logic), 'empty' (Logic), 'data_in[7:0]' (Array), 'read' (Logic), 'valid' (Logic), 'result[11:0]' (Array), 'stim[0:31]' (Array), and 'clk_period' (Physical). The waveform viewer shows a table of signal values over time, with a red box highlighting the 'Untitled 1' tab. The Tcl Console at the bottom shows simulation completion messages.

Name	Value	624,996 ps	624,998 ps	625,000 ps	625,002 ps
clk	1				
rst	0				
empty	0				
data_in[7:0]	f9		#9		
read	1				
valid	0				
result[11:0]	060		060		
stim[0:31]	35,166,5,233,25,240,41,80,110,77,...				
clk_period	10000 ps		10000 ps		

```

xsim: Time (s): cpu = 00:00:08 ; elapsed = 00:00:06 . Memory (MB): peak = 1333.395 ; gain = 18.457
INFO: [USF-XSim-96] XSim completed. Design snapshot 'average_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:10 ; elapsed = 00:00:22 . Memory (MB): peak = 1333.395 ; gain = 18.457
  
```

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Step 16 – At the moment, the results are in hexadecimal but they make more sense in decimal. Select all the signals, right click, and select **unsigned decimal** from the **radix**.

The screenshot shows the Vivado 2021.1 interface during a behavioral simulation. The 'Objects' window displays a list of signals with their current values and data types. A context menu is open over the waveform, with the 'Radix' option selected and 'Unsigned Decimal' highlighted. The waveform shows signals in hexadecimal format.

Name	Value	Data...
i	15	Integer
i	31	Integer
clk	1	Logic
rst	0	Logic
emp	0	Logic
empty	0	Logic
data_in[7:0]	f9	Array
read	1	Logic
valid	0	Logic
result[11:0]	060	Array
stim[0:31]	35,166,6	Array
clk_period	10000 p	Physical

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Step 17 – This will change the results to decimal. Correct operation has result showing 118 then 96. This is the block average of 16 input values.

The screenshot displays the Vivado 2021.1 interface during a behavioral simulation. The main window shows the simulation results for the 'average_tb' testbench. The 'Scope' pane lists the design units: 'average_tb(Behavioral)' and 'average(rtl)'. The 'Objects' pane shows the current state of the simulation, including variables like 'i', 'clk', 'rst', 'empty', 'data_in[7:0]', 'read', 'valid', 'result[11:0]', 'stim[0:31]', and 'clk_period'. The 'Timing Diagram' pane shows the waveforms for 'clk', 'rst', 'empty', 'data_in[7:0]', 'read', 'valid', 'result[11:0]', 'stim[0:31]', and 'clk_period'. The 'Tcl Console' pane shows the simulation logs, including the completion of the XSim simulation and the launch_simulation command.

Name	Value	Data...
i	15	Integer
i	31	Integer
clk	1	Logic
rst	0	Logic
empty	0	Logic
data_in[7:0]	f9	Array
read	1	Logic
valid	0	Logic
result[11:0]	060	Array
stim[0:31]	35,166,5	Array
clk_period	10000 ps	Physical

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Step 18 – Often we want to be able to see the signals in the UUT. To do this, first let's insert a divider. Right click on the **bottom signal** and select **New Divider**.

The screenshot displays the Vivado IDE interface during a behavioral simulation. The main window shows a waveform viewer with a context menu open over the 'clk' signal. The menu options include 'Go To Source Code', 'Show in Object Window', 'Report Drivers', 'Force Constant...', 'Force Clock...', 'Remove Force', 'Cut', 'Copy', 'Paste', 'Delete', 'Find...', 'Find Value...', 'Select All', 'Expand', 'Collapse', 'Ungroup', 'Rename', 'Name', 'Waveform Style', 'Signal Color', 'Divider Color', 'Radix', 'Show as Enumeration', 'Reverse Bit Order', 'New Group', and 'New Divider'. The 'New Divider' option is highlighted. The waveform shows a clock signal and other signals like 'data_in[7:0]', 'read', and 'valid'. The Tcl Console at the bottom shows simulation logs.

Name	Value	Data...
i	15	Integer
i	31	Integer
clk	1	Logic
rst	0	Logic
empty	0	Logic
data_in[7:0]	f9	Array
read	1	Logic
valid	0	Logic
result[11:0]	060	Array
stim[0:31]	35,166,1	Array
clk_period	10000 p	Physical

```
xsim: Time (s): cpu = 00:00:08 ; elapsed = 00:00:06 . Memory (MB): peak = 333.395 ;
INFO: [USF-XSim-96] XSim completed. Design snapshot 'average_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:10 ; elapsed = 00:00:22 . Memory (MB): peak
```

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Step 19 – When prompted, enter the name **UUT** and you will see the new divider in the waveform.

The screenshot displays the Vivado IDE interface during a behavioral simulation. The main window shows a waveform for 'average_tb'. The waveform includes signals such as 'clk' (clock), 'rst' (reset), 'empty', 'data_in[7:0]', 'read', 'valid', 'result[11:0]', and 'stim[0:31]'. A red box highlights the 'UUT' divider in the waveform, which is currently empty. The Tcl Console at the bottom shows the following simulation completion messages:

```

xsim: Time (s): cpu = 00:00:08 ; elapsed = 00:00:06 . Memory (MB): peak = 1333.395 ; gain = 18.457
INFO: [USF-XSim-96] XSim completed. Design snapshot 'average_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:10 ; elapsed = 00:00:22 . Memory (MB): peak = 1333.395 ; gain = 18.457

```

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Step 20 – To add in the UUT, right click on the **UUT** under the scope and select **Add to Wave Window**.

The screenshot displays the Vivado 2021.1 interface during a simulation. The 'Scope' window is open, showing a tree view of the design hierarchy. The 'UUT' (User Under Test) is highlighted, and a context menu is open over it. The menu options are:

- Add to Wave Window
- Log to Wave Database
- Go to Source Code
- Go to Instantiation Source Code
- Set Current Scope To Active

The background shows a simulation waveform with various signals like 'clk', 'rst', 'data_in[7:0]', 'result[11:0]', and 'stim[0:31]'. The Tcl Console at the bottom shows the command:

```
add_wave (/average_tb/uut)
current_wave_config (Untitled 1)
Untitled 1
add_wave (/average_tb/uut)
```

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Step 21 – This will add in the UUT signals, however, some information may be missing as it was not saved during the simulation.

The screenshot displays the Vivado 2021.1 interface during a behavioral simulation. The main window shows the 'Scope' window with the following table:

Name	Design Unit	Block Type
average_tb(Behavioral)		VHDL Entity
average(rtl)		VHDL Entity

The 'Objects' window shows the following table:

Name	Value	Unit
clk	1	L
rst	0	L
empty	0	L
data_in[7:0]	f9	A
read	1	L
valid	0	L
result[11:0]	060	A
accumulator[11:0]	6cf	A
counter	7	li
output[19:0]	06000	A
rd_int	1	L
rd_int_del	1	L
average	16	li
reciprocal[7:0]	10	A

The Waveform window shows a timing diagram with a yellow vertical line at 235.000 ns. The signals listed in the Waveform window are:

Name	Value
UUT	
clk	1
rst	0
empty	0
data_in[7:0]	50
read	1
valid	0
result[11:0]	000
accumulator[11:0]	
counter	
output[19:0]	
rd_int	

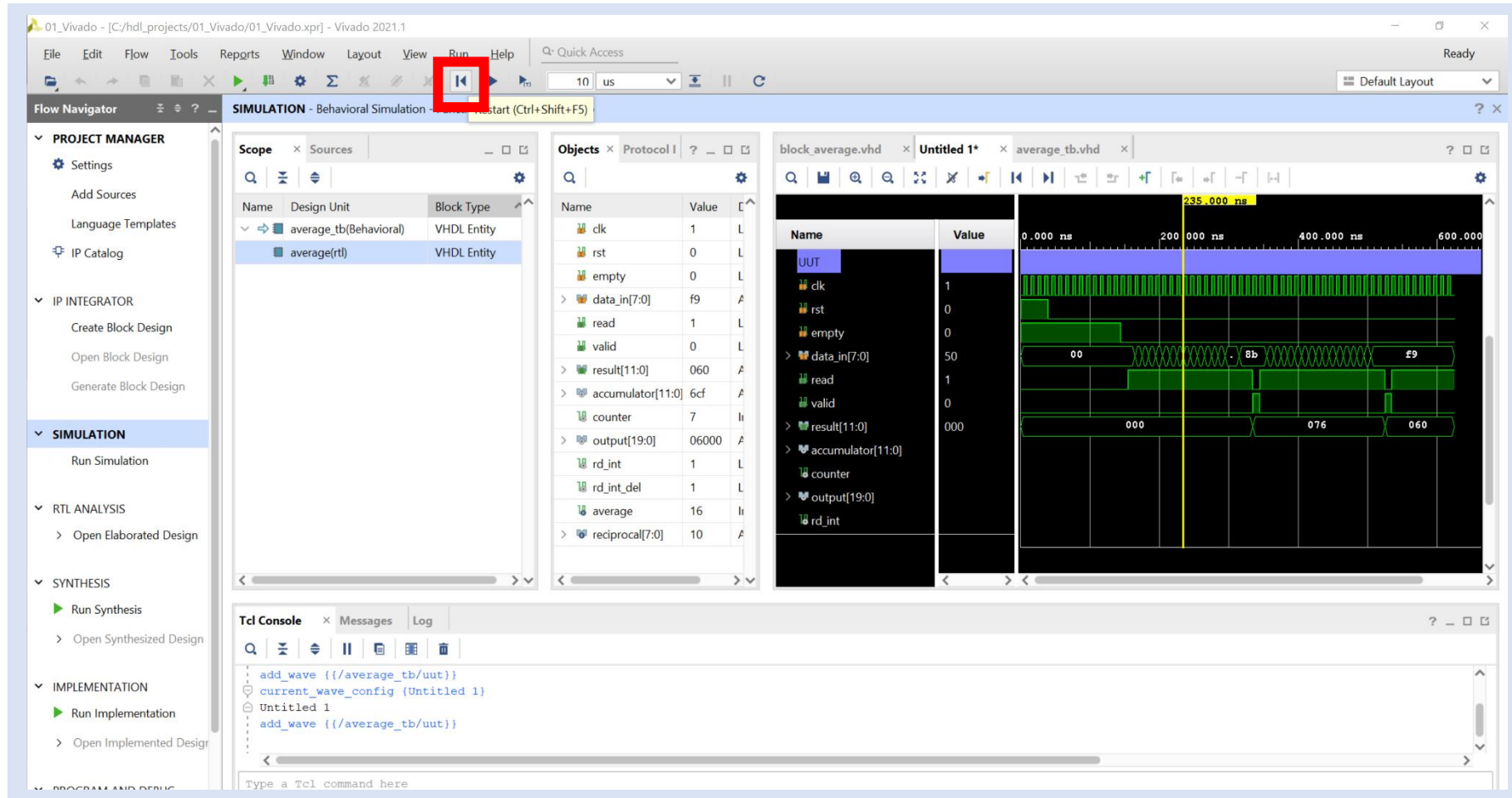
The Tcl Console shows the following commands:

```

add_wave (/average_tb/uut)
current_wave_config {Untitled 1}
Untitled 1
add_wave (/average_tb/uut)
  
```

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Step 22 – To add in the missing waveform, we need to restart the simulation. Select **Restart** from menu bar.



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Step 23 – This will clear all waveform data and restart the simulation.

The screenshot displays the Vivado IDE interface during a behavioral simulation. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, Run, and Help. The main workspace is divided into several panes:

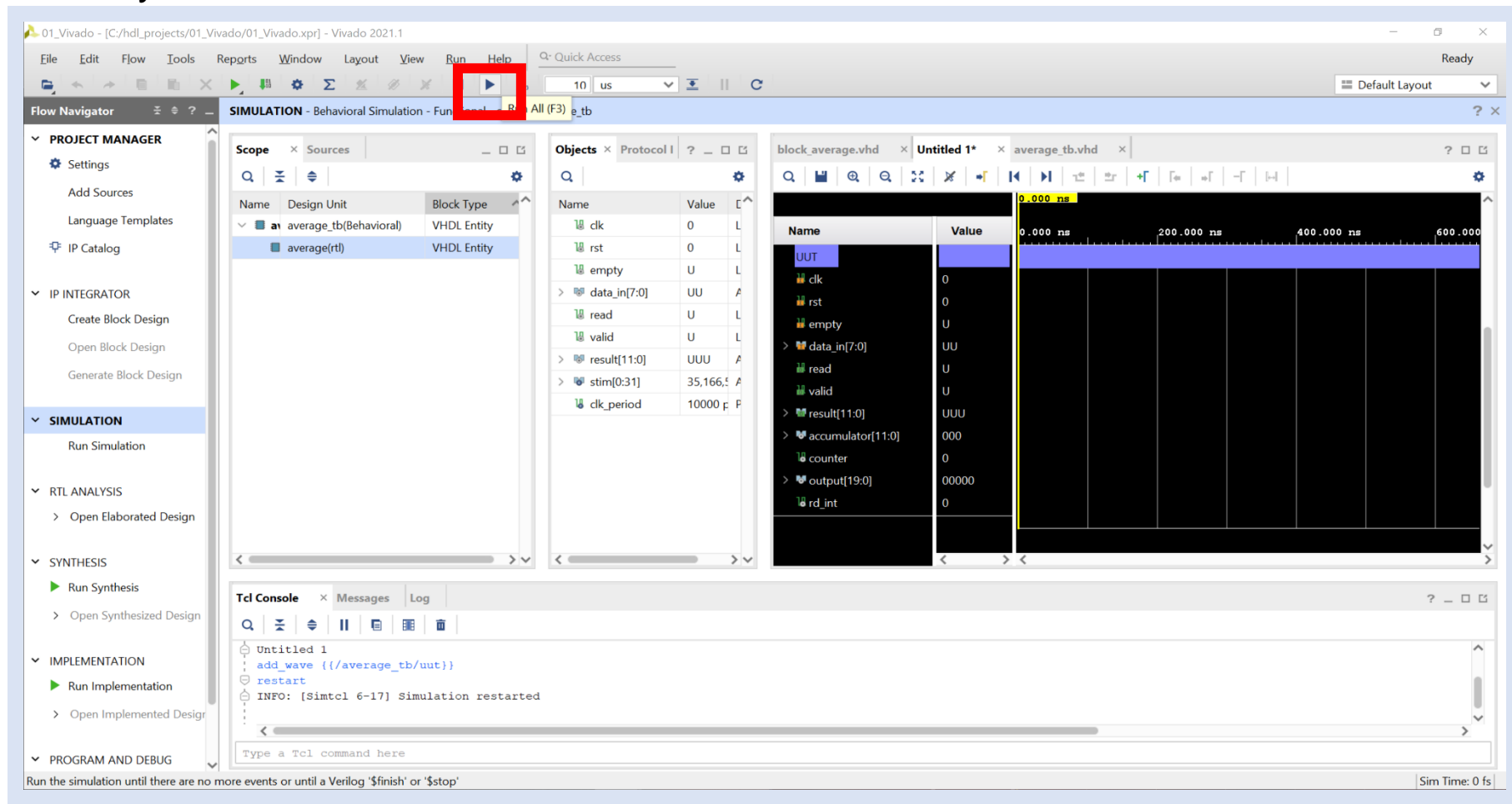
- Flow Navigator:** Shows the project structure with sections for PROJECT MANAGER, IP INTEGRATOR, SIMULATION, RTL ANALYSIS, SYNTHESIS, IMPLEMENTATION, and PROGRAM AND DEBUG.
- Scope:** Lists design units and block types, including 'average_tb(Behavioral)' and 'average(rtl)'.
- Objects:** Displays simulation variables and their values, such as 'clk' (0), 'rst' (0), 'empty' (U), 'data_in[7:0]' (UU), 'read' (U), 'valid' (U), 'result[11:0]' (UUU), 'stim[0:31]' (35,166,5), and 'clk_period' (10000).
- Waveform Window (highlighted in red):** Shows a list of signals on the left and a corresponding waveform plot on the right. The signals listed are UUT, clk, rst, empty, data_in[7:0], read, valid, result[11:0], accumulator[11:0], counter, output[19:0], and rd_int. The waveform plot shows a time axis from 0.000 ns to 600.000 ns.
- Tcl Console:** Contains the following commands and output:

```
Untitled 1
add_wave (/average_tb/uut)
restart
INFO: [Simtcl 6-17] Simulation restarted
```

The status bar at the bottom right indicates 'Sim Time: 0 fs'.

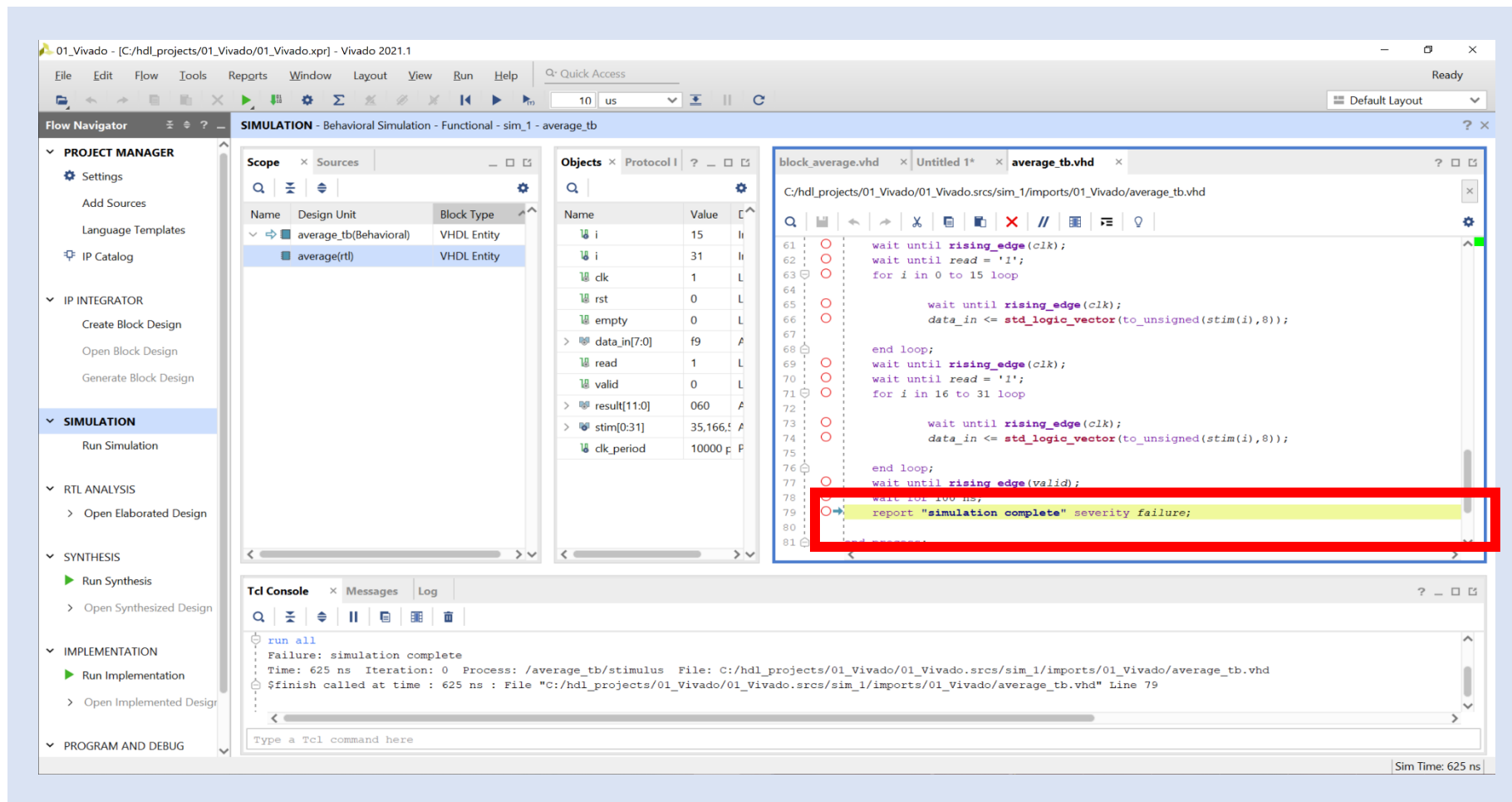
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Step 24 – To rerun the simulation, select the **Run** button on the menu. The simulation will stop automatically.



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Step 25 – When the simulation completes, you will see the highlighted line in the test bench.



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Step 26 – Selecting the **waveform tab** again will show all the signals for the UUT.

The screenshot displays the Vivado 2021.1 interface during a behavioral simulation. The main window shows the 'SIMULATION - Behavioral Simulation - Functional - sim_1 - average_tb' project. The 'Scope' pane on the left lists the design units and block types. The 'Objects' pane in the center shows the current object's properties. The 'Waveform' pane on the right displays the simulation results, with the 'UUT' signals highlighted in a red box. The 'Tcl Console' at the bottom shows the simulation completion message.

Name	Value
stim[0:31]	35,166,5,233,25,240,41,80,110,77,117,94,220,160,16...
clk period	10000 ps
UUT	
clk	1
rst	0
empty	0
data_in[7:0]	#9
read	1
valid	0
result[11:0]	060
accumulator[11:0]	6cf
counter	7

```
run all
...
Failure: simulation complete
...
Time: 625 ns Iteration: 0 Process: /average_tb/stimulus File: C:/hdl_projects/01_Vivado/01_Vivado.srcs/sim_1/imports/01_Vivado/average_tb.vhd
$finish called at time : 625 ns : File "C:/hdl_projects/01_Vivado/01_Vivado.srcs/sim_1/imports/01_Vivado/average_tb.vhd" Line 79
```

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Step 27 – If you make changes to the source code, you need to relaunch the simulation. This can be achieved using the relaunch button on the menu.

The screenshot shows the Vivado IDE interface during a simulation. The top menu bar includes 'File', 'Edit', 'Flow', 'Tools', 'Reports', 'Window', 'Layout', 'View', 'Run', and 'Help'. The 'Run' menu is open, and the 'Launch Simulation' button is highlighted with a red box. The main workspace is divided into several panels:

- Project Manager:** Shows the project structure with 'average_tb(Behavioral)' and 'average(rt)' selected.
- Scope:** Lists the design units and block types.
- Objects:** Lists the objects in the simulation, including 'i', 'clk', 'rst', 'empty', 'data_in[7:0]', 'read', 'valid', 'result[11:0]', 'stim[0:31]', and 'clk_period'.
- Simulation Waveform:** Displays the timing diagram for the simulation, showing signals like 'stim[0:31]', 'clk_period', 'UUT', 'clk', 'rst', 'empty', 'data_in[7:0]', 'read', 'valid', 'result[11:0]', 'accumulator[11:0]', and 'counter'.
- Tcl Console:** Shows the simulation results, including the command 'run all' and the output 'Failure: simulation complete'.

The bottom status bar indicates 'Sim Time: 625 ns'.

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Step 28 – With the simulation complete, we are now ready to implement the design. Close the simulation view.

The screenshot shows the Vivado IDE interface during a behavioral simulation. The main window displays the simulation results, including a table of signal values and a timing diagram. The 'Close Simulation' button is highlighted with a red box.

Simulation Results Table:

Name	Value
stim[0:31]	35,166,5,233,...
clk_period	10000 ps
UUT	
clk	1
rst	0
empty	0
data_in[7:0]	f9
read	1
valid	0
result[11:0]	060
stim[0:31]	35,166,5,233,...
clk_period	10000 ps

Timing Diagram:

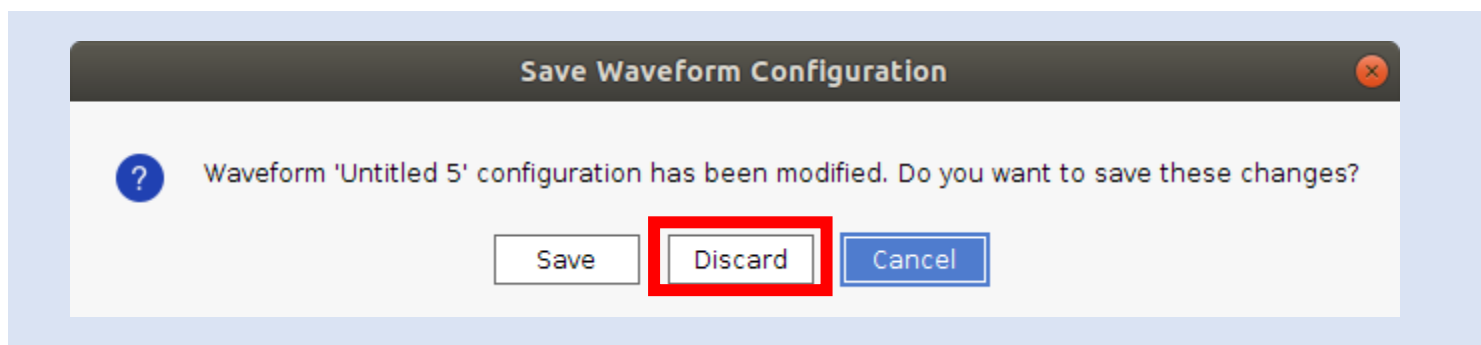
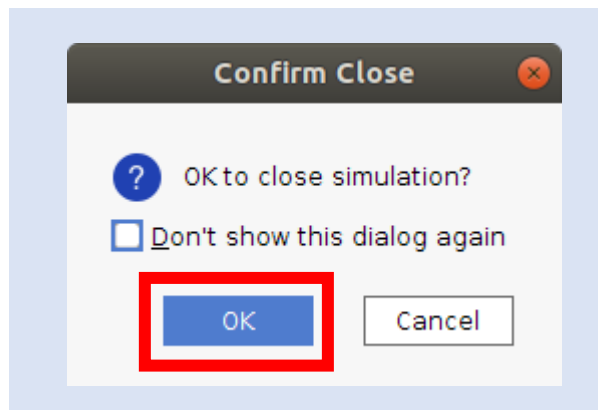
The timing diagram shows the signals over time. The x-axis represents time in nanoseconds (ns), with markers at 200.000 ns, 400.000 ns, 600.000 ns, and 825.000 ns. The signals shown include stim[0:31], clk, rst, empty, data_in[7:0], read, valid, result[11:0], accumulator[11:0], and counter. The diagram shows the signals changing over time, with the result[11:0] signal showing values 000, 076, and 060.

Tcl Console:

```
run all
Failure: simulation complete
Time: 625 ns Iteration: 0 Process: /average_tb/stimulus File: C:/hdl_projects/01_Vivado/01_Vivado.srscs/sim_1/imports/01_Vivado/average_tb.vhd
$finish called at time : 625 ns : File "C:/hdl_projects/01_Vivado/01_Vivado.srscs/sim_1/imports/01_Vivado/average_tb.vhd" Line 79
```

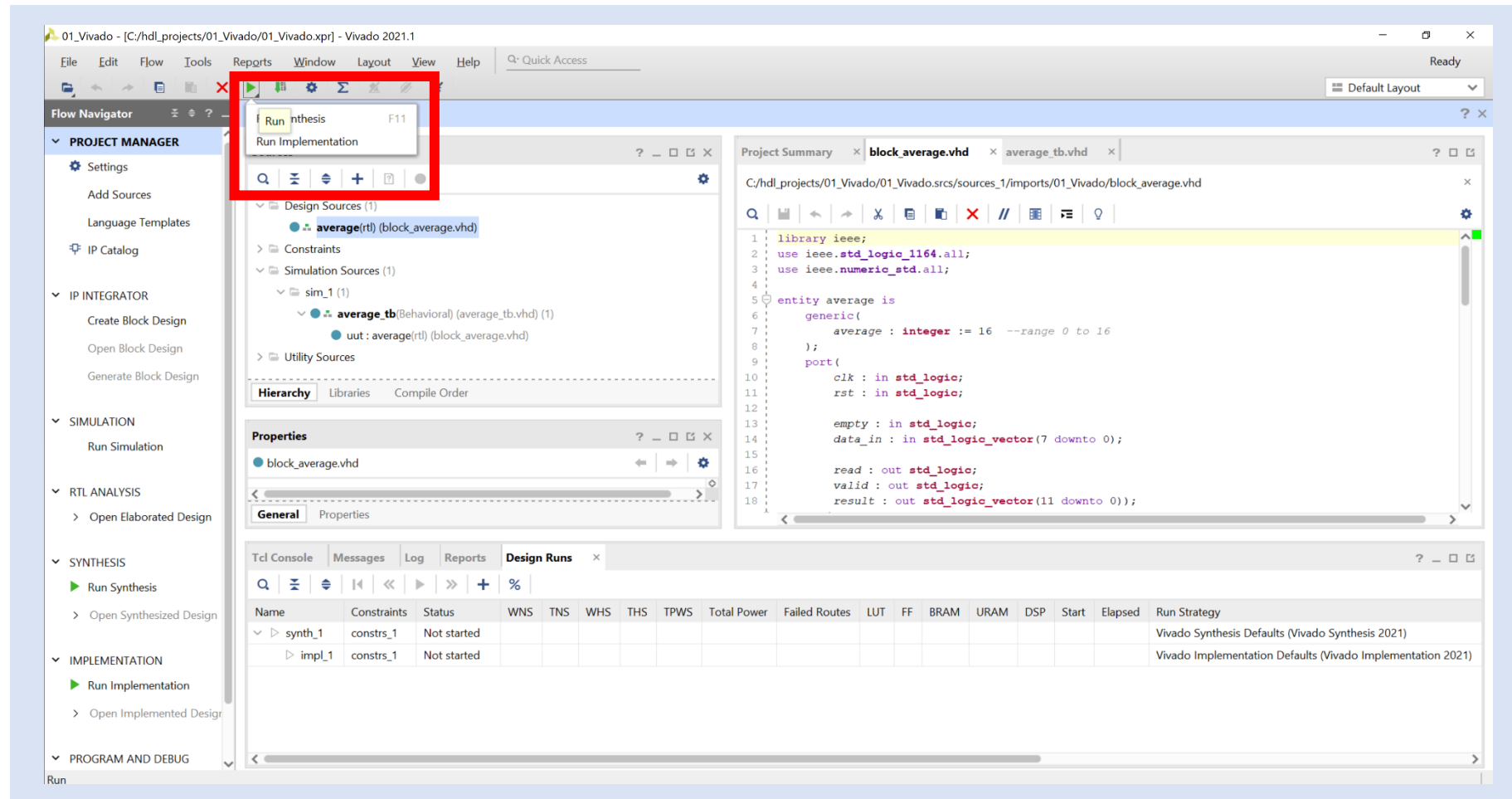
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Step 29 – When asked to confirm, click **OK**. If a save waveform dialog pops up, select **Discard**.



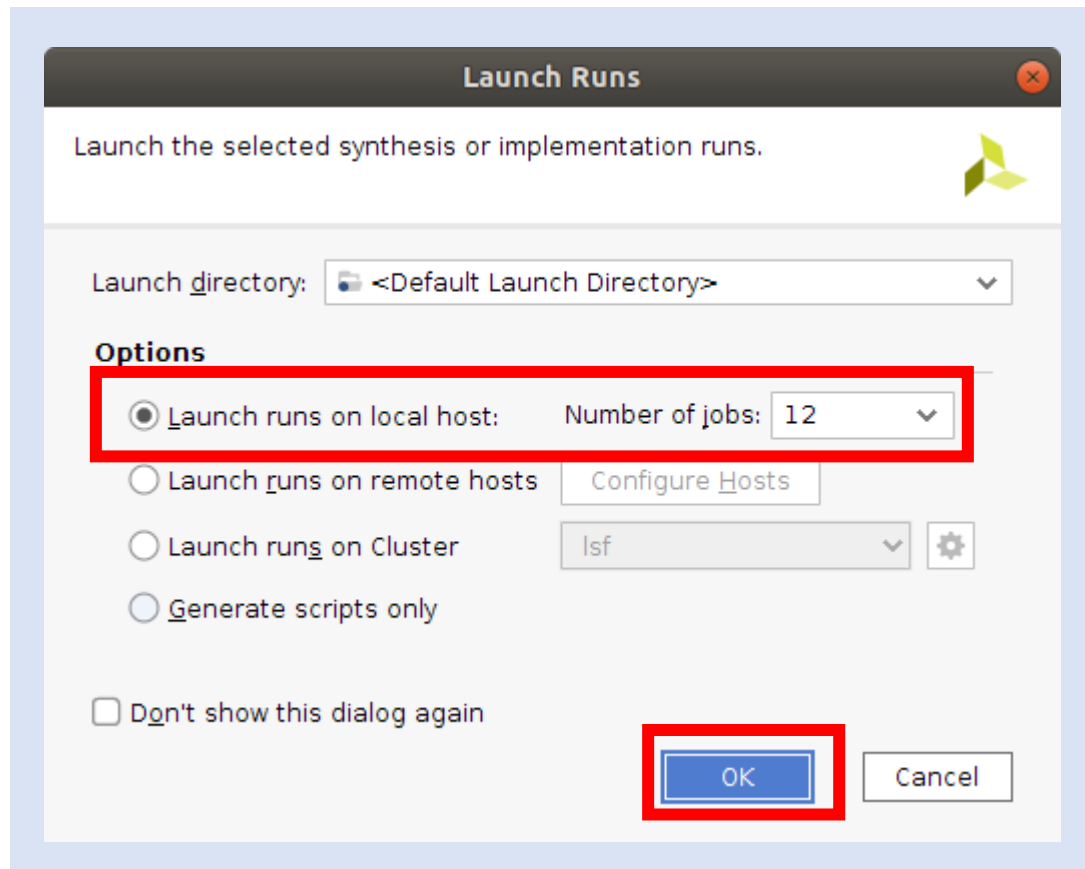
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Step 30 – To synthesize the design, click the **green run arrow** and select **Run Synthesis**.



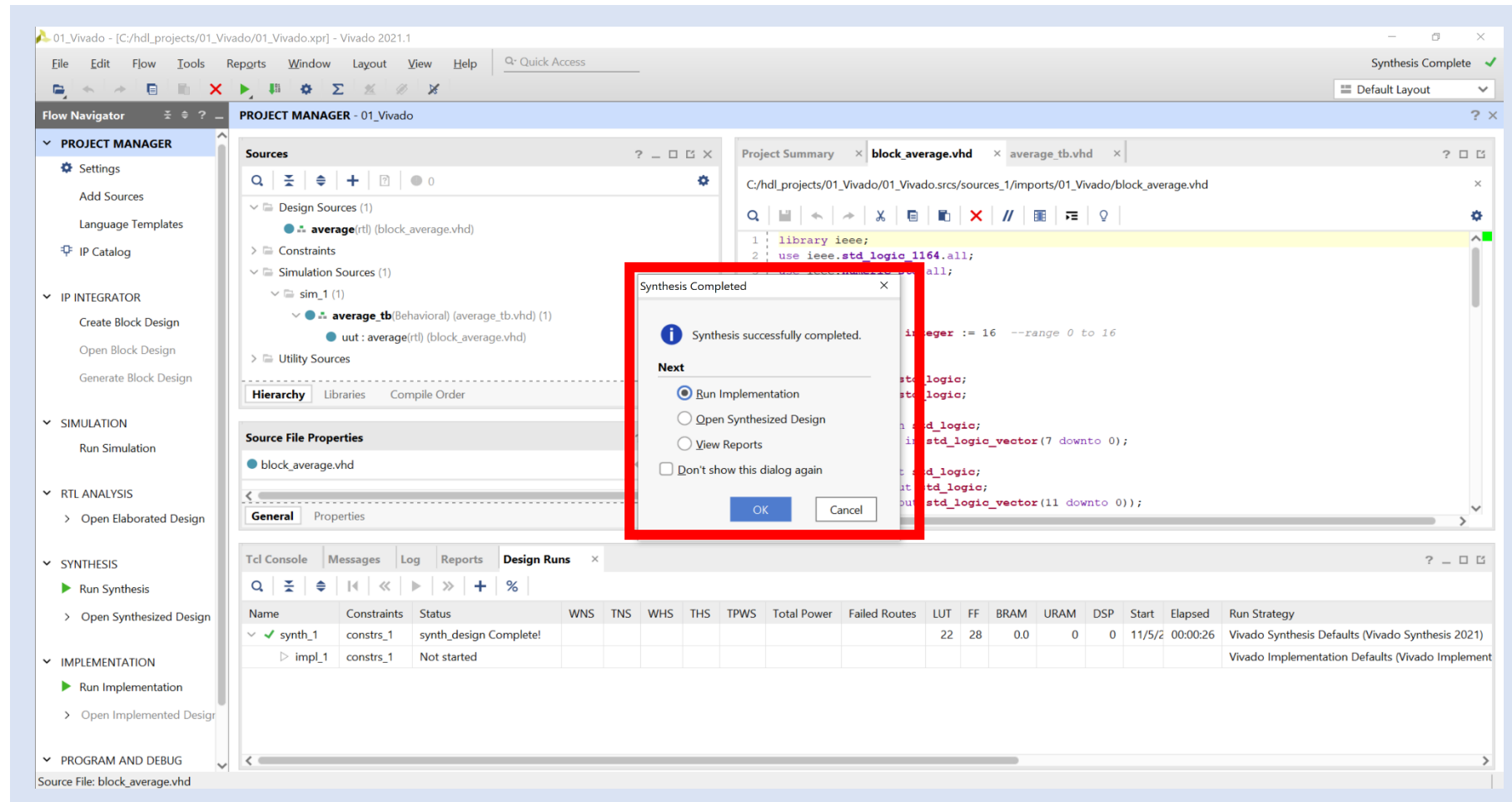
Lab 4: Overview and Introduction to Vivado

Step 31 – On the Launch Runs dialog, select the number of jobs you want to run on your system and click **OK**.



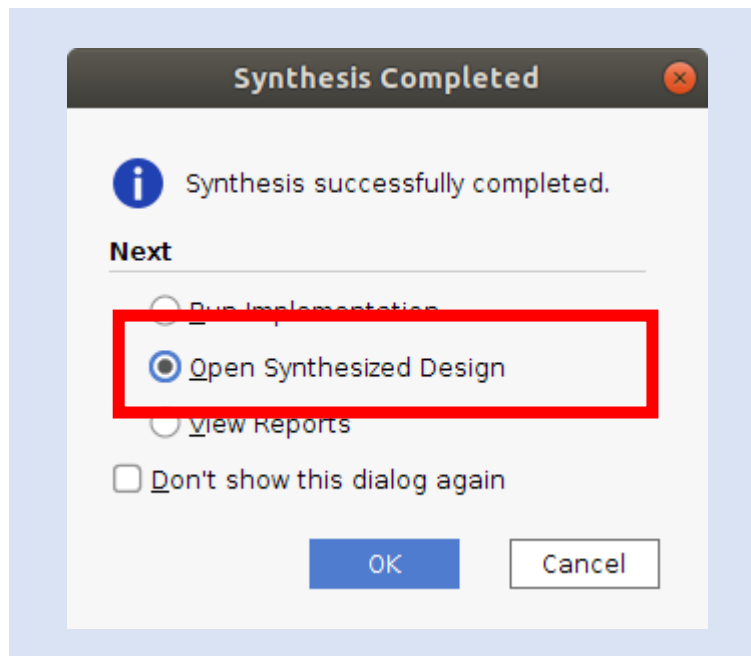
Lab 4: Overview and Introduction to Vivado

Step 32 – When synthesis is complete, you will see a dialog box appear.



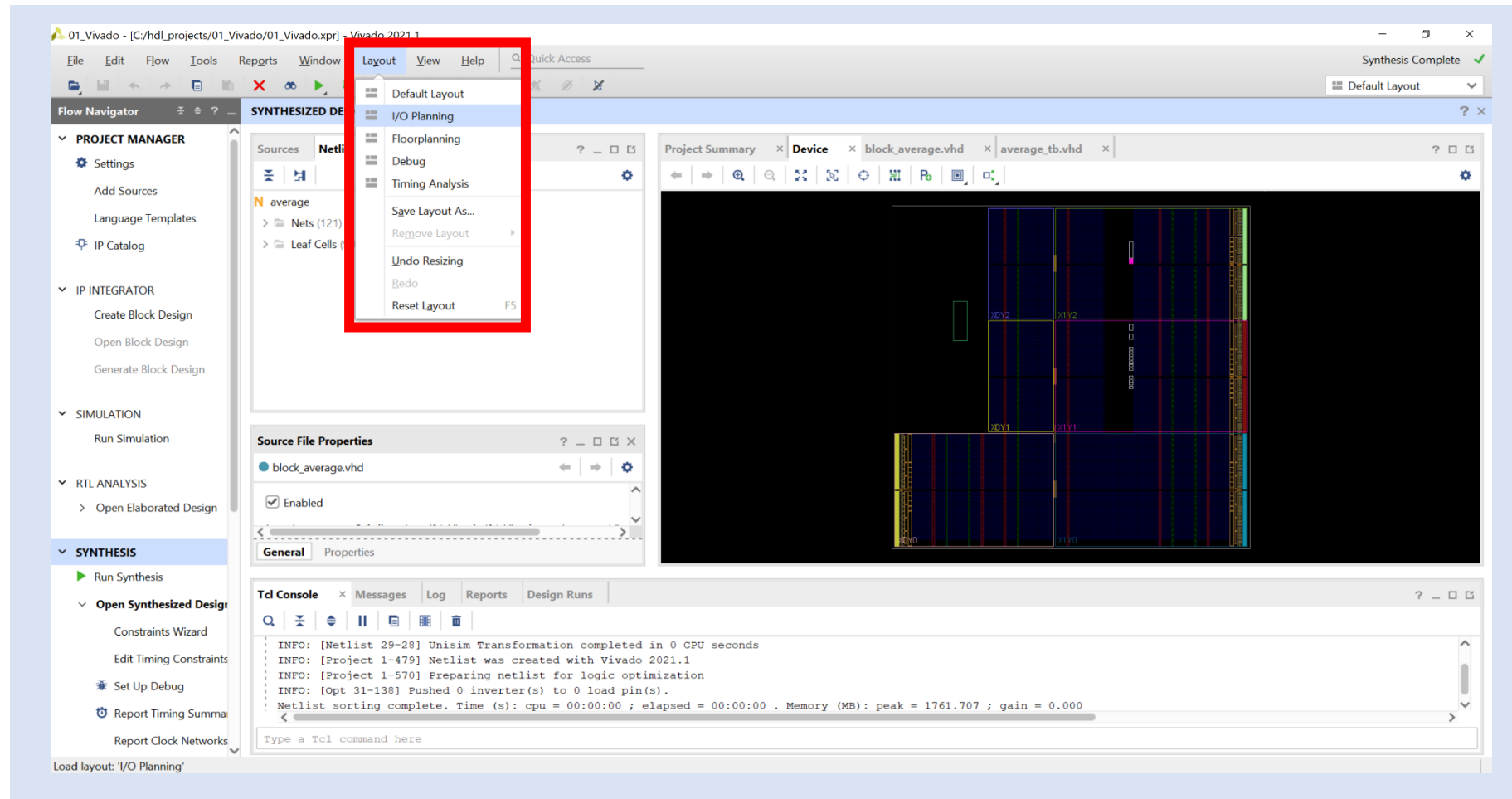
Lab 4: Overview and Introduction to Vivado

Step 33 – Select Open Synthesized Design.



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Step 34 – This will open the synthesis view. From the menu layout, select **I/O Planning**.



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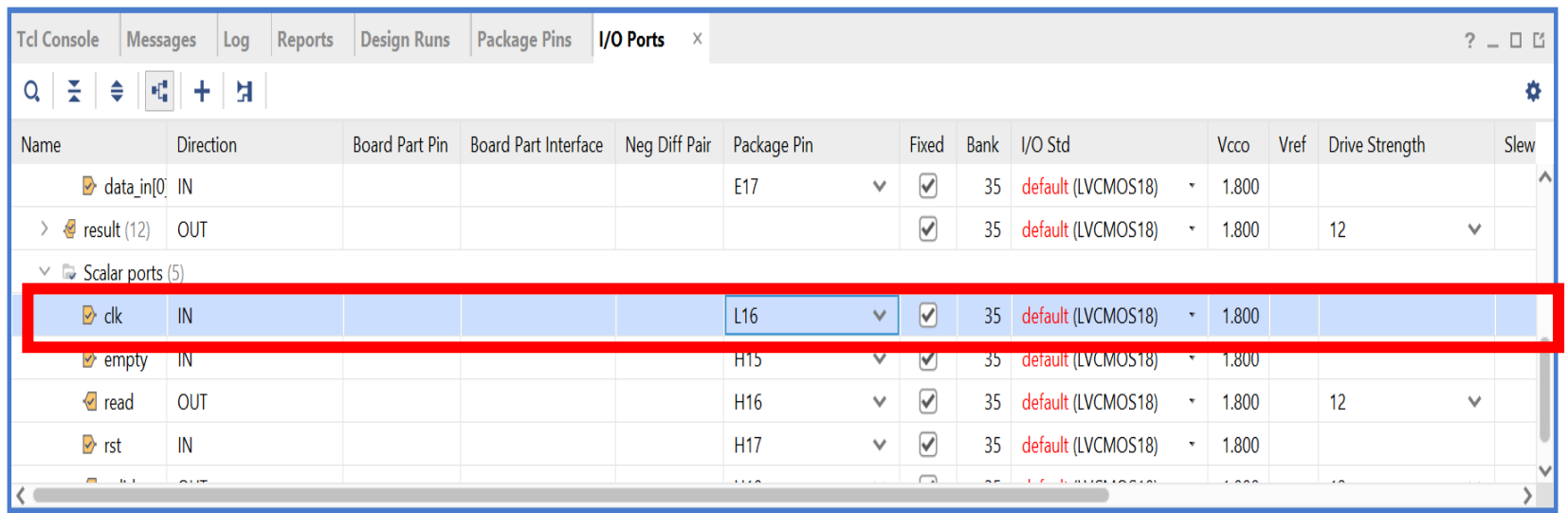
Step 35 – Expand the **Data_In, Result and Scalar Ports** and assign them to pins. All EXCEPT the clock pin can be assigned to any pin.

The screenshot shows the Vivado IDE interface. The I/O Pin Properties window is open, showing the Name: clk. The I/O Pin Table is highlighted with a red box and contains the following data:

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew
data_in[6]	IN				B19	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800			
data_in[5]	IN				B20	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800			
data_in[4]	IN				C20	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800			
data_in[3]	IN				D18	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800			
data_in[2]	IN				D19	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800			
data_in[1]	IN				D20	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800			
data_in[0]	IN				E17	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800			

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Step 36 – Assign the **clock pin to L16**. Clocks have to be assigned to clock capable pins.

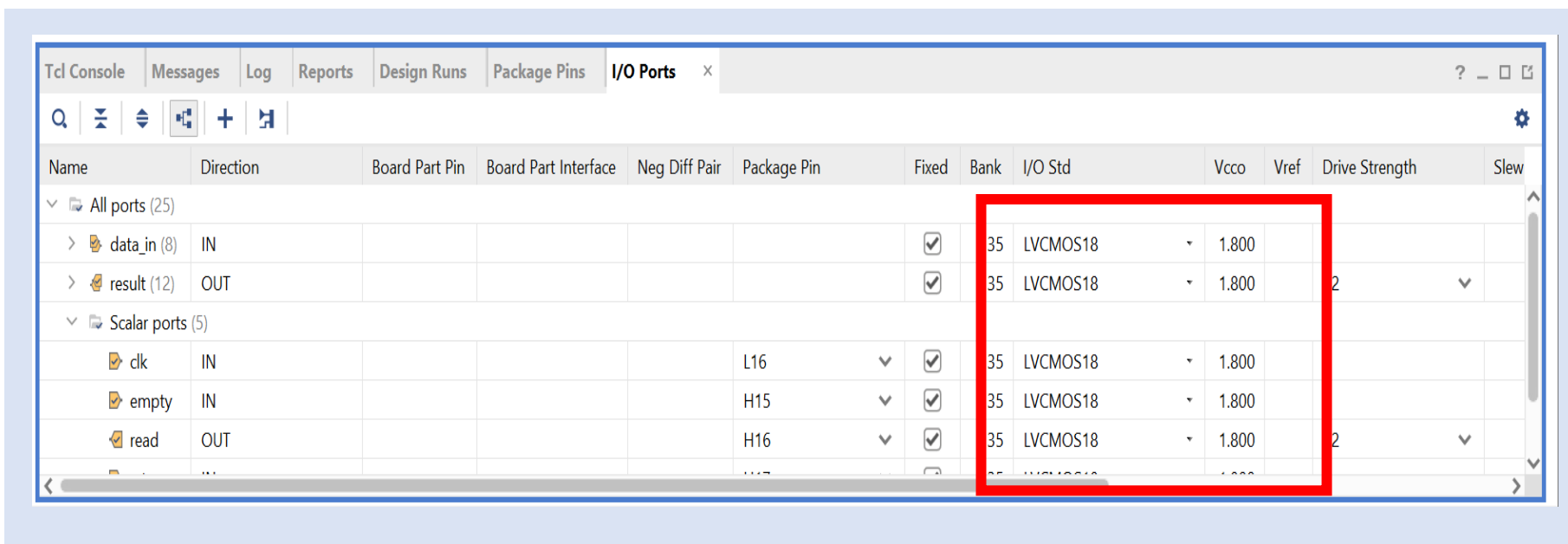


The screenshot shows the Vivado I/O Ports window with a table of ports. The 'clk' port is highlighted with a red box, indicating it is assigned to pin L16. The table columns include Name, Direction, Board Part Pin, Board Part Interface, Neg Diff Pair, Package Pin, Fixed, Bank, I/O Std, Vcco, Vref, Drive Strength, and Slew.

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew
data_in[0]	IN				E17	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800			
result (12)	OUT					<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800		12	
Scalar ports (5)												
clk	IN				L16	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800			
empty	IN				H15	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800			
read	OUT				H16	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800		12	
rst	IN				H17	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800			
...	

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Step 37 – Ensure the **IO Standard** is set to **LVC MOS18**. Do not leave it as default because this will lead to a failure to implement and generate a bitstream.



The screenshot shows the 'I/O Ports' configuration window in Vivado. The table below lists the configured ports and their settings. A red box highlights the 'I/O Std' column, which is set to 'LVC MOS18' for all ports.

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew
▼ All ports (25)												
> data_in (8)	IN					<input checked="" type="checkbox"/>	35	LVC MOS18	1.800			
> result (12)	OUT					<input checked="" type="checkbox"/>	35	LVC MOS18	1.800		2	▼
▼ Scalar ports (5)												
clk	IN				L16	<input checked="" type="checkbox"/>	35	LVC MOS18	1.800			
empty	IN				H15	<input checked="" type="checkbox"/>	35	LVC MOS18	1.800			
read	OUT				H16	<input checked="" type="checkbox"/>	35	LVC MOS18	1.800		2	▼
...					H17	<input checked="" type="checkbox"/>	35	LVC MOS18	1.800			

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Step 38 – Save the Constraints we just edited.

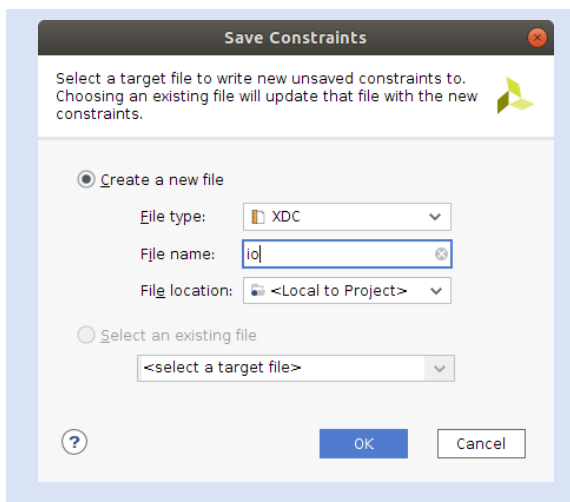
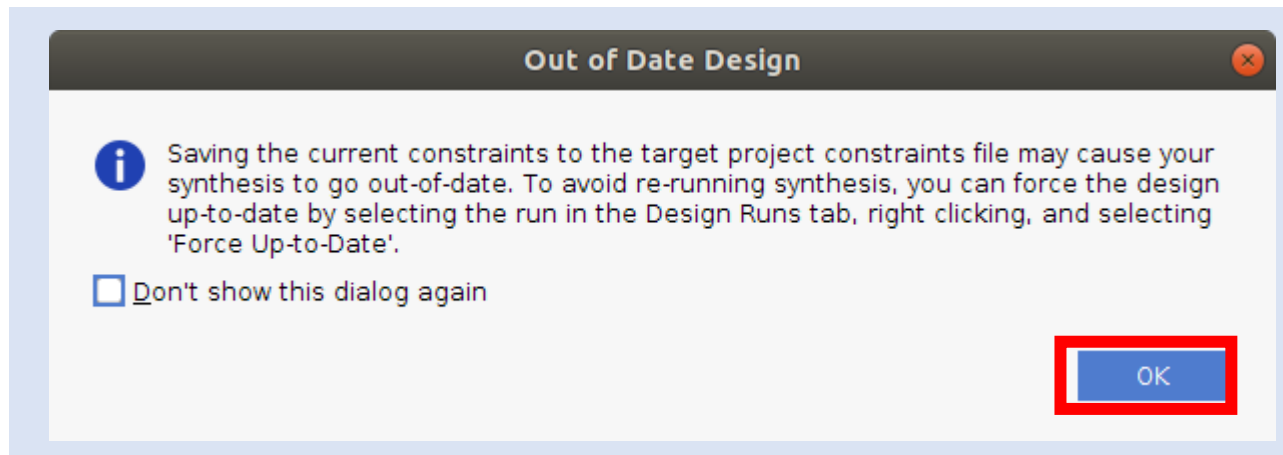
The screenshot shows the Vivado 2021.1 interface. The Project Manager on the left is highlighted with a red box, showing the 'Save Constraints (Ctrl+S)' option. The Synthesized Design window displays the 'Device Constraints' for 'Internal VREF' and 'NONE (3)'. The I/O Port Properties window shows 'Name: valid', 'Direction: OUT', and 'Package pin: H18'. The I/O Ports table is visible at the bottom.

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew
All ports (25)												
data_in (8)	IN					<input checked="" type="checkbox"/>	35	LVC MOS18	-	1.800		
result (12)	OUT					<input checked="" type="checkbox"/>	35	LVC MOS18	-	1.800	12	
Scalar ports (5)												
clk	IN				L16	<input checked="" type="checkbox"/>	35	LVC MOS18	-	1.800		
empty	IN				H15	<input checked="" type="checkbox"/>	35	LVC MOS18	-	1.800		
read	OUT				H16	<input checked="" type="checkbox"/>	35	LVC MOS18	-	1.800	12	

Save the constraints for the current design.

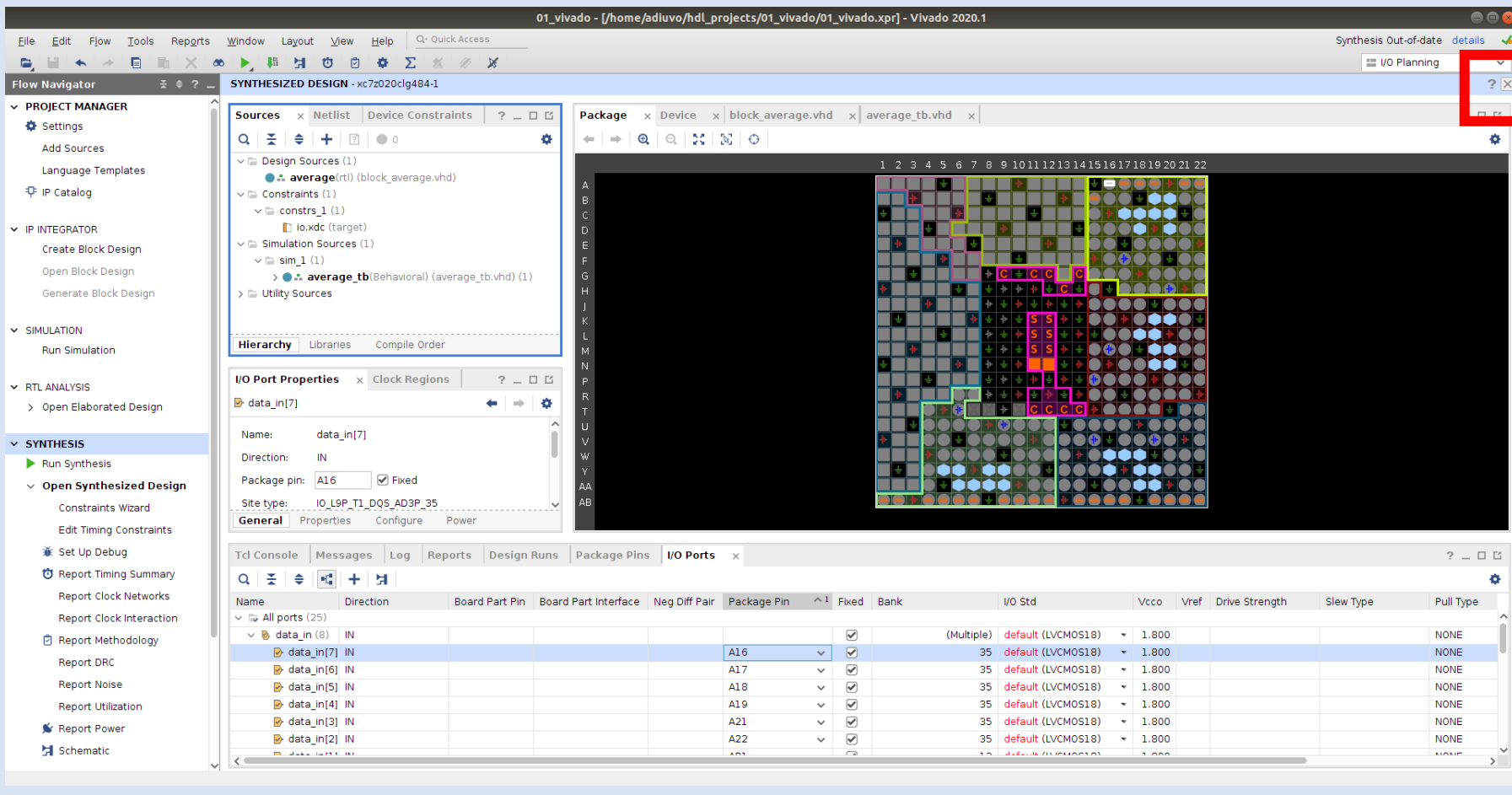
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Step 39 – This will present two new dialogs. Click **OK** on the first and enter a **file name** for the second.



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Step 40 – Close the Synthesis View.



The screenshot shows the Vivado 2020.1 interface with the Synthesis View open. The I/O Planning window is highlighted with a red box, indicating the step to close it. The interface includes the Project Manager, Sources, I/O Port Properties, and I/O Ports tables.

Sources

- Design Sources (1)
 - average(rtl) (block_average.vhd)
- Constraints (1)
 - constrs_1 (1)
 - io.xdc (target)
- Simulation Sources (1)
 - sim_1 (1)
 - average_tb(Behavioral) (average_tb.vhd) (1)
- Utility Sources

I/O Port Properties

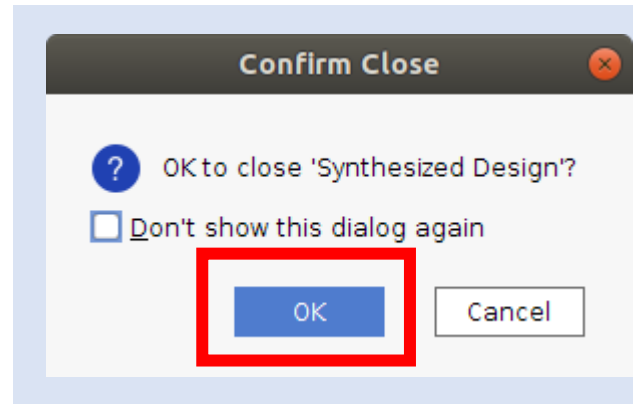
Name: data_in[7]
Direction: IN
Package pin: A16 Fixed
Site type: IO_L9P_T1_DQS_AD3P_35

I/O Ports

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type
data_in (8)	IN					<input checked="" type="checkbox"/>	(Multiple)	default (LVCMOS18)	1.800				NONE
data_in[7]	IN				A16	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800				NONE
data_in[6]	IN				A17	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800				NONE
data_in[5]	IN				A18	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800				NONE
data_in[4]	IN				A19	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800				NONE
data_in[3]	IN				A21	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800				NONE
data_in[2]	IN				A22	<input checked="" type="checkbox"/>	35	default (LVCMOS18)	1.800				NONE

Lab 4: Overview and Introduction to Vivado

Step 41 – Confirm the decision to close by clicking **OK**. This will take us back to the project manager view.



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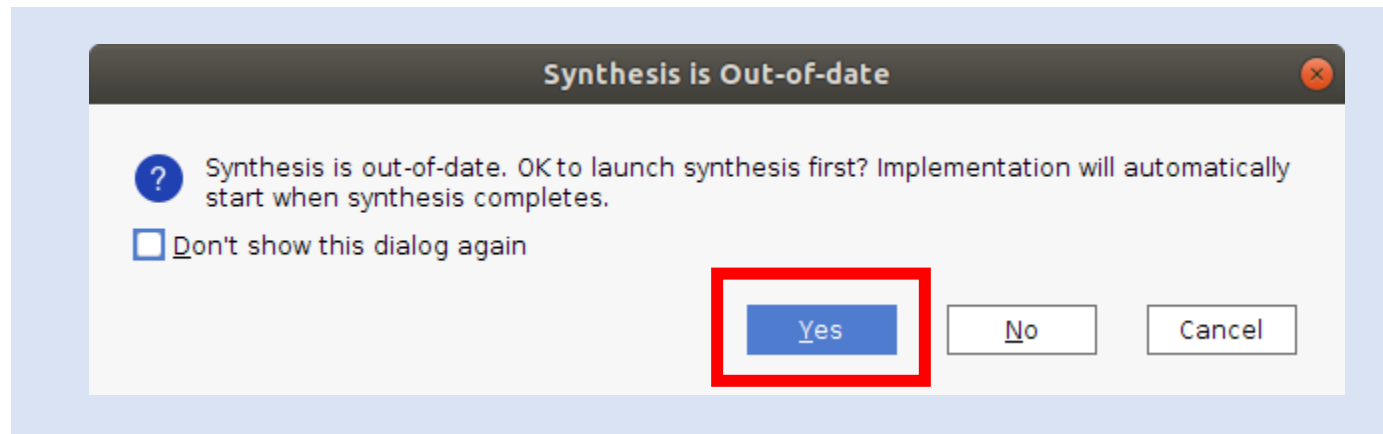
Step 42 – We are now ready to Run Implementation.

The screenshot displays the Vivado 2021.1 IDE interface. The Flow Navigator on the left shows the project hierarchy, with the 'Run Implementation' button highlighted in a red box. The Properties window shows the 'block_average.vhd' file is enabled. The Design Runs table at the bottom shows the following data:

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synthesis De
impl_1	constrs_1	Not started															Vivado Implementat

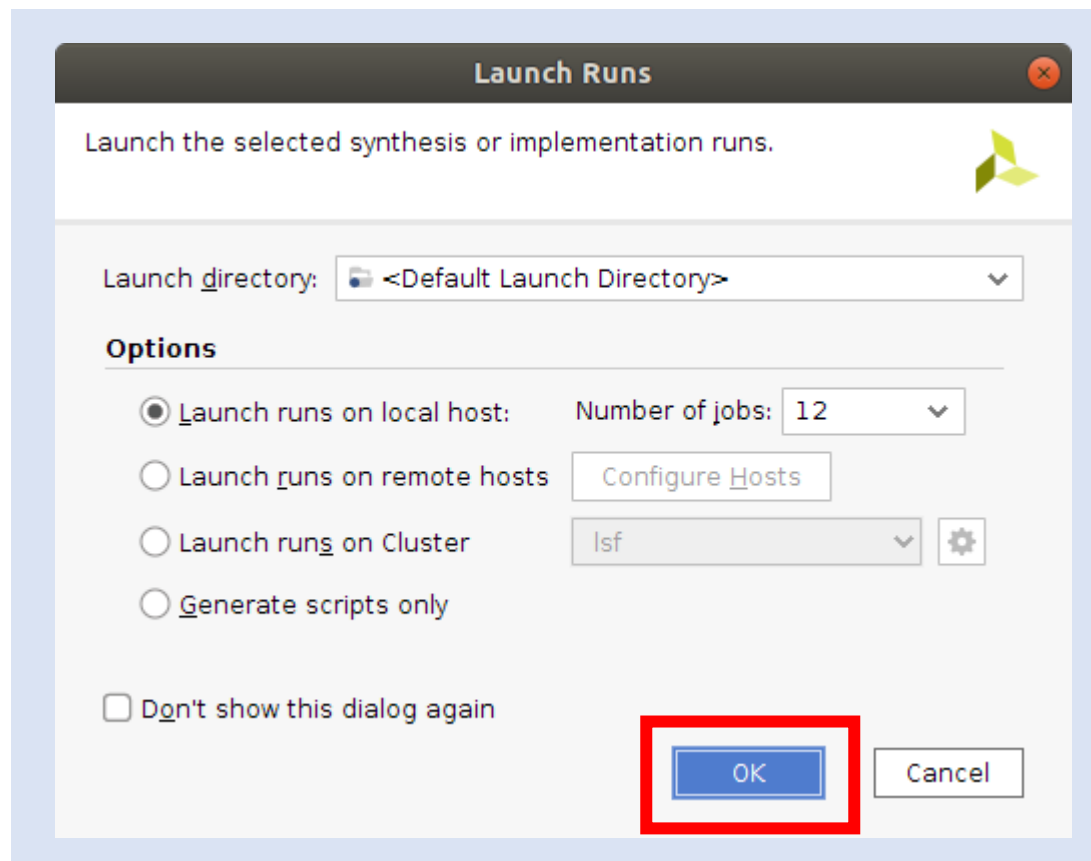
Lab 4: Overview and Introduction to Vivado

Step 43 – Click **Yes** when the Synthesis Out-of-Date dialog pops up.



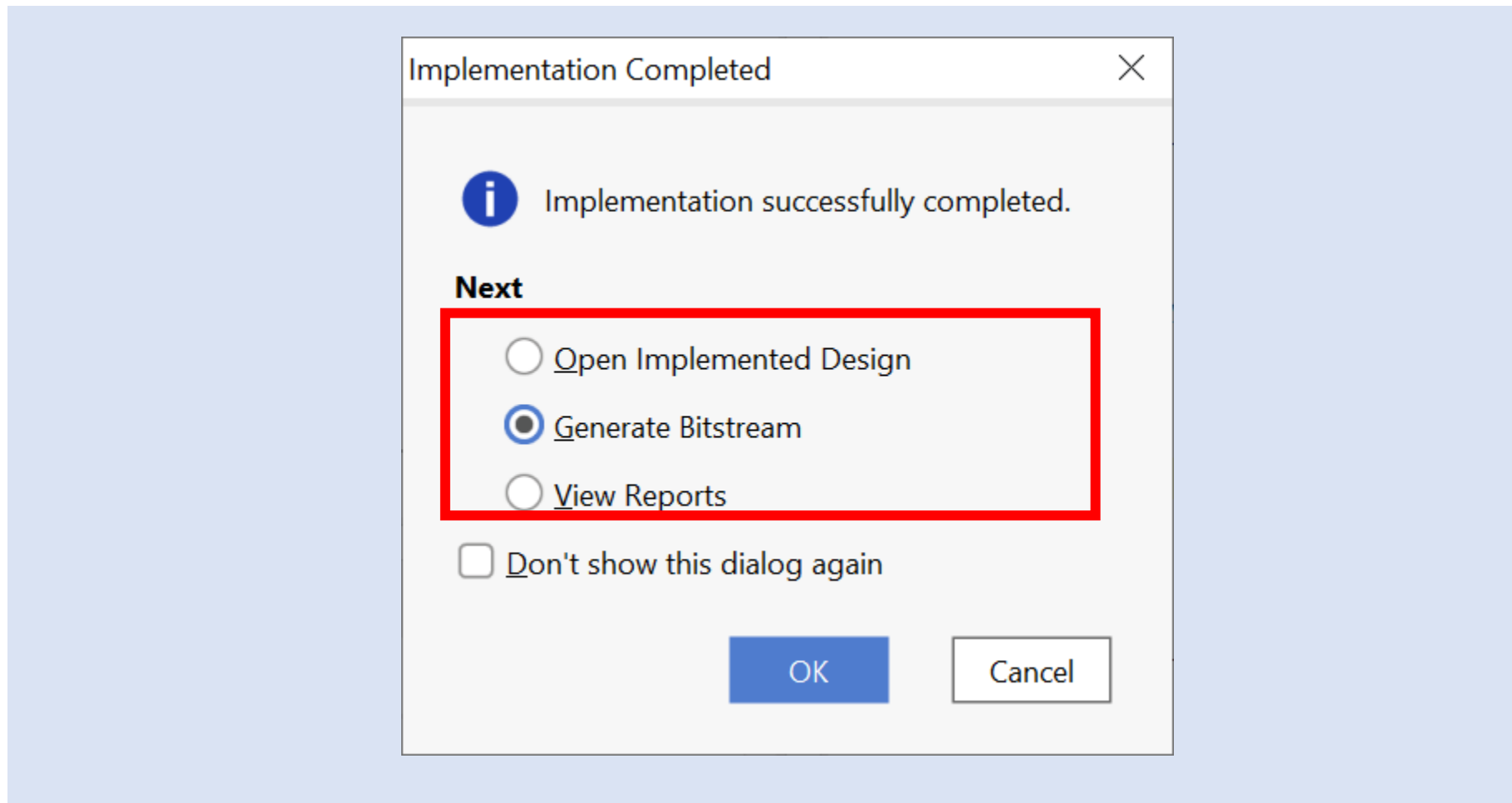
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Step 44 – Select **OK** on the Launch Runs dialog.



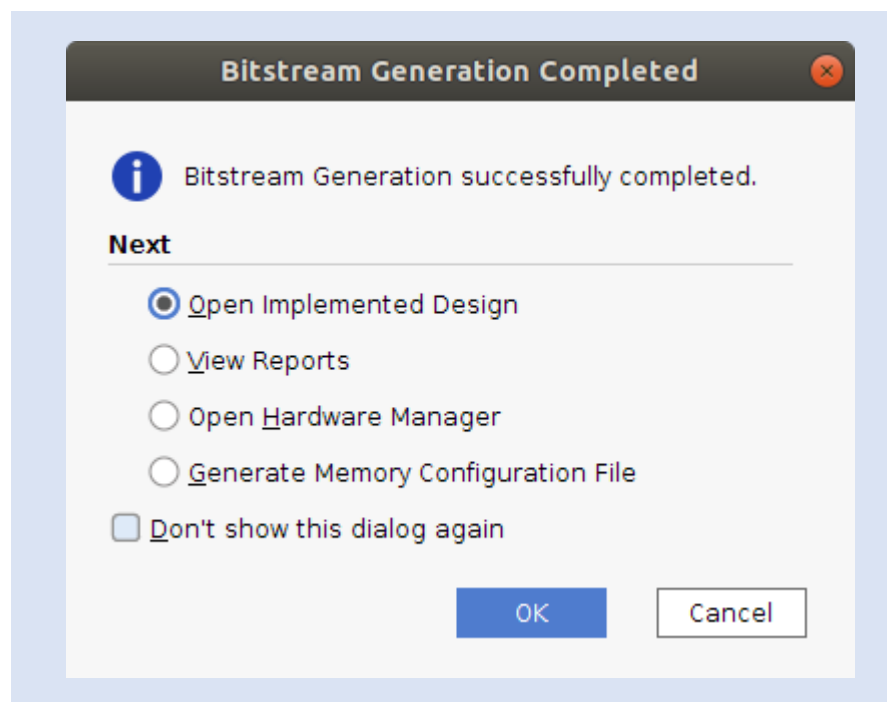
Lab 4: Overview and Introduction to Vivado

Step 45 – When the implementation completes, you will see a dialog appear. Select **Generate Bitstream**.



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Step 46 – A dialog box will appear when the bitstream generates. Congratulations you have completed your first Vivado FPGA implementation.

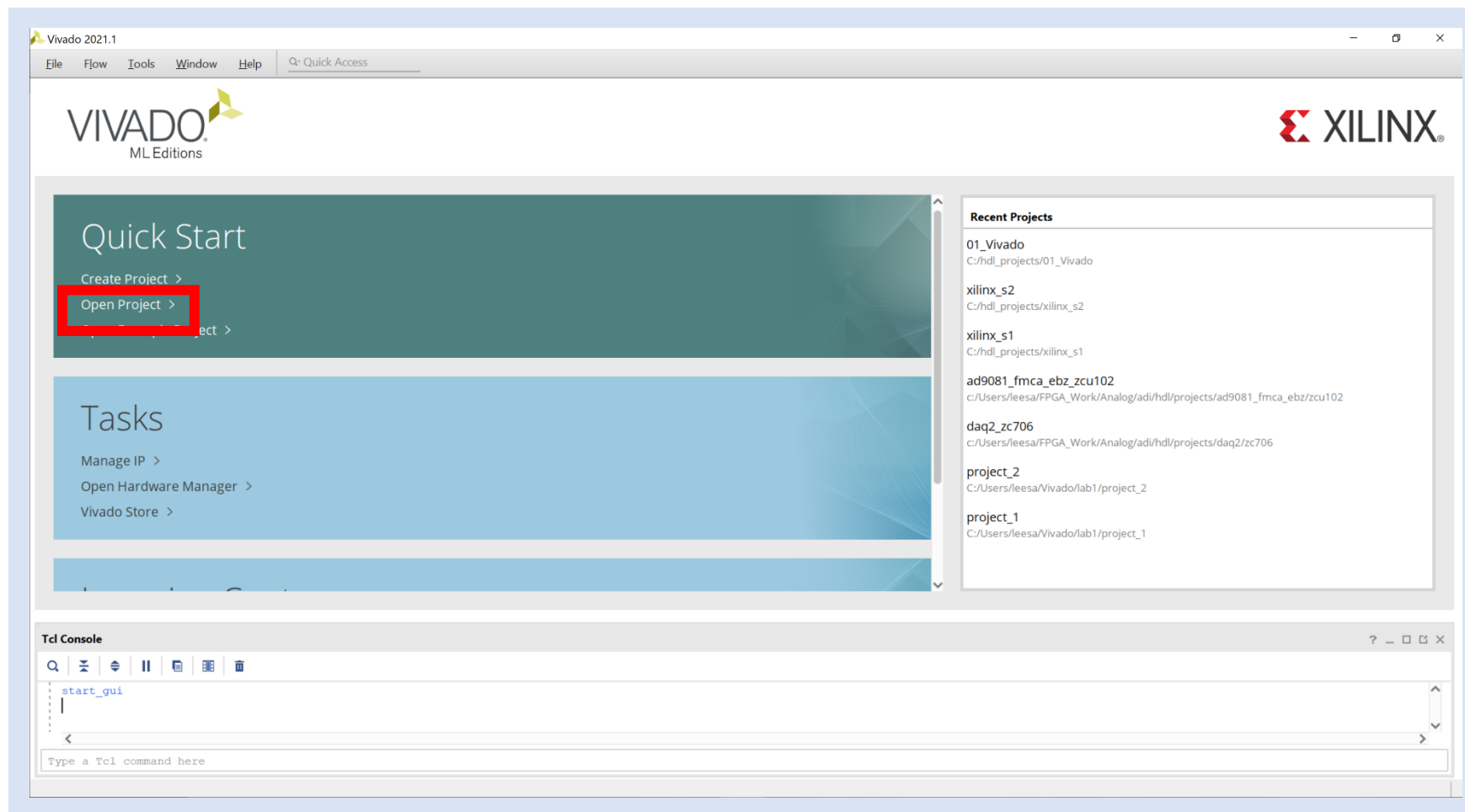


Lab 5

Intermediate Vivado

Lab 5: Intermediate Vivado

Step 1 – Open the project created in part one.



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Step 2 – This will open in project management view. Click on **Create Block Diagram**.

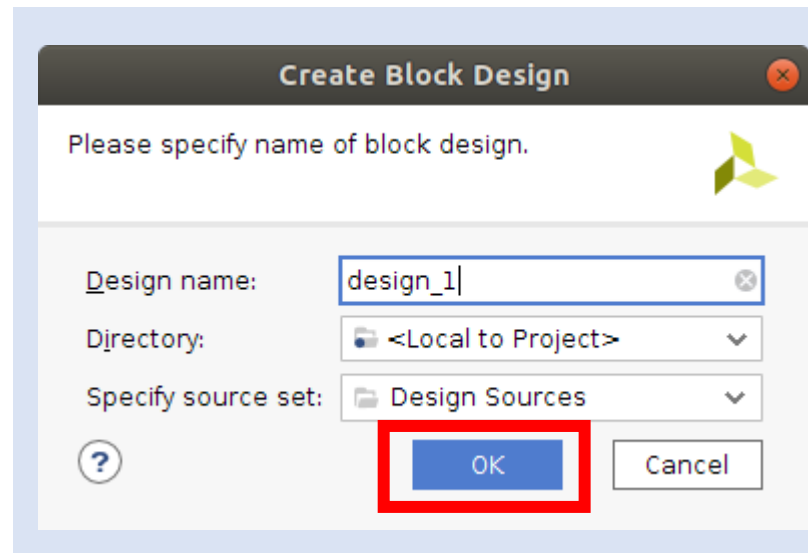
The screenshot displays the Vivado 2021.1 Project Manager interface. The left sidebar shows the 'IP INTEGRATOR' section highlighted with a red box, with 'Create Block Design' selected. The main workspace is divided into several panels:

- Sources:** Shows 'Design Sources (1)' containing 'average(rtl) (block_average.vhd)'. It also lists 'Constraints (1)', 'Simulation Sources (1)', and 'Utility Sources'.
- Project Summary:** Provides an overview of the project '01_Vivado', including its location, product family (Zynq-7000), project part (Arty Z7-20), top module name (average), target language (VHDL), and simulator language (Mixed).
- Board Part:** Lists the display name (Arty Z7-20), board part name (digilentinc.com:arty-z7-20:part0:1.0), and board revision (A.0).
- Design Runs:** A table showing the status of synthesis and implementation runs.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	synth_design Complete!								22	28	0.0	0	0	11/5/21, 3:51 PM	00:00:38	Vivado Synthesis Defaults (Viva
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	0.633	0	22	28	0.0	0	0	11/5/21, 3:52 PM	00:01:31	Vivado Implementation Default

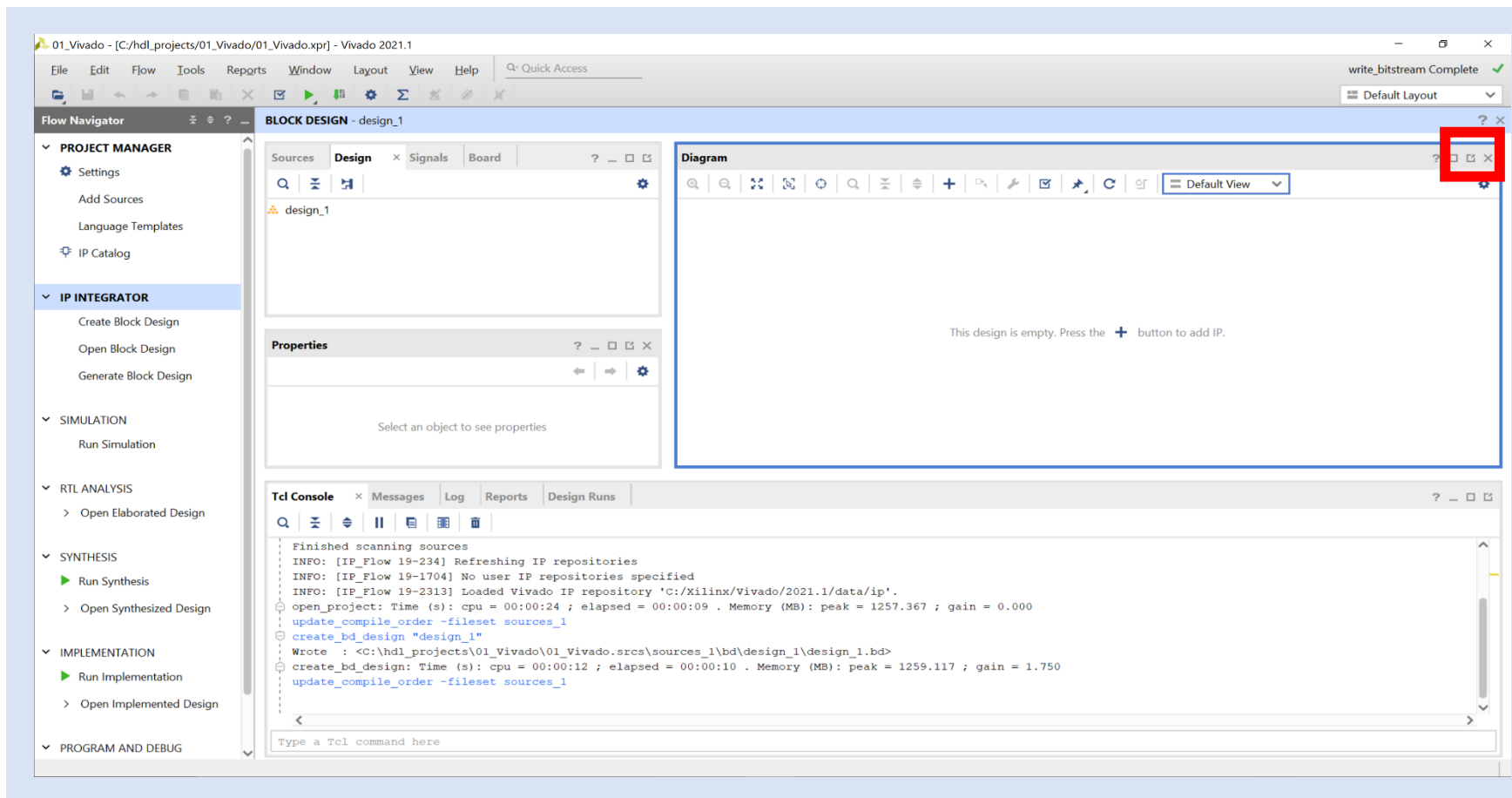
Lab 5: Intermediate Vivado

Step 3 – Leave the predefined name and locations unchanged and click **OK**.



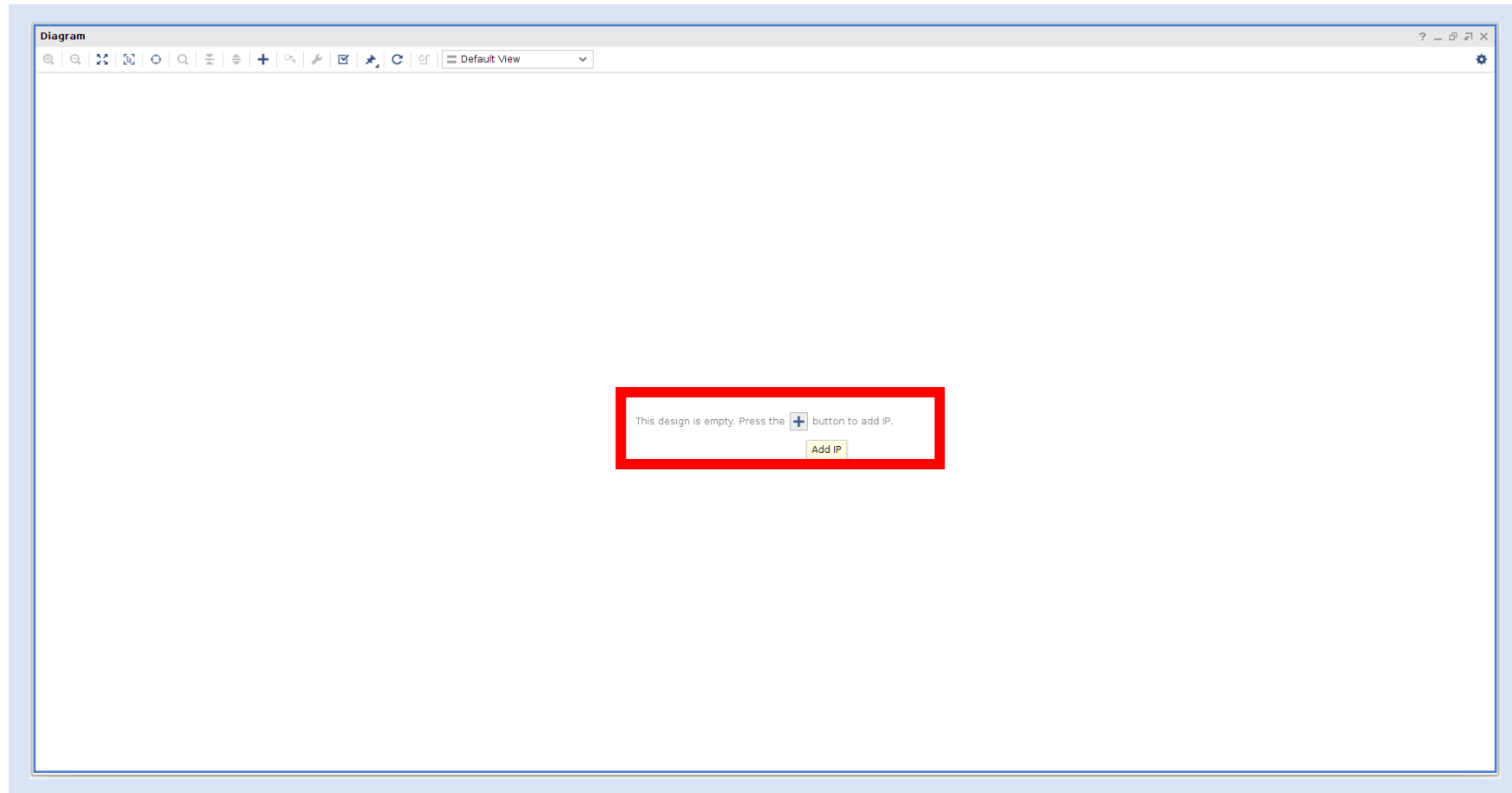
Lab 5: Intermediate Vivado

Step 4 – Undock the block diagram window and maximize it.



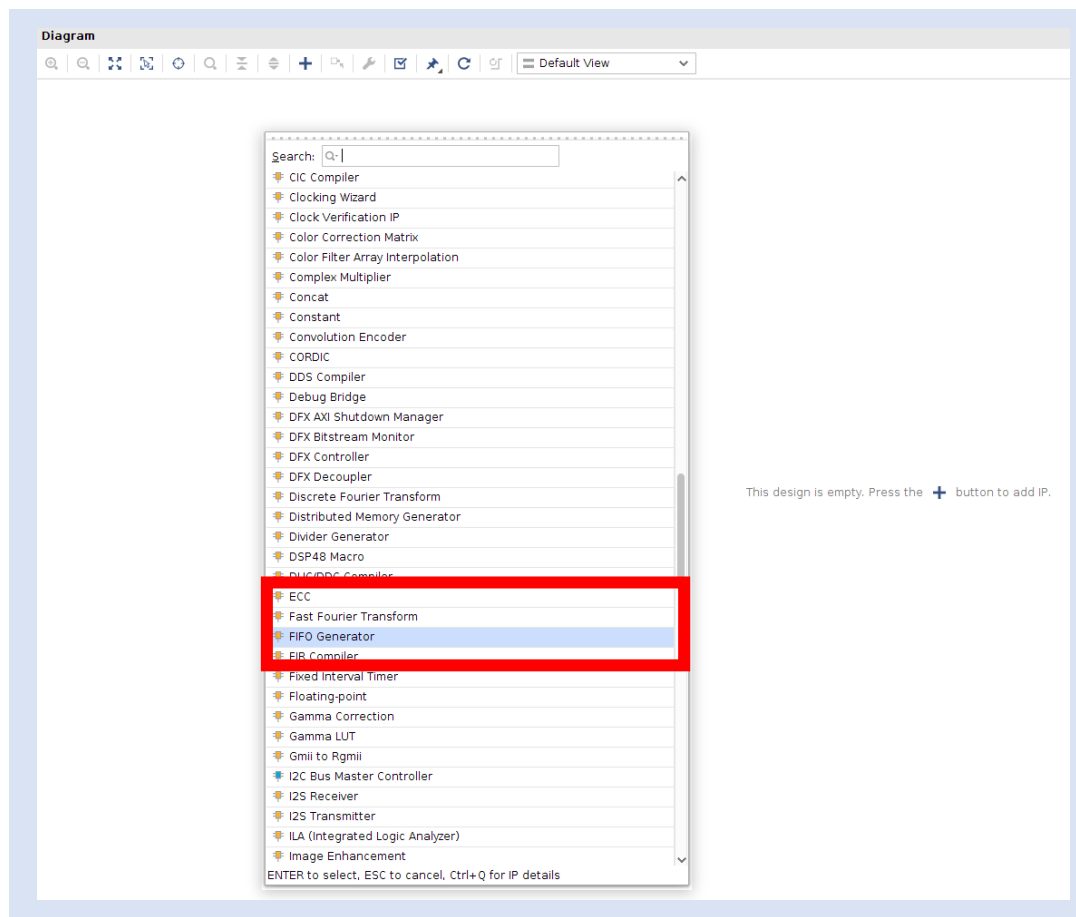
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Step 5 – We are going to add in new IP. Click on the **+** button.



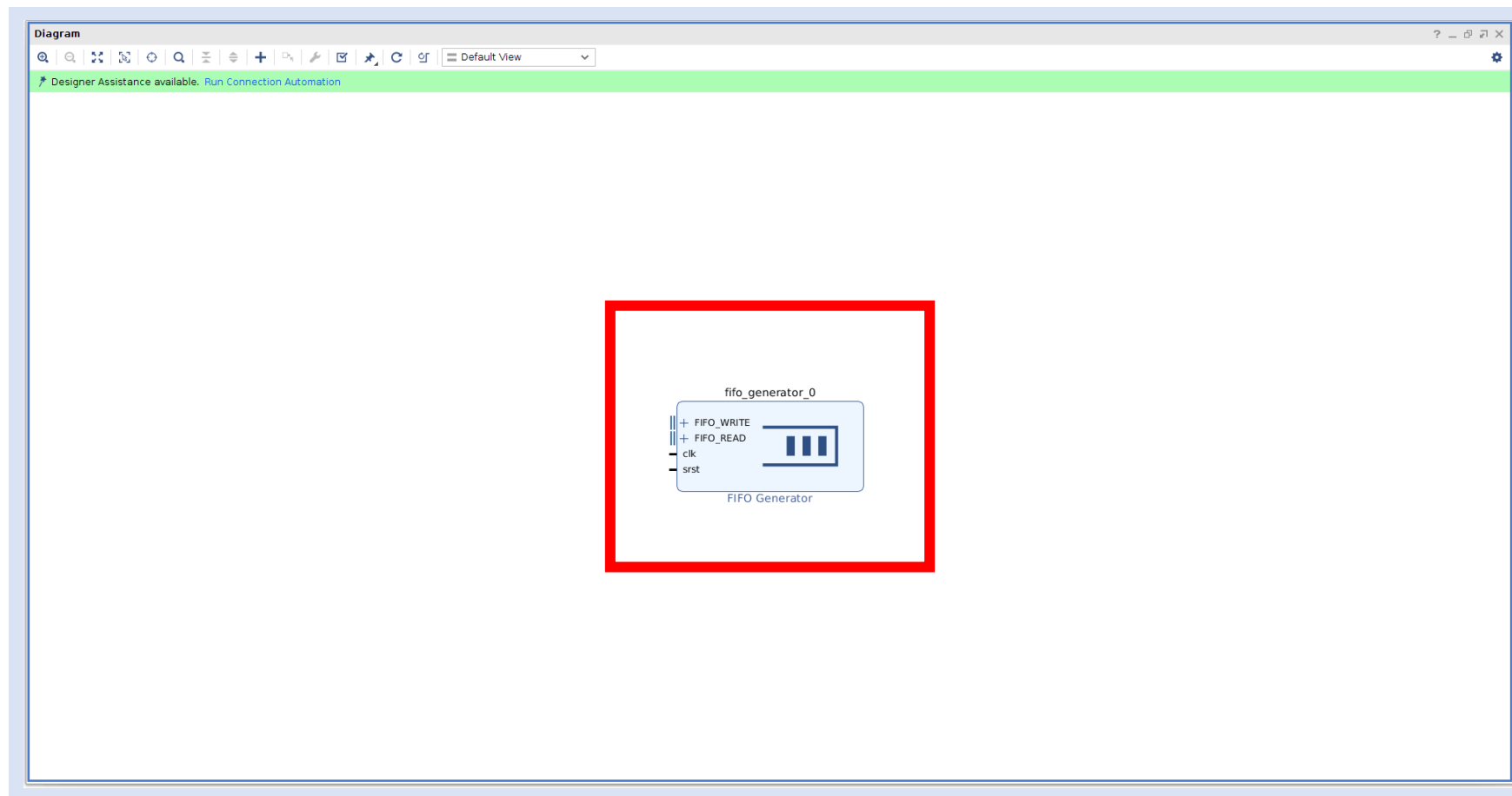
Lab 5: Intermediate Vivado

Step 6 – Select the FIFO Generator. This will add a FIFO to the block diagram.



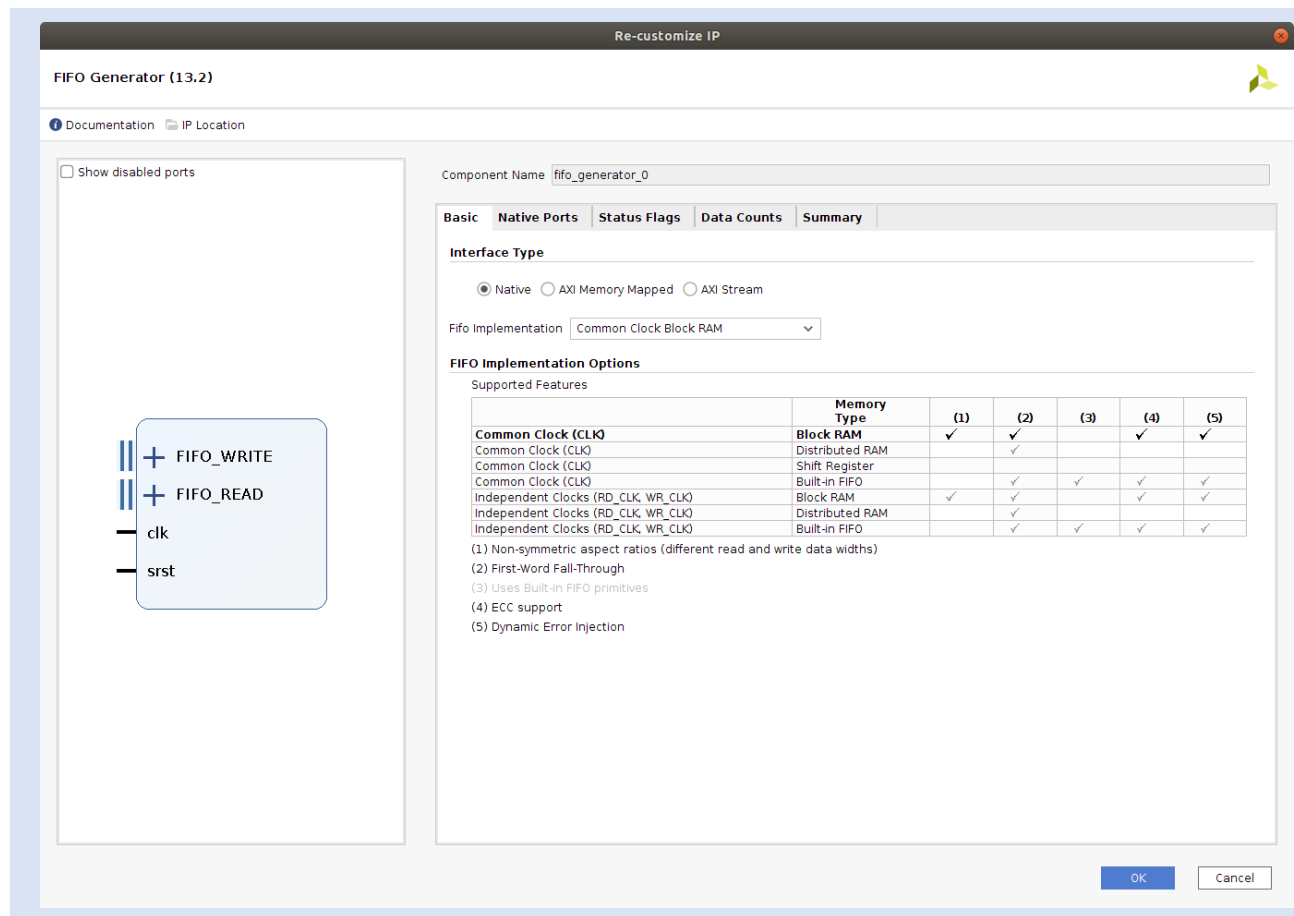
Lab 5: Intermediate Vivado

Step 7 – Double click on the **FIFO Generator** to customize it.



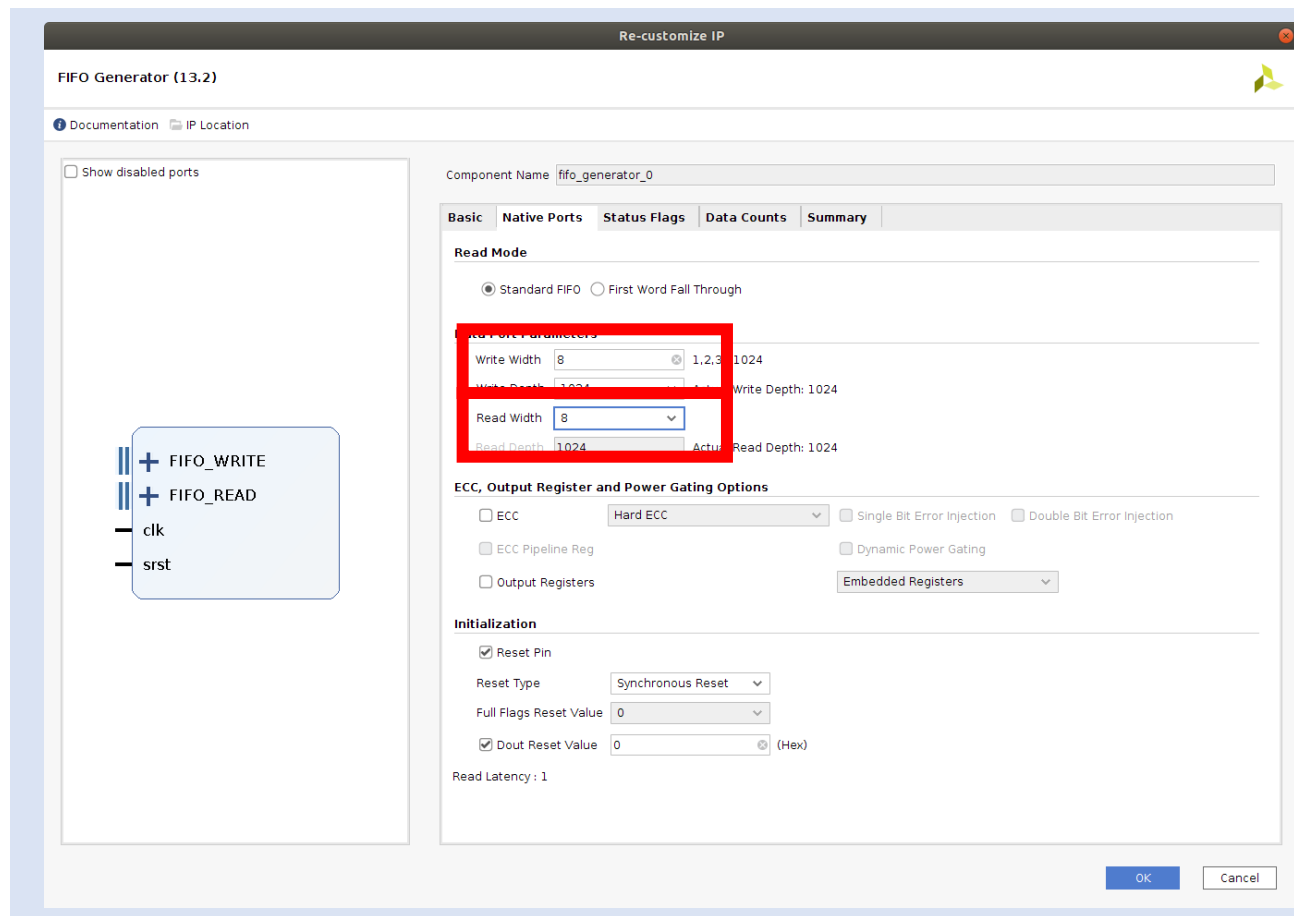
Lab 5: Intermediate Vivado

Step 8 – Leave the first page unchanged.



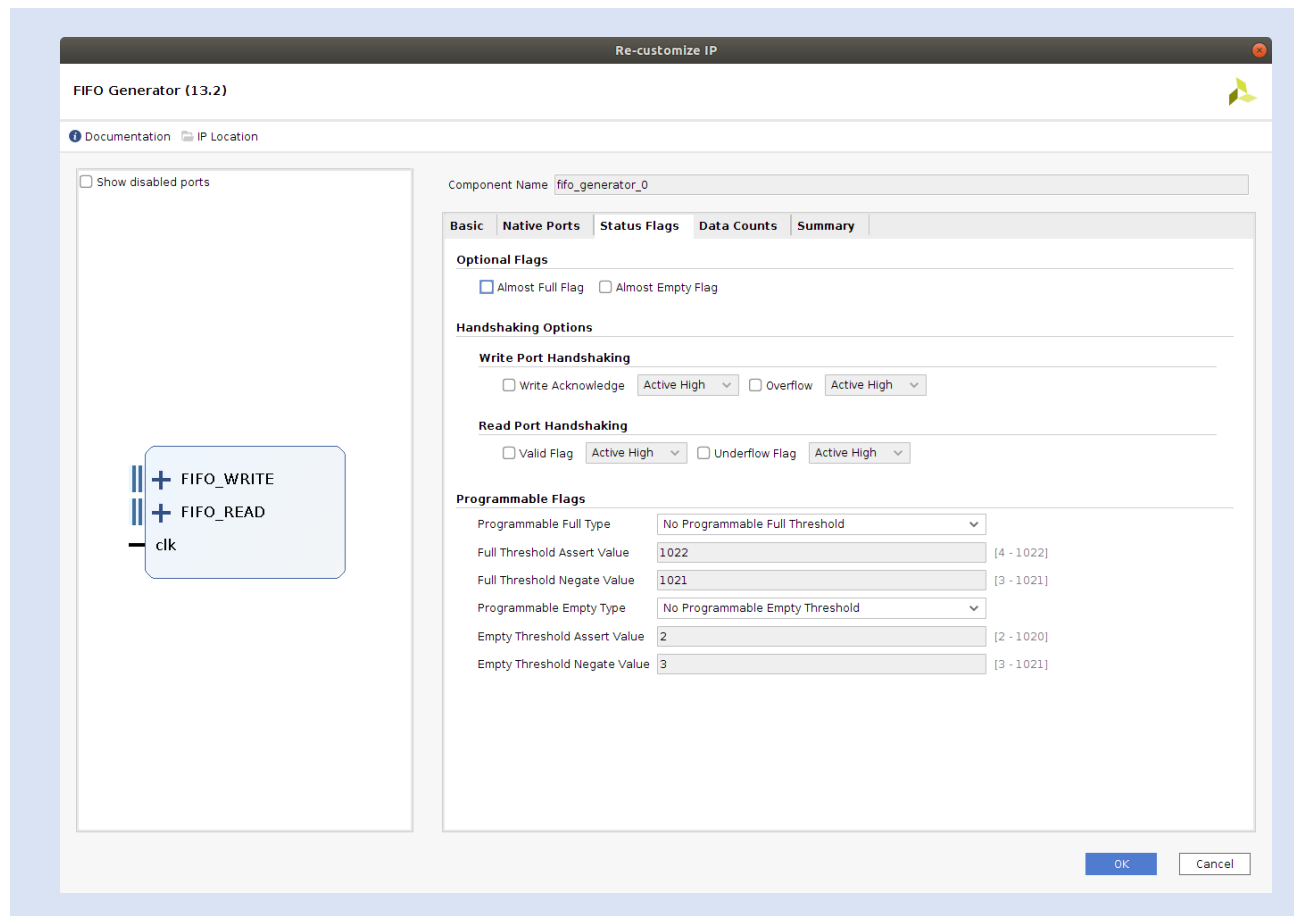
Lab 5: Intermediate Vivado

Step 9 – Change the Write and Read Width to be **8 bits**.



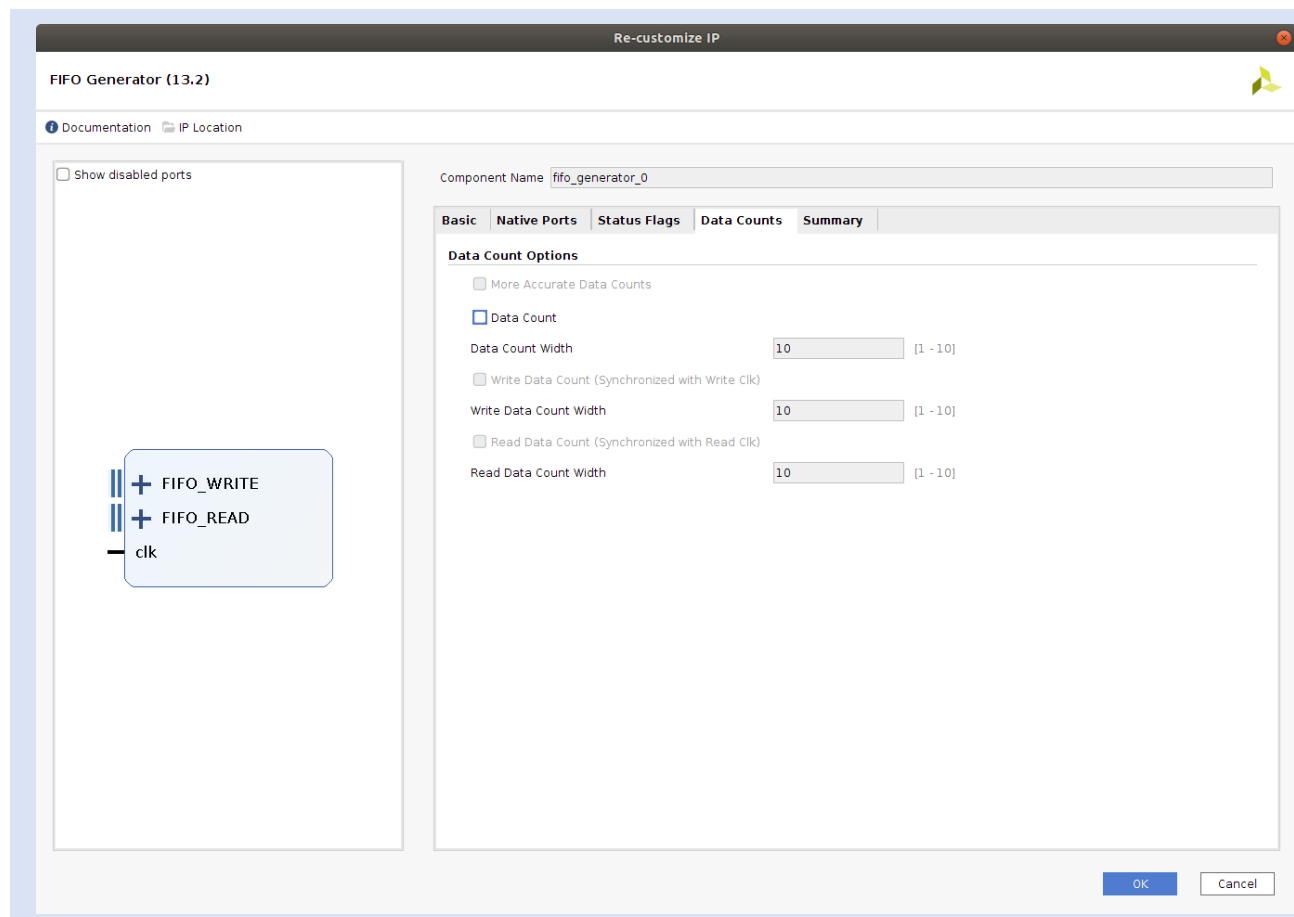
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Step 10 – Leave the third page unchanged.



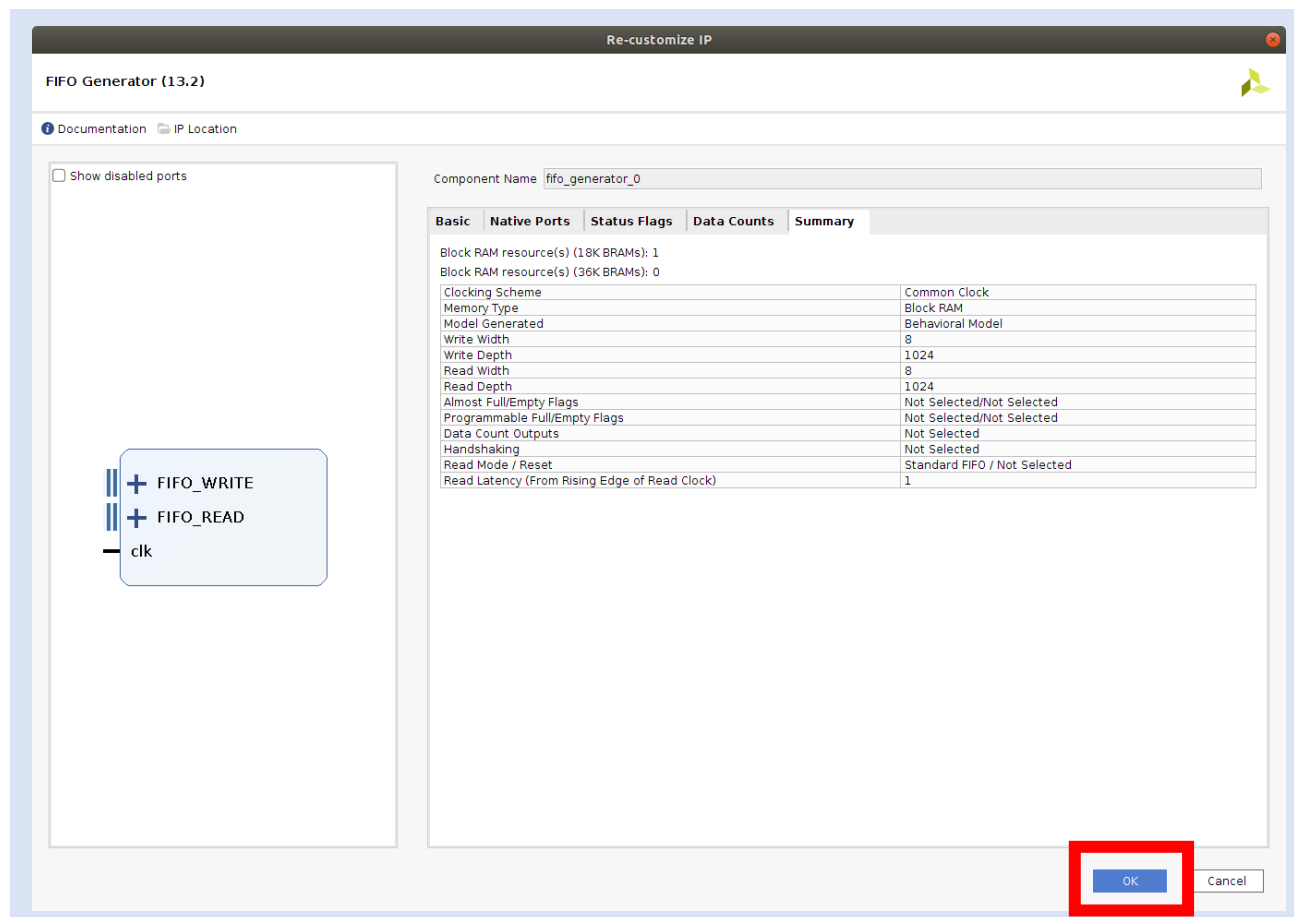
Lab 5: Intermediate Vivado

Step 11 – Leave the fourth page unchanged.



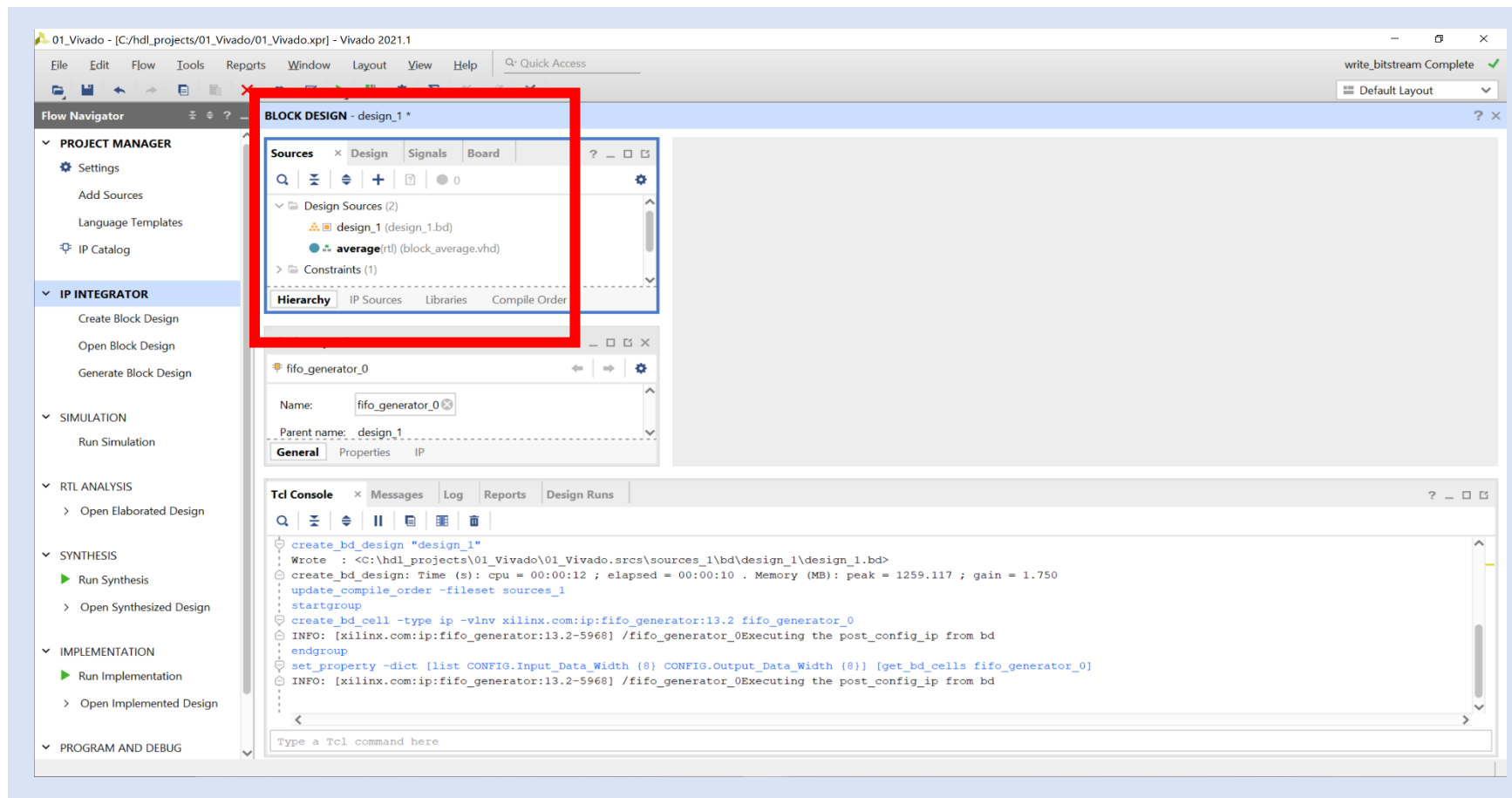
Lab 5: Intermediate Vivado

Step 12 – Leave the final page unchanged. Note that the FIFO OP are unregistered. Click **OK**.



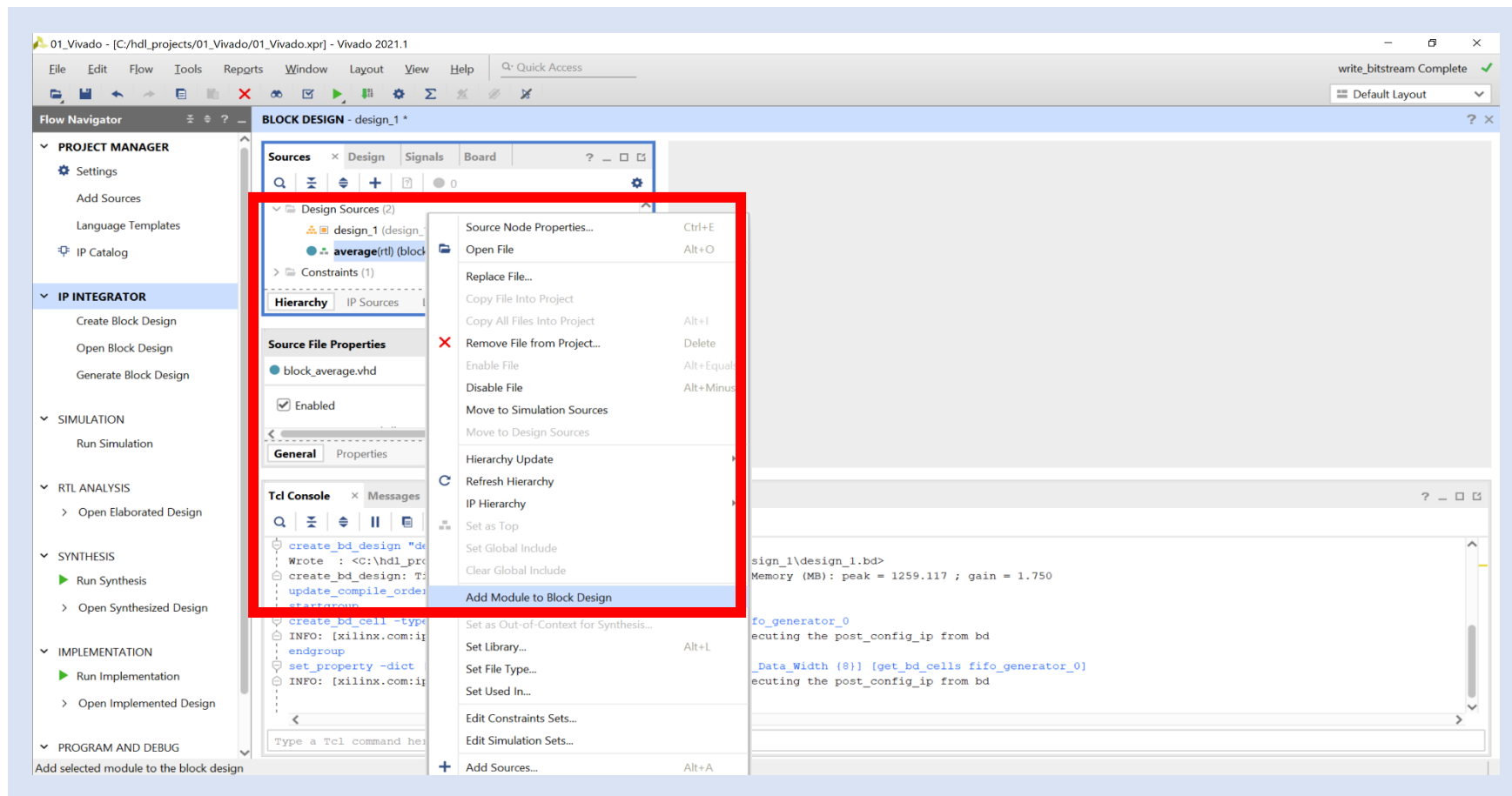
Lab 5: Intermediate Vivado

Step 13 – Click back on the Vivado Project Management view you will see the block diagram under the design sources.



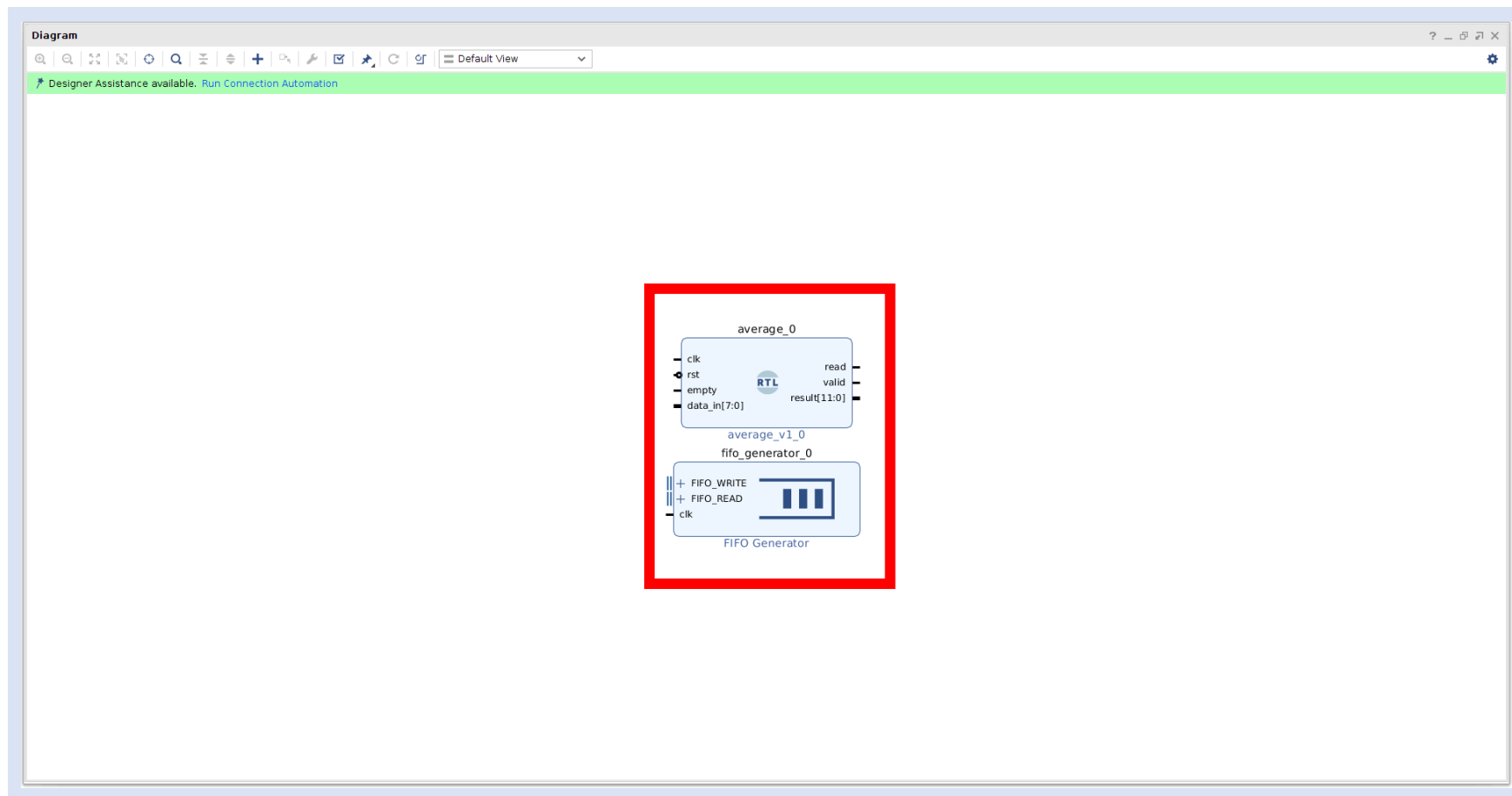
Lab 5: Intermediate Vivado

Step 14 – Right click on the average RTL block and select **Add Module to Block Design**.



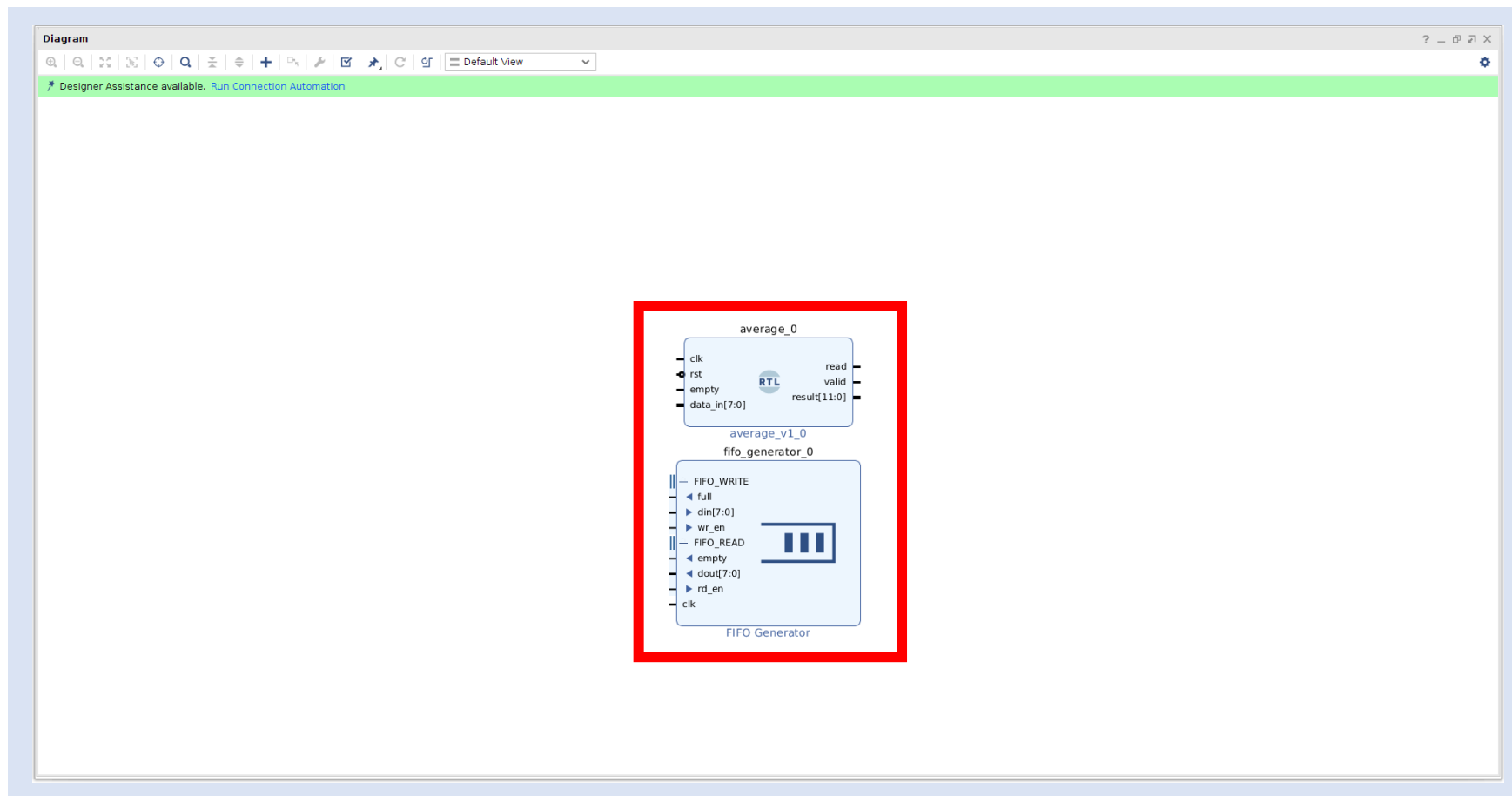
Lab 5: Intermediate Vivado

Step 15 – This will add the average block to the block diagram.



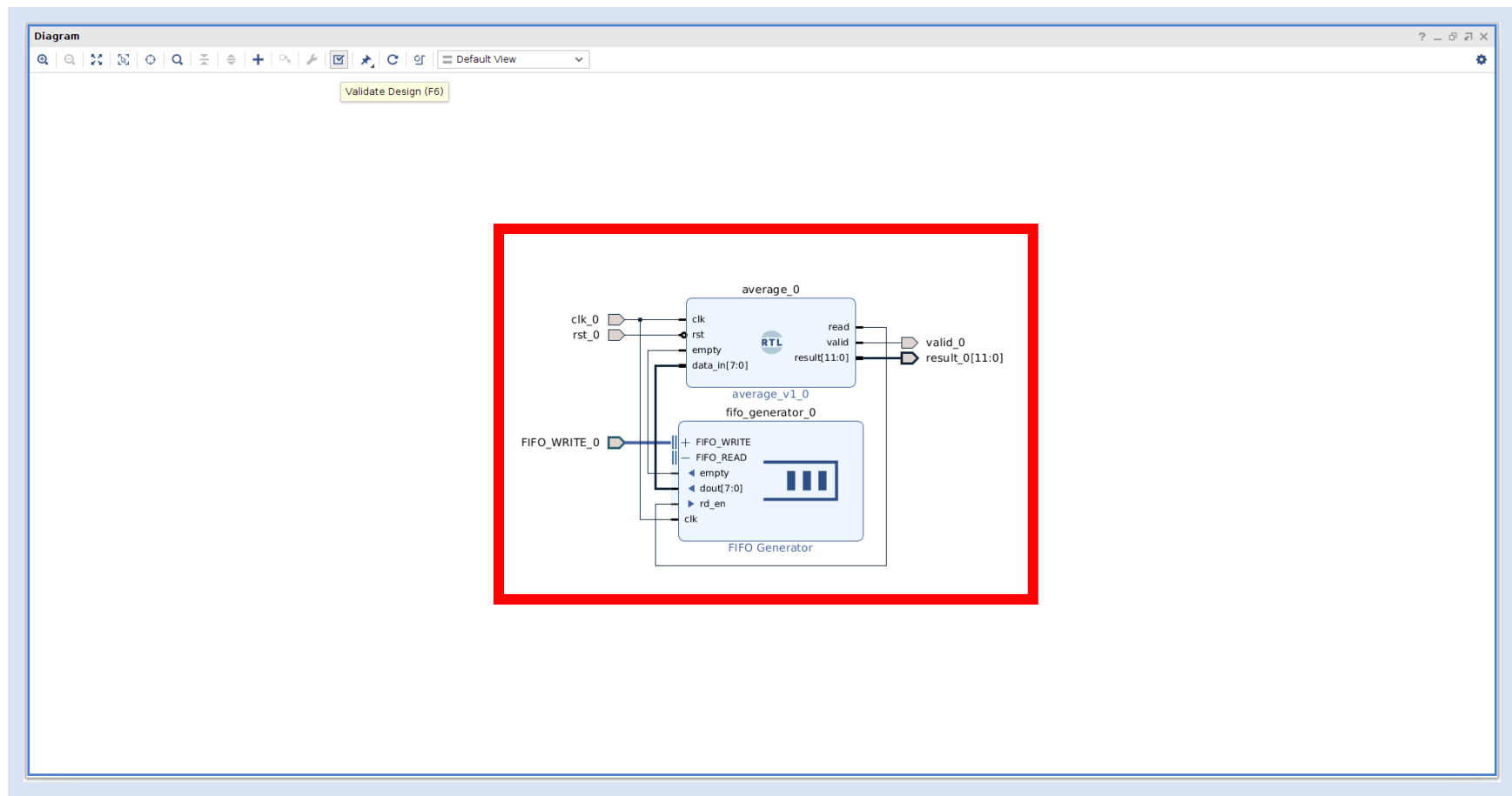
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Step 16 – Expand the FIFO Write and Read Interfaces.



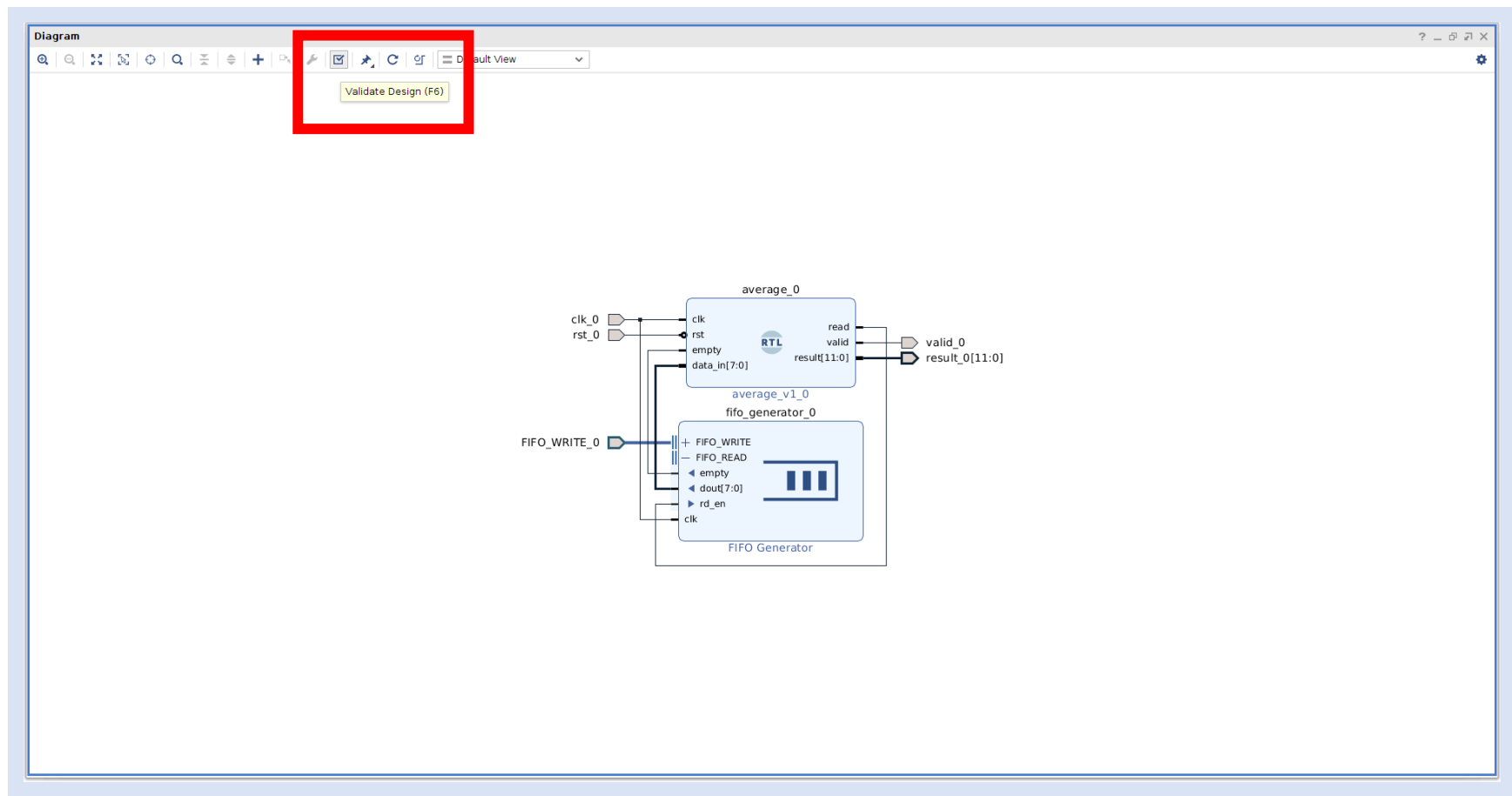
Lab 5: Intermediate Vivado

Step 17 – Make the Clk, Reset, Result, Valid and FIFO Write interfaces external by right-clicking on each pin and selecting **Make External**. Connect the remaining interfaces as below.



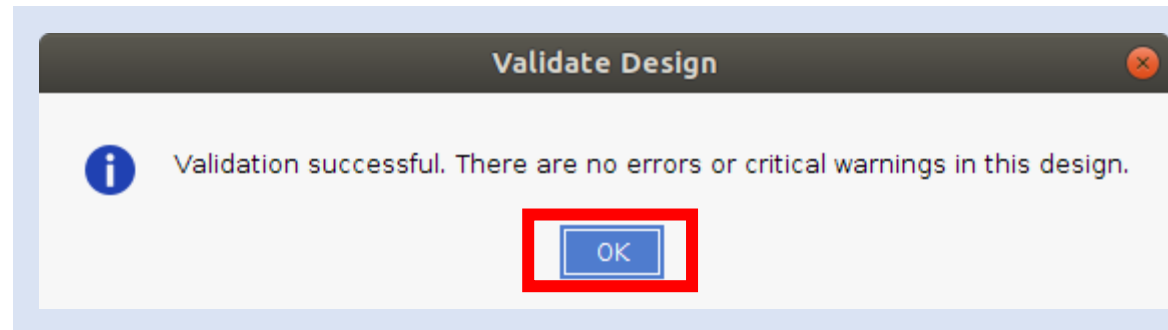
Lab 5: Intermediate Vivado

Step 18 – Click on **Validate Design**.



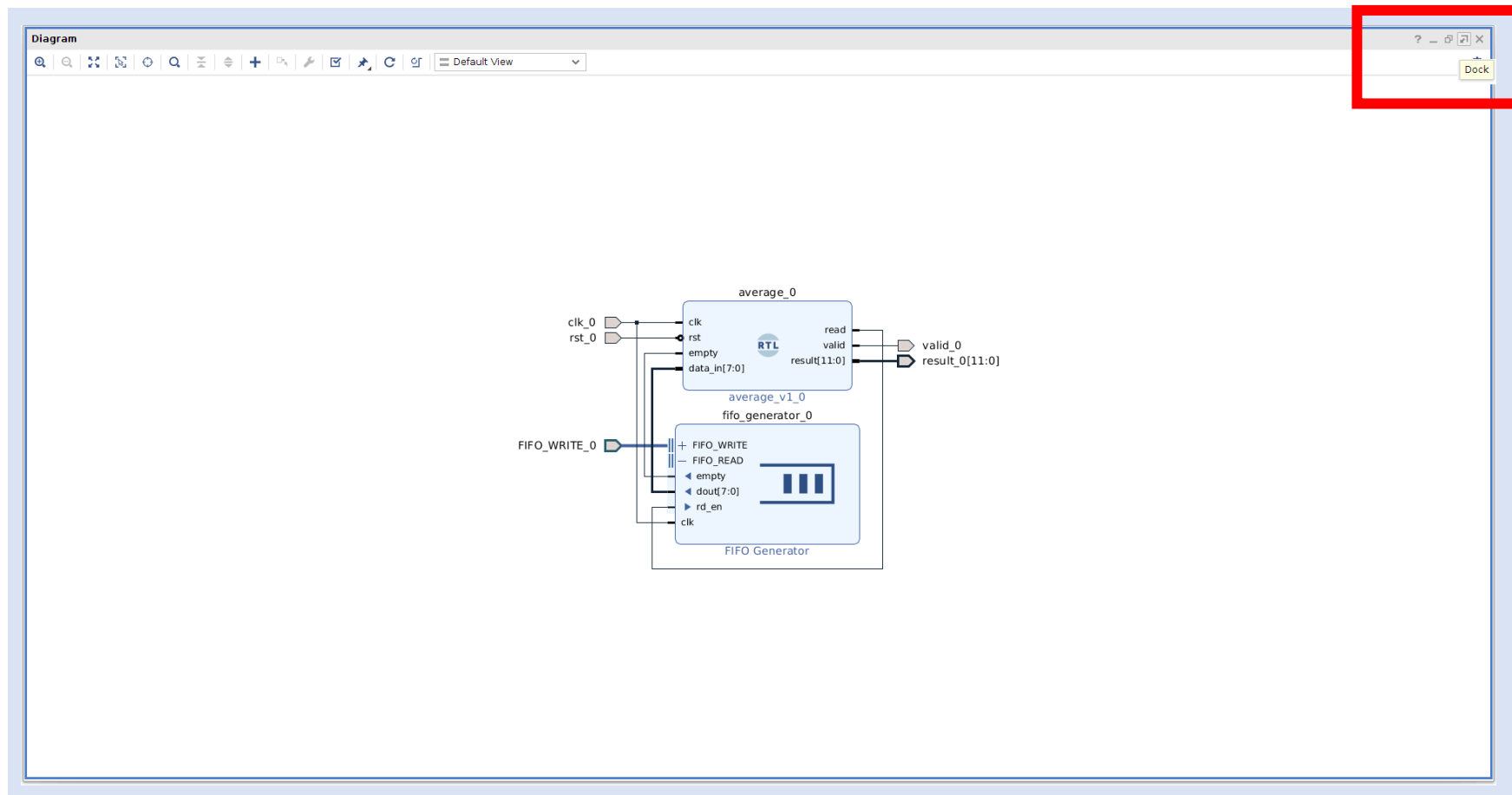
Lab 5: Intermediate Vivado

Step 19 – The validated design should result in no error or critical warnings. Click **OK**.



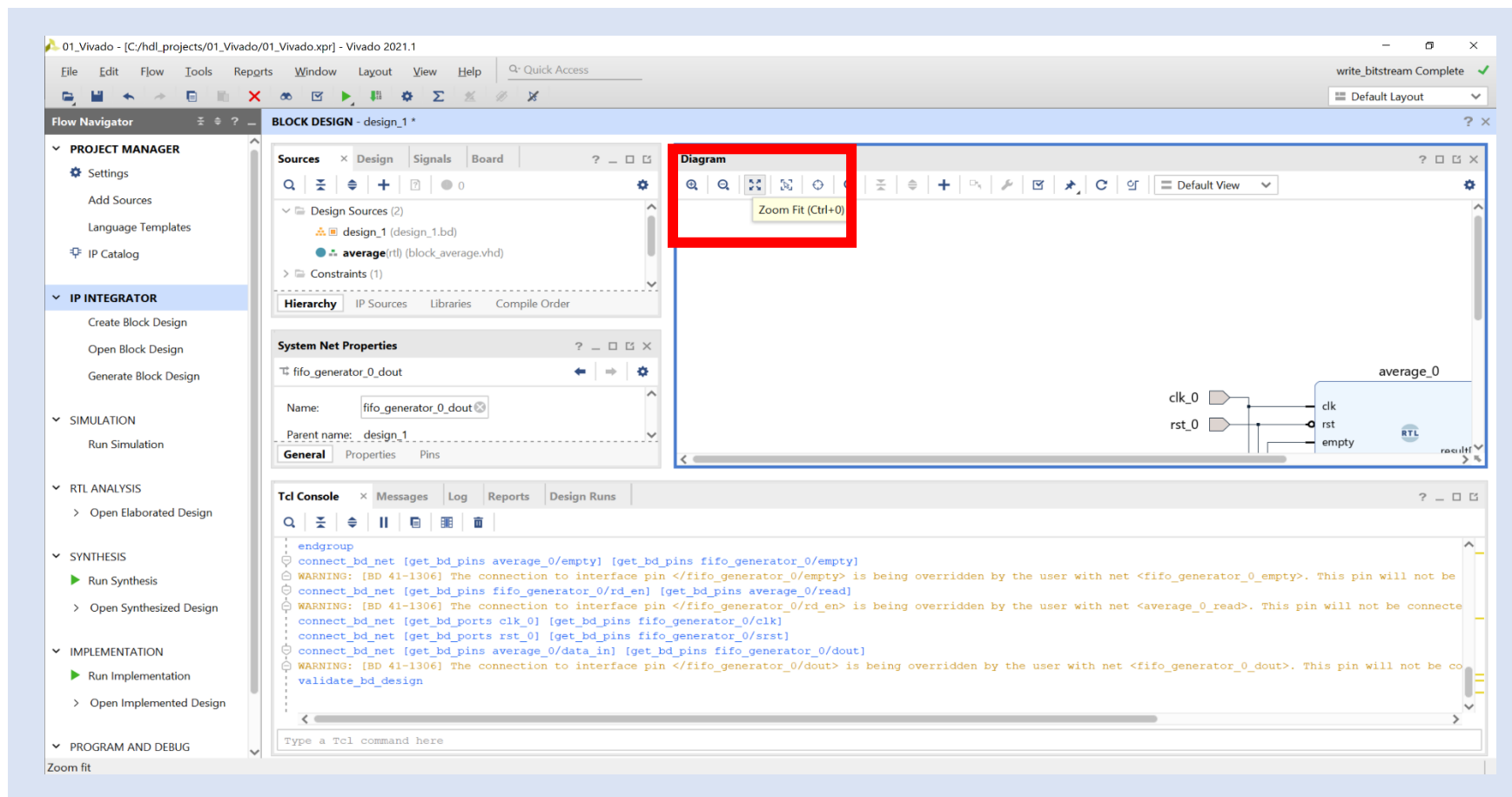
Lab 5: Intermediate Vivado

Step 20 – Re-dock the block diagram window into the Vivado Project Manager.



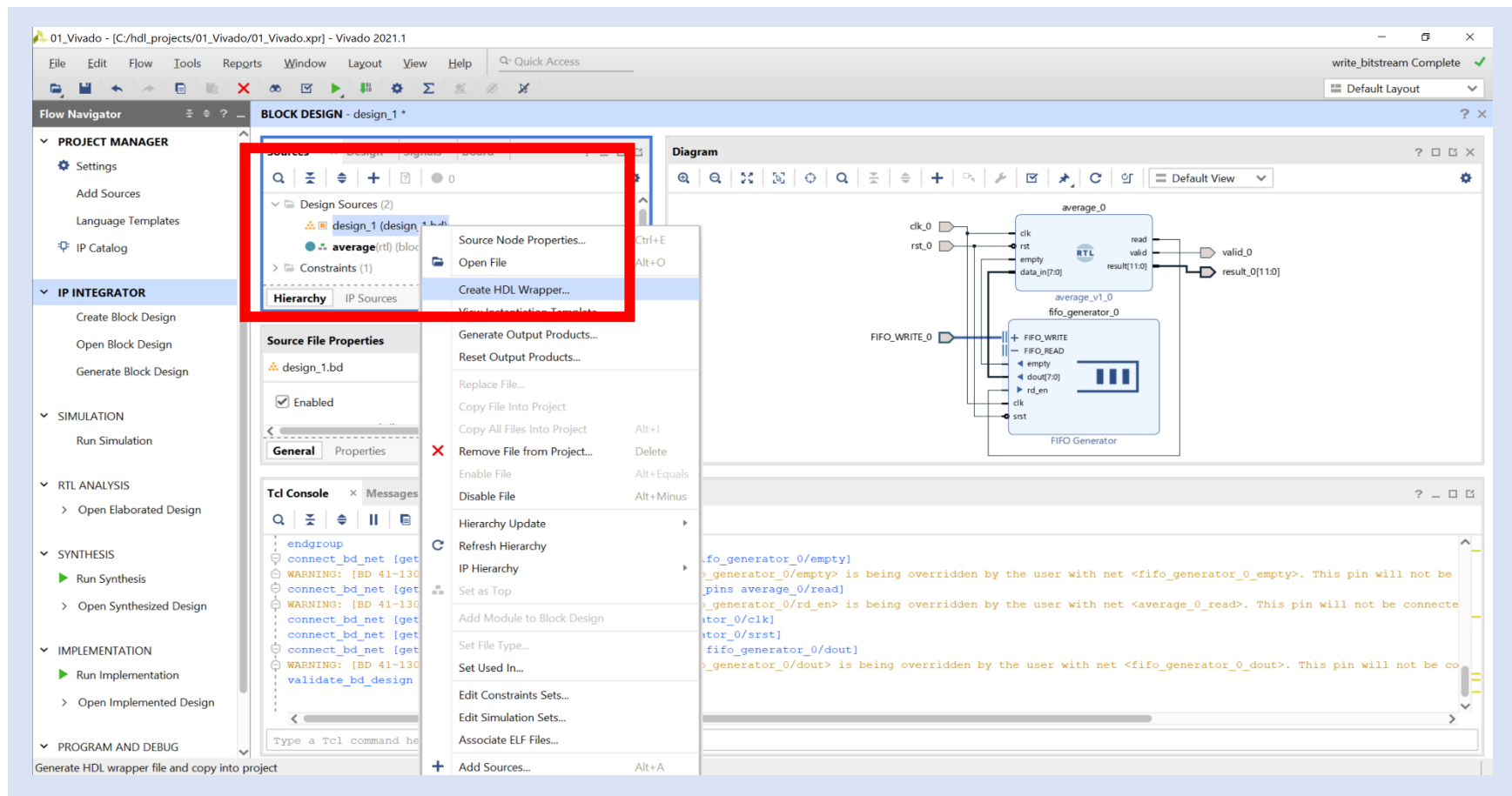
Lab 5: Intermediate Vivado

Step 21 – Click on the **Zoom Fit** button to fit the design to the window.



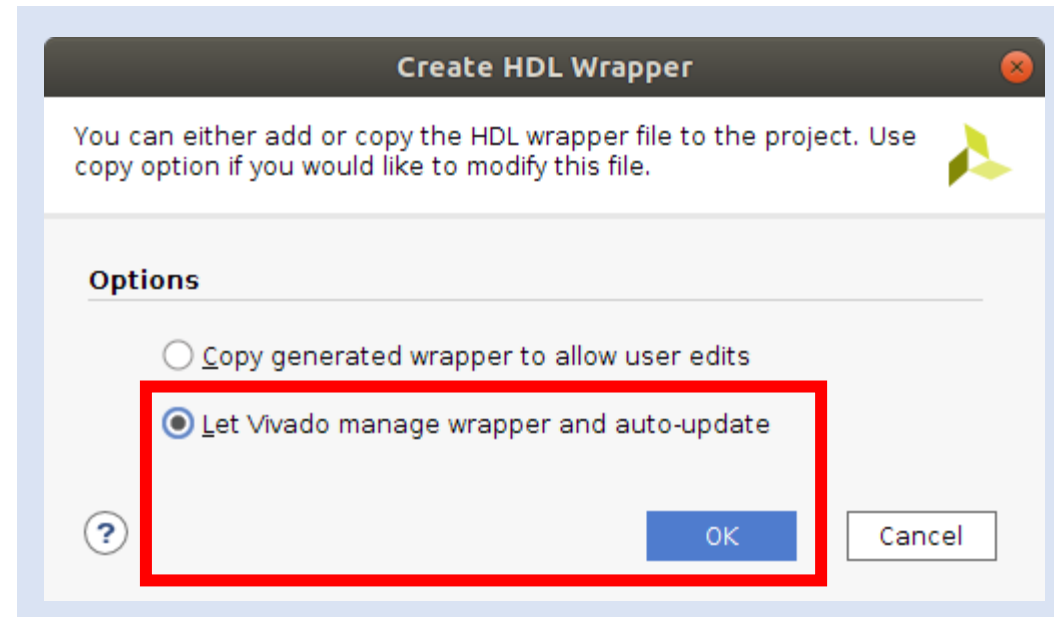
Lab 5: Intermediate Vivado

Step 22 – Right click on the block diagram design under the Design Sources tab and select **Create HDL Wrapper.**



Lab 5: Intermediate Vivado

Step 23 – Allow Vivado to manage the wrapper and click **OK**.



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Step 24 – Expand the newly created wrapper and you will see the entire design.

The screenshot displays the Vivado 2021.1 interface for a Block Design named 'design_1'. The 'Sources' window, highlighted with a red border, shows the design hierarchy:

- design_1_wrapper (STRUCTURE) (design_1_wrapper.vhd) (1)
 - design_1_i: design_1 (design_1.bd) (1)
 - design_1 (STRUCTURE) (design_1.vhd) (2)
 - average_0: design_1_average_0_0 (Module Reference) (1)
 - fifo_generator_0: design_1_fifo_generator_0_0 (Module Reference) (1)
 - average (rtl) (block_average.vhd)

The 'Diagram' window shows the RTL implementation of the design. It features an 'average_0' block (RTL) and a 'FIFO Generator' block. The 'average_0' block has inputs 'clk_0', 'rst', and 'empty', and outputs 'read', 'valid', and 'result[11:0]'. The 'FIFO Generator' block has inputs 'FIFO_WRITE_0', 'FIFO_READ', 'empty', 'dout[7:0]', 'rd_en', and 'clk', and outputs 'rst' and 'result_0[11:0]'. The 'FIFO Generator' block is connected to the 'average_0' block via 'FIFO_READ' and 'FIFO_WRITE_0' signals.

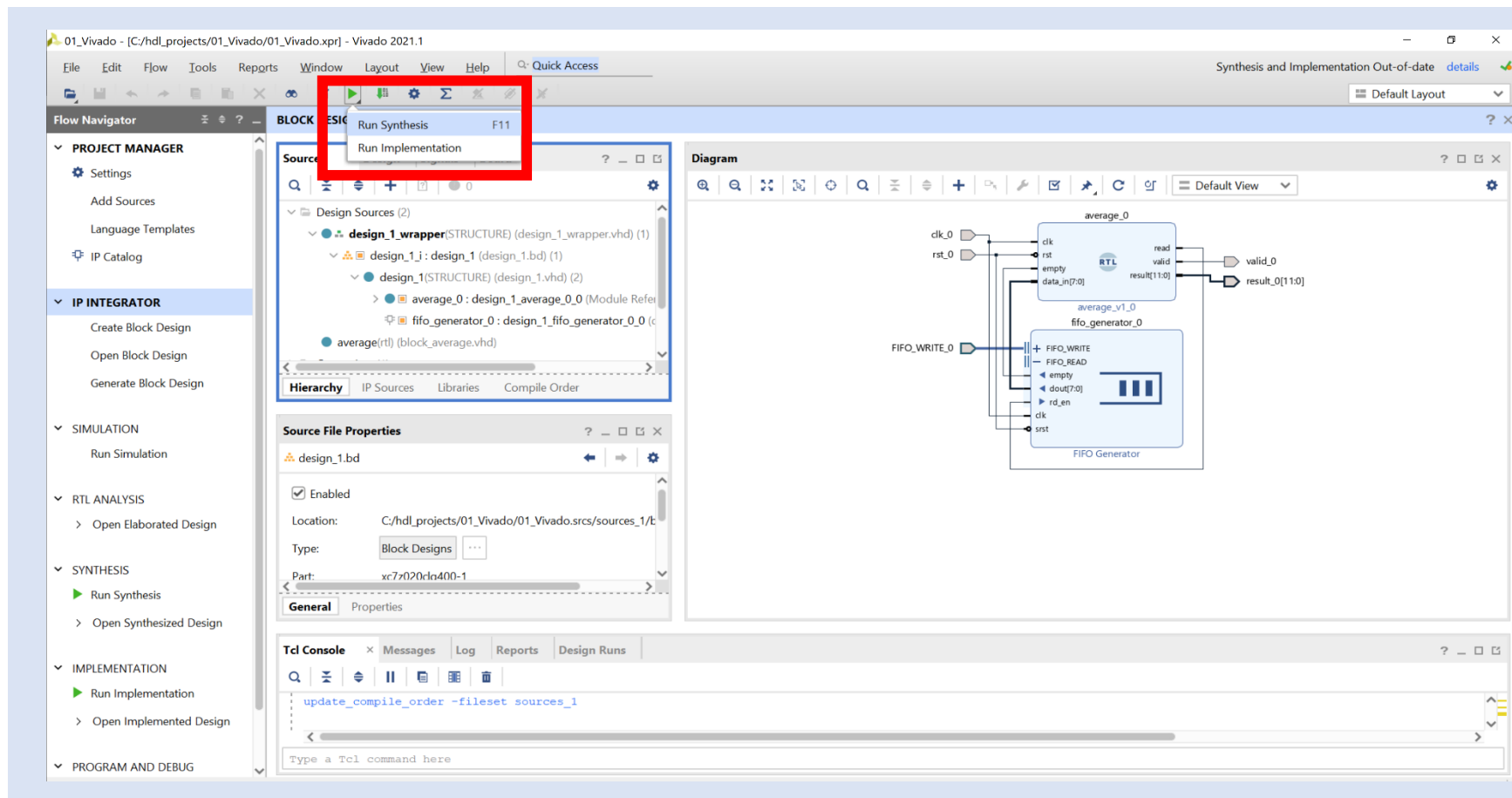
The 'Source File Properties' window shows the properties for 'design_1.bd':

- Enabled:
- Location: C:/hdl_projects/01_Vivado/01_Vivado.srcs/sources_1/
- Type: Block Designs
- Part: xc7z020clg400-1

The 'Tcl Console' window shows the command: `update_compile_order -fileset sources_1`

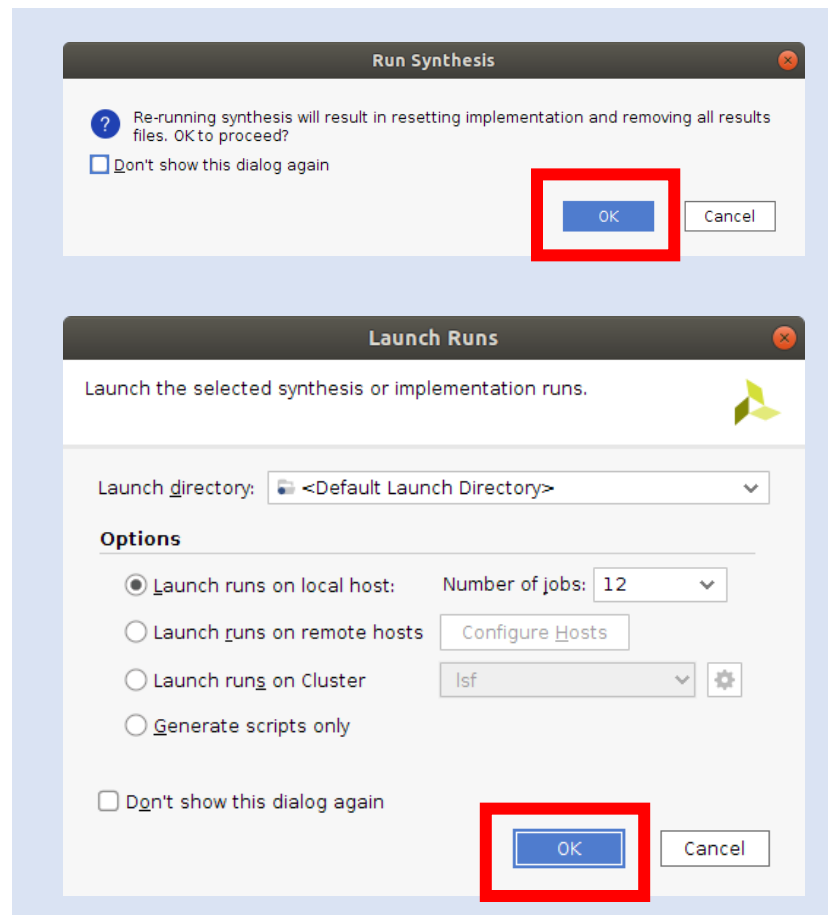
Lab 5: Intermediate Vivado

Step 25 – Run the Synthesis.



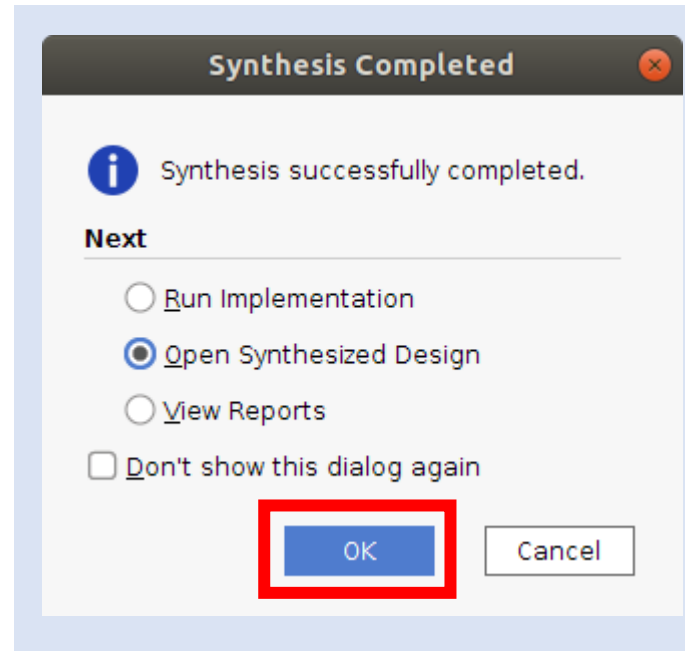
Lab 5: Intermediate Vivado

Step 26 – On both resultant dialogs click **OK** and wait for synthesis to complete.



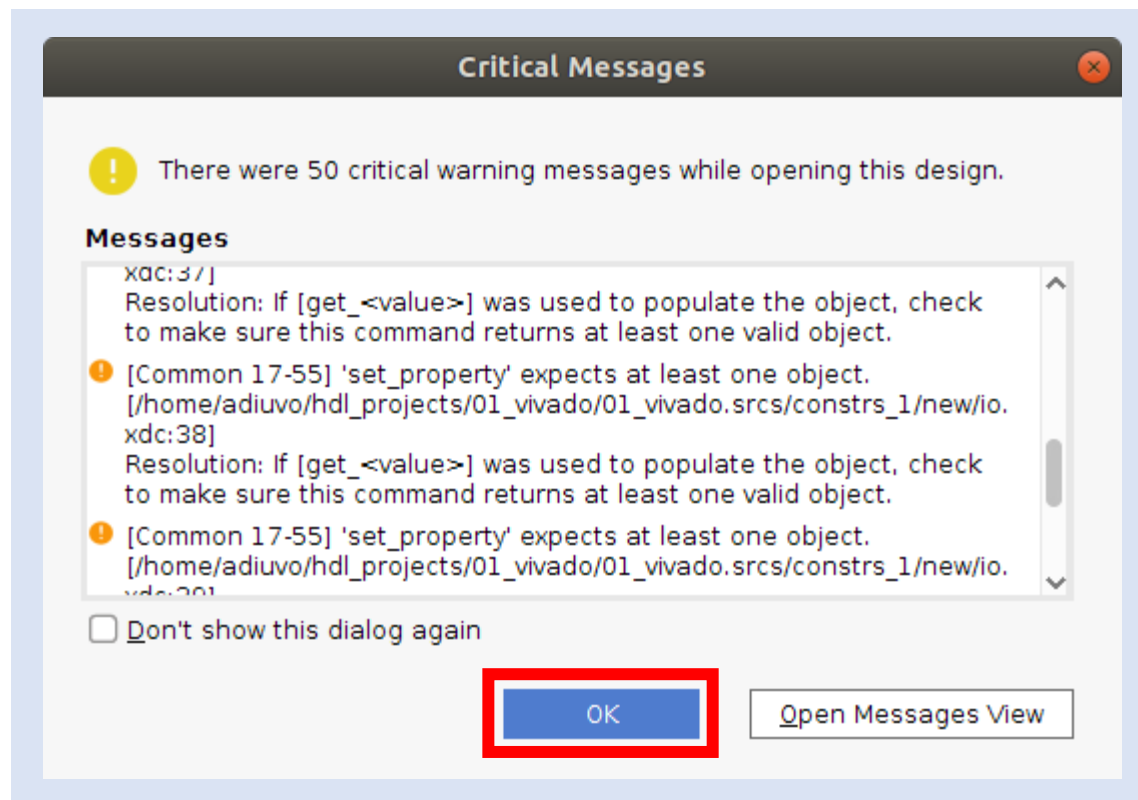
Lab 5: Intermediate Vivado

Step 27 – When synthesis completes, **Open the Synthesized Design.**



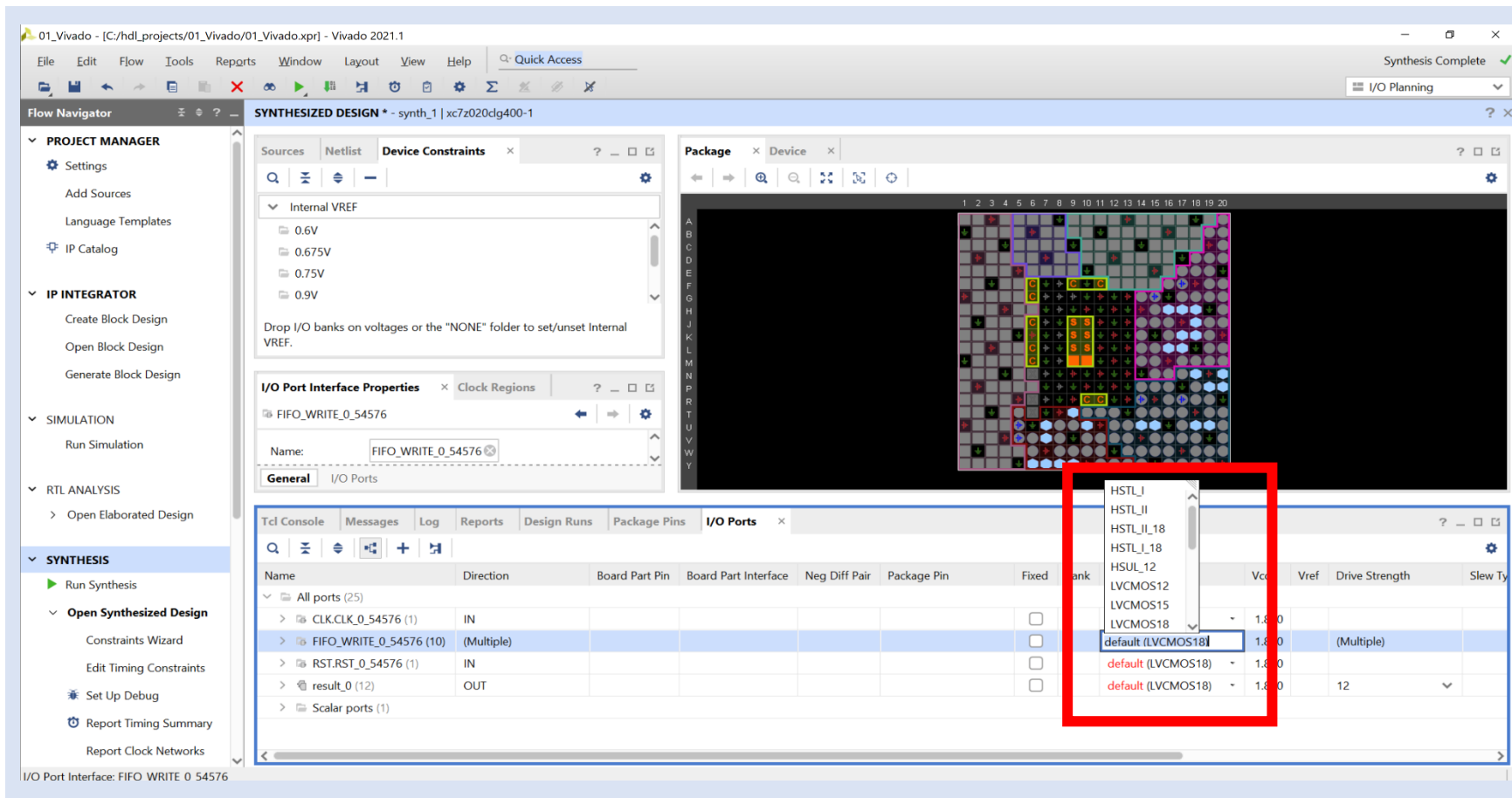
Lab 5: Intermediate Vivado

Step 28 – If any critical warnings pop up, select **OK**. This is due to out of data constraints which we are about to address.



Lab 5: Intermediate Vivado

Step 29 – Change the I/O standard from default to LVCMOS18.



The screenshot shows the Vivado IDE interface. The main window displays the I/O Port Interface Properties for the port FIFO_WRITE_0_54576. The I/O standard is set to default (LVCMOS18). A dropdown menu is open, showing options like HSTL_I, HSTL_I18, and LVCMOS18. The I/O Ports table is also visible, showing the port name, direction, board part pin, board part interface, neg diff pair, package pin, fixed, bank, vcc, vref, drive strength, and slew type.

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	Vcc	Vref	Drive Strength	Slew Ty
All ports (25)											
> CLK.CLK_0_54576 (1)	IN					<input type="checkbox"/>					
> FIFO_WRITE_0_54576 (10)	(Multiple)					<input type="checkbox"/>				(Multiple)	
> RST.RST_0_54576 (1)	IN					<input type="checkbox"/>					
> result_0 (12)	OUT					<input type="checkbox"/>					
Scalar ports (1)											

Lab 5: Intermediate Vivado

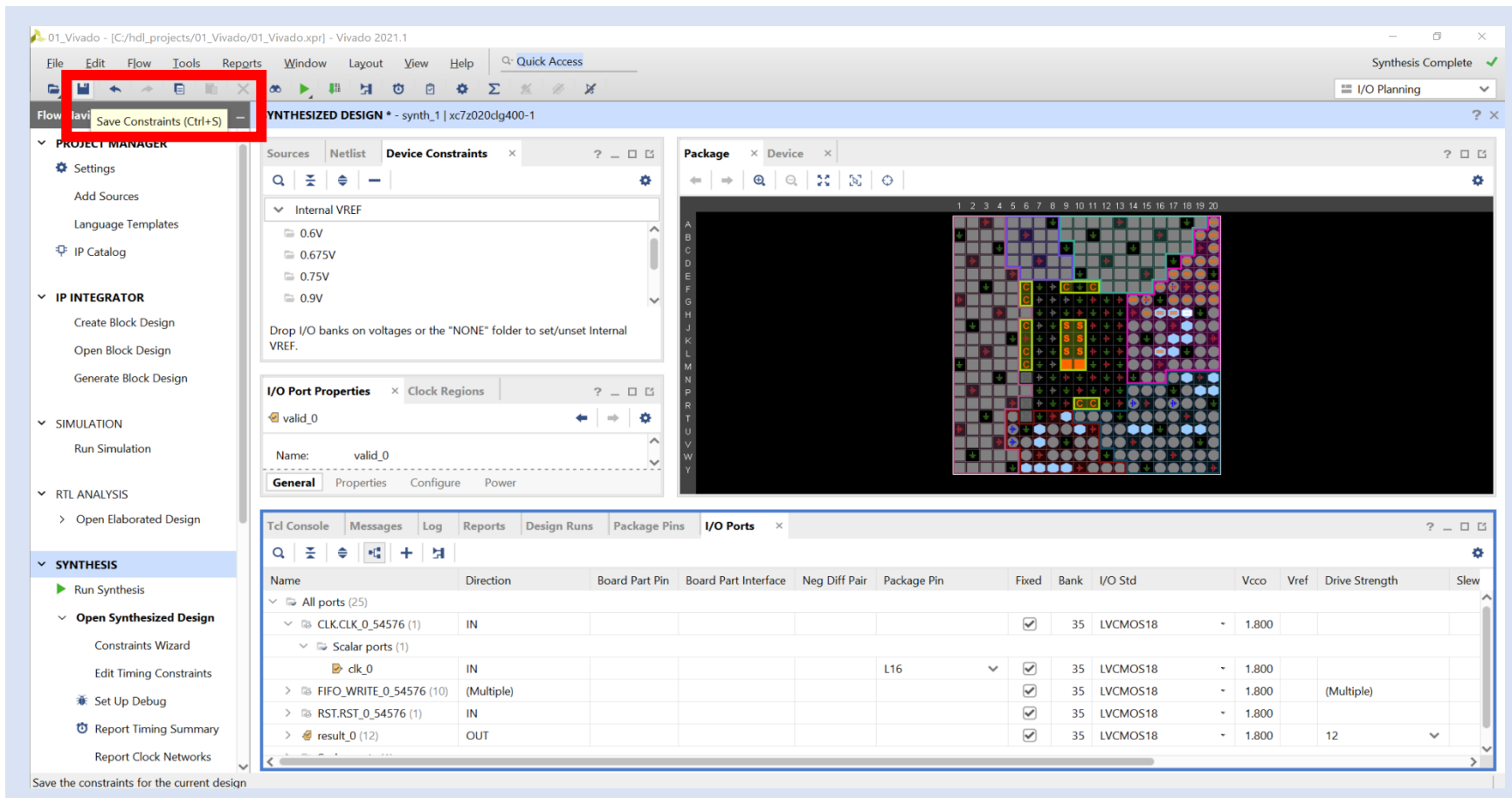
Step 30 – Assign the clock input to pin **L16**. Assign all other IO to pins of your choice.

The screenshot shows the Vivado 2021.1 I/O Planning window. The 'I/O Ports' table is visible, with a red box highlighting the row for the clock input 'clk_0' assigned to pin L16.

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew
CLK.CLK_0_54576 (1)	IN					<input checked="" type="checkbox"/>	35	LVCMS18	-	1.800		
Scalar ports (1)												
clk_0	IN				L16	<input checked="" type="checkbox"/>	35	LVCMS18	-	1.800		
EIO.WRITE_0_54576 (10)	(Multiple)					<input checked="" type="checkbox"/>	35	LVCMS18	-	1.800	(Multiple)	
RST.RST_0_54576 (1)	IN					<input checked="" type="checkbox"/>	35	LVCMS18	-	1.800		
result_0 (12)	OUT					<input checked="" type="checkbox"/>	35	LVCMS18	-	1.800	12	

Lab 5: Intermediate Vivado

Step 31 – Click on Save Constraints.



The screenshot shows the Vivado IDE interface for a synthesized design. The top toolbar has a red box around the 'Save Constraints (Ctrl+S)' button. The main workspace is divided into several panels:

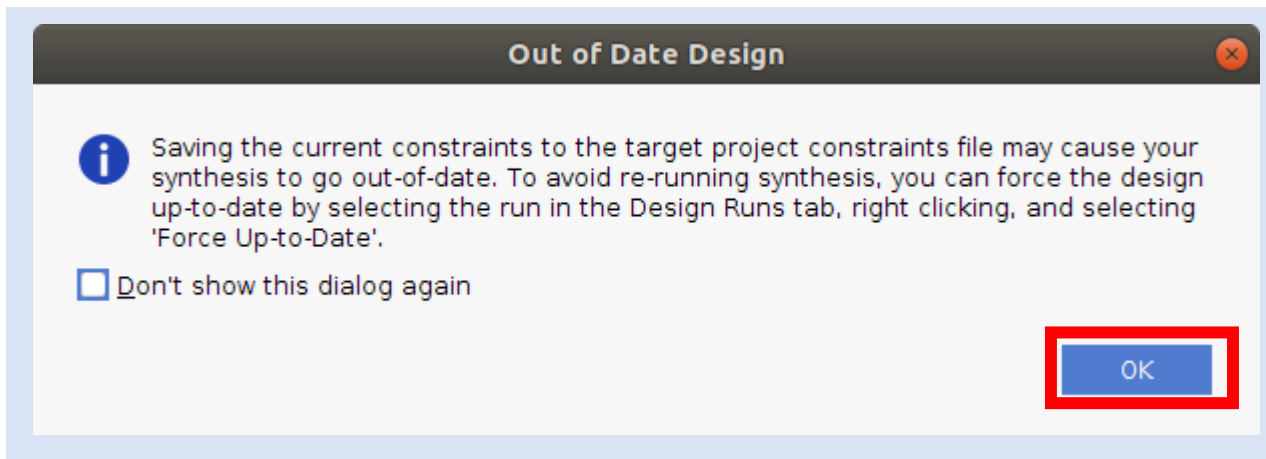
- PROJECT MANAGER:** Contains settings, IP integrator, simulation, and RTL analysis options.
- SYNTHESIS:** Shows the 'Open Synthesized Design' section with options like 'Constraints Wizard', 'Edit Timing Constraints', 'Set Up Debug', 'Report Timing Summary', and 'Report Clock Networks'.
- Device Constraints:** Lists internal VREF values (0.6V, 0.675V, 0.75V, 0.9V) and provides instructions to drop I/O banks on voltages or the "NONE" folder.
- I/O Port Properties:** Shows properties for a port named 'valid_0'.
- I/O Ports:** A table listing all ports with their directions, board part pins, interfaces, package pins, and electrical characteristics.

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew
All ports (25)												
CLK.CLK_0_54576 (1)	IN					<input checked="" type="checkbox"/>	35	LVCMS18	-	1.800		
Scalar ports (1)												
clk_0	IN				L16	<input checked="" type="checkbox"/>	35	LVCMS18	-	1.800		
FIFO_WRITE_0_54576 (10)	(Multiple)					<input checked="" type="checkbox"/>	35	LVCMS18	-	1.800	(Multiple)	
RST.RST_0_54576 (1)	IN					<input checked="" type="checkbox"/>	35	LVCMS18	-	1.800		
result_0 (12)	OUT					<input checked="" type="checkbox"/>	35	LVCMS18	-	1.800	12	

Save the constraints for the current design

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Step 32 – If an out-of-date warning appears, click **OK**.



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Step 33 – From the sources tab, open the **IO constraints**. You will see the old pin out for the previous project and your new project. This is because we have evolved the original project.

The screenshot shows the Vivado 2021.1 interface. The 'Sources' tab is active, displaying the 'io.xdc' file. The 'I/O Ports' table is visible at the bottom, showing the configuration for various ports.

IO Constraints (io.xdc):

```

1 set_property PACKAGE_PIN A20 [get_ports {data_in[7]}]
2 set_property PACKAGE_PIN B19 [get_ports {data_in[6]}]
3 set_property PACKAGE_PIN B20 [get_ports {data_in[5]}]
4 set_property PACKAGE_PIN C20 [get_ports {data_in[4]}]
5 set_property PACKAGE_PIN D18 [get_ports {data_in[3]}]
6 set_property PACKAGE_PIN D19 [get_ports {data_in[2]}]
7 set_property PACKAGE_PIN D20 [get_ports {data_in[1]}]
8 set_property PACKAGE_PIN E17 [get_ports {data_in[0]}]
9 set_property PACKAGE_PIN E18 [get_ports {result[11]}]
10 set_property PACKAGE_PIN E19 [get_ports {result[10]}]
11 set_property PACKAGE_PIN F16 [get_ports {result[9]}]
12 set_property PACKAGE_PIN F17 [get_ports {result[8]}]
13 set_property PACKAGE_PIN F19 [get_ports {result[7]}]
14 set_property PACKAGE_PIN F20 [get_ports {result[6]}]
15 set_property PACKAGE_PIN G14 [get_ports {result[5]}]
16 set_property PACKAGE_PIN G15 [get_ports {result[4]}]

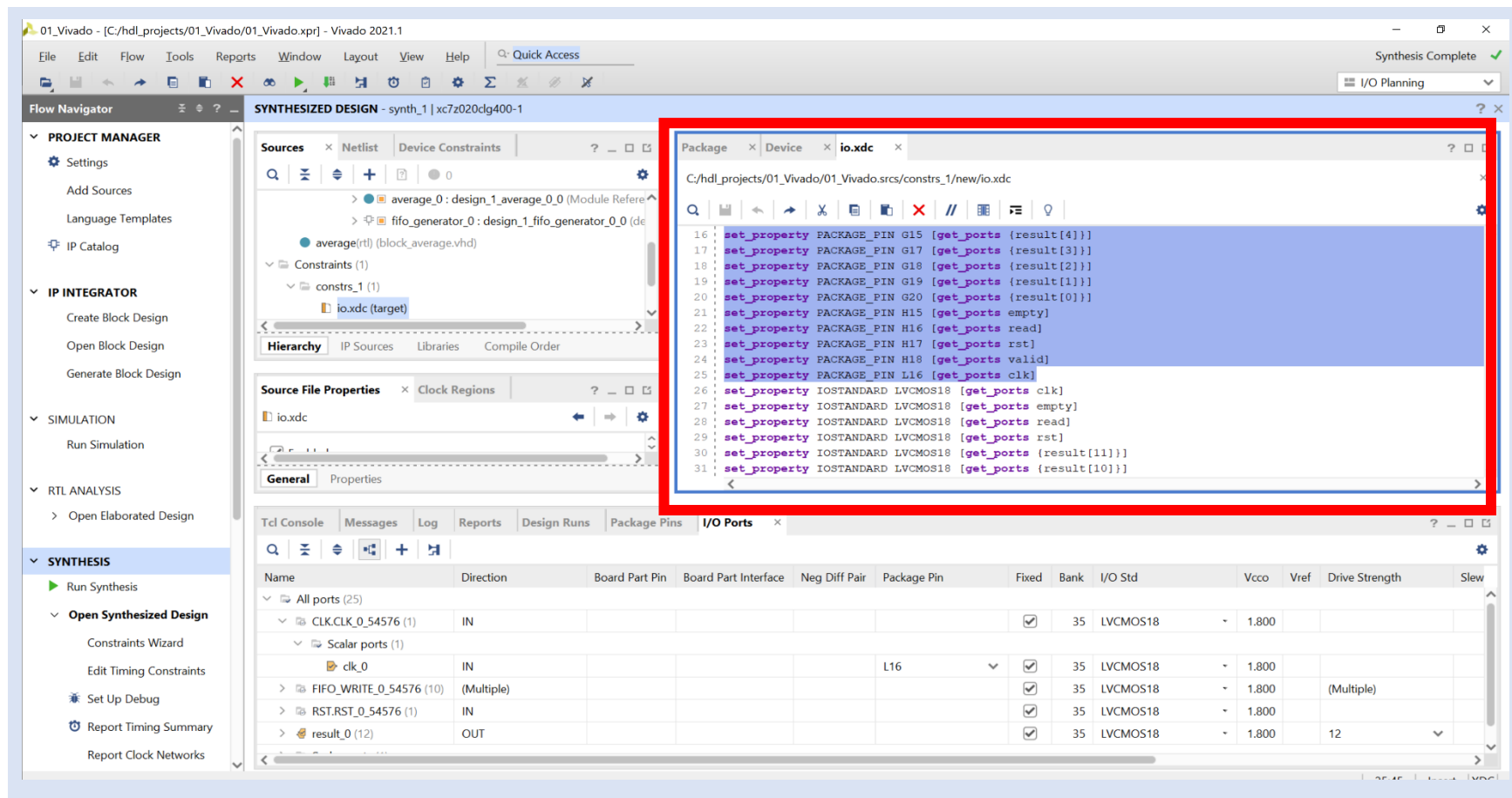
```

I/O Ports Table:

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew
CLK.CLK_0_54576 (1)	IN					<input checked="" type="checkbox"/>	35	LVCMOS18	1.800			
clk_0	IN				L16	<input checked="" type="checkbox"/>	35	LVCMOS18	1.800			
FIFO_WRITE_0_54576 (10)	(Multiple)					<input checked="" type="checkbox"/>	35	LVCMOS18	1.800		(Multiple)	
RST.RST_0_54576 (1)	IN					<input checked="" type="checkbox"/>	35	LVCMOS18	1.800			
result_0 (12)	OUT					<input checked="" type="checkbox"/>	35	LVCMOS18	1.800		12	

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Step 34 – Select the old constraints (at the top of the file) and delete them. Save the file.



The screenshot shows the Vivado IDE interface. The main window displays the 'io.xdc' file, which contains a list of constraints. A red rectangular box highlights the top portion of the file, specifically lines 16 through 25, which contain the following constraints:

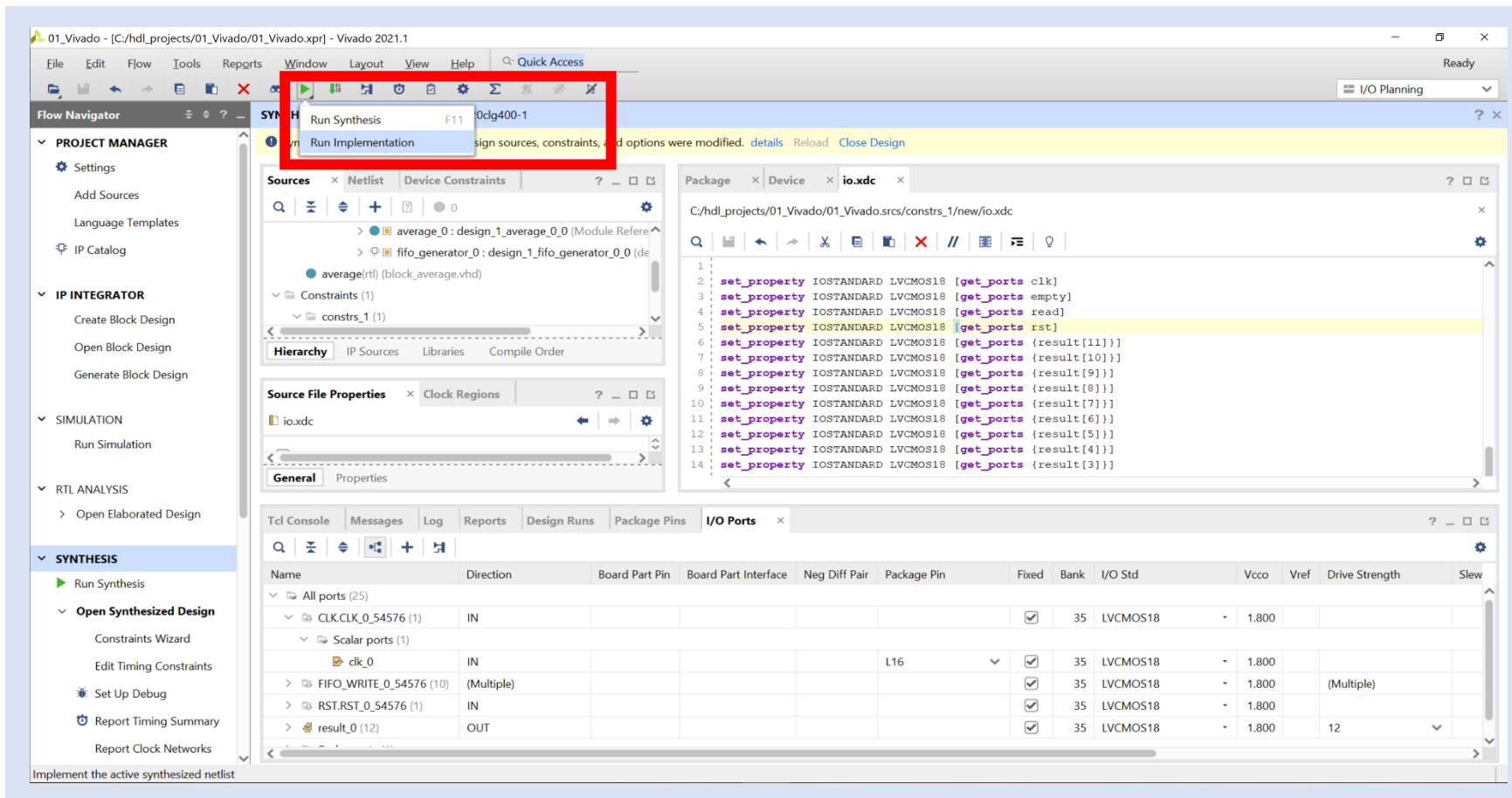
```
16: set_property PACKAGE_PIN G15 [get_ports {result[4]}]
17: set_property PACKAGE_PIN G17 [get_ports {result[3]}]
18: set_property PACKAGE_PIN G18 [get_ports {result[2]}]
19: set_property PACKAGE_PIN G19 [get_ports {result[1]}]
20: set_property PACKAGE_PIN G20 [get_ports {result[0]}]
21: set_property PACKAGE_PIN H15 [get_ports empty]
22: set_property PACKAGE_PIN H16 [get_ports read]
23: set_property PACKAGE_PIN H17 [get_ports rst]
24: set_property PACKAGE_PIN H18 [get_ports valid]
25: set_property PACKAGE_PIN L16 [get_ports clk]
```

The bottom portion of the screenshot shows the 'I/O Ports' table, which lists the ports and their properties:

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew
All ports (25)												
CLK.CLK_0_54576 (1)												
Scalar ports (1)												
clk_0	IN				L16	<input checked="" type="checkbox"/>	35	LVCOS18	1.800			
FIFO_WRITE_0_54576 (10)	(Multiple)					<input checked="" type="checkbox"/>	35	LVCOS18	1.800		(Multiple)	
RST.RST_0_54576 (1)	IN					<input checked="" type="checkbox"/>	35	LVCOS18	1.800			
result_0 (12)	OUT					<input checked="" type="checkbox"/>	35	LVCOS18	1.800		12	

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Step 35 –Run the Implementation, Re run synthesis if you get an out of date warning

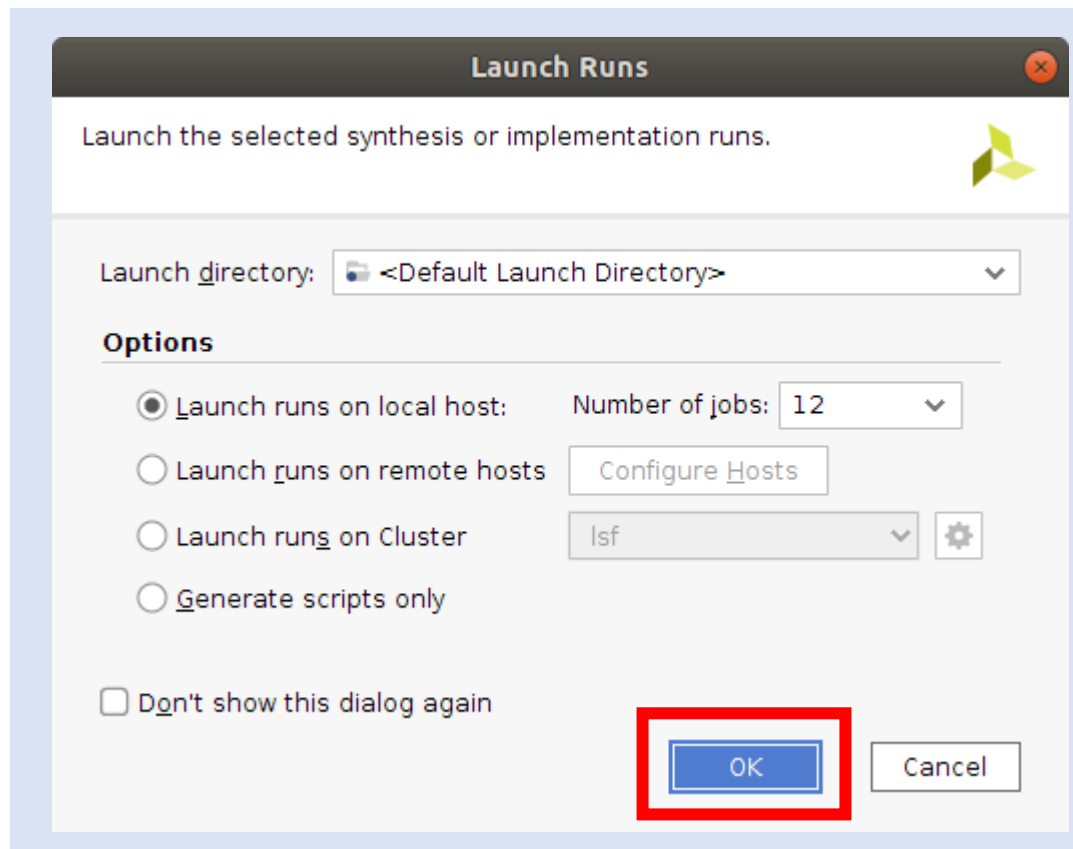


The screenshot shows the Vivado 2021.1 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, and Help. The toolbar contains various icons, with the Run Synthesis icon (a green play button) highlighted by a red rectangle. The Run Synthesis button is labeled 'Run Synthesis' and has the keyboard shortcut 'F11'. Below the toolbar, a yellow status bar displays a warning: 'Design sources, constraints, and options were modified. details Reload Close Design'. The main workspace is divided into several panes. On the left is the 'Flow Navigator' pane, which shows the project hierarchy under 'PROJECT MANAGER' and 'SYNTHESIS'. The 'SYNTHESIS' section is expanded, showing 'Run Synthesis' and 'Open Synthesized Design'. The central pane shows the 'Sources' pane with a list of sources including 'average_0', 'fifo_generator_0', and 'constrs_1'. The right pane shows the 'io.xdc' file with a list of I/O constraints. The bottom pane shows the 'I/O Ports' table, which lists the ports and their properties.

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew
All ports (25)												
CLK.CLK_0_54576 (1)												
Scalar ports (1)												
clk_0	IN				L16	<input checked="" type="checkbox"/>	35	LVCOS18	1.800			
FIFO_WRITE_0_54576 (10)	(Multiple)					<input checked="" type="checkbox"/>	35	LVCOS18	1.800		(Multiple)	
RST.RST_0_54576 (1)	IN					<input checked="" type="checkbox"/>	35	LVCOS18	1.800			
result_0 (12)	OUT					<input checked="" type="checkbox"/>	35	LVCOS18	1.800		12	

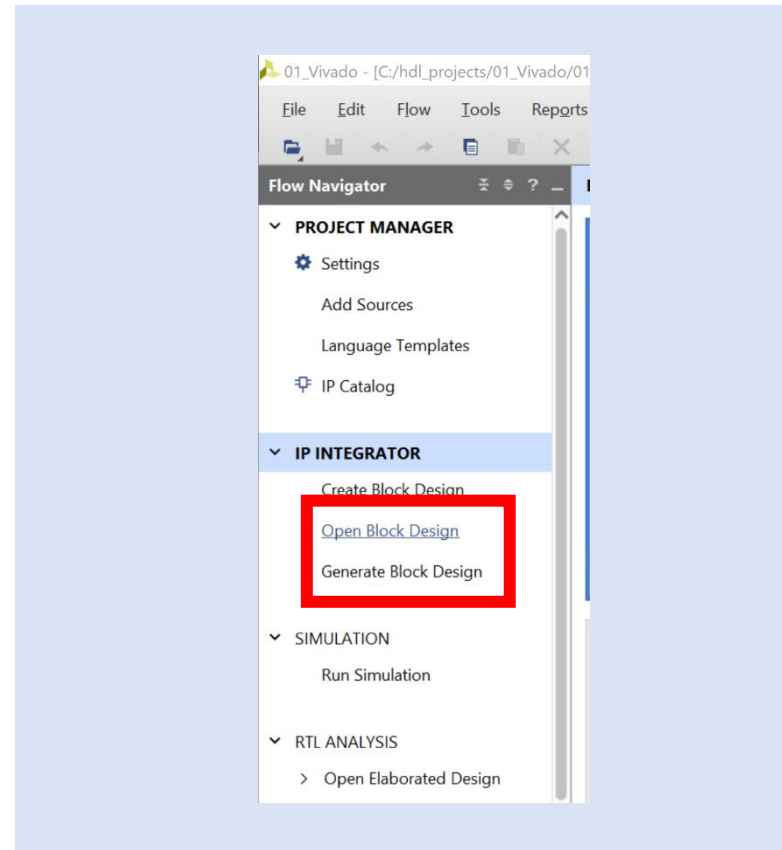
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Step 36 – Click **OK** to run the implementation.



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Step 37 – Open the Block Design when design has built.



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Step 38 – Select Constraints under Design Sources.

The screenshot displays the Vivado 2021.1 interface. The 'Sources' window is open, showing a project hierarchy. A red box highlights the 'constrs_1 (1)' folder under 'Simulation Sources (2)'. The 'Constraint Set Properties' window is also open, showing the 'constrs_1' constraint set with a file count of 1 and format XDC. The 'Diagram' window shows a block design with an 'average_0' block and a 'FIFO Generator' block. The 'Tcl Console' window is at the bottom, showing the command 'open_bd_design (C:/hdl_projects/01_Vivado/01_Vivado.srcs/sources_1/bd/design_1/design_1.bd)'.

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Step 39 – Click on the **Add Source** button.

The screenshot displays the Vivado 2021.1 software interface. The main window is titled "BLOCK DESIGN - design_1". The "Sources" tab is active, showing a tree view of the design's sources. A red box highlights the "Add Sources (Alt+A)" button in the top-left corner of the Sources panel. The "Constraint Set Properties" window is open, showing details for "constrs_1". The "Diagram" window shows a block diagram with two main components: "average_v1_0" and "fifo_generator_0". The "average_v1_0" block has inputs for "clk_0", "rst_0", "empty", and "data_in[7:0]", and outputs for "read", "valid", and "result[11:0]". The "fifo_generator_0" block has inputs for "FIFO_WRITE_0", "FIFO_READ", "empty", "rd_en", "clk", and "srst", and an output for "dout[7:0]". The "Tcl Console" at the bottom shows the command "open_bd_design (C:/hdl_projects/01_Vivado/01_Vivado.srcs/sources_1/bd/design_1/design_1.bd)".

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Step 40 – Select Add or Create Constraints. Then **Create File**, enter the name “**timing**” for the file, and click **Finish**.

The image displays three sequential screenshots of the Vivado 'Add Sources' dialog, illustrating the process of creating a timing constraint file.

Top Left Screenshot: The 'Add Sources' dialog is shown with the 'Add or create constraints' radio button selected and highlighted by a red box. The 'Add or create simulation sources' radio button is unselected.

Top Right Screenshot: The 'Add or Create Constraints' sub-dialog is shown. The 'Specify constraint set' dropdown is set to 'constrs_1 (active)'. A table lists the constraint files:

Constraint File	Location
io.xdc	C:\hdl_projects\01_Vivado\01_Vivado.srcs\constrs_1\new

The 'Create File' button is highlighted by a red box. The 'Copy constraints files into project' checkbox is checked.

Bottom Left Screenshot: The 'Create Constraints File' sub-dialog is shown. The 'File type' is set to 'XDC'. The 'File name' field contains 'timing' and is highlighted by a red box. The 'File location' is set to '<Local to Project>'. The 'OK' button is visible.

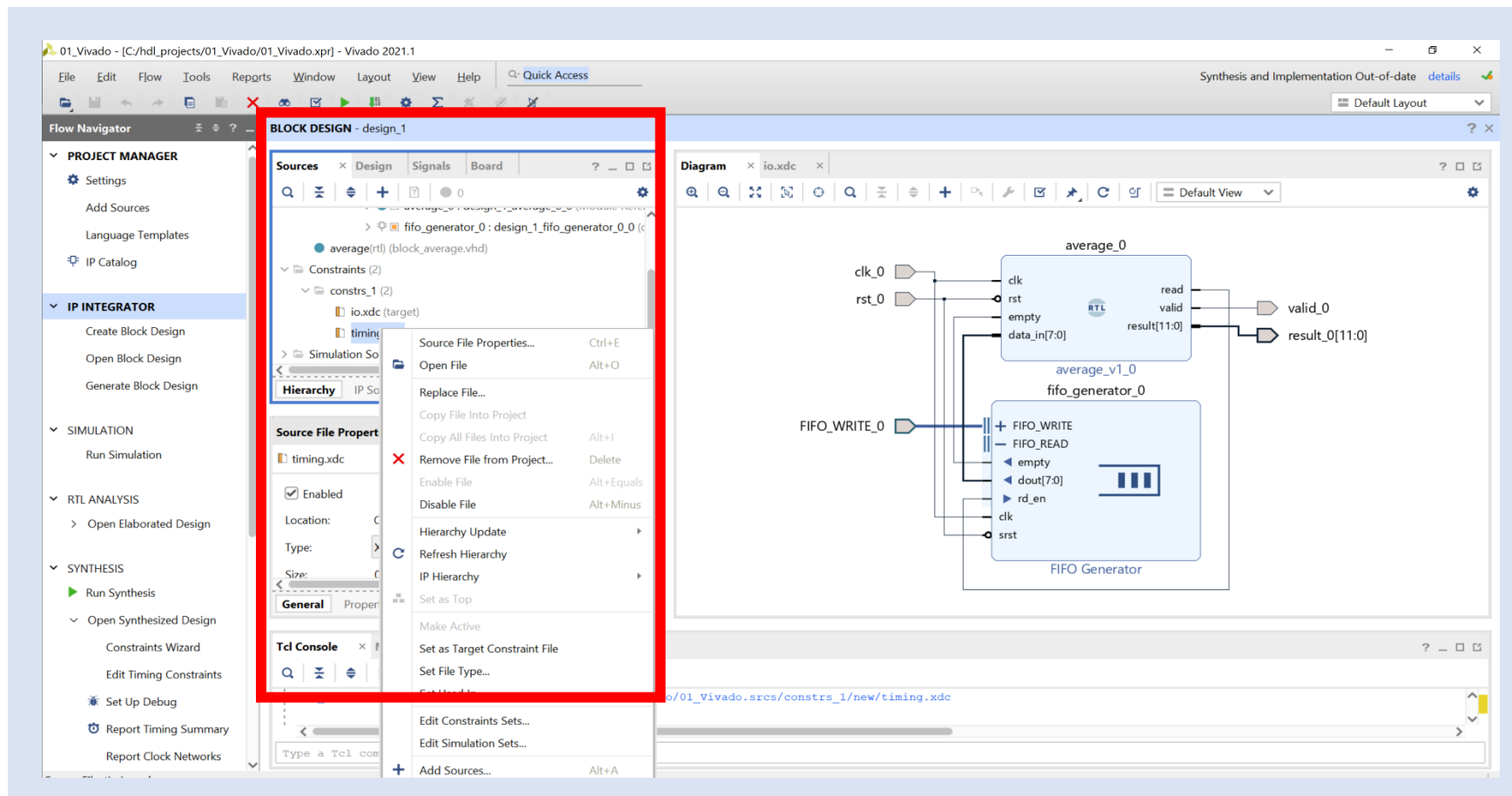
Bottom Right Screenshot: The 'Add or Create Constraints' sub-dialog is shown again. The table now includes the newly created file:

Constraint File	Location
io.xdc	C:\hdl_projects\01_Vivado\01_Vivado.srcs\constrs_1\new
timing.xdc	<Local to Project>

The 'Finish' button is highlighted by a red box. The 'Copy constraints files into project' checkbox is checked.

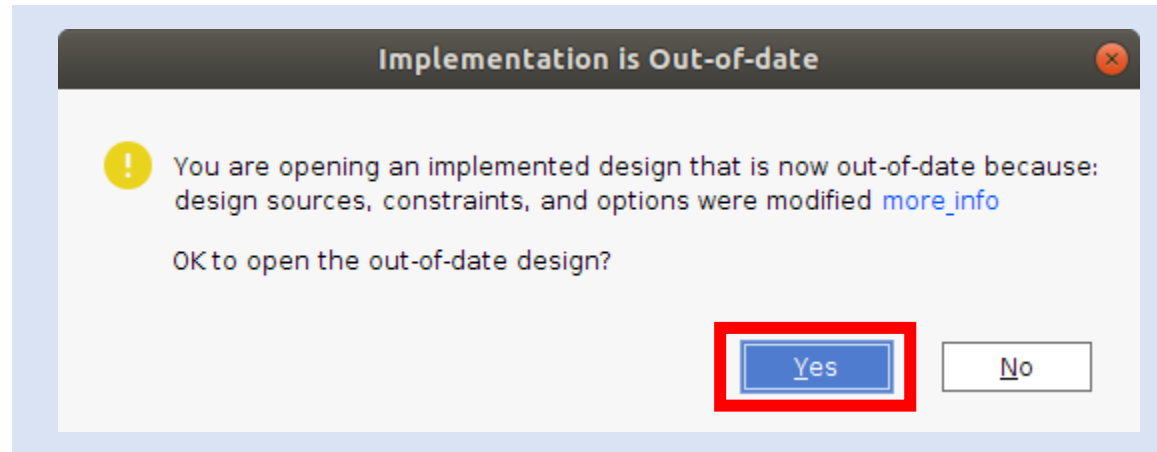
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Step 41 – Right click on the newly created constraint file and select **Set as Target Constraints File**.



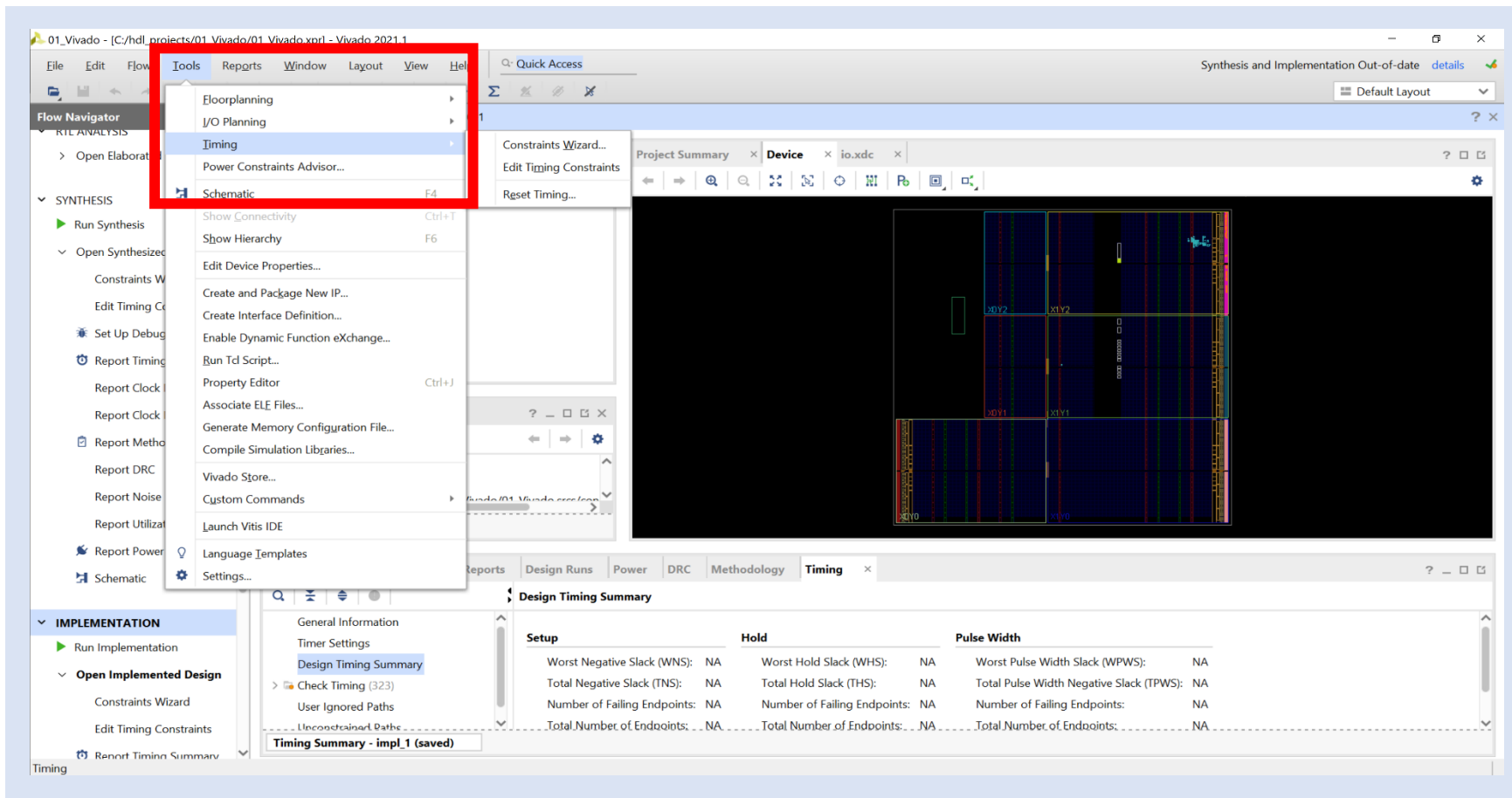
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Step 42 – Open the implemented design. If you see the warning below click **OK**.



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Step 43 – From the Tools menu, select **Timing** -> **Constraints Wizard**.



The screenshot shows the Vivado IDE interface. The **Tools** menu is open, and the **Timing** option is selected. The **Constraints Wizard** dialog box is open, showing the **Design Timing Summary** window. The summary table is as follows:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): NA	Worst Hold Slack (WHS): NA	Worst Pulse Width Slack (WPWS): NA
Total Negative Slack (TNS): NA	Total Hold Slack (THS): NA	Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA	Number of Failing Endpoints: NA	Number of Failing Endpoints: NA
Total Number of Endpoints: NA	Total Number of Endpoints: NA	Total Number of Endpoints: NA

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Step 44 – On the welcome screen, click **Next** and then enter **200 MHz** for the clock frequency. Once done, select **Skip to Finish**.

The image displays two screenshots of the Vivado Timing Constraints Wizard. The left screenshot shows the 'Identify and Recommend Missing Timing Constraints' page. The right screenshot shows the 'Primary Clocks' page with a table of recommended constraints for 'clk_0' at 200.000 MHz, 5.000 ns period, and 2.500 ns jitter. The 'Skip to Finish >>' button is highlighted in a red box.

Identify and Recommend Missing Timing Constraints

The Timing Constraints Wizard guides you through creating timing constraints per Xilinx design methodology. It analyzes your design for missing timing constraints and makes recommendations. You need to review and understand all of the recommendations to ensure they are appropriate for your design.

Clocks:

- Primary Clocks
- Generated Clocks
- Forwarded Clocks
- External Feedback Delays

Input and Output Ports:

- Input Delays
- Output Delays
- Combinational Delays

Clock Domain Crossings:

- Physically Exclusive Clock Groups
- Logically Exclusive Clock Groups with No Interaction
- Logically Exclusive Clock Groups with Interaction
- Asynchronous Clock Domain Crossings

Clicking 'Next' on a page applies the constraints to the design in memory, so that missing constraints on subsequent pages can be identified. Each page may require considerable runtime to discover missing constraints.

The Clock Networks report is available on every page to help you review the constraints. Schematics and timing path reports are available on the Asynchronous Clock Domain Crossings page.

To leave the Wizard and automatically save the new constraints to the target XDC file, click Finish. To discard the new constraints click Cancel.

Primary Clocks

Primary clocks usually enter the design through input ports. Specify the period and optionally a name and waveform (rising and falling edge times) to describe the duty cycle if not 50%. [More info](#)

Recommended Constraints

Object	Name	Frequency (MHz)	Period (ns)	Rise At (ns)	Fall At (ns)	Jitter (ns)
<input checked="" type="checkbox"/>	clk_0	200.000	5.000	0.000	2.500	

Constraints for Pulse Width Check Only

Object	Name	Frequency (MHz)	Period (ns)	Rise At (ns)	Fall At (ns)	Jitter (ns)
<input type="checkbox"/>						

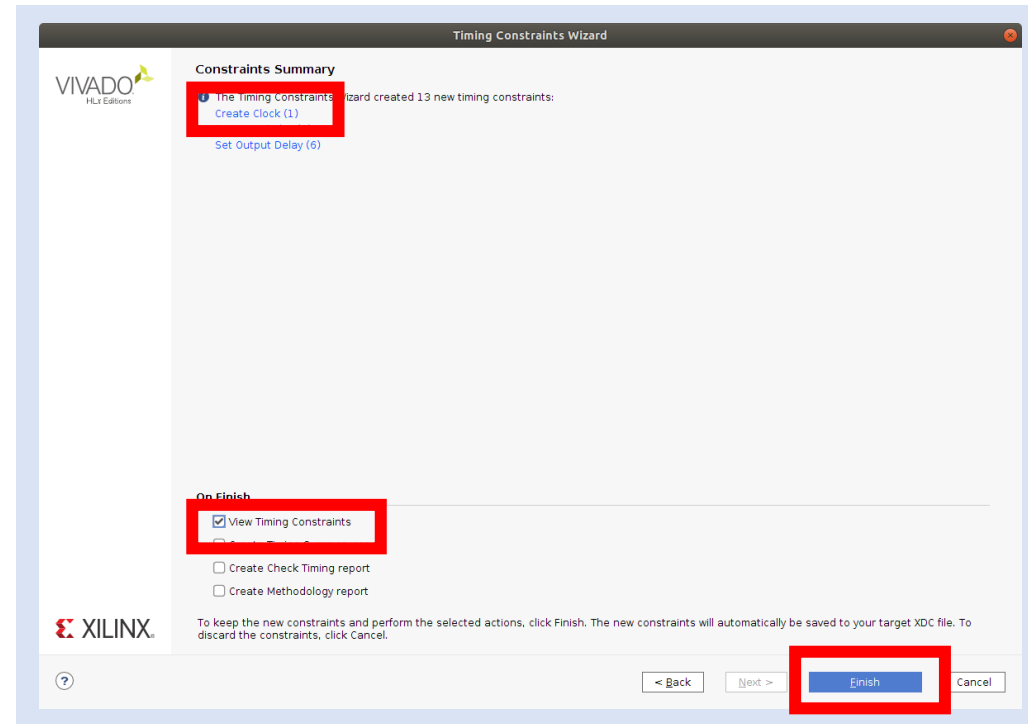
Tcl Command Preview (1) Existing Create Clock Constraints (0)

```
create_clock -period 5.000 -name clk_0 -waveform {0.000 2.500} [get_ports {clk_0}]
```

Navigation: Next > Skip to Finish >> Cancel

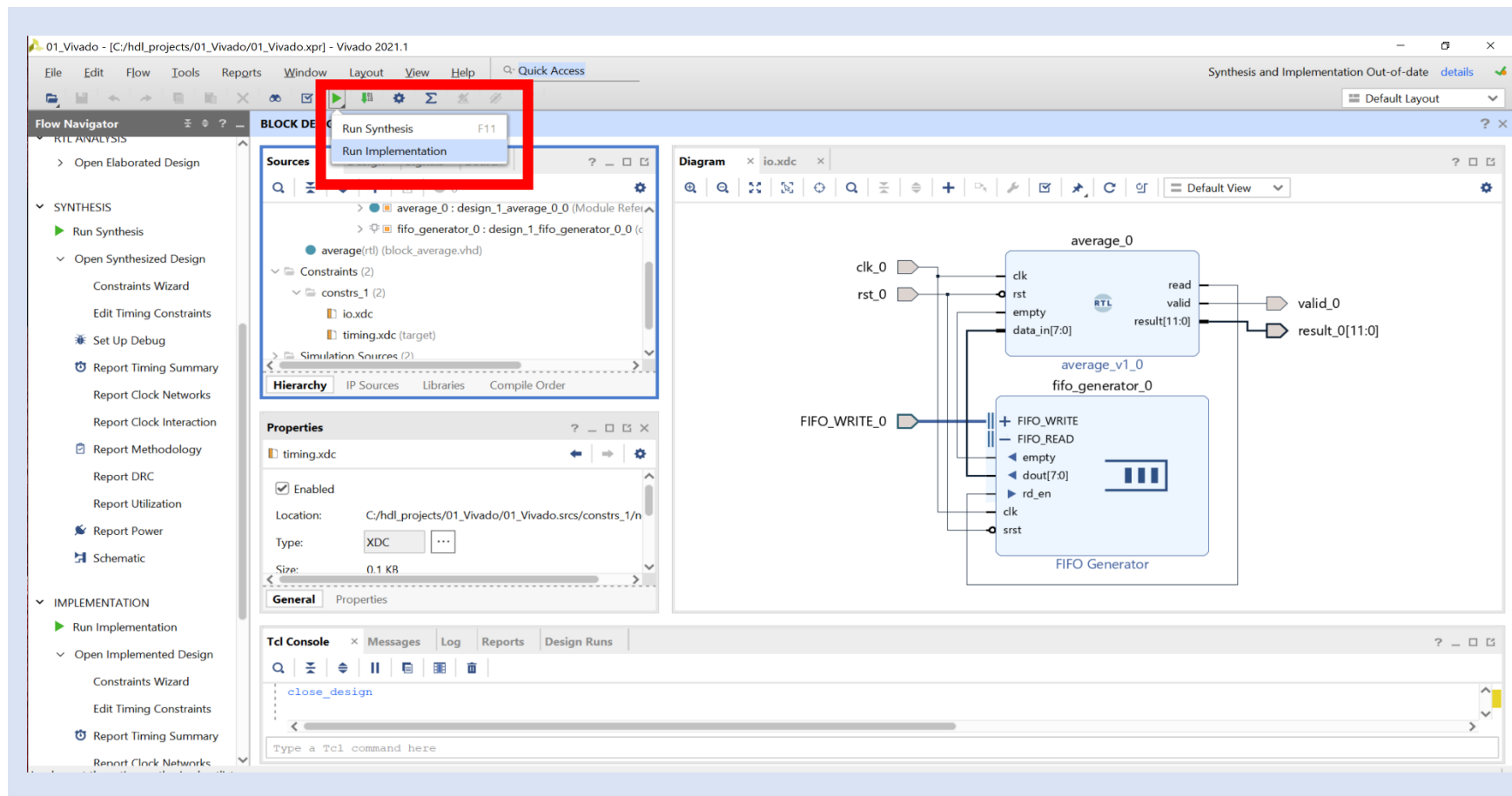
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Step 45 – On the final page, check that only one constraint is being created, check the **View Timing Constraints**, and click **Finish**.



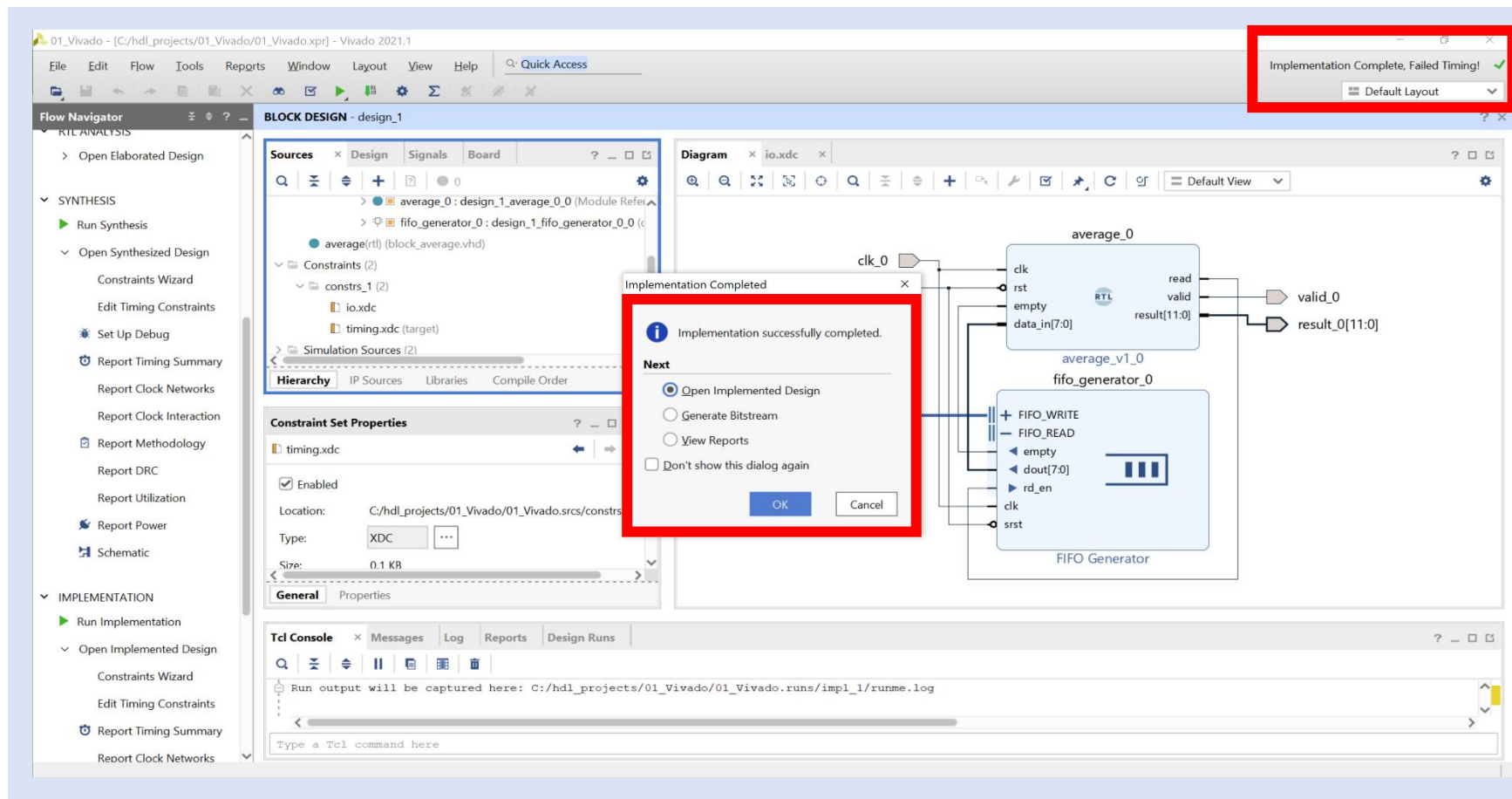
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Step 46 – Close the implementation view and **rerun the implementation**. **Run synthesis if you get out of date pop up**. Click **OK** on any dialogs which pop up prior to implementation starting.



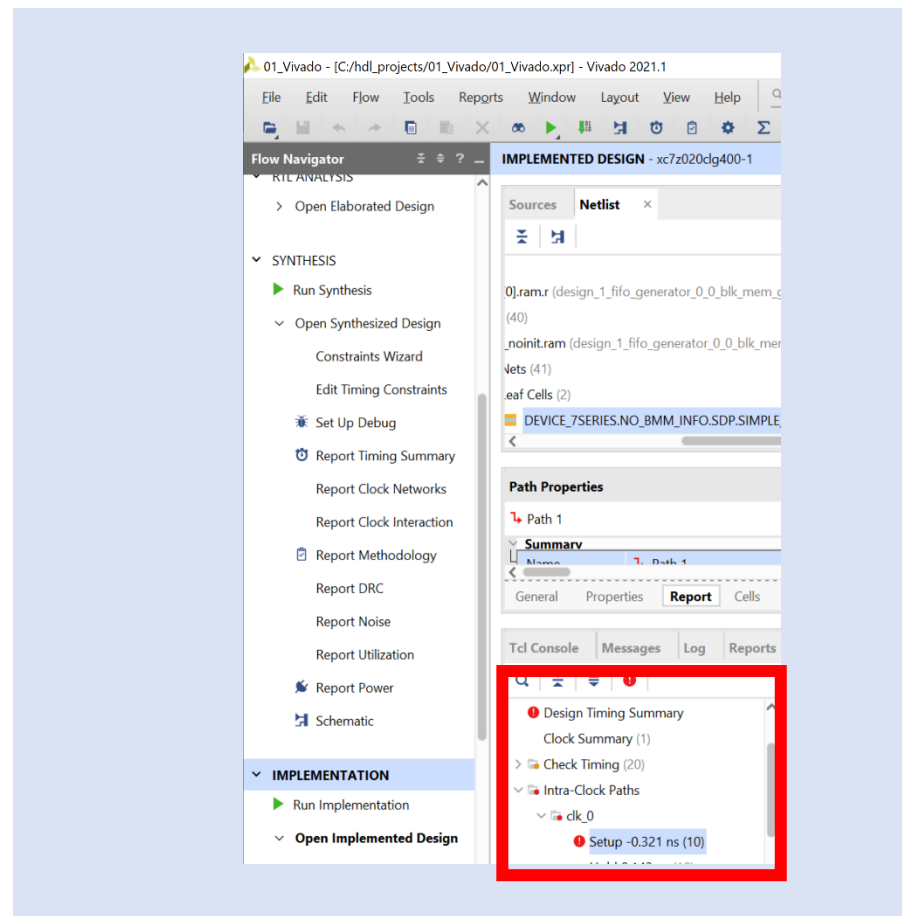
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Step 47 – Once the implementation completes, Timing will fail. Open the **Implemented Design**.



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Step 48 – In the implemented design, select the failing **Intra-Clock Paths**.



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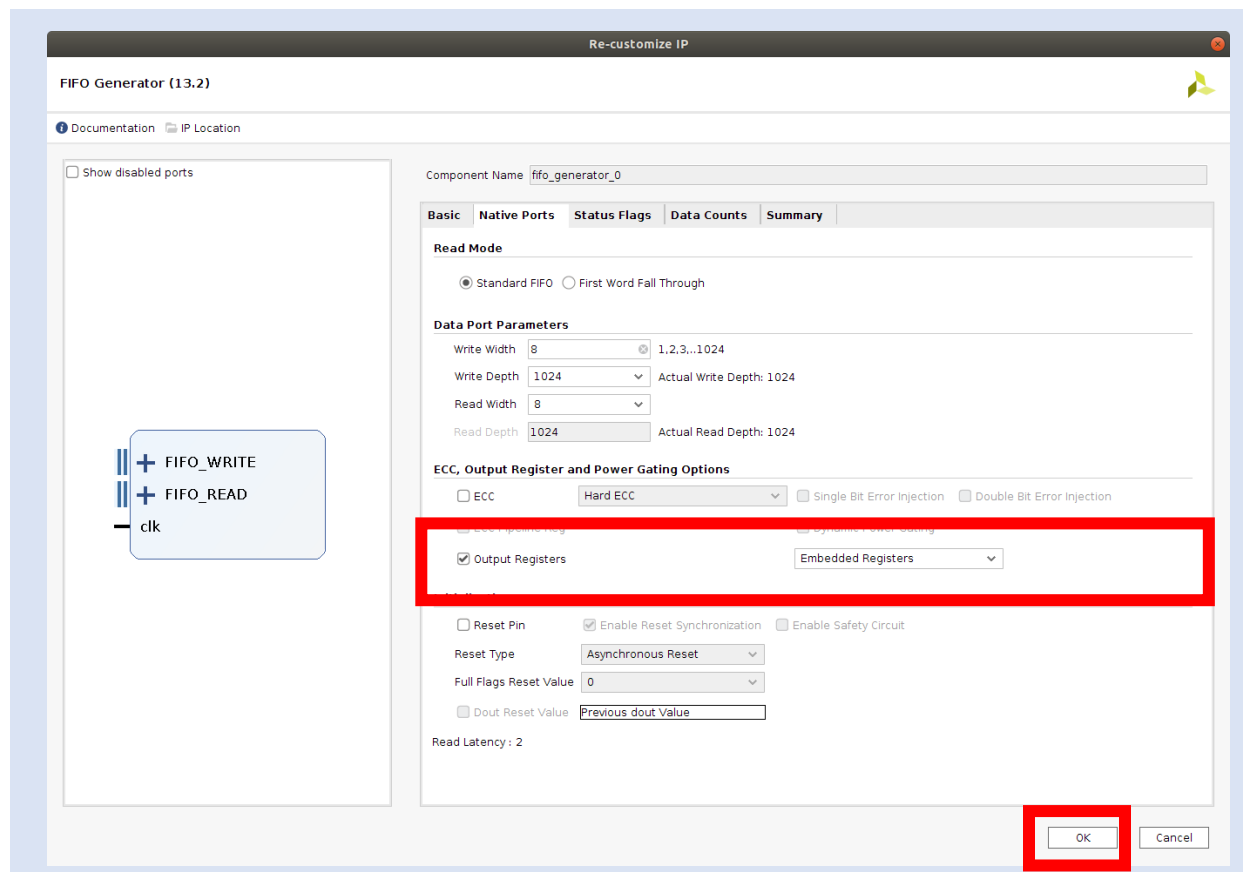
Step 49 – Select **Path 1** and zoom in. You will see that the FIFO output data passes through LUTs before finally being registered. This path is too long for timing at 200 MHz.

The screenshot displays the Vivado 2021.1 interface. The 'Flow Navigator' on the left shows the 'IMPLEMENTATION' phase. The 'Timing' report is open, showing a table of 'Intra-Clock Paths - clk_0 - Setup'. The table lists several paths, with 'Path 1' highlighted in red, indicating a timing violation. The zoomed-in schematic view shows the physical path of the signal through the FPGA fabric, passing through multiple Look-Up Tables (LUTs) before reaching a register.

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination
Path 1	-0.321	5	1	design_1...LKBWRCLK	design_1...r_reg[9]/D	5.292	3.887	1.405	5.0	clk_0	clk_0
Path 2	-0.298	5	1	design_1...LKBWRCLK	design_1...r_reg[11]/D	5.233	3.872	1.361	5.0	clk_0	clk_0
Path 3	-0.275	4	1	design_1...LKBWRCLK	design_1...r_reg[5]/D	5.212	3.773	1.439	5.0	clk_0	clk_0
Path 4	-0.210	5	1	design_1...LKBWRCLK	design_1...r_reg[10]/D	5.101	3.765	1.336	5.0	clk_0	clk_0
Path 5	-0.182	4	1	design_1...LKBWRCLK	design_1...r_reg[7]/D	5.119	3.758	1.361	5.0	clk_0	clk_0
Path 6	-0.122	4	1	design_1...LKBWRCLK	design_1...r_reg[4]/D	5.013	3.631	1.382	5.0	clk_0	clk_0

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Step 50 – To fix this, we need to register the output of the FIFO. Close the implementation view and reopen the block diagram. Double click on the **FIFO** to customize.



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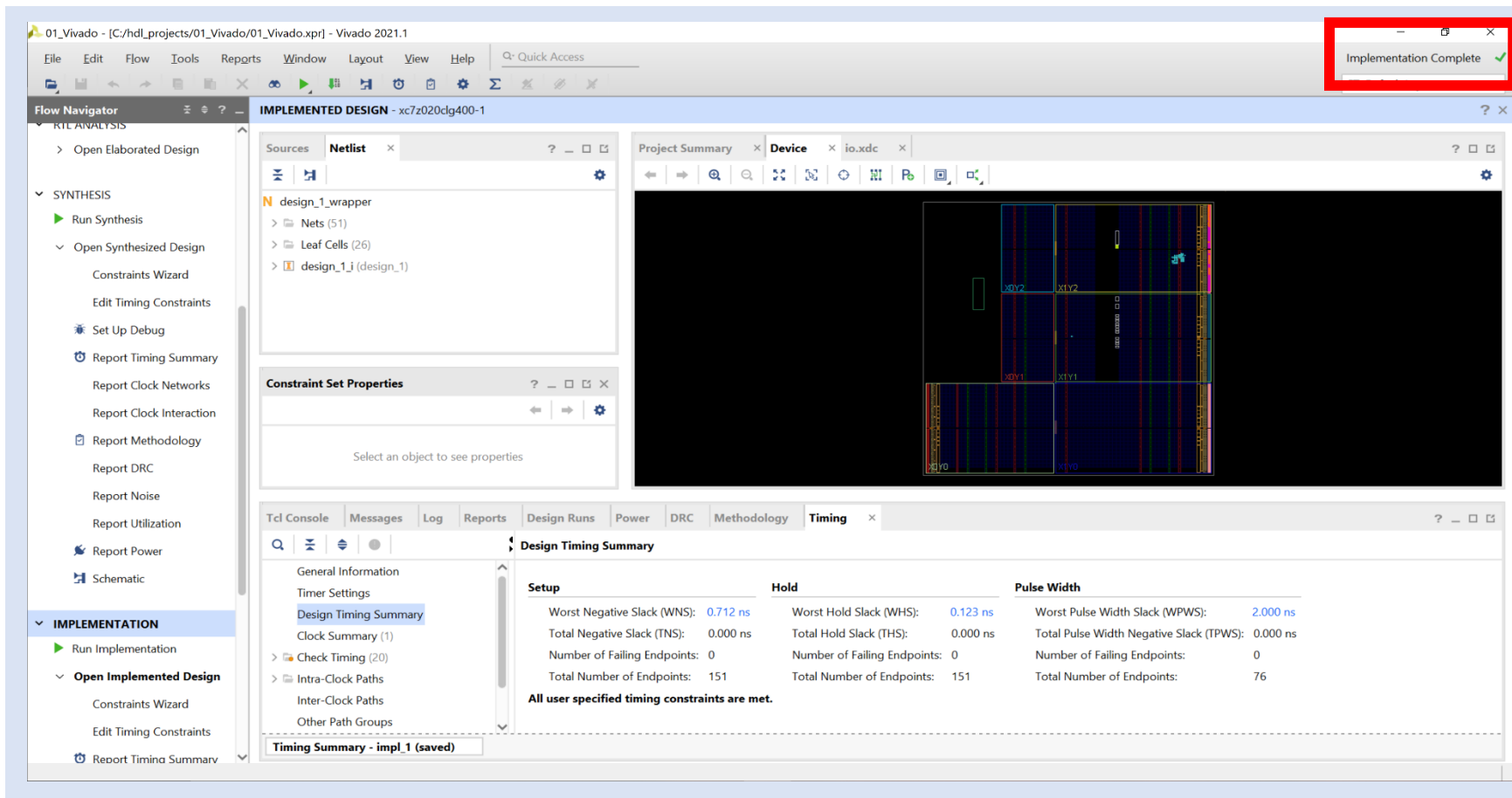
Step 51 – Note the latency has changed from 1 to 2 clocks. We would need to correct for this in the average block, however, we proceed assuming that we have.

The screenshot shows the 'Re-customize IP' dialog for the 'FIFO Generator (13.2)'. The 'Summary' tab is active, displaying a table of parameters. The 'Read Latency (From Rising Edge of Read Clock)' is highlighted with a red box and has a value of 2. The 'OK' button is also highlighted with a red box.

Parameter	Value
Block RAM resource(s) (18K BRAMs)	1
Block RAM resource(s) (36K BRAMs)	0
Clocking Scheme	Common Clock
Memory Type	Block RAM
Model Generated	Behavioral Model
Write Width	8
Write Depth	1024
Read Width	8
Read Depth	1024
Almost Full/Empty Flags	Not Selected/Not Selected
Programmable Full/Empty Flags	Not Selected/Not Selected
Handshaking	Not Selected
Read Mode / Reset	Standard FIFO / Not Selected
Read Latency (From Rising Edge of Read Clock)	2

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Step 52 – Reimplement the design. When the timing is completed, you should see that the implementation is correct and the timing is met.



The screenshot shows the Vivado IDE interface. The top right corner of the window displays a red-bordered box with the text "Implementation Complete" and a green checkmark. The main workspace is divided into several panes:

- Flow Navigator:** Shows the project flow, with the "IMPLEMENTATION" section expanded to show "Run Implementation" and "Open Implemented Design".
- Sources:** Displays the project files, including "design_1_wrapper", "Nets (51)", "Leaf Cells (26)", and "design_1_j (design_1)".
- Constraint Set Properties:** A pane for viewing and editing constraints.
- Project Summary:** Shows the device and other project details.
- Timing Summary:** A detailed report showing the results of the timing analysis.

The **Design Timing Summary** report is displayed in the bottom pane, showing the following data:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.712 ns	Worst Hold Slack (WHS): 0.123 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 151	Total Number of Endpoints: 151	Total Number of Endpoints: 76

Below the table, it states: "All user specified timing constraints are met."