PmodAMP1™ Demo Project

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Overview

The PmodAMP1 demo project outputs a tone using a pulse width modulated (PWM) signal generated by a Digilent FPGA system board. The tone varies for different boards, due to their different clock frequencies. The project was developed in Xilinx ISE Design Suite 13.2 for use with a Nexys3 board. The PmodAMP1 is connected to the upper row of connector JA on the Nexys3.

Functional Description

The project contains four modules: PmodAmp1, PWM, sinerom, and synth.

PmodAMP1

This is the main module that calls each component. The components are called in the following order:

1. synth: Divides the input clock and outputs a value (syn_out) between 0 and 255.
2. sinerom: Receives syn_out as input and outputs a corresponding value (sin) in the sine wave table.
3. PWM: Takes sin as input and generates a PWM signal. This PWM signal is output to pin 1 and 3 of the upper row of connector JA. The pins are defined in the .ucf file.

PWM

This module generates a PWM wave on pwm_out output using a 100MHz clock input and a switch signal. For more information, see the *Pulse-Width Modulation Reference Component* document for Nexys2, available at www.digilentinc.com. Note: The frequency on the Nexys3 board is 100MHz opposing to the 50MHz for the Nexys2 board.

sinerom

This module defines a sine wave table and returns a corresponding value (sin) in the sine wave table for the given position (addr). There are 256 points in the sine wave table.

synth

This module divides the clock input (clk) to a lower frequency, so that PmodAMP1 outputs the middle-C tone. Specifically, the clock input is divided by 1493. That value was calculated by first dividing the frequency of the clock (100MHz) by the frequency of middle C (261.6Hz). The result was then divided by 256, the number of points in the sine wave table (to accommodate each point in the sine wave). The output (syn_out) is incremented by one on each divided clock tick.