PmodCLS Interface Reference Project

1300 NE Henley Court, Suite 3
Pullman, WA 99163
(509) 334 6306 Voice | (509) 334 6300 Fax

Revision: June 25, 2012

Overview

This document presents HDL implementation details for interfacing with the PmodCLS. The project displays the message “Hello From Digilent” on the PmodCLS, which can then be cleared and rewritten.

Functional Description

The PmodCLS Interface Reference Project utilizes a serial port interface (SPI) controller that communicates with the PmodCLS. This project was developed on a Spartan-6 XCSLX16 Nexys3 board, but it is easily retargeted to any other FPGA/board. The onboard 100 MHz oscillator is used to generate a 100 kHz signal. The 100 MHz signal is used in the Master Interface, and the 100 kHz signal is used in the SPI interface for generating a serial clock.

The Nexys3 uses a serial interface to communicate with the PmodCLS connected via a 6 pin cable, on port JA(6:1) of the board. Overall the design consists of several HDL files, but only the major SPI components will be discussed.

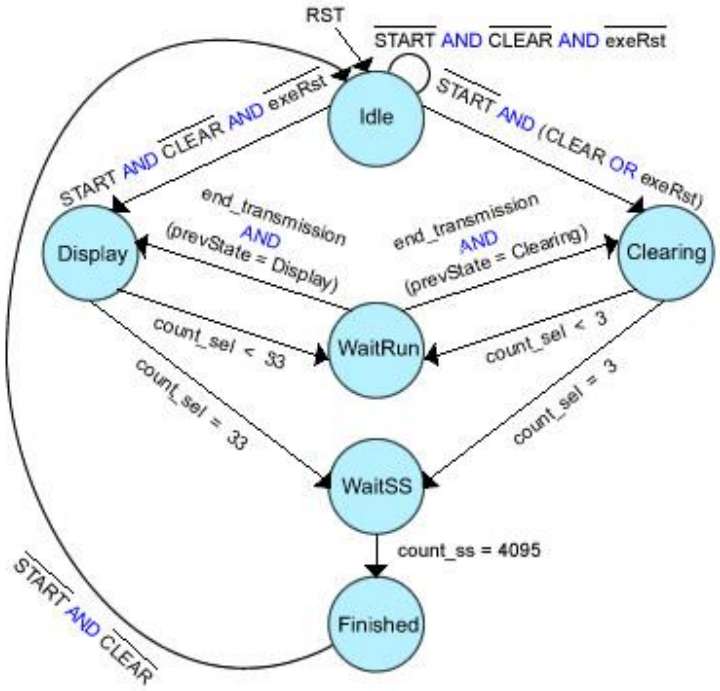

Figure 1: State Diagram for Master Interface

Block Description

Master Interface

The Master Interface block produces the internal signals that control other components in the project, and it controls the *slave select* output of the design. In order to transmit data between the slave (PmodCLS) and master (Nexys3), the *slave select* signal must be de-asserted, i.e. it is an active low signal. The *slave select* output is tied to *JA0*.

The Master Interface has several inputs, but only *reset*, *clear*, and *start* will be discussed. *Reset* sets the system back to its power up state and clears the PmodCLS screen. The *reset* input is tied to *SW0* on the Nexys3, and when it is asserted *LD0* on the board will illuminate. *Clear* is tied to *SW1* on the Nexys3, it sends a clear screen command to the PmodCLS and clears the display. This is needed because the PmodCLS will display any information sent to it since the last power cycle. *Start* is tied to

Master Interface (*continued*)

SW2 on the Nexys3, and it will display the message “Hello From Digilent” on the PmodCLS screen when asserted.

Master Interface utilizes the Nexys3’s onboard 100 Mhz clock, and updates on rising edges. The *begin transmission* and *end transmission* signals communicate between the modules to determine when to either enter, or exit the current state. Begin transmission signifies the beginning of a data transmission to the PmodCLS, and conversely *end transmission* indicates the end of a data transmission. The Master Interface’s state diagram is shown in figure 1 on page 1.

SPI Interface

The SPI Interface handles all data transmissions to and from the PmodCLS, and produces a 100 kHz serial clock (*SCLK*) for the PmodCLS. When the *begin transmission* signal is asserted, the data on the *send data* input bus is written into a shift register. Next the most significant bit (MSB) of the shift register is transmitted to the PmodCLS on the *MOSI* output (tied to *JA1*) on the falling edge of *SCLK*. On the rising edge of *SCLK* a bit is shifted into the same register’s least significant bit (LSB) from the PmodCLS on the *MISO* input (tied to JA2). This process repeats until an entire byte has been shifted out of and into the shift reigster. While the SPI Interface is in the *Idle* state *SCLK* is held high (i.e. asserted), and communication between the Nexys3 and PmodCLS is disabled.

Command Lookup

The Command Lookup component is a ROM that holds the sequence of commands that are to be sent to the PmodCLS for this demo. The values are stored in ASCII format, and the input signal *SEL* is used to select which command to output to the PmodCLS on the *data out* bus.