Genesys BSB
Standard and Custom IP Addition

Using EDK 11 SP 4

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Overview

- Initial Hardware Setup
- Software Requirements
- Adding Standard Supported IP
  - PLB bus and bridge
  - util_bus_split
  - GPIO (LCD)
  - PS2
  - xps_epc (Usb Host and Device)
  - xps_tft (HDMI Out)
- Adding Custom IP
  - AC '97 audio codec (ac97_if_00)
  - Digilent USB-EPP interface (usb_epp_if)
- Generate a Bitstream
- Transfer the Bitstream onto the FPGA
- Setting SDK workspace and Hardware Specification File
- SDK demo projects and Hardware setup for each project

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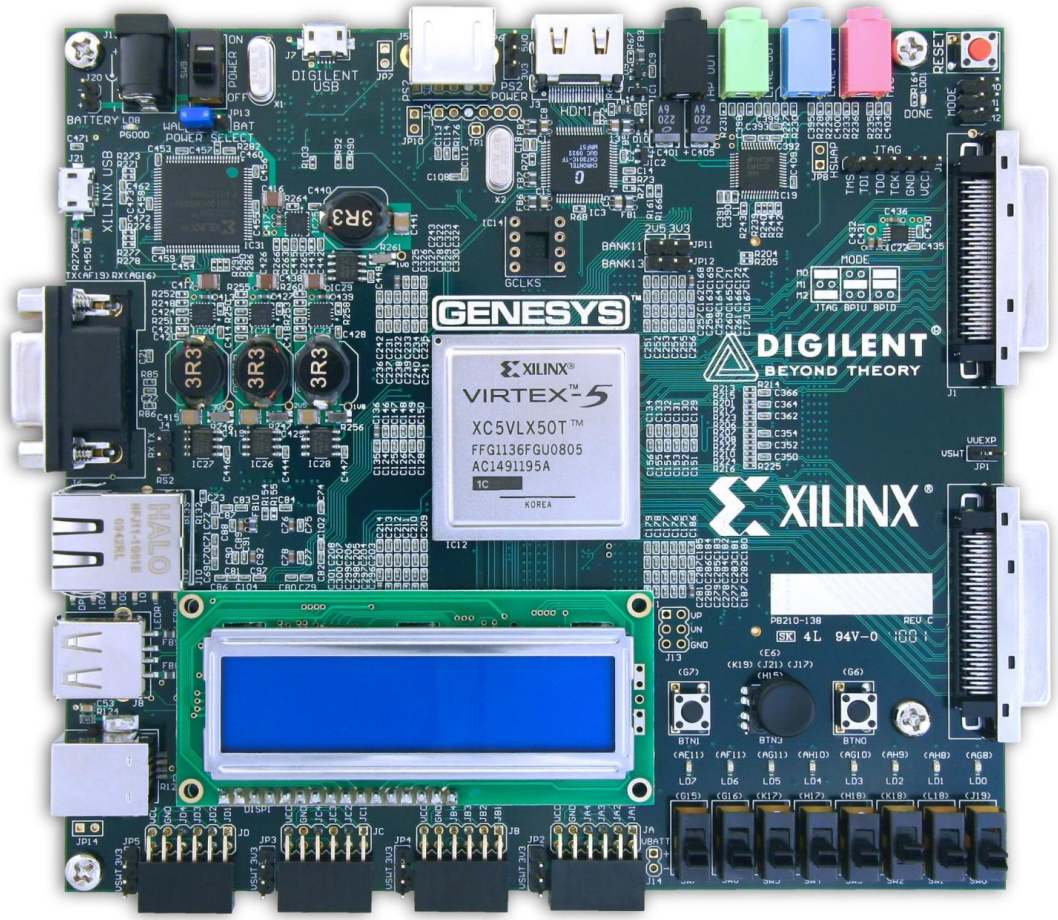
Genesys board



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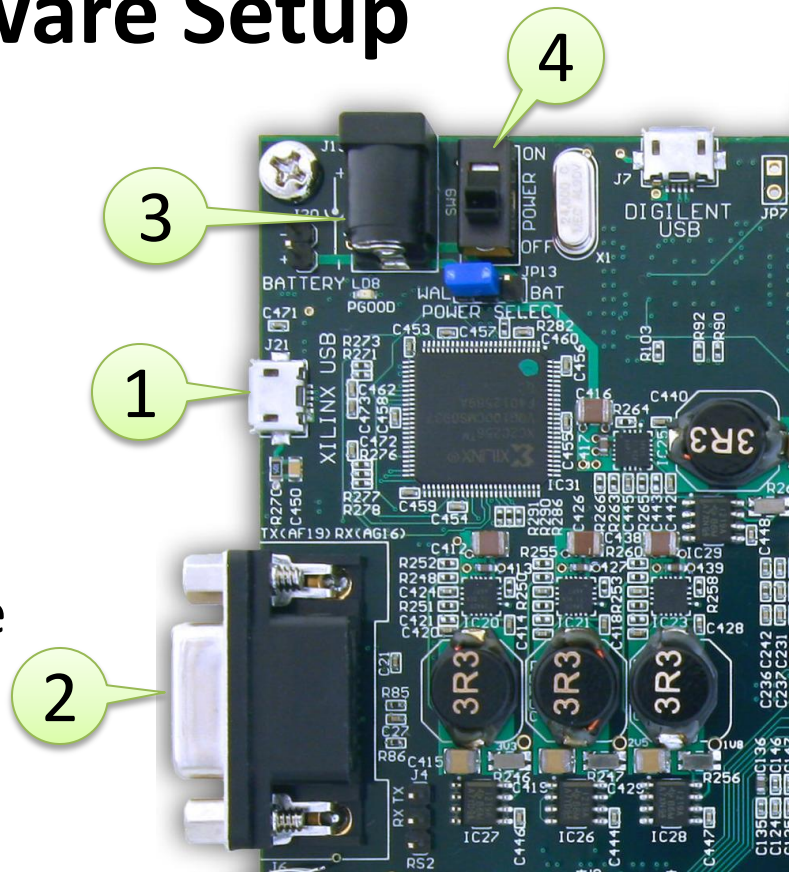
Initial Hardware Setup

- Connect the micro USB cable to the Xilinx USB programming connector (1)
- Connect the RS232 serial cable to the Genesys board (2)
- Connect the power supply to the board (3) and power on the board (4)



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Software Setup

- Software requirement
  - Xilinx ISE 11.4 or later
  - Xilinx EDK 11.4 or later
  - A terminal emulator program (Hyperterminal, Putty, AccessPort, Teraterm etc)
  - Adept 2.3 or later
- Software setup
  - Start the terminal program and set the serial port parameters to baudrate 9600, 8 data bits, 1 stop bit, no parity

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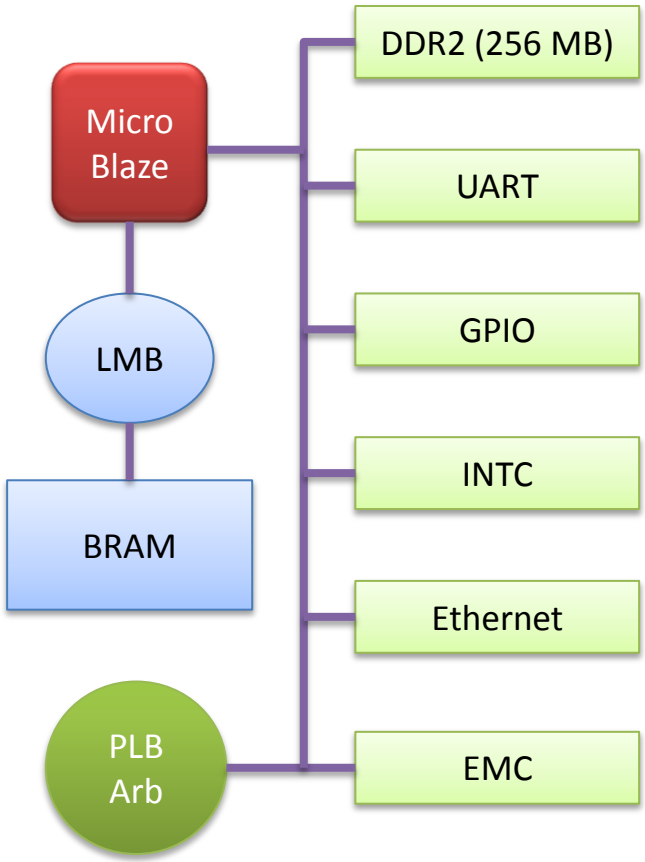
Genesys Initial BSB Hardware

- The Genesys MicroBlaze design hardware includes:
  - DDR2 Interface (256 MB)
  - BRAM
  - External Memory Controller (EMC)
    - 32MB Numonyx FLASH
  - Networking
  - UART (RS_232_UART_0, RS_232_UART_1)
  - Interrupt Controller
  - GPIO (Switches, LEDs and Pushbuttons)
  - PLB Arbiter

Genesys BSB System



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Using the Pre-Built Design (1)

- Unzip **Genesys_ip_cores.zip** and locate pre-built bitstream files:
  - **Genesys_ip_cores/implementation/system.bit**
  - **Genesys_ip_cores/implementation/download.bit** (BRAM is loaded with the TestAppMemory application)

- Also locate the pre-built Hardware Specification File for SDK:
  - **Genesys_ip_cores/SDK/SDK_Export/hw/system.xml**

- Locate pre-built executable software files:
  - **Genesys_ip_cores_UCF_SDK/SDK/SDK_Workspace/Audio_Demo/Debug/Audio_Demo.elf**
  - **Genesys_ip_cores_UCF_SDK/SDK/SDK_Workspace/LCD_Demo/Debug/LCD_Demo.elf**
  - **Genesys_ip_cores_UCF_SDK/SDK/SDK_Workspace/PS2_Demo/Debug/PS2_Demo.elf**
  - **Genesys_ip_cores_UCF_SDK/SDK/SDK_Workspace/TFT_Demo/Debug/TFT_Demo.elf**
  - **Genesys_ip_cores_UCF_SDK/SDK/SDK_Workspace/USB_EPP_Demo/Debug/USB_EPP_Demo.elf**
  - **Genesys_ip_cores_UCF_SDK/SDK/SDK_Workspace/USB_HPI_Demo/Debug/USB_HPI_Demo.elf**

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Using the Pre-Built Design (2)

- Configure FPGA
  - Launch XPS project, Genesys_bsb_design/system.xmp
  - From the menu, select "**Project**" → "**Launch EDK Shell**" and type:
    - **impact –batch etc/download.cmd**
  - Go to Slide 56 to run SDK and the software applications
- For a tutorial on how to create the contents of the **Genesys_ip_cores.zip** continue to the next slide

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Create a Base System

- Create a Base System for the Genesys Board, similar to the one described in the Base System Guide: **Genesys_BSB_Guide.pdf**
  - Use **64KB BRAM** (Look at Slide 17 in Genesys_BSB_Guide)
  - Set "**HARD_ETHERNET_MAC**" to use **DMA** and **Interrupt** (Look at Slide 18 in Genesys_BSB_Guide)
  - Set both UART core types to **xps_uart16650** (Look at Slide 19 in Genesys_BSB_Guide)
  - Enable both instruction and data cache memory (recommended)

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Add and Configure Standard IP

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Add Standard IP

- The maximum number of slaves on a **PLB bus** is 16
  - Assuming that all of the peripherals were used in **Base System Builder**, the actual number of **PLB slaves** is 10
  - There are five peripherals to add, therefore all of them could fit in the maximum number of slaves
  - However, taking into account that **PLB slaves** use OR logic on the data bus it results that increasing the number of slaves also reduces PLB bus operation speed
- It is recommended to use one PLB bus for the high-speed peripherals such as **Ethernet_MAC**, interrupt controller and a separate bus for the low-speed devices such as **UART**, **PS2** etc
- On the other hand one port of the **xps_tft** core connects to the PLB bus as master and performs burst reads from the DDR2 memory
  - Therefore it is a good idea to connect the **xps_tft PLB master** interface to a separate **PLB bus**
- Taking into account the above considerations, in the following two **PLB buses** and a **PLB to PLB bus bridge** will be added

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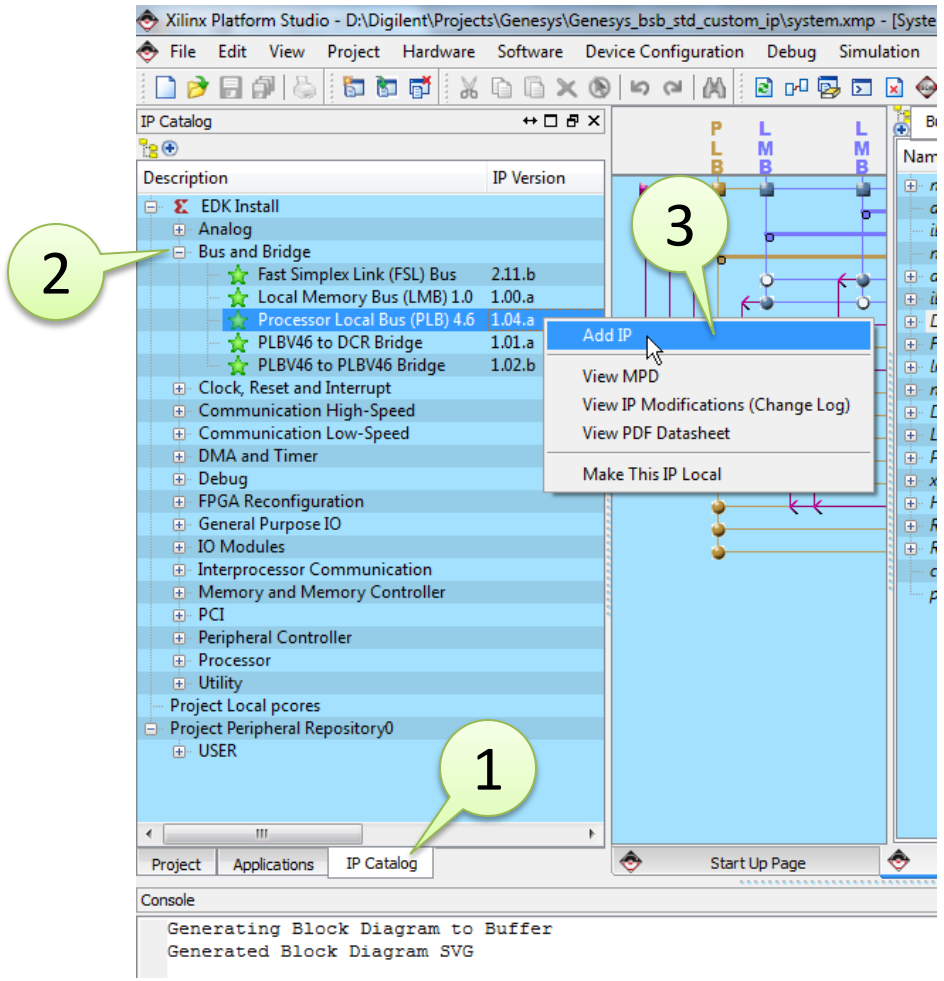
Add Standard IP: plbv46 Bus and Bridge

- In the Project window click on "**IP catalog**" tab (1), expand "**Bus and Bridge**" (2)
- Right-click on **Processor Local Bus (PLB) V4.6** and select "**Add IP**" (3)
- Add one more PLBV4.6 bus and a **PLBV46 to PLBV46 Bridge** (4)



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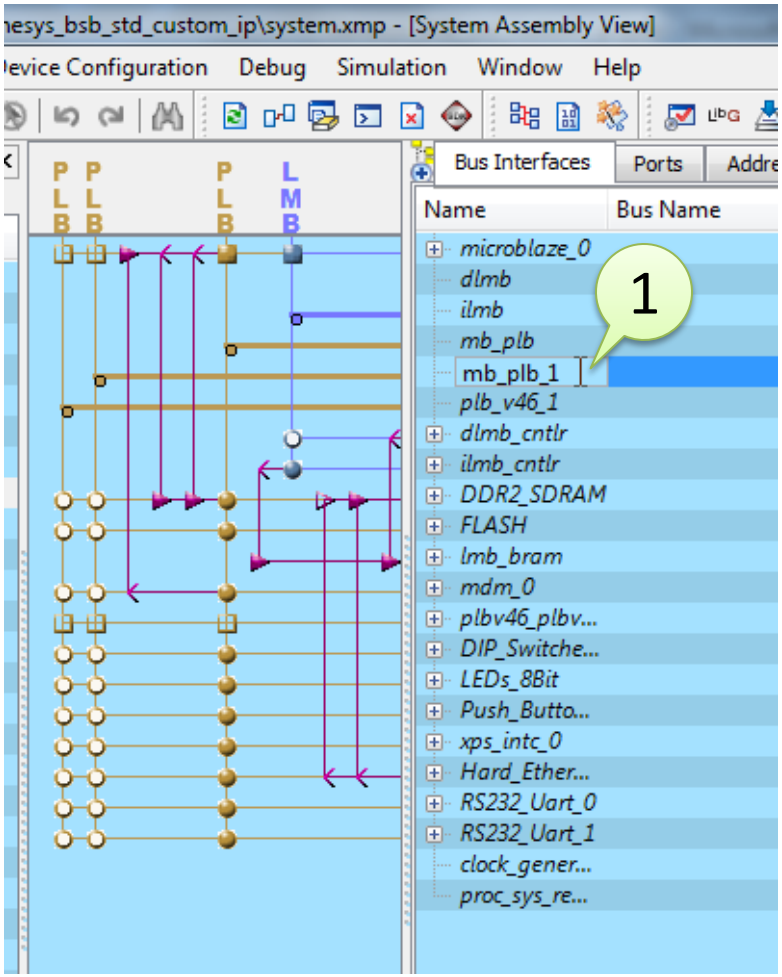
Add Standard IP: plbv46 Bus

- In the System Assembly view click on the second PLB bus name and rename it to **mb_plb_1** (1)
- Rename the third PLB bus to **mb_plb_2**



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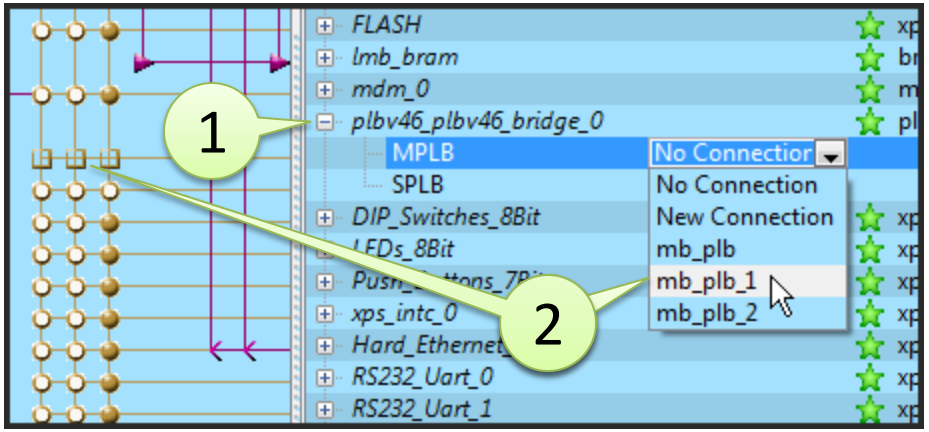
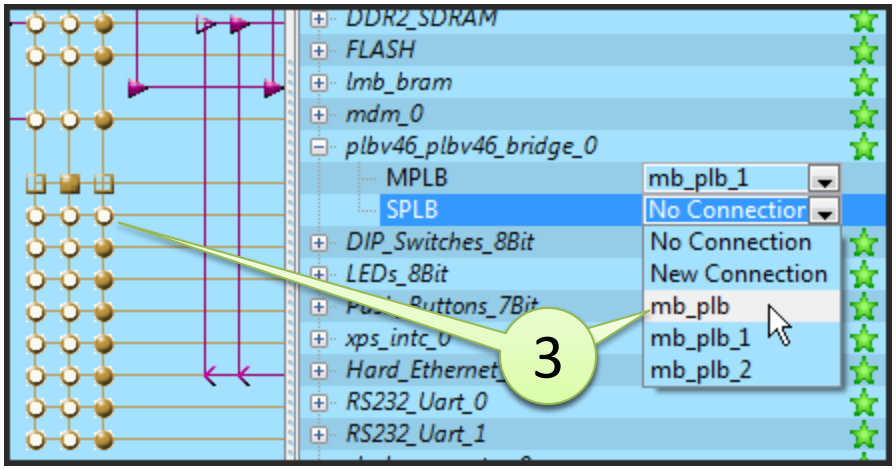
Connect plbv46 bridge

- Expand **plbv46_plbv46_bridge_0** bridge (1) and connect its Master Interface (MPLB) to **mb_plb_1** (2)
- Connect the bridge slave interface (SPLB) to **mb_plb** (3)





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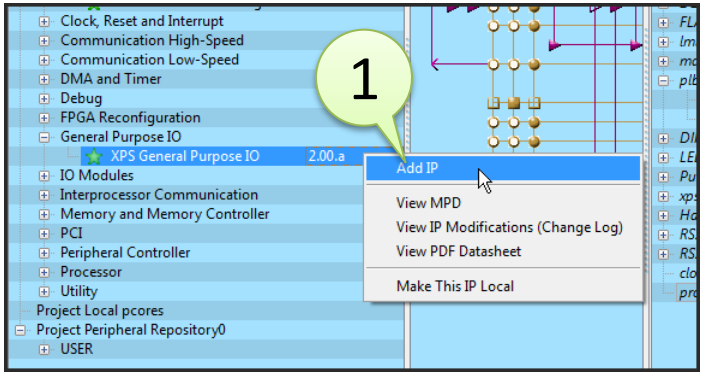
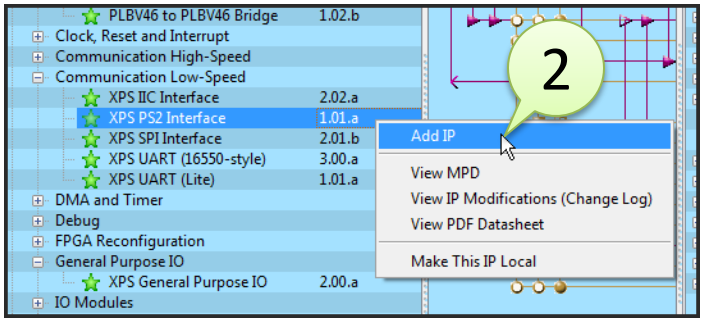
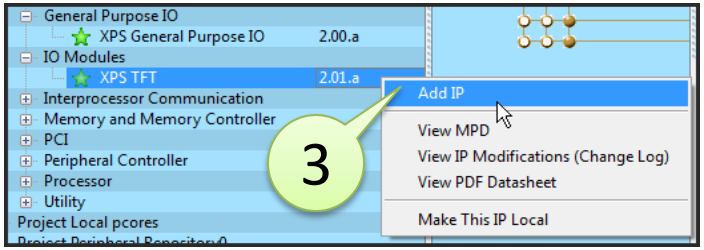
Add Standard IP: GPIO, PS2, TFT

- Expand "**General Purpose IO**" and add a "**XPS General Purpose IO**" (**xps_gpio**) module to the system (1)
- Expand "**Communication Low-Speed**" and add a "**XPS PS2 Interface**" (**xps_ps2**) module (2)
- Expand "**IO Modules**" and add a "**XPS TFT**" (**xps_tft**) module (3)







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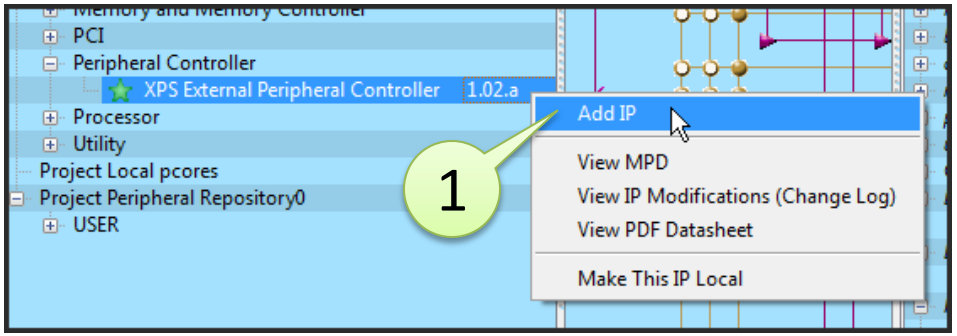
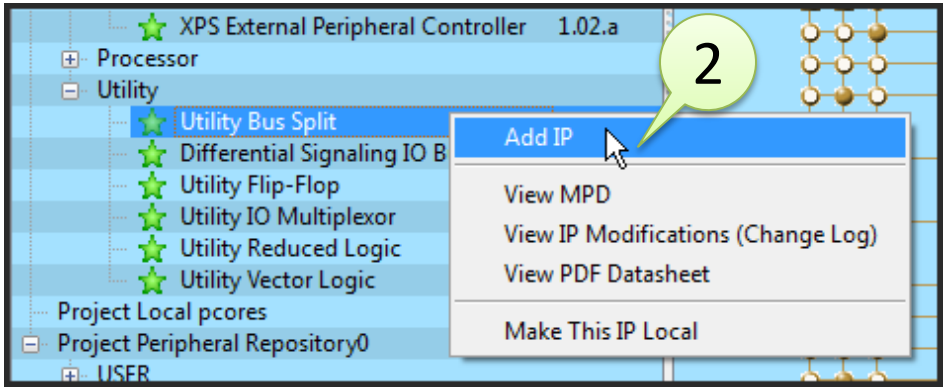
Add Standard IP: xps_epc and Bus Split

- Expand "**Peripheral Controller**" and add a **XPS External Peripheral Controller** (**xps_epc**) to the system (1)
  - Note: EDK will generate errors regarding the **xps_epc** parameters before the parameters are set. Ignore the errors until **xps_epc** is configured, at slides 24-28
- Expand "**Utility**" and add a "**Utility Bus Split**" (**util_bus_split**) the system (2)





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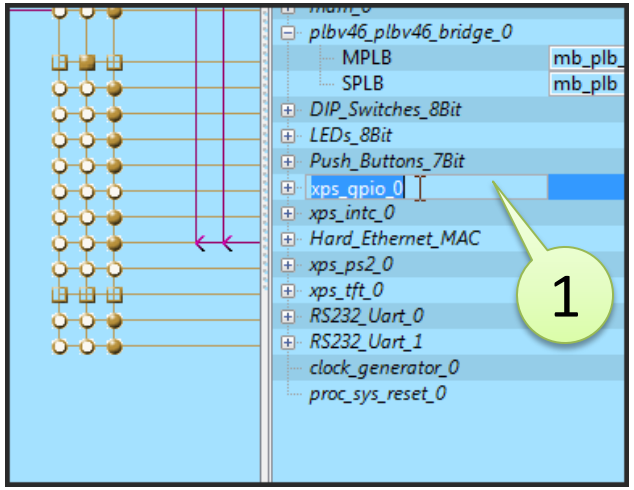
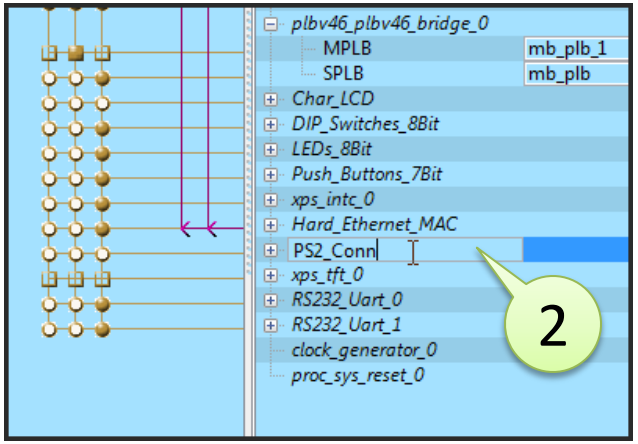
Add Standard IP: GPIO, PS2

- Rename the newly added **xps_gpio** peripheral to **Char_LCD** (1)
- Rename the **xps_ps2** peripheral to **PS2_Conn** (2)
- These are necessary to ensure that the .ucf file nets match with the system external port names





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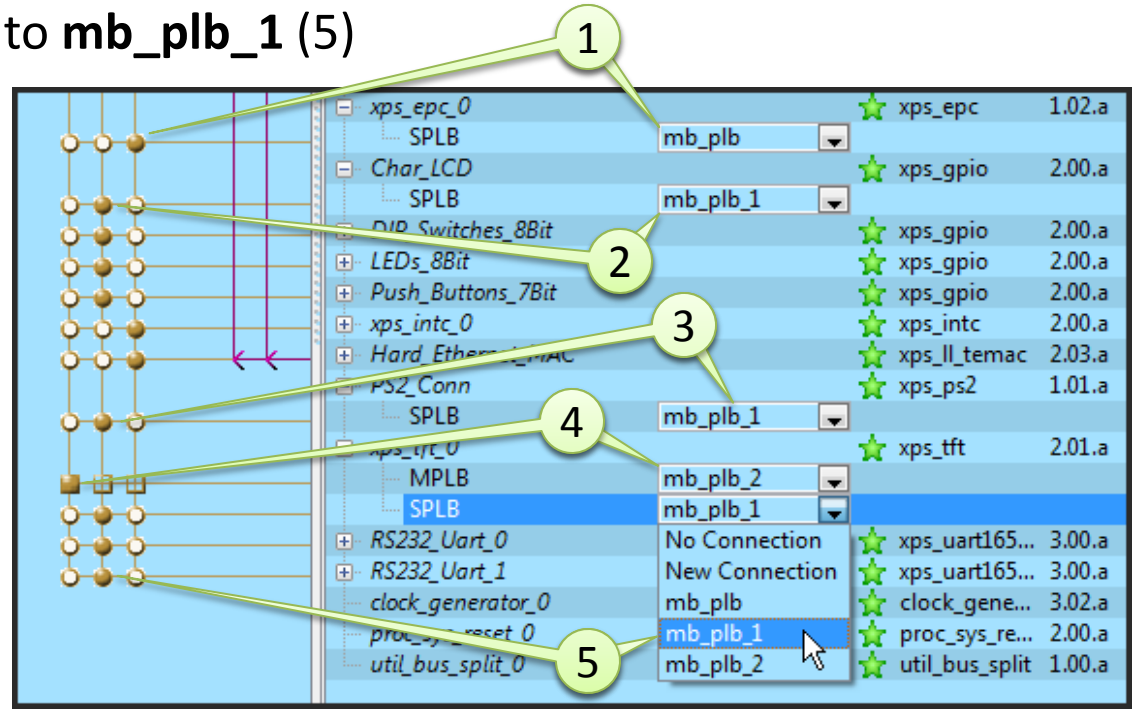
Add Standard IP: Bus connections (1)

- Connect **xps_epc_0** to **mb_plb** (1)
- Connect **Char_LCD** to **mb_plb_1** (2)
- Connect **PS2_Conn** to **mb_plb_1** (3)
- Connect the master interface of **xps_tft_0** to **mb_plb_2** (4) and the slave interface to **mb_plb_1** (5)



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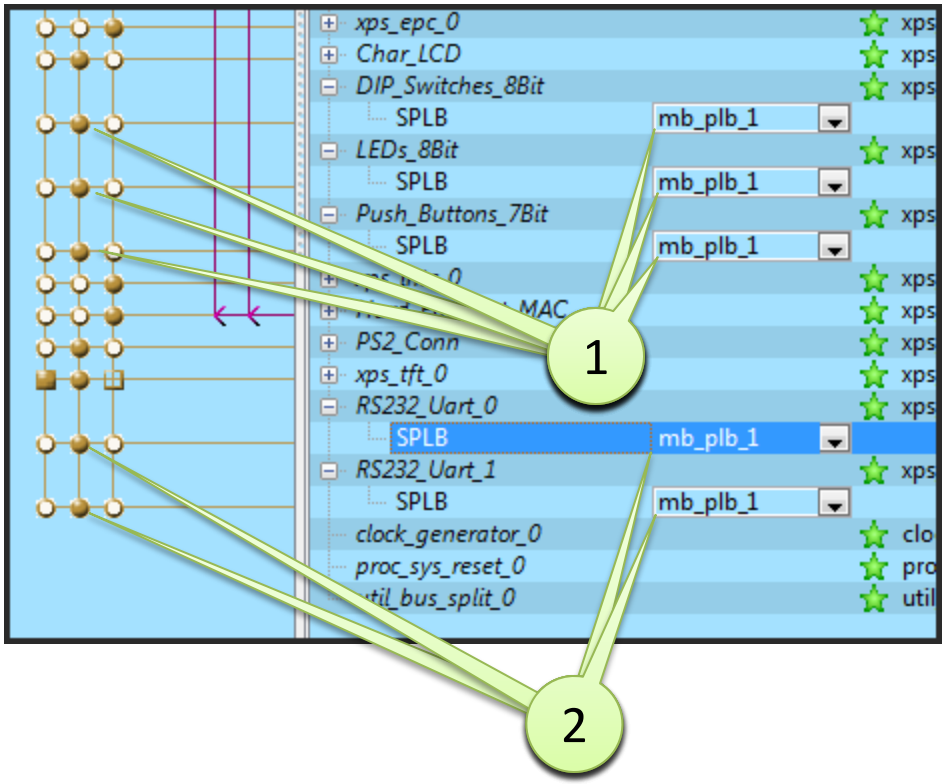
Add Standard IP: Bus connections (2)

- Optionally change the connection for the other GPIO peripherals (1) and the UART peripherals (2) from **mb_plb** to **mb_plb_1**
- In this way **mb_plb_1** contains low-speed peripherals only



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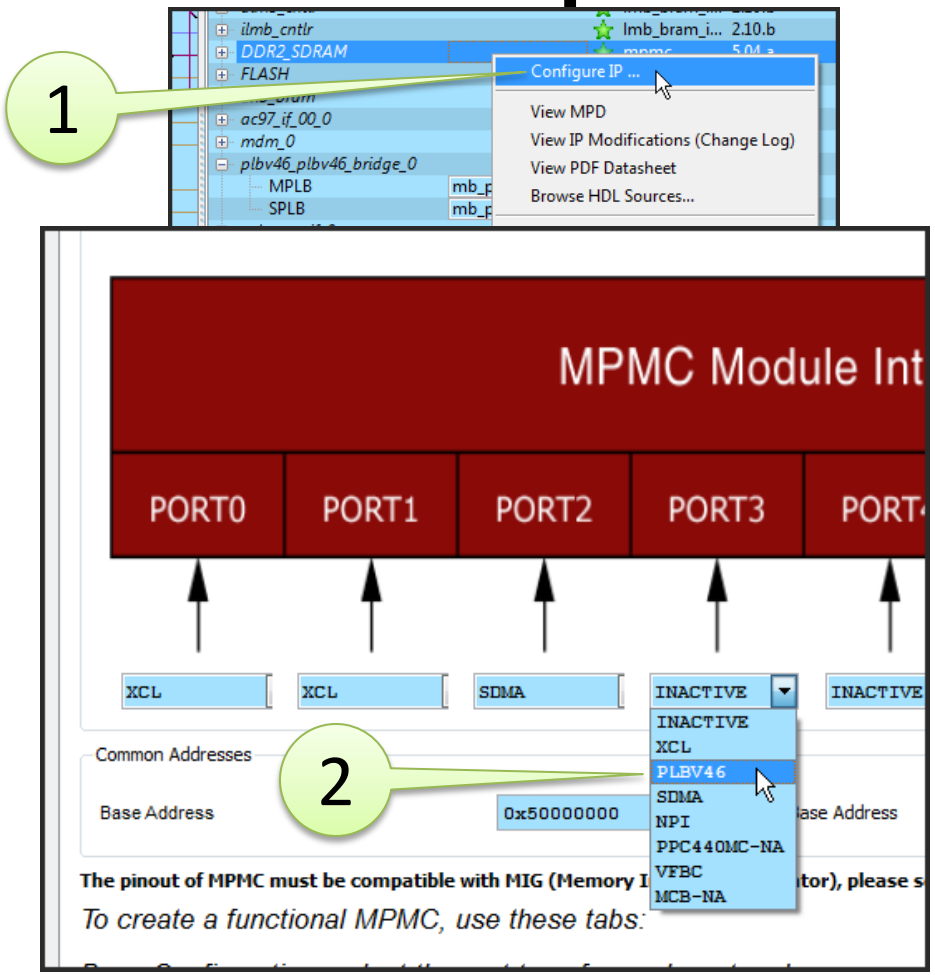
Add Standard IP: MPMC new port

- Right-click on the **DDR2_SDRAM** core and select "**Configure IP**" (1)
- In the next window activate one more port for the Multi-Port Memory Controller and select for the port type "**PLBV46**" (2)
- Click "**OK**" in the MPMC configuration window



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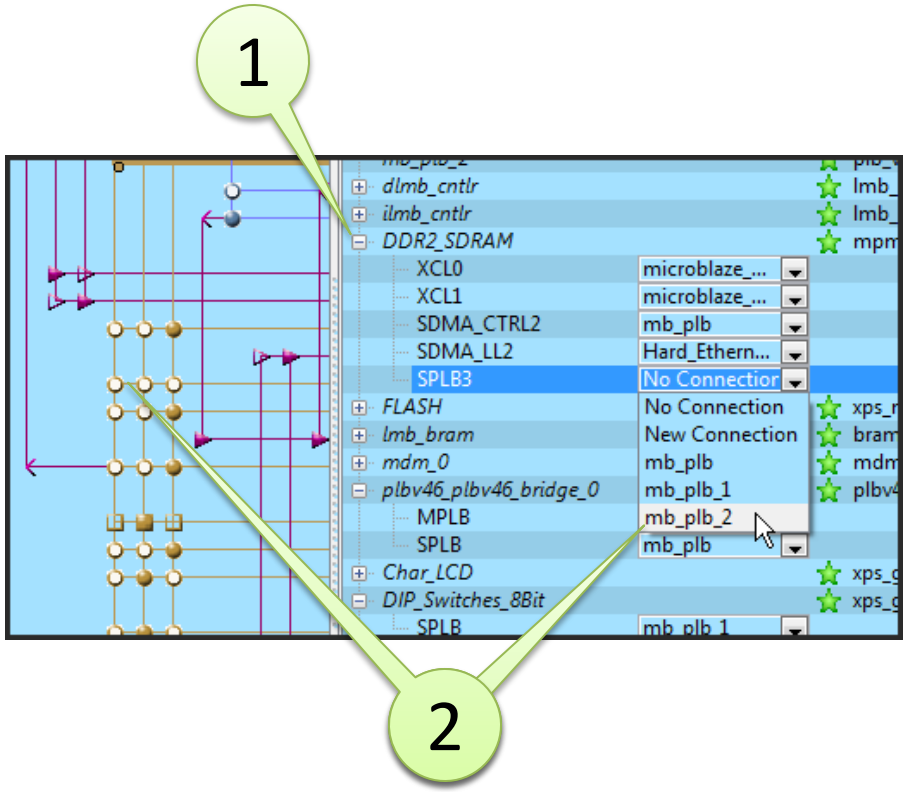
Add Standard IP: MPMC bus connection

- Expand **DDR2_SDRAM** (1) and connect the new port to **mb_plb_2** (2)
- In this way a separate bus connection is created between the **xps_tft** PLBV46 master interface and the DDR2 memory



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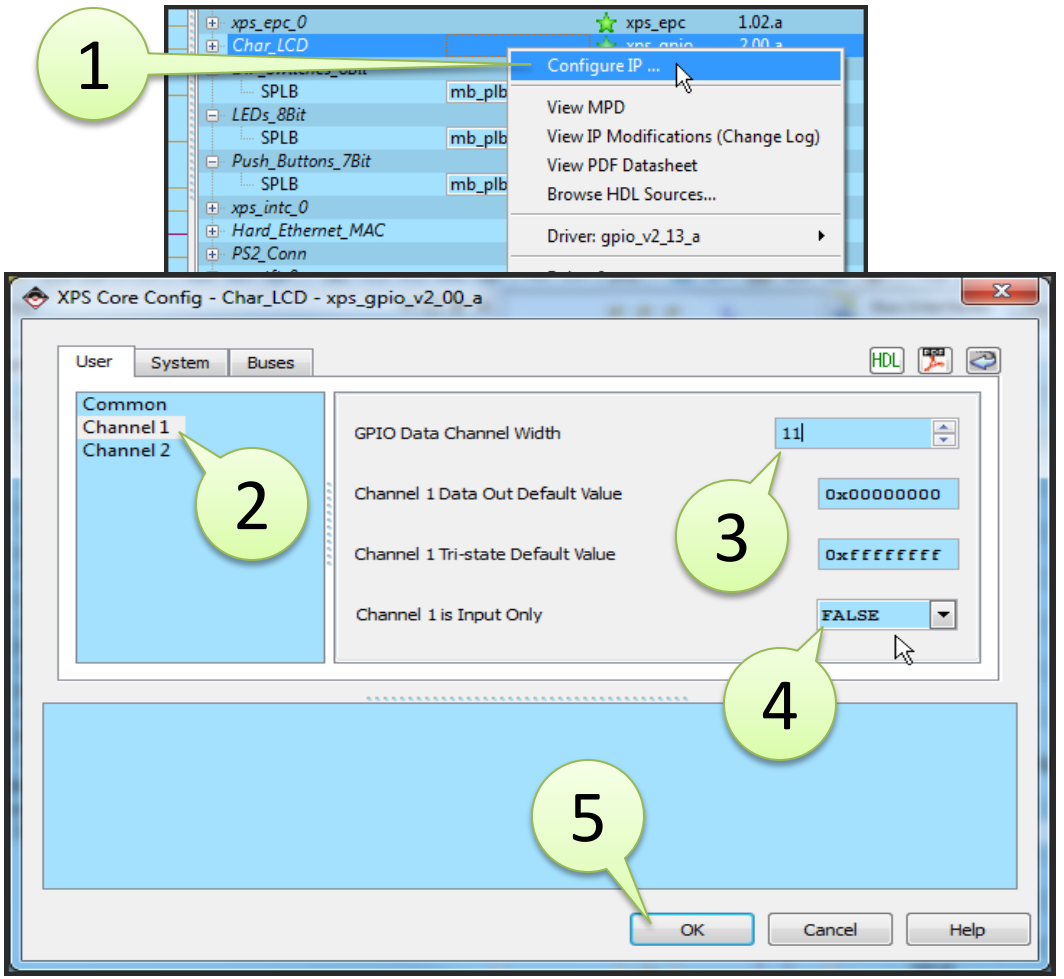
Add Standard IP: Configure LCD

- Right-click on the "**Char_LCD**" peripheral and select "**Configure IP**" (1)
- Select "**Channel 1**" (2)
- Set "**GPIO Data Channel Width**" to 11 (3)
  - The 11 bits represent the 8 data bits, the LCD-E (enable), LCD-RW (Read/Write) and LCD-RS (Reset) signals
- Check if the "**Channel 1 is Input only**" is set to "**FALSE**" (4)
- Click "**OK**" (5)



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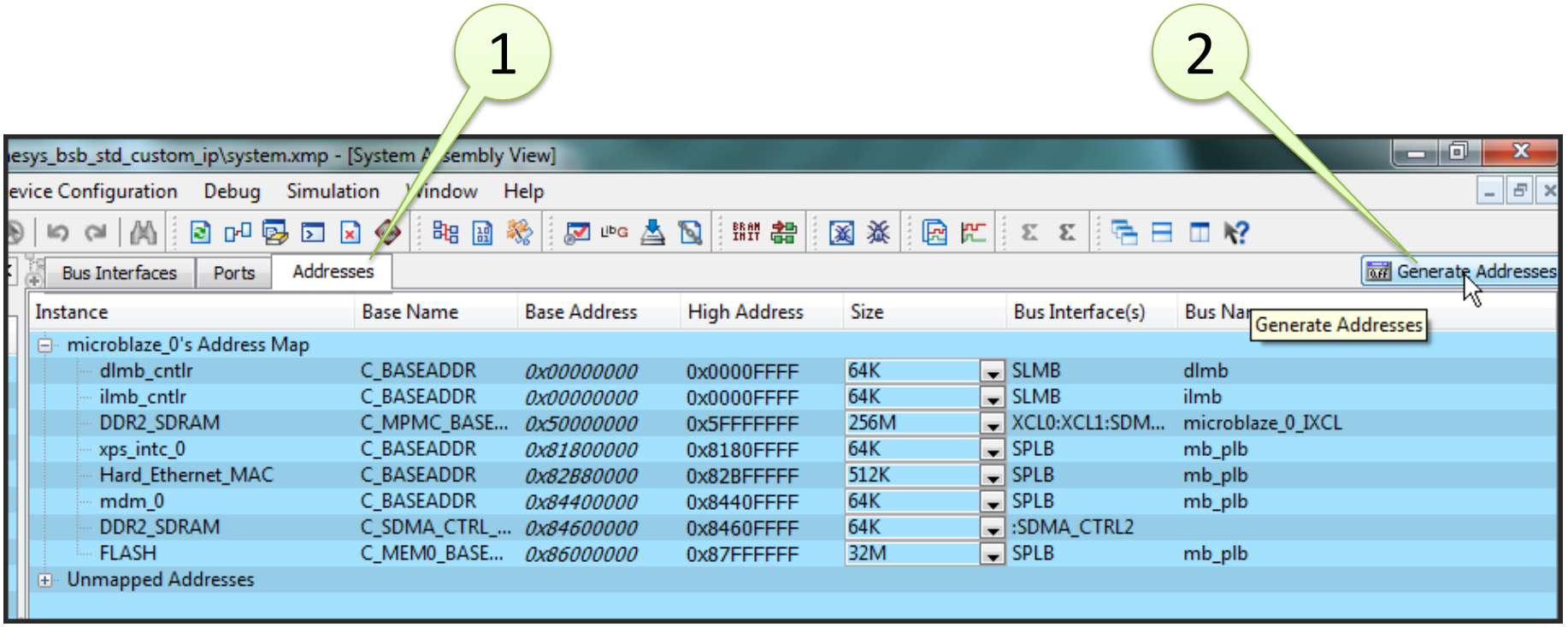
Add Standard IP: Generate Addresses

- Click on the "**Addresses**" tab in the **System Assembly View** (1) then click "**Generate Addresses**" (2)



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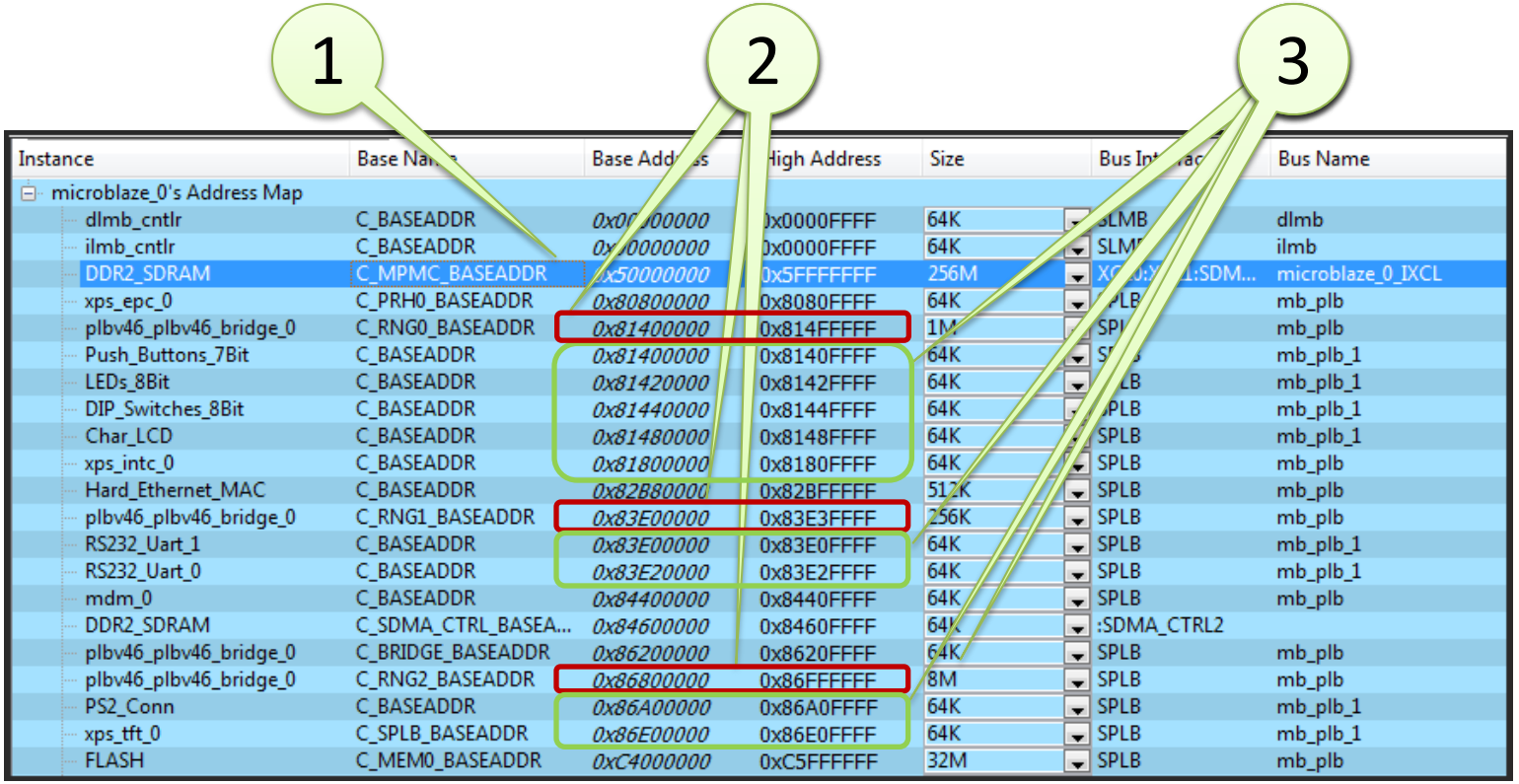
Add Standard IP: Generate Addresses

- Note the base address of the **DDR2_SDRAM** memory (1), in this case **0x50000000**
- Also note that all of the peripherals connecting to **mb_plb_1** having their addresses within the **plbv46_plbv46_bridge_0** range addresses (**C_RNG_0_BASEADDR – C_RNG_0_HIGHADDR**, **C_RNG_1_BASEADDR – C_RNG_1_HIGHADDR or C_RNG_2_BASEADDR – C_RNG_2_HIGHADDR**) (2), (3)



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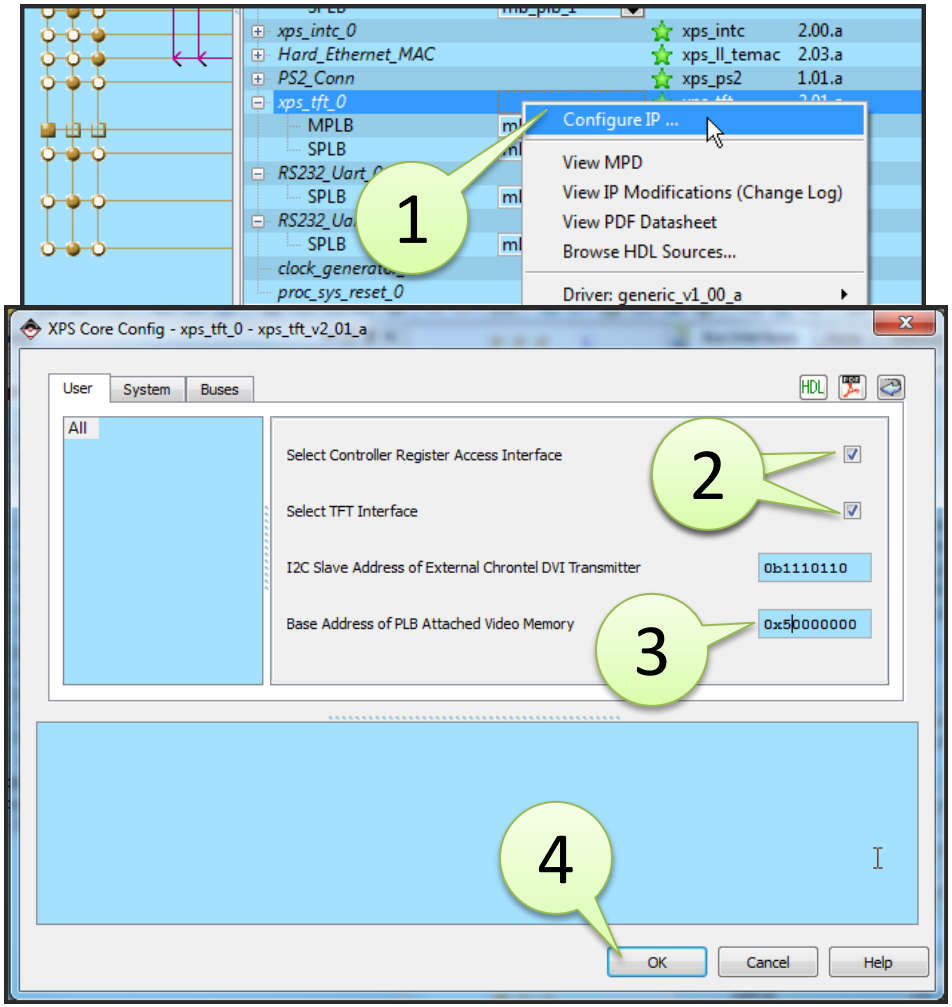
Add Standard IP: Configure xps_tft

- Right-click on the **xps_tft_0** peripheral and select "**Configure IP**" (1)
- In the next window, make sure that the "**Select Controller Register Address Interface**" and "**Select TFT Interface**" checkboxes are checked (2)
- Set the "**Base Address of PLB attached Video Memory**" parameter to the base address of the **DDR2_SDRAM** memory, in this case 0x50000000 (3)
- Click "**OK**" (4)



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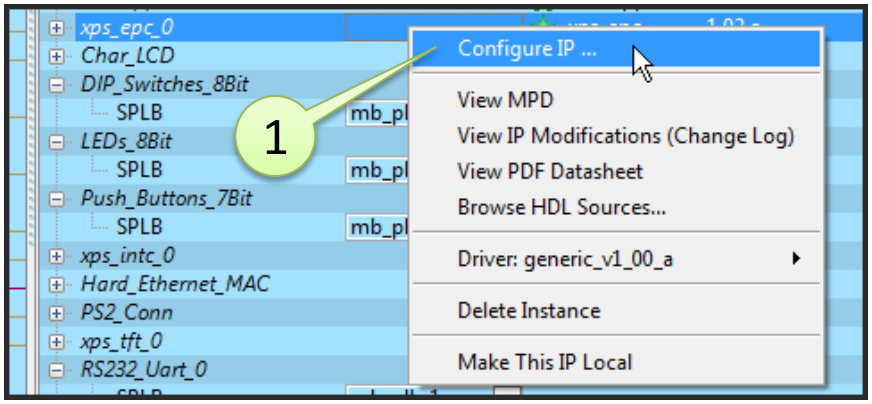
Add Standard IP: Configure xps_epc (1)

- Right-click on the **xps_epc_0** peripheral and select "**Configure IP**" (1)



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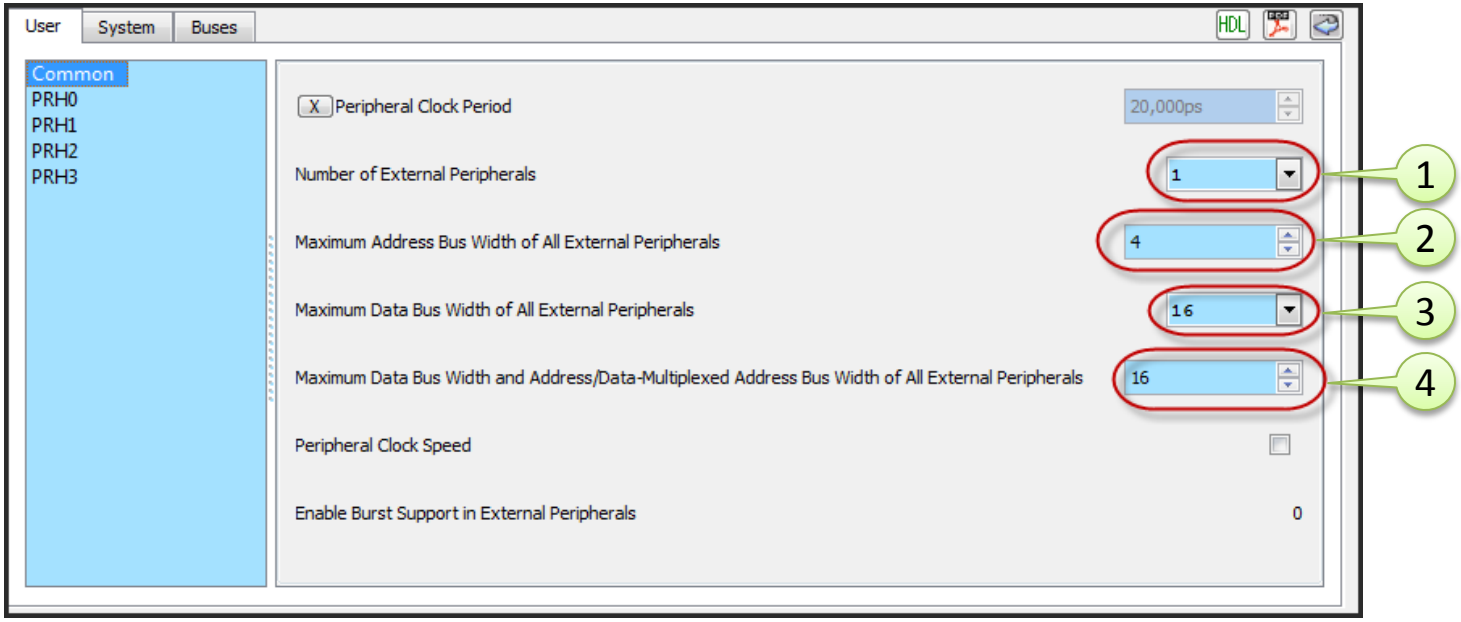
Add Standard IP: Configure xps_epc (2)

- In the next window, set the following parameters:
  - **Number of external Peripherals: 1** (1)
  - **Maximum Address Bus Width of All External Peripherals: 4** (2)
  - **Maximum Data Bus Width of All External Peripherals: 16** (3)
  - **Maximum Data Bus Width and Address/Data-Multiplexed Address Bus Width of All External Peripherals: 16** (4)



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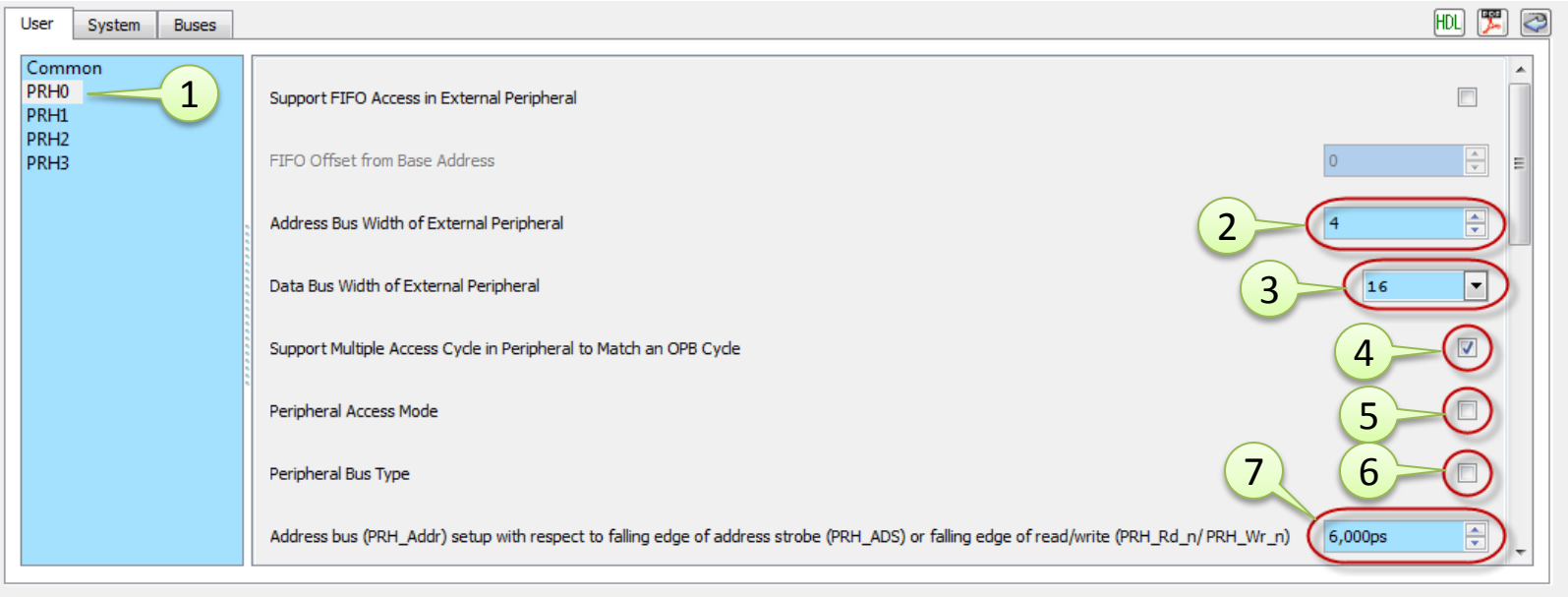
Add Standard IP: Configure xps_epc (3)

- (continued from previous slide) Click on "**PRH0"** (1) then set the following parameters
  - **Address Bus Width of External Peripheral: 4** (2)
  - **Data Bus Width of External Peripheral: 16** (3)
  - Check "**Support Multiple Access Cycle in Peripheral to Match an OPB Cycle"** (4)
  - Uncheck **"Peripheral Access Mode"** (5) and **"Peripheral Bus Type"** (6)
  - **Address bus (PRH_ADDR) setup with respect to falling edge of address strobe (PRH_ADS) or falling edge of read/write (PRH_Rd_n/PRH_Wr_n): 6000 ps**



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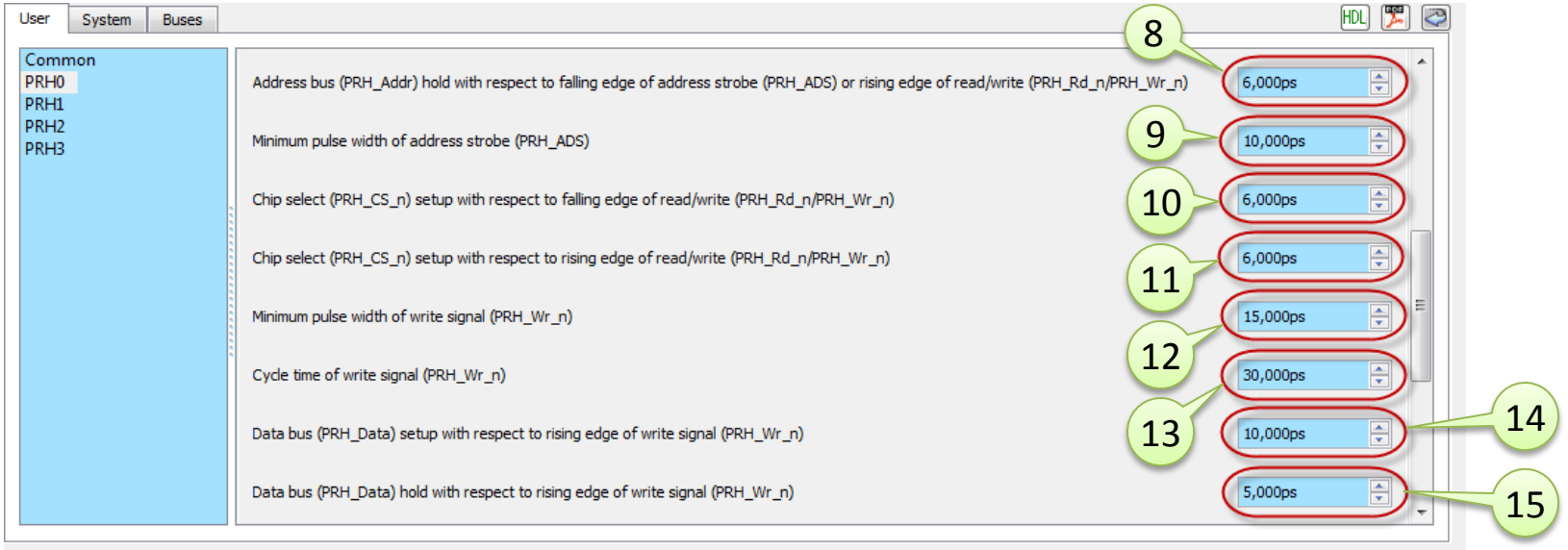
Add Standard IP: Configure xps_epc (4)

- (continued from previous slide)
  - **Address Bus (PRH_ADDR) hold with respect to falling edge of address strobe (PRH_ADS) or rising edge of read/write (PRH_Rd_n/PRH_Wr_n) : 6000 ps** (8)
  - **Minimum pulse width of address strobe (PRH_ADS): 10000 ps** (9)
  - **Chip select (PRH_CS_n) setup with respect to falling edge of read/write (PRH_Rd_n/PRH_Wr_n): 6000 ps** (10)
  - **Chip select (PRH_CS_n) setup with respect to rising edge of read/write (PRH_Rd_n/PRH_Wr_n): 6000 ps** (11)
  - **Minumim pulse width of write signal (PRH_Wr_n): 15000 ps** (12)
  - **Cycle time of write signal (PRH_Wr_n): 30000 ps** (13)
  - **Data bus (PRH_DATA) setup with respect to rising edge of write signal (PRH_Wr_n): 10000 ps** (14)
  - **Data bus (PRH_DATA) hold with respect to rising edge of write signal (PRH_Wr_n): 5000 ps** (15)



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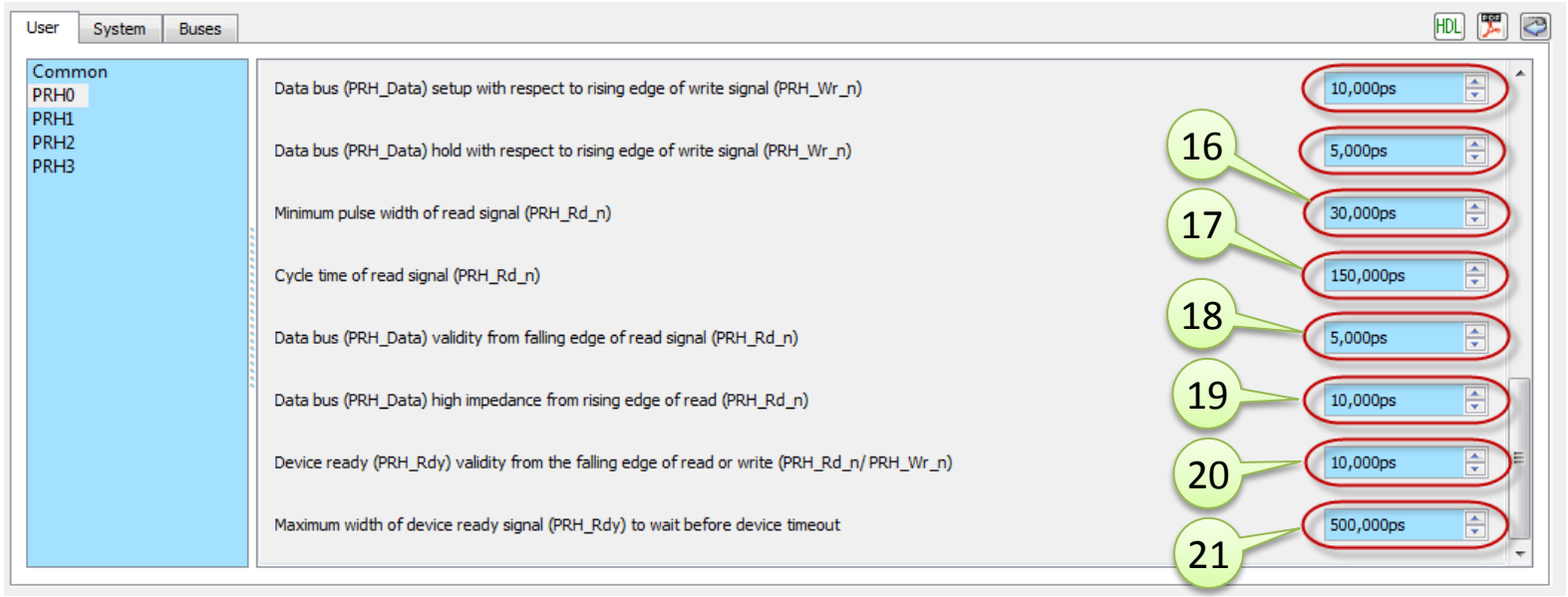
Add Standard IP: Configure xps_epc (5)

- (continued from previous slide)
  - **Minimum pulse width of read signal (PRH_Rd_n): 30000 ps** (16)
  - **Cycle time of read signal (PRH_RD_n): 150000 ps** (17)
  - **Data bus (PRH_Data) validity from falling edge of read signal (PRH_Rd_n): 5000 ps** (18)
  - **Data bus (PRH_Data) high impedance from rising edge of read (PRH_Rd_n): 10000 ps** (19)
  - **Device ready (PRH_Rdy) validity from the falling edge of read or write (PRH_Rd_n/PRH_Wr_n): 10000 ps** (20)
  - **Maximum width of device ready signal (PRH_Rdy) to wait before timeout: 500000 ps** (21)
- Click "**OK**" to close the configuration window



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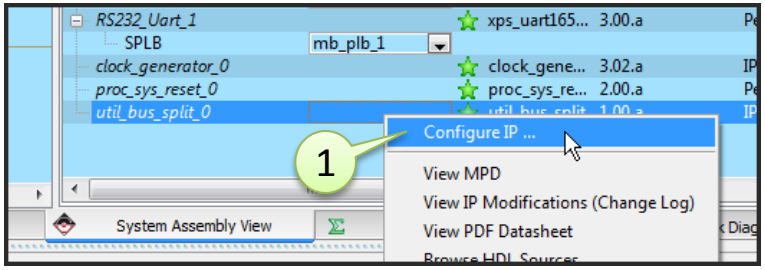
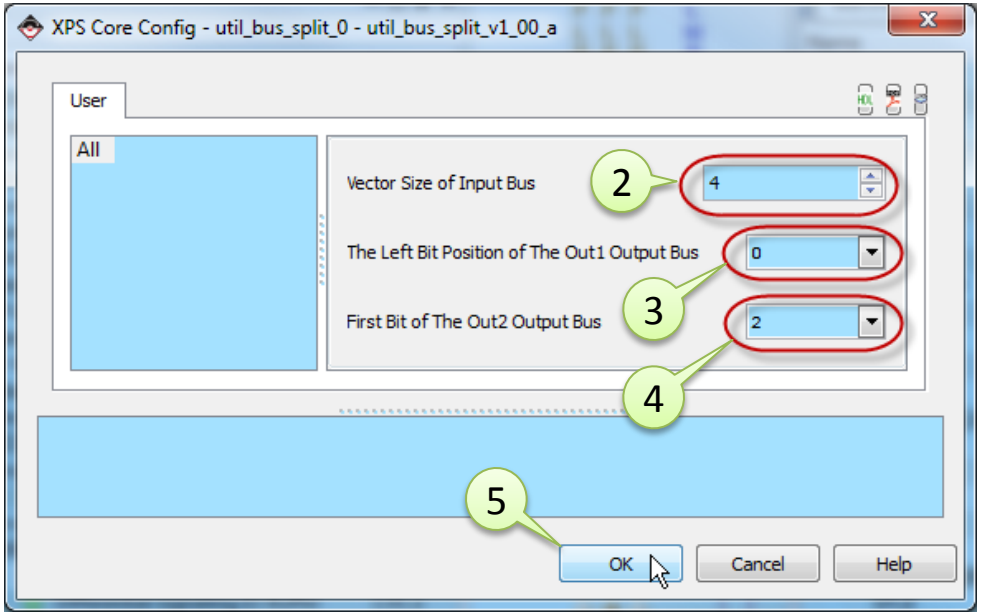
Add Standard IP: Configure Bus Split

- Right-click on the **util_bus_split_0** peripheral and select "**Configure IP**" (1)
- Set the following parameters:
  - **Vector size of Input Bus: 4** (2)
  - **The Left Bit Position of The Out1 Output Bus: 0** (3)
  - **First bit of The Out2 Output Bus: 2** (4)
- Click "**OK**" (5)





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Add and Configure Custom IP

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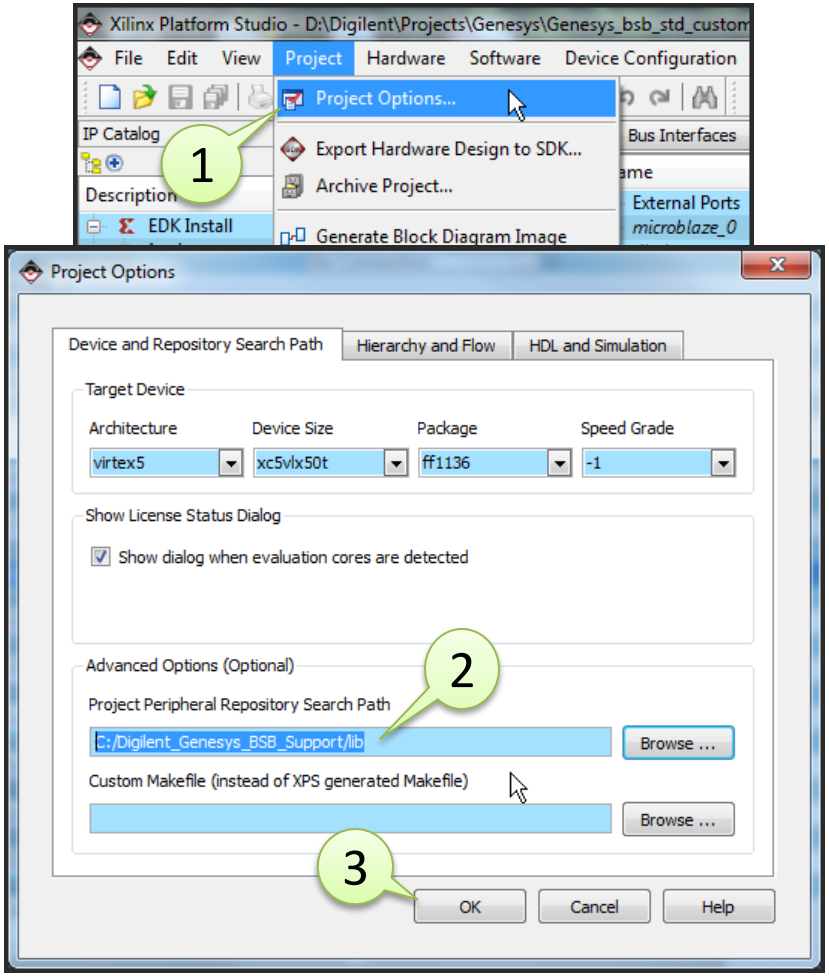
Add Custom IP: Peripheral Repository

- From the menu select "**Project**" -> "**Project Options**" (1)
- In the next window, make sure that the "**Project Peripheral Repository Search Path**"includes the path to the Genesys BSB Support files (2)
- Note: If the Base System was built using the BSB wizard and the Genesys BSB Support files then the "**Project Peripheral Repository**" Search path automatically includes the path to the Genesys BSB support files
- Click "**OK**" (3)



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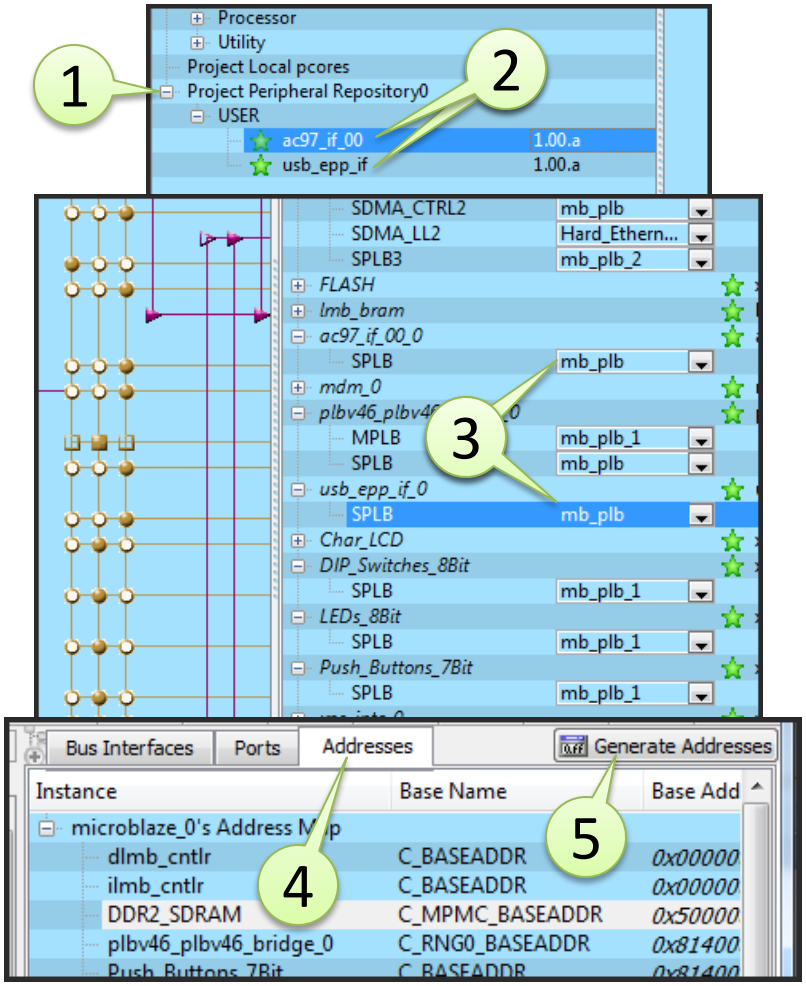
Add Custom IP: AC '97, USB_EPP

- From the **Project Window**, select the "**IP Catalog**" tab and expand the "**User**" group under "**Project Peripheral Repository0**" (1)
- Add a "**ac97_if_00**" and a "**usb_epp_if**" core to the system (2)
- Connect the cores to either the **mb_plb** or **mb_plb_1** bus (3) (If the cores will be connected to the **mb_plb** bus then the bus loading is more uniformized)
- Click on the "**Addresses**" tab in **System Assembly View** (4) then click "**Generate Addresses**" again (5)



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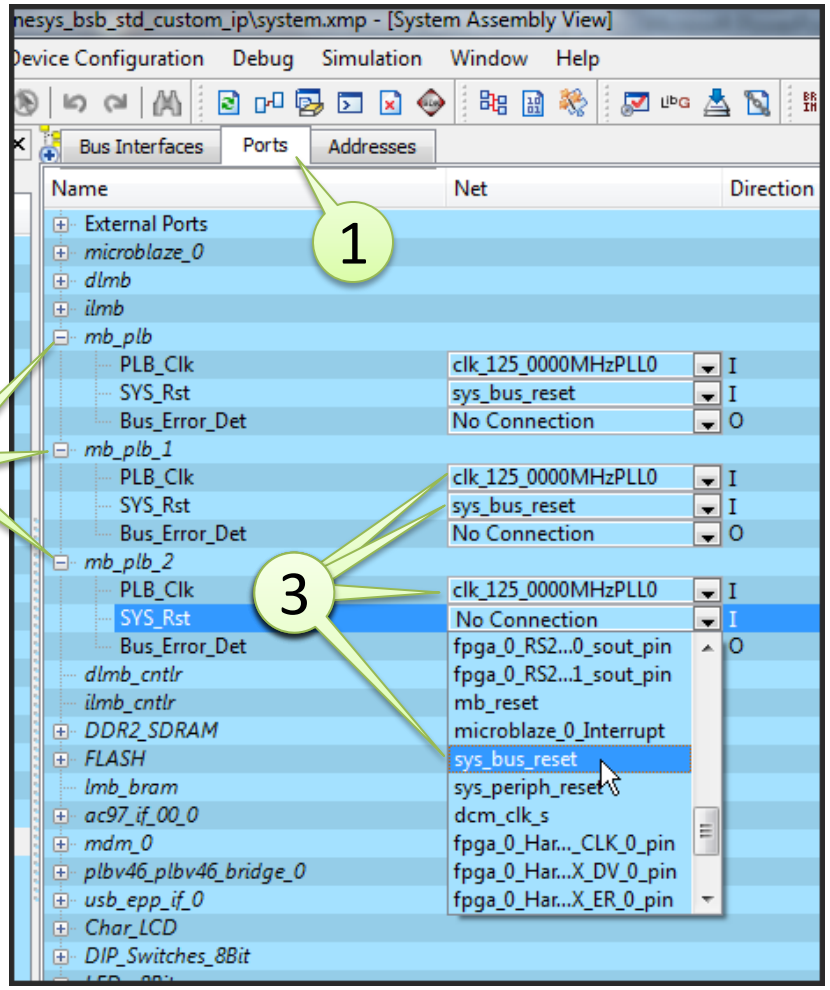
Make Port Connections: Bus clock and reset ports

- In **System Assembly View** click on the "**Ports**" tab (1)
- Expand "**mb_plb**", "**mb_plb_1**" and "**mb_plb_2**" (2)
- Connect "**PLB_Clk**" to "**clk_125_000MHzPLL0**" and "**SYS_Rst**" to "**sys_bus_reset**" for both "**mb_plb_1**" and "**mb_plb_2**", same as for "**mb_plb**" (3)



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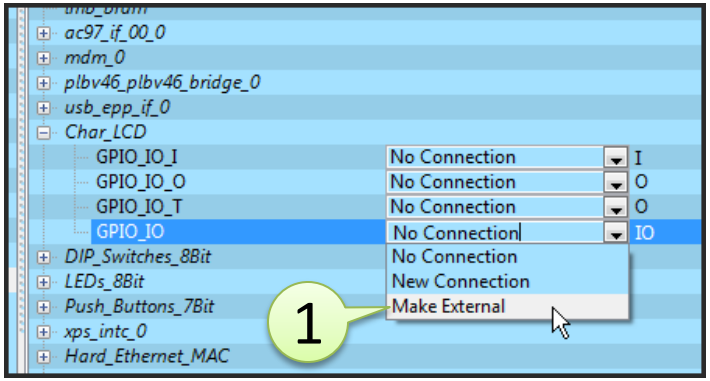
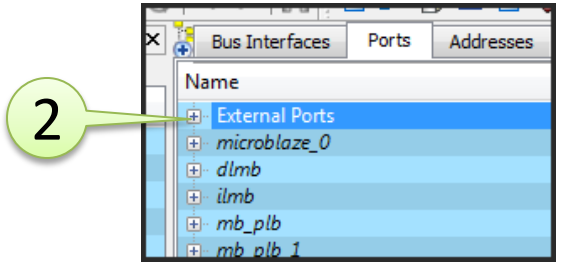
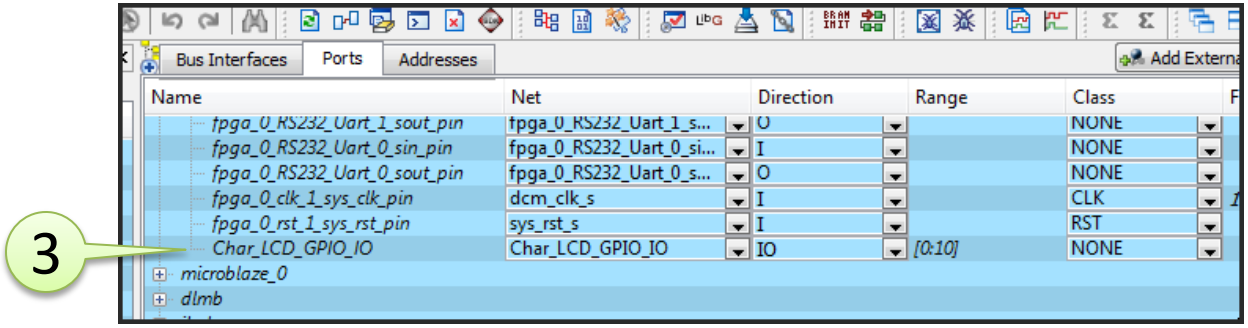
Make Port Connections: LCD

- Expand the "**External Ports**" group (1)
- Expand "**Char_LCD**" and make the "**GPIO_IO**" port external (2)
- Check for the newly created port in the "**External Ports**" group(3)







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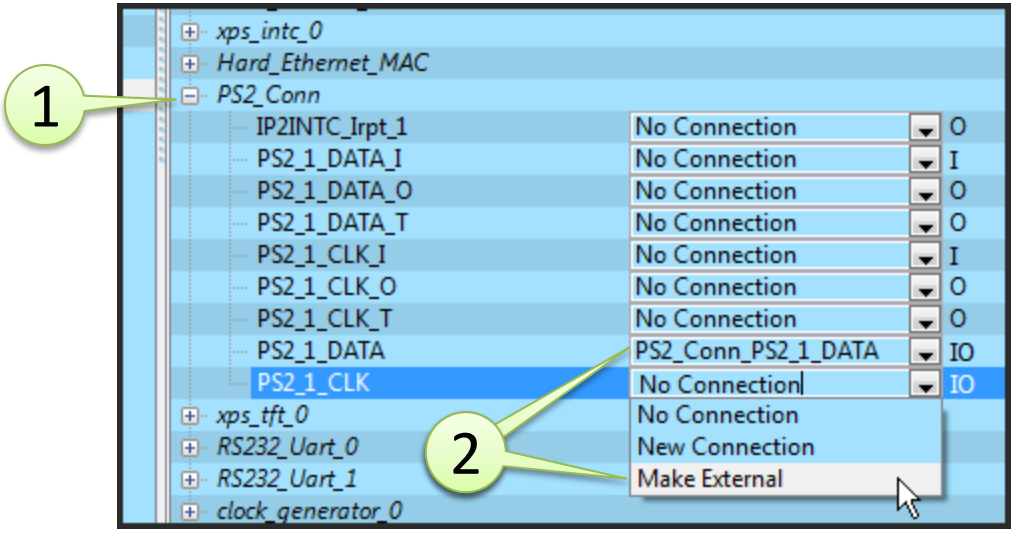
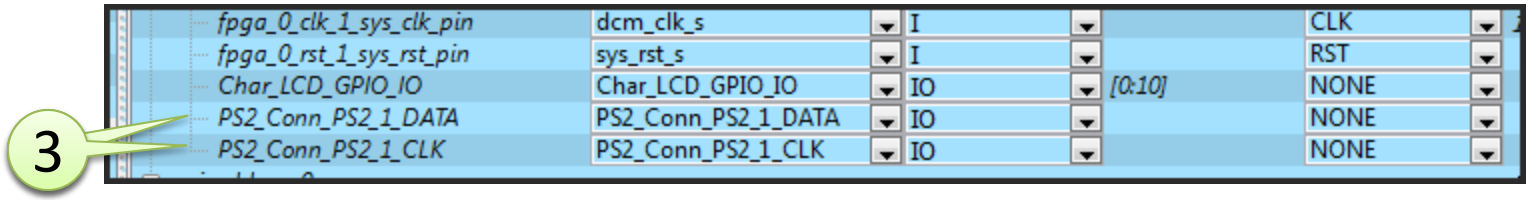
Make Port Connections: PS2

- Expand "**PS2_Conn**" (1)
- Make external the "**PS2_1_DATA**" and the **PS2_1_CLK** ports (2)
- Also check for the newly created ports in the "**External Ports**" group (3)





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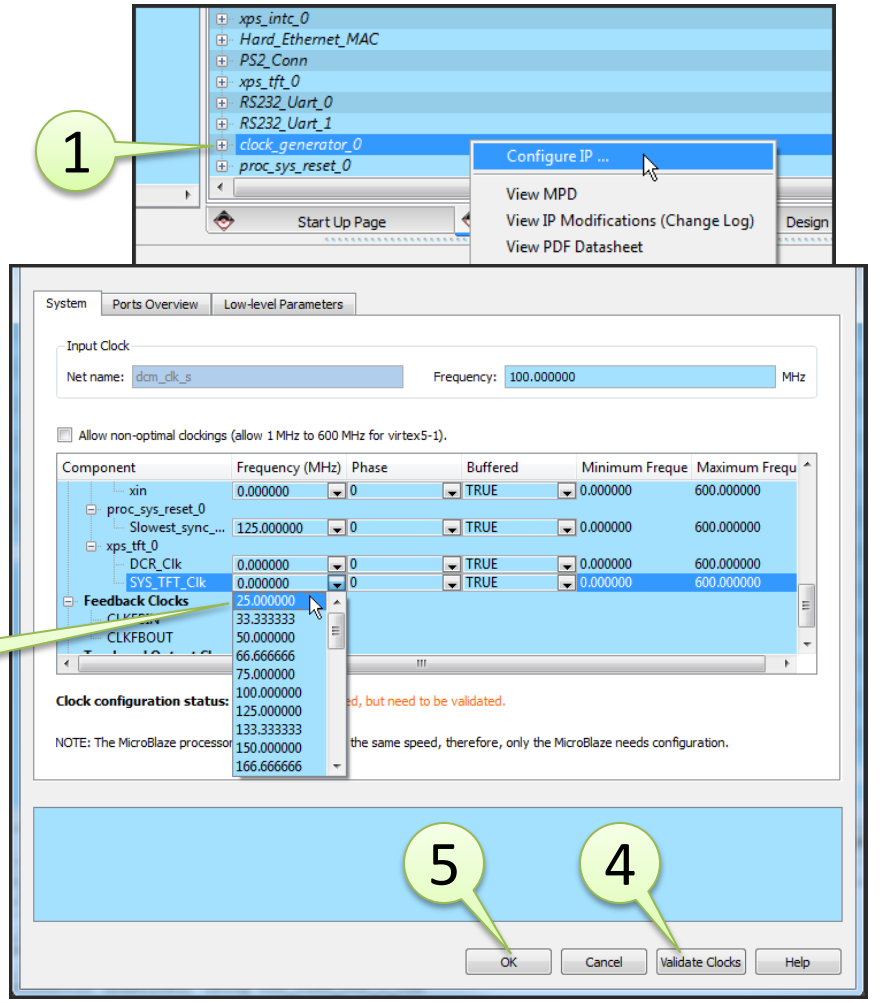
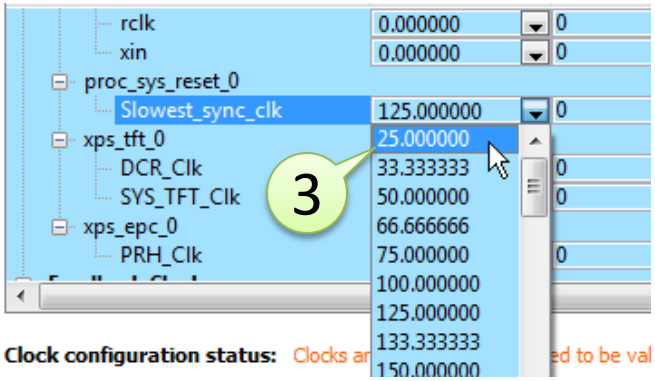
Make Port Connections: TFT Clock

- Right-click on the "**clock_generator_0**" IP core and select "**Configure IP**" (1)
- Scroll down to "**xps_tft_0**" and select for "**SYS_TFT_Clk**" 25 MHz (2)
- Scroll to "**proc_sys_reset_0**" and select "**Slowest_sync_clock**" to 25.00000 (3)
- Click "**Validate Clocks**" (4) then, after the clocks are validated, click "**OK**" (5)





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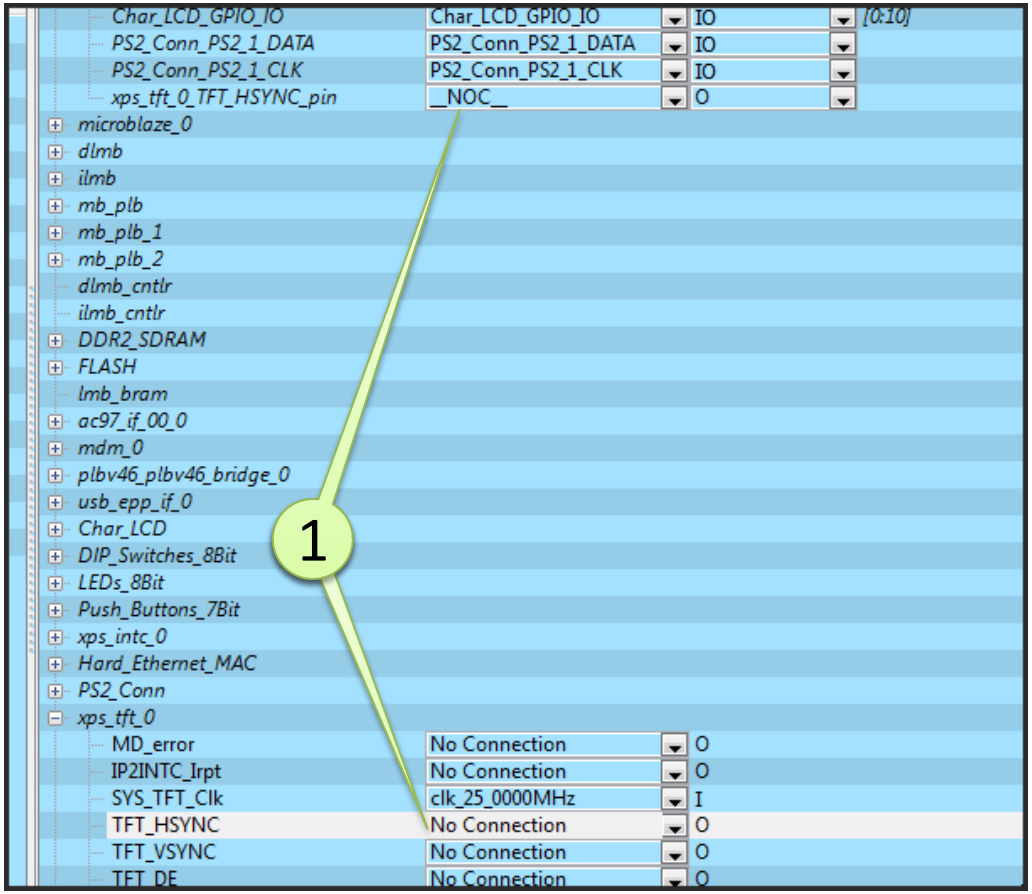
Output Port Connection Issue (1)

- Note: It might happen that EDK 11.3-11.4 does not automatically connect output signals (that were made external) to output pins
- Instead connects them to a "**__NOC__**" connection (1)
- Look to Xilinx Answer Record 33935 at http://www.xilinx.com/support/answers/33935.htm or follow the instructions on the next slide



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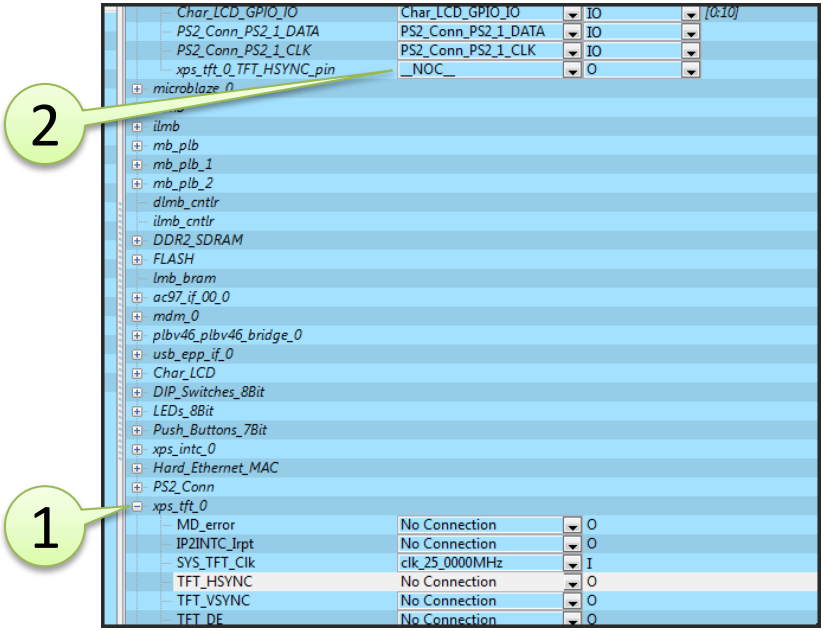
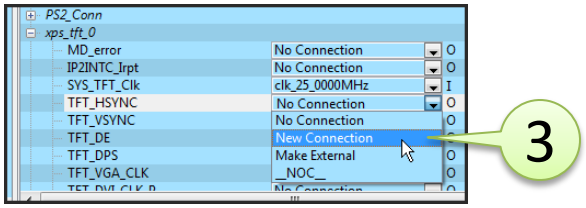
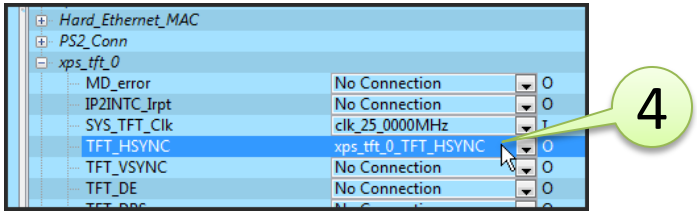
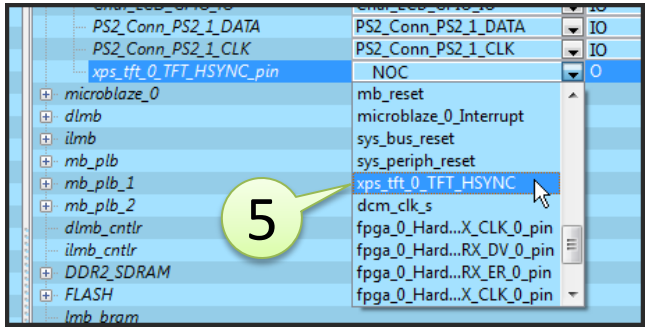
Output Port Connection Issue (2)

- Workaround example:
  - Expand "**xps_tft_0**" (1)
  - Make the "**TFT_HSYNC**" port external, if is not already made
  - Check for the "**__NOC__**" connection in the "External Ports group (2)
  - Open the net connection again and select "**New Connection**" (3), (4)
  - Connect the external port to the newly created connection either by selecting it from the list or by typing the net name manually (5)









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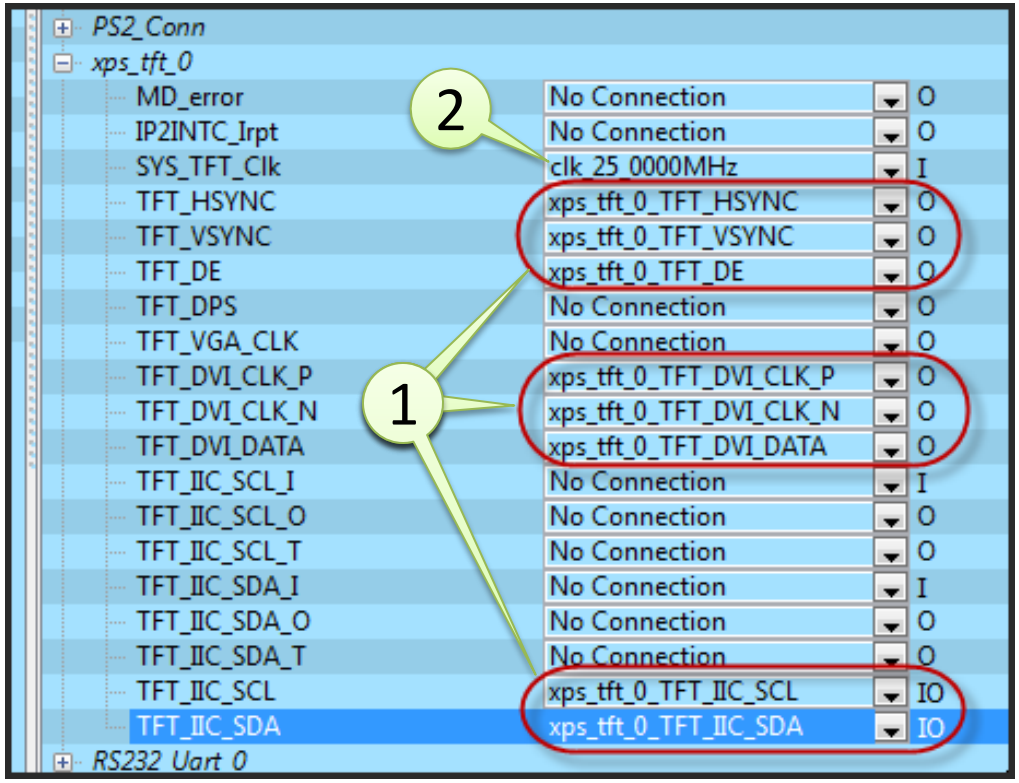
Make Port Connections: TFT

- Make external the following ports (1):
  - **TFT_HSYNC, TFT_VSYNC**
  - **TFT_DE**
  - **TFT_DVI_CLK_P, TFT_DVI_CLK_N**
  - **TFT_DVI_DATA**
  - **TFT_IIC_SCL, TFT_IIC_SDA**
- Check if "**SYS_TFT_Clk**" connects to "**clk_25_0000MHz**" (2). If doesn't then connect the port manually



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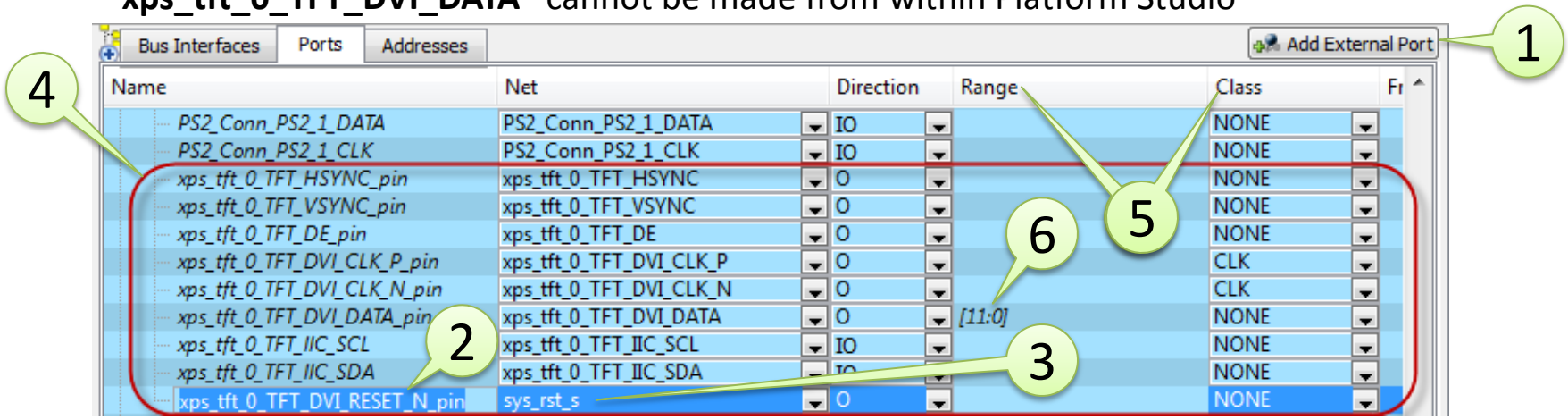
Make Port Connections: TFT Reset. Check External ports

- Add a new external port by clicking on the "**Add External Port**" button (1)
- Rename the newly created port to "**xps_tft_0_TFT_DVI_RESET_N_pin**" (2) and connect it to "**sys_rst_s**" (3). In this way the DVI transmitter reset signal is connected to the system reset
- Go to the "**External Ports"** group
  - Check for the TFT ports connections (4)
  - Check also for signal class and data width (range) (5). These can be changed in the "**External Ports"** group.
  - For example, the data range for the "**xps_tft_0_TFT_DVI_DATA_pin**" signal should be **[11:0]**. If this is missing then it has to be introduced manually (6), otherwise the connection to "**xps_tft_0_TFT_DVI_DATA**" cannot be made from within Platform Studio



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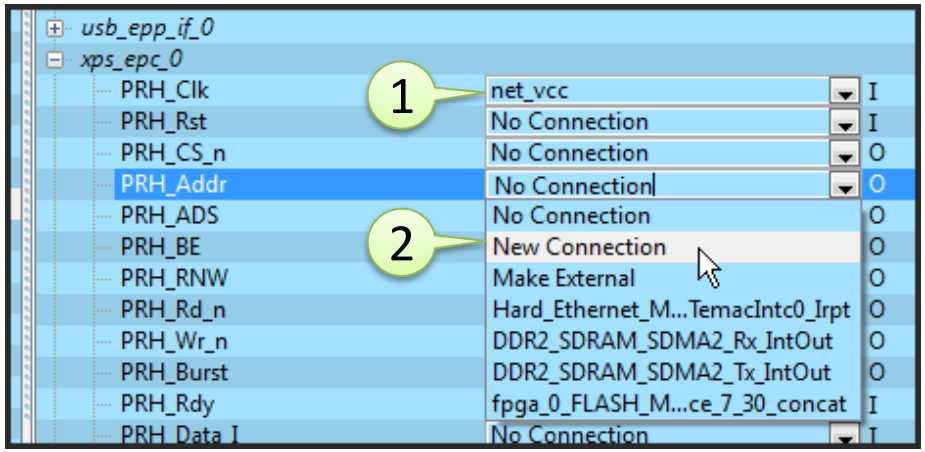
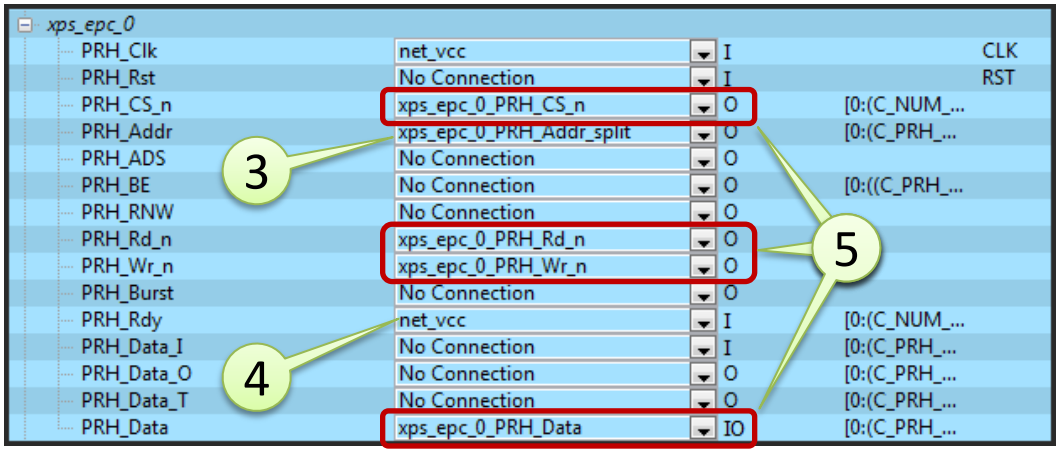
Make Port Connections: xps_epc

- Expand xps_epc_0 and make the following connections:
  - Connect "**PRH_Clk"** to "**net_vcc"** (1)
  - Right-click on the "**PRH_ADDR**" net connection and select "**New Connection**" (2)
  - By simply clicking twice on the new net connection and typing, rename it manually to "**xps_epc_0_PRH_Addr_split**" (3) in order to suggest that the address bus will split
  - Connect "**PRH_Rdy**" to "**net_vcc**" (4)
- Make external the following ports (5):
  - **PRH_CS_n**
  - **PRH_Rd_n**
  - **PRH_Wr_n**
  - **PRH_Data**





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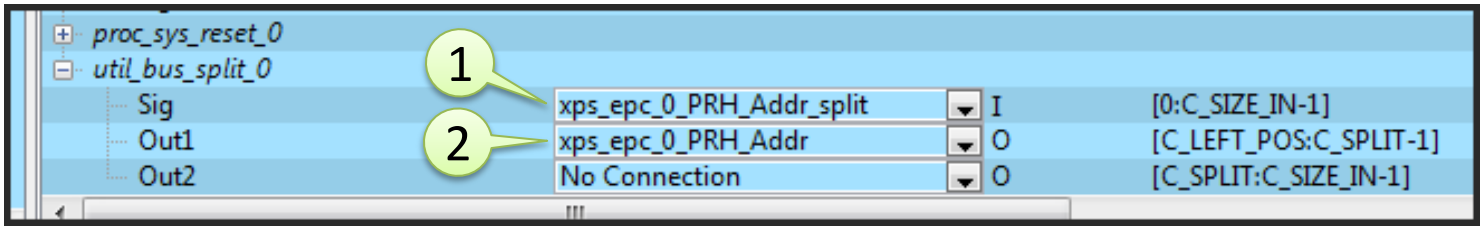
Make Port Connections: xps_epc Address bus

- Expand "**util_bus_split_0**" and make the following connections:
  - Connect "**Sig**" to the previously created "**xps_epc_0_PRH_Addr_split**" net (1)
  - Make external the "**Out1**" port. Name the net manually "**xps_epc_0_PRH_Addr**" (2)



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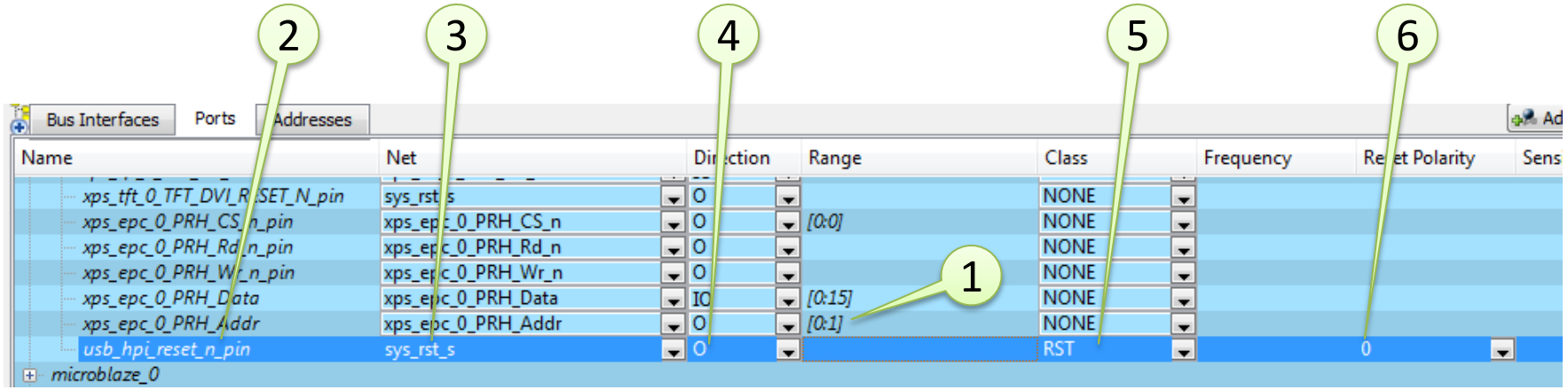
Make Port Connections: xps_epc Address and Reset

- Make sure that for the "**xps_epc_0_PRH_Addr**" output port the range is **[0:1]** (1). If not, change it to
- Add a new external port and name it to **usb_hpi_reset_n_pin** (2). Set the following parameters for the port:
  - Net: **sys_rst_s** (3)
  - Direction: **O** (4)
  - Class: **RST** (5)
  - Reset Polarity: **0** (6)



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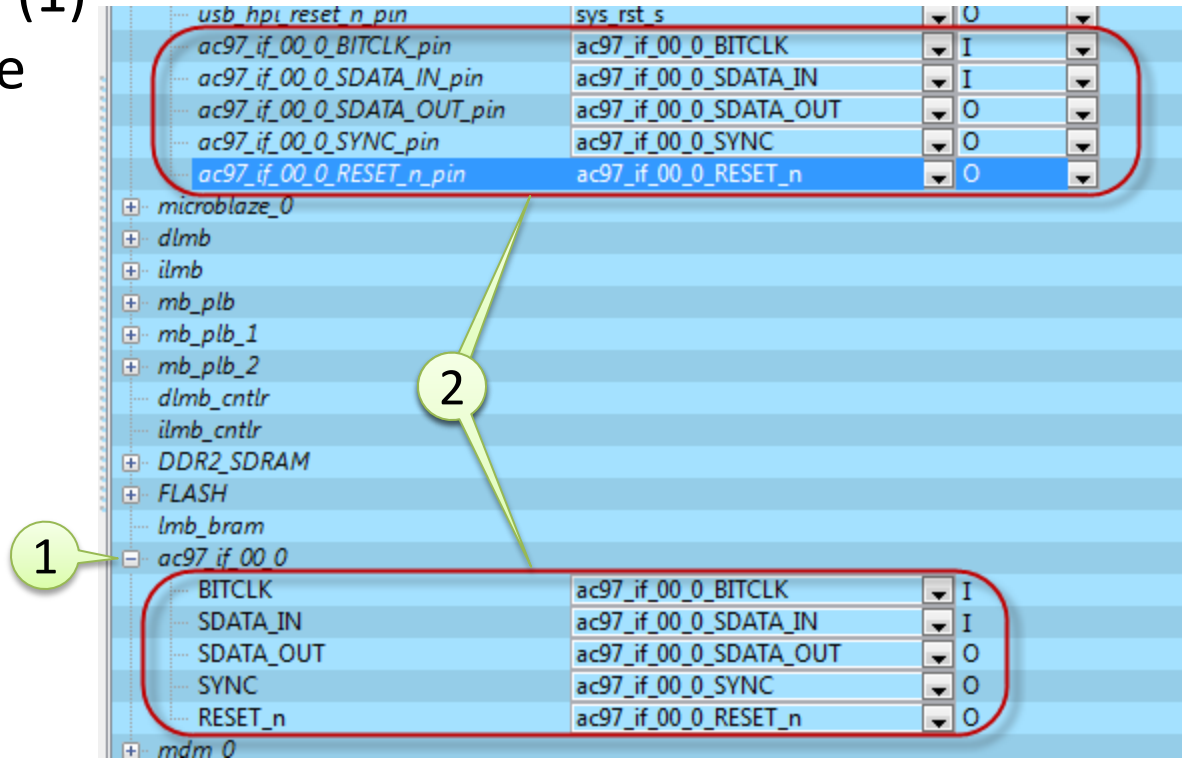
Make Port Connections: AC '97

- Expand **ac97_if_00_0** (1) and make external the following ports (2):
  - **BITCLK**
  - **SDATA_IN**
  - **SDATA_OUT**
  - **SYNC**
  - **RESET_n**



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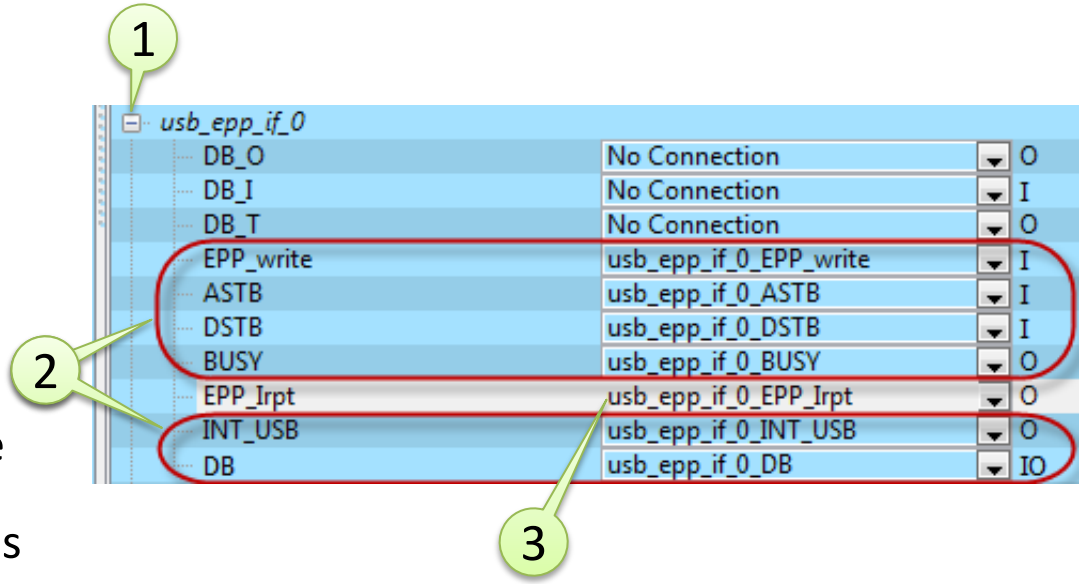
Make Port Connections: USB-EPP

- Expand "**usb_epp_if_0**" (1) and make external the following ports (2):
  - **EPP_write**
  - **ASTB**
  - **DSTB**
  - **BUSY**
  - **INT_USB**. Make sure that the signal class of the external port connecting to INT_USB is "**INTERRUPT**"
  - **DB**
- Create a new connection for the "**EPP_Irpt**" port (3)



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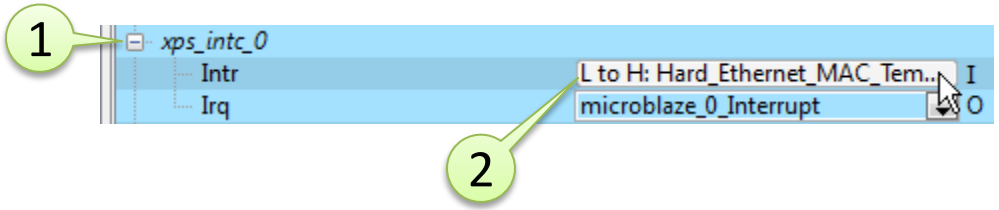
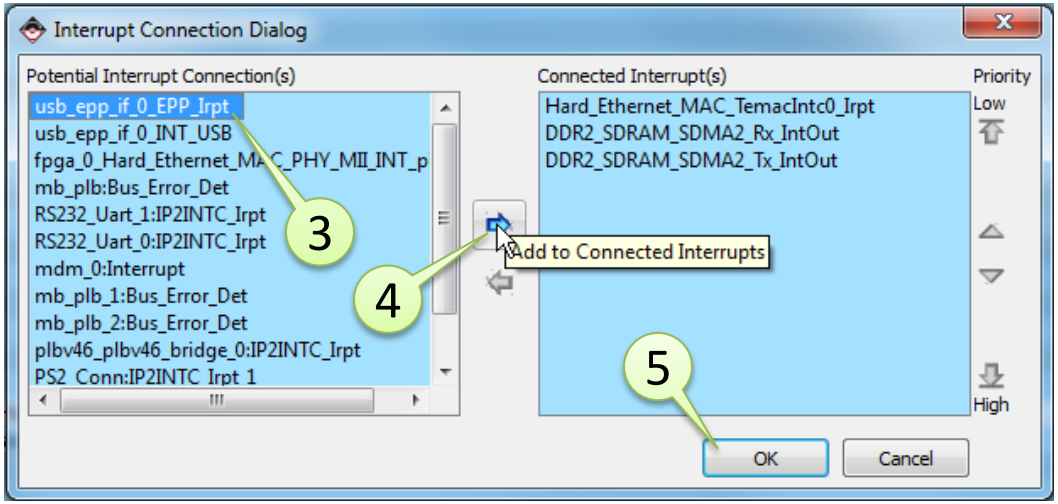
Make Port Connections: Connect USB-EPP interrupt

- If the Base System was built using interrupts for any peripheral, there is an interrupt controller, by default named "**xps_intc_0"**.
- If there is no interrupt controller, add one from the IP catalog and connect it to the "**mb_plb**" or "**mb_plb_1**" bus
- If the interrupt controller is added manually, then its "**Irq**" port has to be also manually connected to the **microblaze_0** microprocessor "**INTERRUPT**" port and the address map has to be generated again
- Expand "**xps_intc_0**" (1) and click on the net connection of the "**Intr**" port (2)
- In the next window select "**usb_epp_if_0_EPP_Irpt**" (3). Click on the "**Add**" button (4), then click "**OK**" (5)





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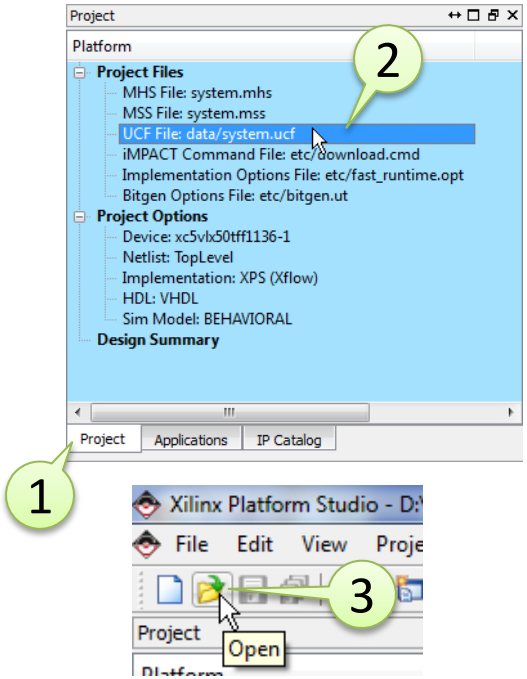
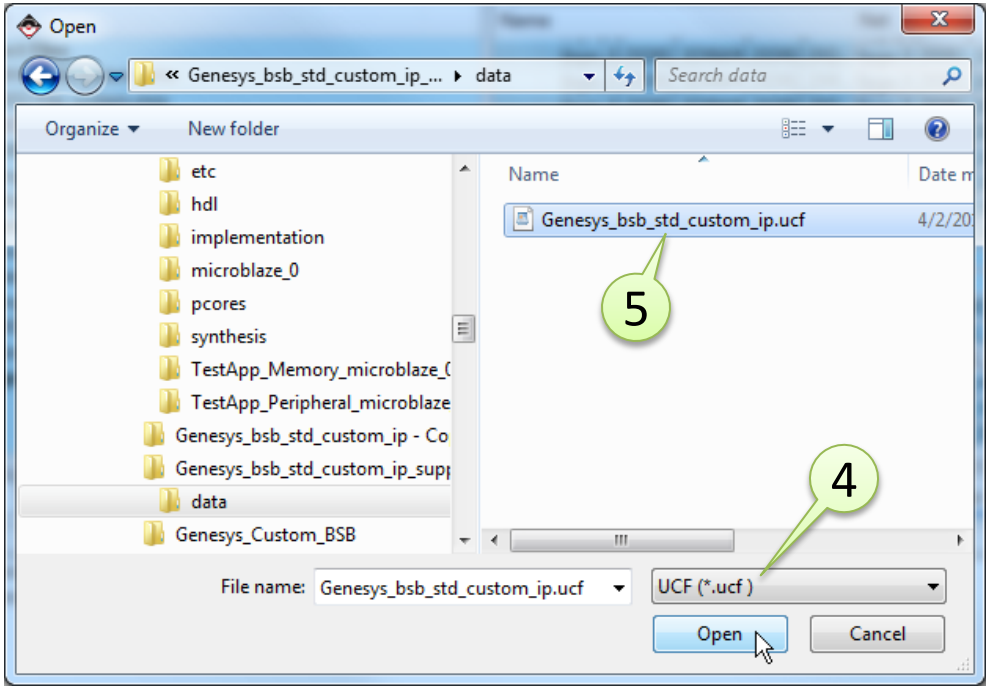
Add ucf constraints (1)

- In the "**Project**" window clock on the "**Project**" tab (1) and then double-click on the project ucf file "**/data/system.ucf**" (2) to open it
- Click "**Open**" in the toolbar (3), set the file filter to "**UCF (*.ucf)**" (4) and navigate to "**Genesys_ip_cores_UCF_SDK /data/Genesys_ip_cores.ucf**" (5). Open the file





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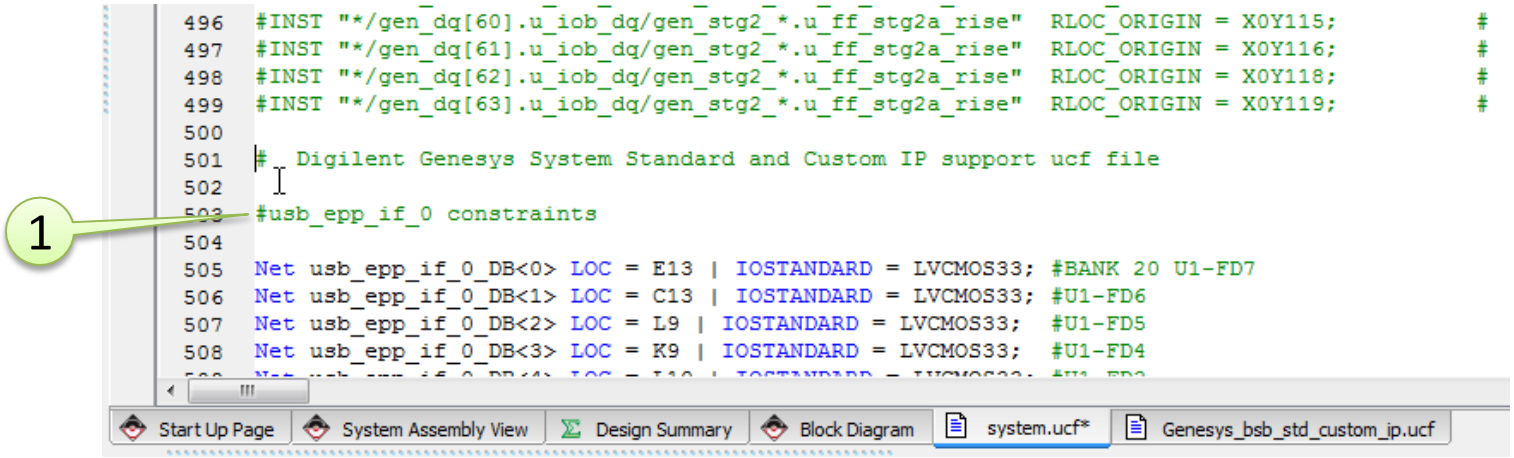
Add ucf constraints (2)

- Select the contents of the "**Genesys_std_custom_ip.ucf**" file, copy and paste it to the end of the "**system.ucf**" file (1)
- Save the **"system.ucf**" file
- Note:
  - The port names are according to the component names in this tutorial. If the user made the same naming as in this tutorial, then no changes are needed in the ucf file.
  - Otherwise, if the components were named differently, the appropriate changes have to be made in the ucf file. The names of the new external ports can be found either in "**System Assembly View**" in the "**Ports**" tab or in the "**system.mhs**" file in the "**Project**" tab, at the "**PORT**" entries



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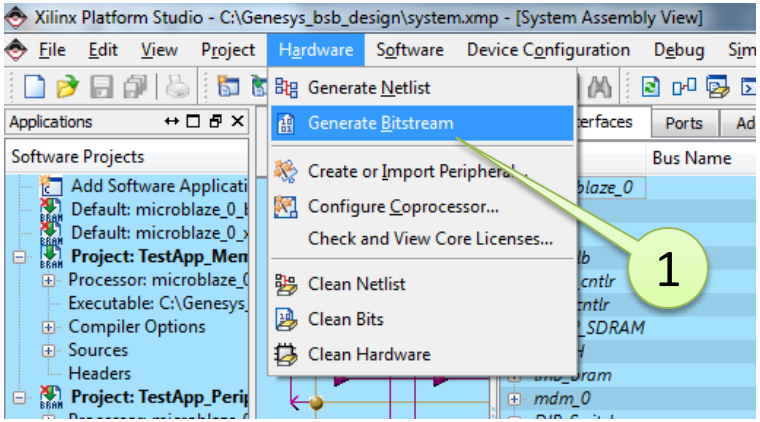
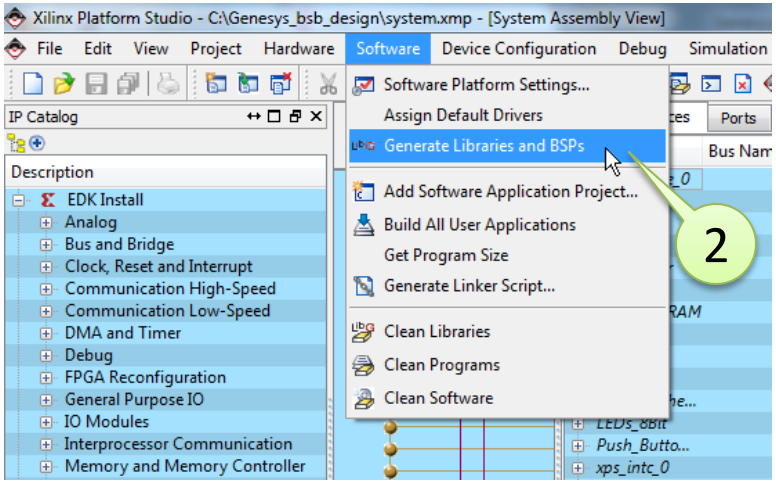
Generate Bitstream and Software Libraries

- Generate the hardware configuration bitstream (project_name.bit, in this case: "**system.bit**")
  - select from the menu "**Hardware**" -> "**Generate Bitstream**" (1) (it takes about 30..60 minutes)



- After the bitstream is generated, generate the libraries needed to create the bitstream
  - From the menu select "**Software**" → "**Generate Libraries and BSPs**" (2)



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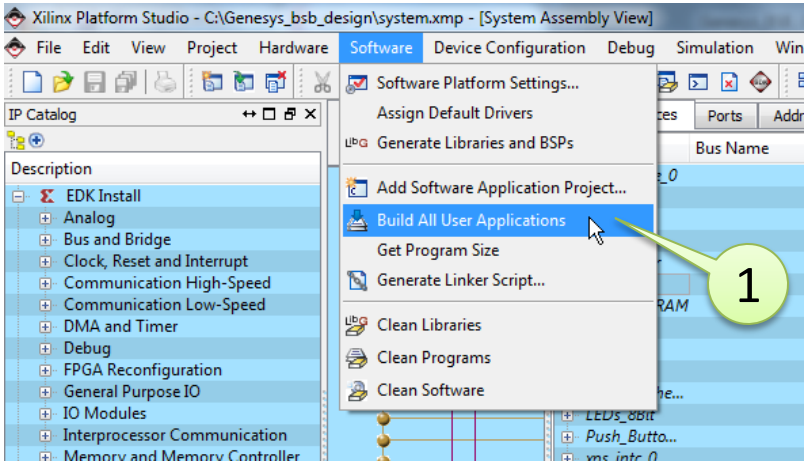
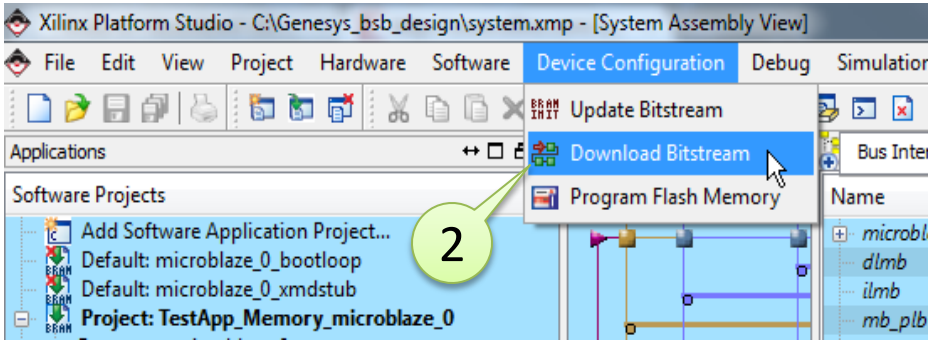
Build Initial Applications and Download Bitstream

- Compile the TestApp projects and create the executable files (executable.elf)
  - Select "**Software**" → "**Build All User Applications**" (1)
- Initialize the compiled "**TestAppMemory**" project in the Block RAM and download the new bitstream ("**download.bit**")
  - Select "**Device Configuration**"→ "**Download Bitstream**" (2)
- Note: The above four operations are automatically chained by simply selecting "**Device Configuration**" -> "**Download Bitstream**"





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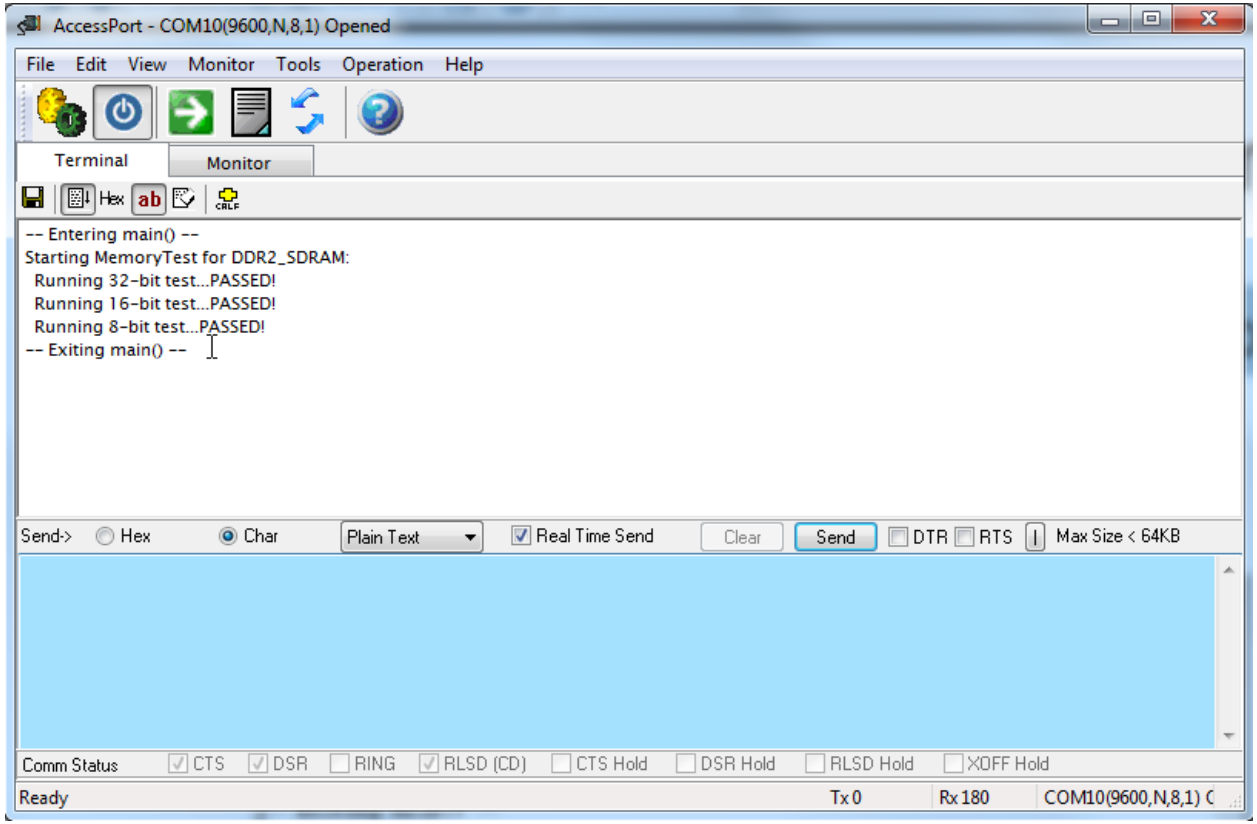
TestAppMemory result

- View the output of a successful bitstream generation and download in the terminal window:



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Export the Hardware Design into SDK and run Demo Applications

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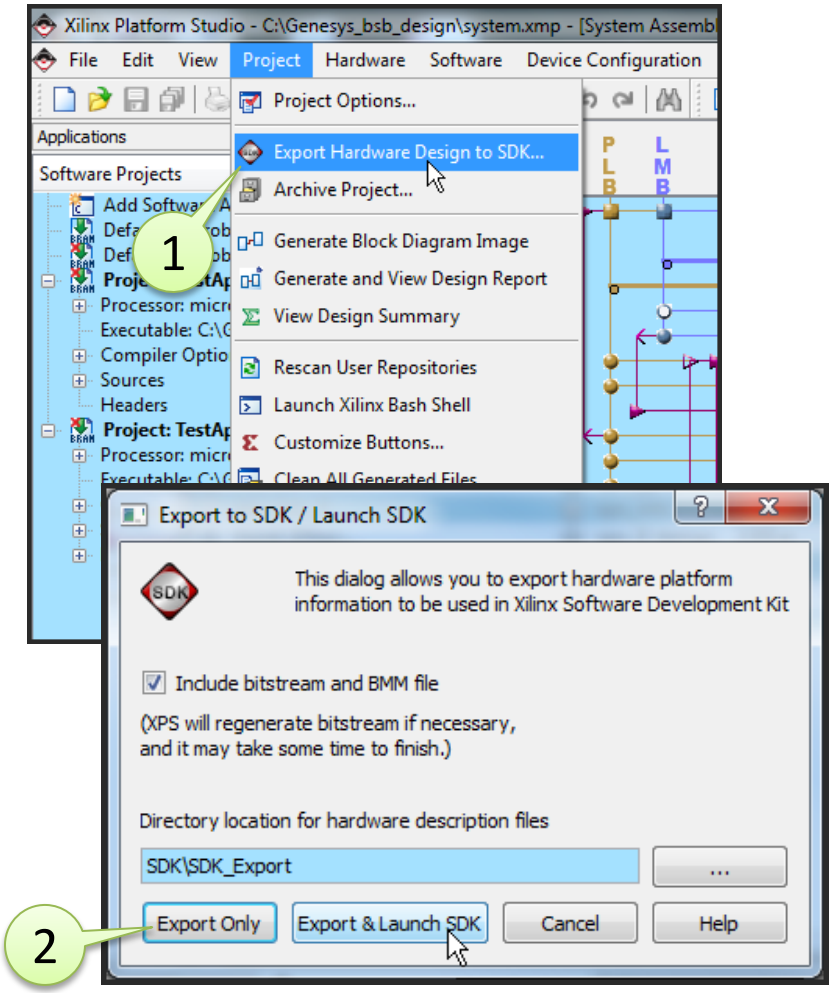
Export Hardware Design to SDK

- Export the hardware design to SDK in order to provide SDK with the hardware specification file
  - From them menu select "**Project**" -> "**Export Hardware Design to SDK**" (1)
  - Because we want to use a different workspace than the one that would result from project exporting, in the next window select "**Export Only**" (2)



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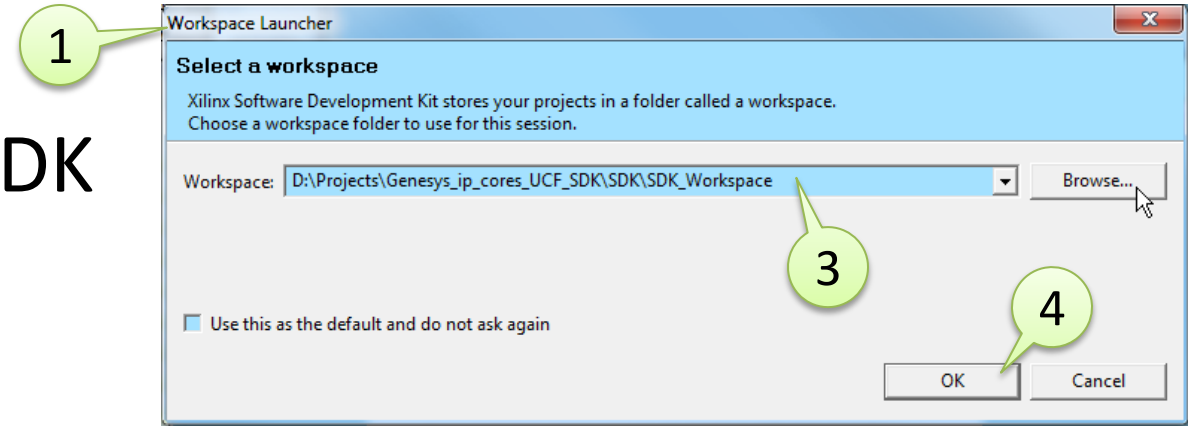
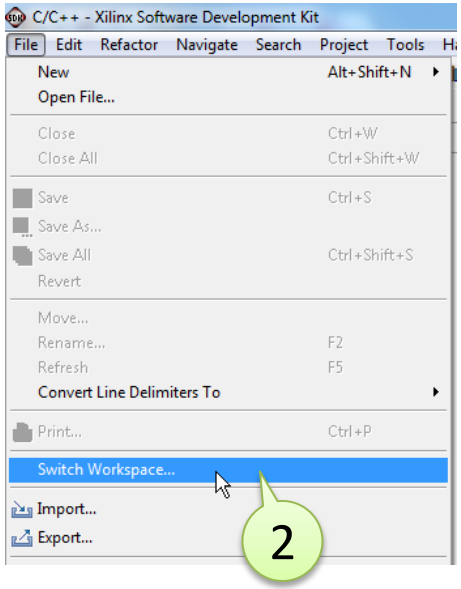
Launch SDK

- Launch Xilinx SDK



- If the "**Workspace Launcher**" dialog box (1) does not show automatically, from the menu select "**File**" -> "**Switch Workspace**" (2)
- Set the workspace to "**..\Genesys_ip_cores_UCF_SDK\SDK\SDK_Workspace**" (3), where **..\Genesys_ip_cores_UCF_SDK** is the folder extracted from the "**Genesys_ip_cores.zip**" file
- Click "**OK**" (4)



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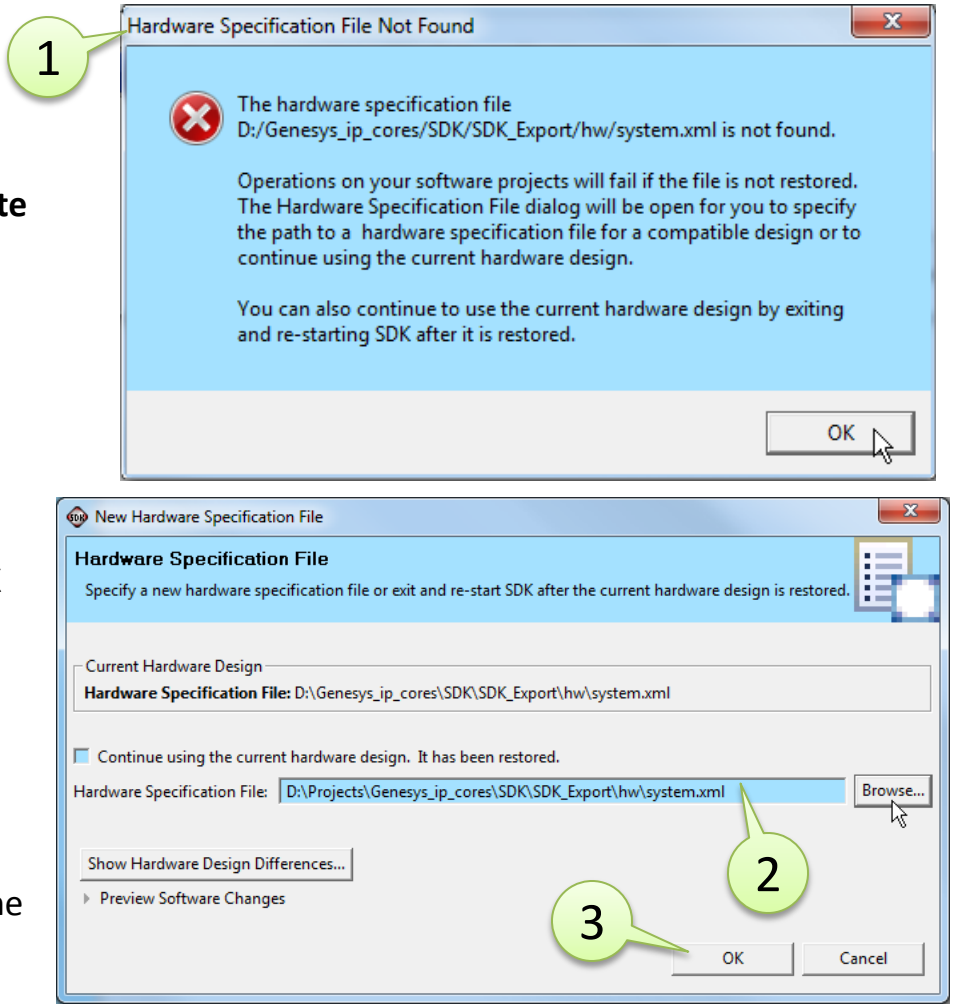
Set the Hardware Specification File in SDK

- SDK will attempt to locate the Hardware Specification File. If not found in the place where previously was used (in this case, "**D:\Genesys_ip_cores\SDK\SDK_Export\hw\system.xml**", SDK will generate an error (1)
- Click "**OK**" and in the next window browse to the hardware specification file (2)
- The hardware specification file is "**system.xml**" located in to the ".**Genesys_ip_cores\SDK\SDK_Export\hw**" (2) subfolder, where ".**Genesys_ip_cores**" is the EDK project directory folder from where the design were exported
- Click "**OK**" (3). SDK will fully rebuild the software platform and projects
- In the case if build error is encountered, from the menu choose "**Project**" -> **"Clean…**" to cleanup the project and do a full rebuild



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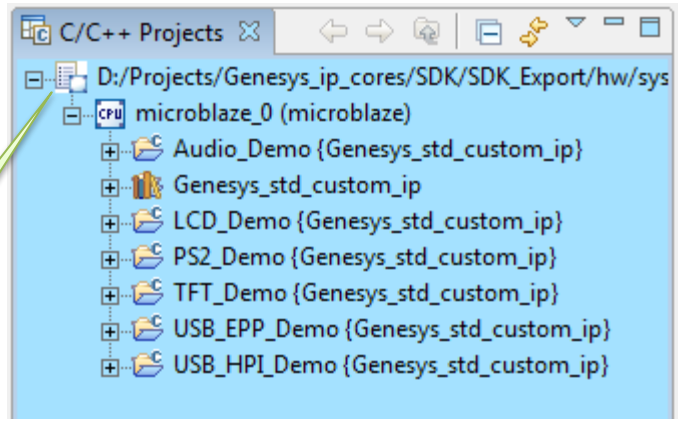
SDK Demo projects

- The following software projects are available in the "**..\Genesys_ip_cores\SDK\SDK_Workspace**" workspace (1):
  - Audio_Demo
  - LCD_Demo
  - PS2_Demo
  - TFT_Demo
  - USB_EPP_Demo
  - USB_HPI_Demo



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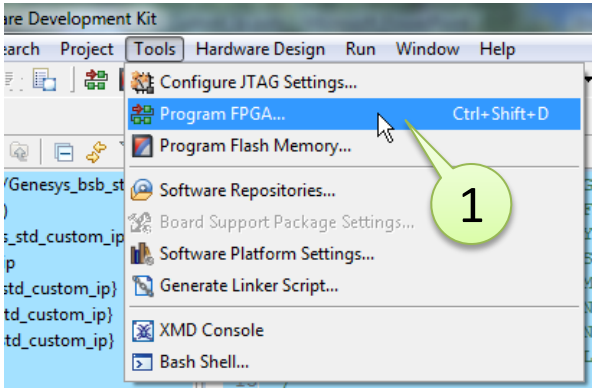
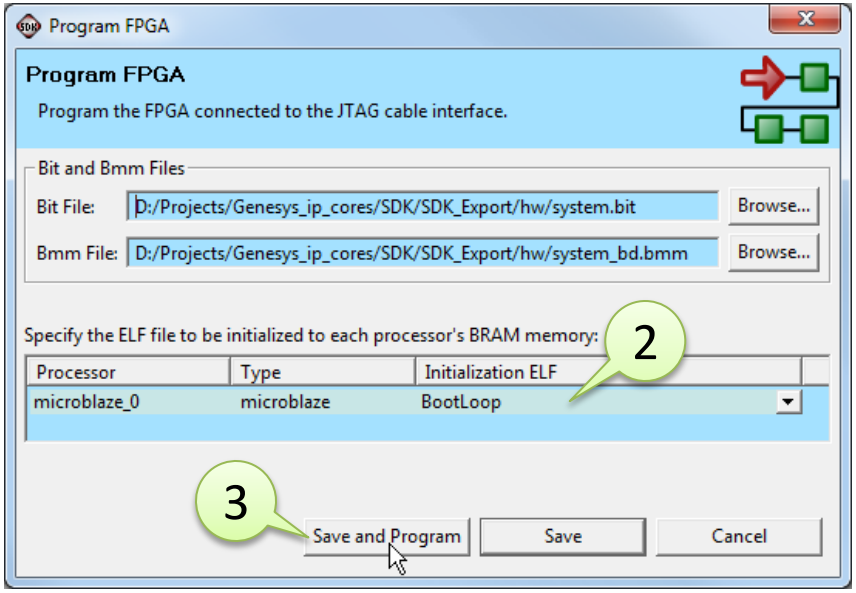
Running SDK projects (1)

- Power on the board
- From the menu select "**Tools**" -> "**Program FPGA**" (1)
- Leave the "**Bootloop**" as Initialization ELF (2) then click "**Save and Program**" (2)





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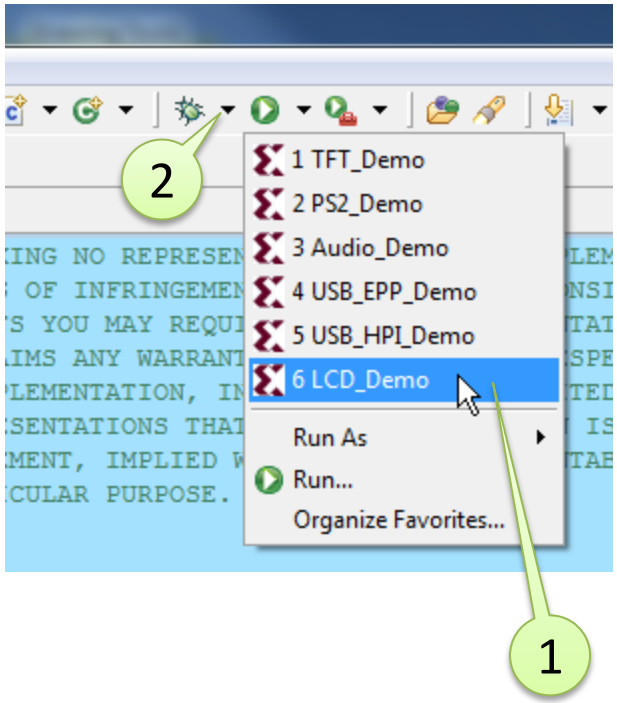
Running SDK projects (2)

Note: if SDK generates an error while programming:

- Close SDK
- Download a configuration from within EDK to check if the Xilinx USB cable is properly connected
- Reopen SDK and try programming again

- Click on the arrow beside the "**Run**" button and select the application You want to run (1)
- Debugging the applications is also possible by clicking on the arrow beside the "**Debug**" button
- The following slides will present hardware setup and a short description of each software application



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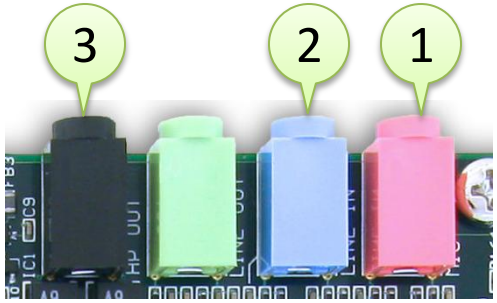
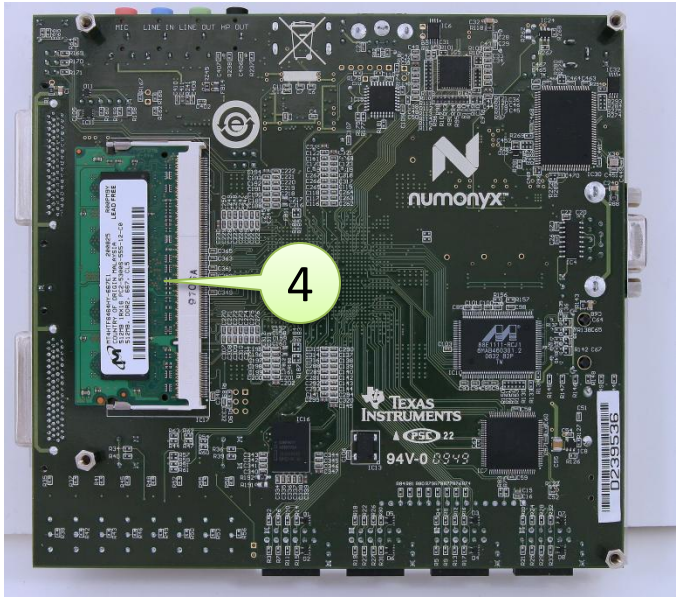
Software Project: Audio_Demo (1)

- Main file: "**.\Audio_Demo\src\audio_demo.c**"
- Executable: "**.\Audio_Demo\Debug\Audio_Demo.elf**"
- Hardware setup
  - Connect microphone to the **MIC** input (1) (not needed if the **LINE IN** input is intended to be used only)
  - Connect an audio source (for example, Headphone or Speaker Output of a computer sound card) to the **LINE IN** input (2) (not needed if the **MIC** input is intended to be used only)
  - Connect headphones or speakers to the **HP_OUT** output (3)
  - Make sure that the DDR2 memory is present on the bottom of the board (4)





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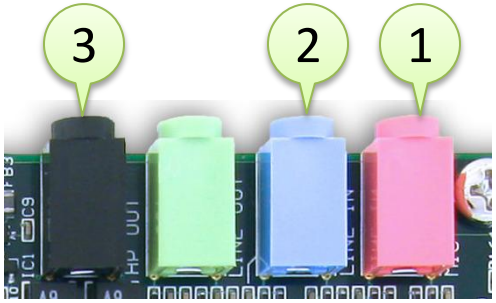
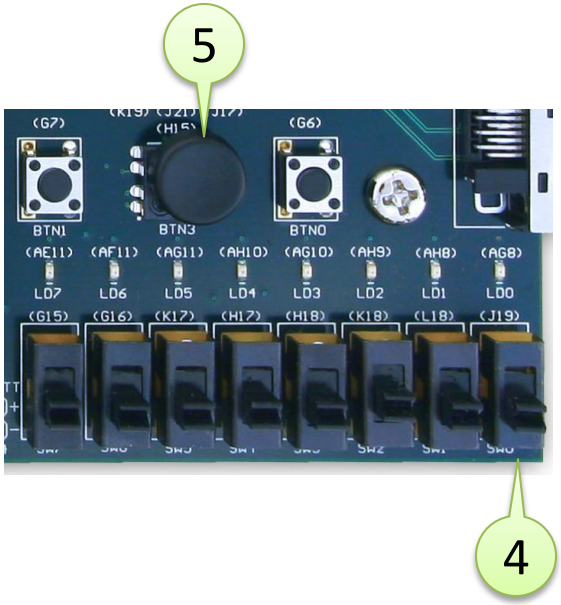
Software Project: Audio_Demo (2)

- Mode of operation:
  - **SW0** switch (4) changes between **LINE IN** or **MIC** input (**SW0** = 0: **MIC**, **SW0** = 1: **LINE_IN**). Toggling SW0 also unmutes the selected input
  - Pressing then releasing the following buttons (5):
    - "**LEFT**" button: Generates a 1KHz square-wave signal for 0.5S on the left channel.
    - "**RIGHT**" button: Generates a 1KHz square-wave signal for 0.5S on the right channel.
    - "**CENTER**" button: Generates a 1KHz square-wave signal for 0.5S on both channels.
    - "**UP**" button: Records for about 5 S audio from the source selected by SW0
    - "**DOWN**" button: Plays back the recorded data.
    - While recording or playing a progress bar is shown on the LEDs.
    - The recording is done on 18 bits resolution, Stereo (for LINE-IN only) at a 48KHz sample rate





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Software Project: LCD_Demo

- Main file: "**.\LCD_Demo\src\lcd_demo.c**"
- Executable: "**.\LCD_Demo\Debug\ LCD_Demo.elf**"
- Hardware setup:
  - None
- Mode of operation:
  - Characters typed in the terminal are displayed on the LCD display
  - Sending the TAB character (0x09) in the terminal changes the LCD line
  - Sending the BACKSPACE character (0x08) clears the LCD display and sets the LCD cursor to home

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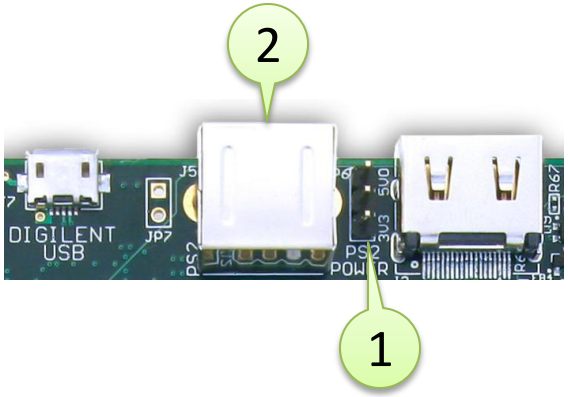
Software Project: PS2_Demo (1)

- Main file: "**.\PS2_Demo\src\ps2_demo.c**"
- Executable: "**.\PS2_Demo\Debug\PS2_Demo.elf**"
- Hardware setup
  - Make sure that the PS2 Power jumper is loaded (1)
    - Most of modern PS2 devices operate at 3.3V so load the jumper to 3V3 (recommended) If a PS2 keyboard is powered correctly, when the keyboard is plugged in the keyboard LEDs flash once
  - Connect either a PS2 keyboard or mouse to the PS2 connector (2)



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Software Project: PS2_Demo (2)

- Mode of operation:
  - The application automatically detects whether the connected device is a keyboard or mouse
  - If a keyboard is detected, the alphanumeric key characters are displayed on the terminal and the LCD screen. Left and right shift presses for alphabetic keys are also handled. Capital letters are displayed for an alphabetic key press if the shift key is also pressed
  - If a PS2 mouse is detected, the mouse is initialized and the mouse data: Left, Right and Mid button status and the mouse X and Y coordinates are displayed on both the terminal and the LCD screen at each mouse status change (movement or click)
- Note: The application is intended to work with standard PS2 devices that are compliant to the PS2 commands described in http://www.computer-engineering.org/ps2protocol/

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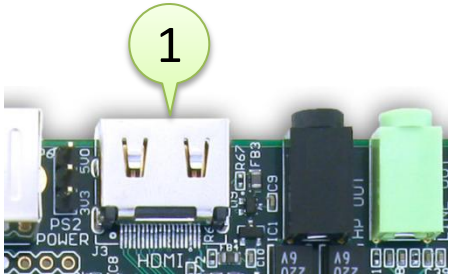
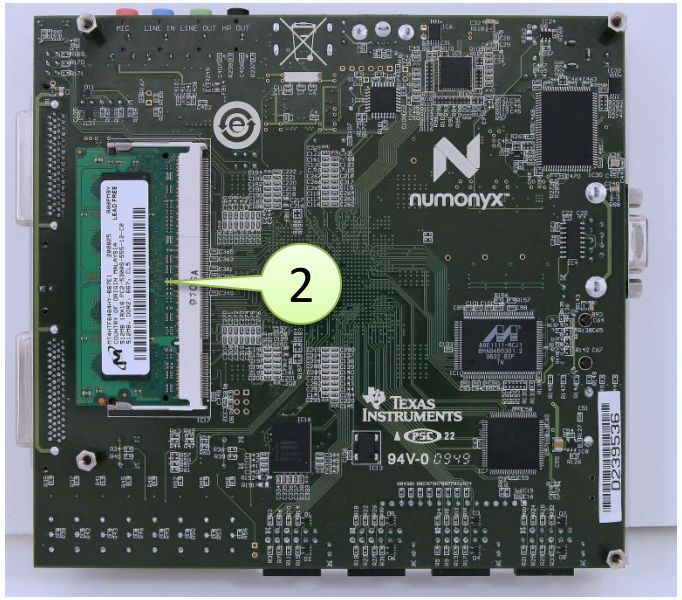
Software Project: TFT_Demo (1)

- Main file: "**.\TFT_Demo\src\tft_demo.c**"
- Executable: "**.\TFT_Demo\Debug\TFT_Demo.elf**"
- Hardware setup:
  - Connect a monitor either with HDMI input directly or with DVI input through a HDMI to DVI adapter to the HDMI connector (1)
  - Make sure that the DDR2 memory is present on the board (2)





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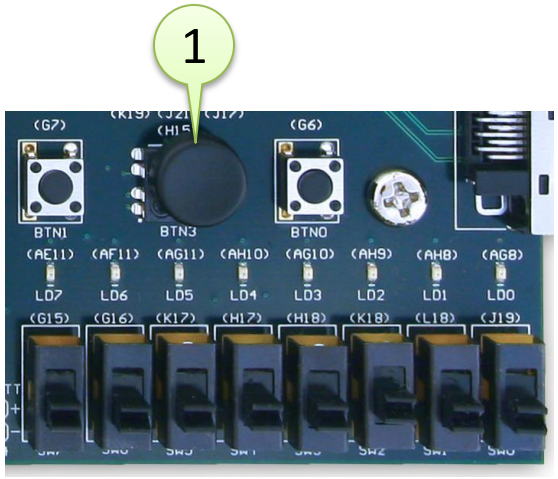
Software Project: TFT_Demo (2)

- Mode of operation:
  - The application loads the bitmap file initially stored in the FLASH memory and displays it in a predefined DDR2 memory area.
  - If the bitmap file is not found in the FLASH memory an error message is displayed on both the terminal, LCD screen and the monitor screen.
  - Then the application loads a colorbar (R, G, B) with gradients into another predefined DDR2 memory area.
  - Pressing the "**Up**" button (1) sets the xps_tft video base address to the colorbar image area, so the colorbar is displayed on the monitor screen
  - Pressing the "**Down**" button (1) sets the video base address to the bitmap image, so the bitmap is displayed on the monitor screen
  - The xps_tft core resolution is 640X480 pixels X 18 bits



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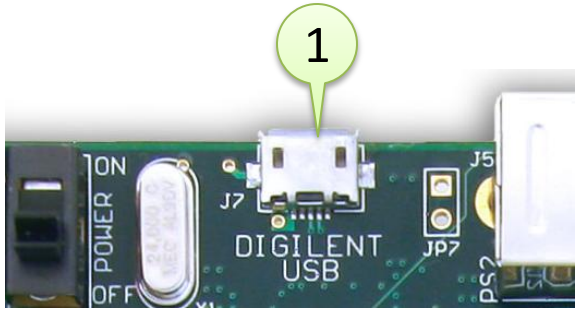
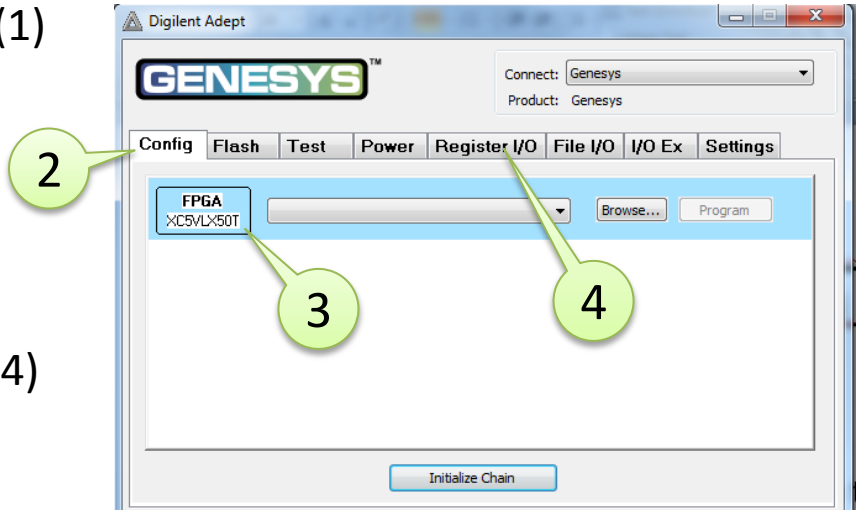
Software Project: USB_EPP_Demo (1)

- Main file: "**.\USB_EPP_Demo\src\usb_epp_demo.c**"
- Executable: "**.\USB_EPP_Demo\Debug\USB_EPP_Demo.elf**"
- Hardware setup:
  - Connect the Digilent USB connector to the computer using a USB-Micro cable (1)
- Software setup:
  - Open Adept (2.3 or later). Check in the "**Config**" tab (2) if the scan chain is initialized and the FPGA device is found board is recognized (3)
  - If yes, switch to the "**Register I/O**" tab (4)





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Software Project: USB_EPP_Demo (2)

- Mode of operation:
  - Use the "**Register I/O**" tab of Adept software to write or read data to or from the interface registers. The register addresses are as follows:
  - Write:
    - **0x01 – LEDs**. Data written into this register is displayed on the LEDs
    - 0x21 **- UART0** (**STDOUT**). Data written into this register is sent on the terminal. Therefore if valid ASCII data is written the corresponding character is displayed on the terminal
    - **0x31 – LCD**. Data written into this register is sent to the LCD screen. Therefore if valid ASCII data is written the corresponding character is displayed on the LCD screen
  - Read:
    - **0x10 - DIP switches**. Data read from this register retrieves the status of the DIP switches
    - 0x11 **– Pushbuttons**. Data read from this register retrieves the status of the seven pushbuttons (bits 6..0 only)

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Software Project: USB_EPP_Demo (3)

- Notes:
  - Writing into any other register address makes the application to answer to the EPP protocol request, but the data written is ignored. Reading from any other register returns the last data read or written through the EPP interface
  - Due to the lower speeds of the UART and LCD interfaces file transfer to this peripherals will not work in the application.

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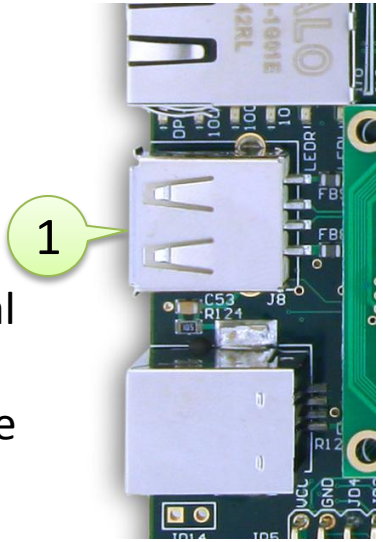
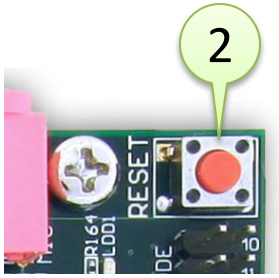
Software Project: USB_HPI_Demo

- Main file: "**.\USB_HPI_Demo\src\usb_hpi_demo.c**"
- Executable: "**.\USB_HPI_Demo\Debug\ USB_HPI_Demo.elf**"
- Hardware setup:
  - Connect a USB keyboard the USB Host connector (1), after the application is started. The keyboard must not have a built-in hub
- Mode of operation:
  - Keys typed on the USB keyboard are displayed on both the terminal and LCD display
- Note: Depending on the moment when the keyboard is inserted into the USB Host connector the Cypress USB controller might not initialize.
  - This happens, for example if the keyboard is inserted before the application is started or the application is restarted with the USB keyboard connected.
  - In this case the application will hang displaying on the terminal "**GENESYS USB Keyboard Demo**". Press the "**Reset**" button (2) on the board to reinitialize both the Cypress USB controller and the application





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References

- **Platform Studio**
  - Embedded Development Kit (EDK) Resources

    http://www.xilinx.com/tools/platform.htm

  - Embedded System Tools Reference Manual

    http://www.xilinx.com/support/documentation/sw_manuals/edk11_est_rm.pdf

  - EDK Concepts, Tools, and Techniques

    http://www.xilinx.com/support/documentation/sw_manuals/edk_ctt.pdf

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References

- **Virtex-5 Resources**
  - Virtex-5 FPGA User Guide

    http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
  - Virtex-5 FPGA Configuration User Guide

    http://www.xilinx.com/support/documentation/user_guides/ug191.pdf
  - Virtex-5 System Monitor User Guide

    http://www.xilinx.com/support/documentation/user_guides/ug192.pdf
  - Virtex-5 Packaging and Pinout Specification

    http://www.xilinx.com/support/documentation/user_guides/ug195.pdf

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References

- **Genesy Resources**
  - Genesys Board Schematics

    http://www.digilentinc.com/Data/Products/GENESYS/Genesys-sch.pdf

  - Other Genesys Board Resources

    http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,819&Prod=GENESYS