Clock Generator (v3.02a)

DS614 December 2, 2009 **Product Specification**

Introduction

The Clock Generator module provides clocks according to system wide clock requirements.

Features

- Automatic instantiation of Digital Clock Manager (DCM) modules and their connections
- Automatic instantiation of PLL modules and their connections
- Automatic instantiation of MMCM modules and their connections
- Automatic BUFG insertion
- Automatic DCM, PLL, and MMCM reset sequence determination and connection

LogiCORE™ IP Facts		
Core Specifics		
Supported Device Family	Spartan®-3A/3A DSP, Spartan-3, Spartan-3E, Automotive Spartan 3/3E/3A/3A DSP, Spartan-6, Virtex®-4/4Q/4QV, Virtex-5/5FX, Virtex-6/6CX	
Resources Used		
	Min	Max
LUTs	N/A	N/A
FFs	N/A	N/A
Block RAMs	N/A	N/A
DCMs	0	4
PLLs	0	2
MMCMs	0	4
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	EDK TCL Generated	
Verification	N/A	
Instantiation Template	EDK	
Design Tool Requirements		
Xilinx Implementation Tools	ISE® 11.4 or later	
Verification	ModelSim PE/SE 6.4b or later	
Simulation	ModelSim PE/SE 6.4b or later	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

Functional Description

The block diagram for the Clock Generator module is shown in Figure 1.

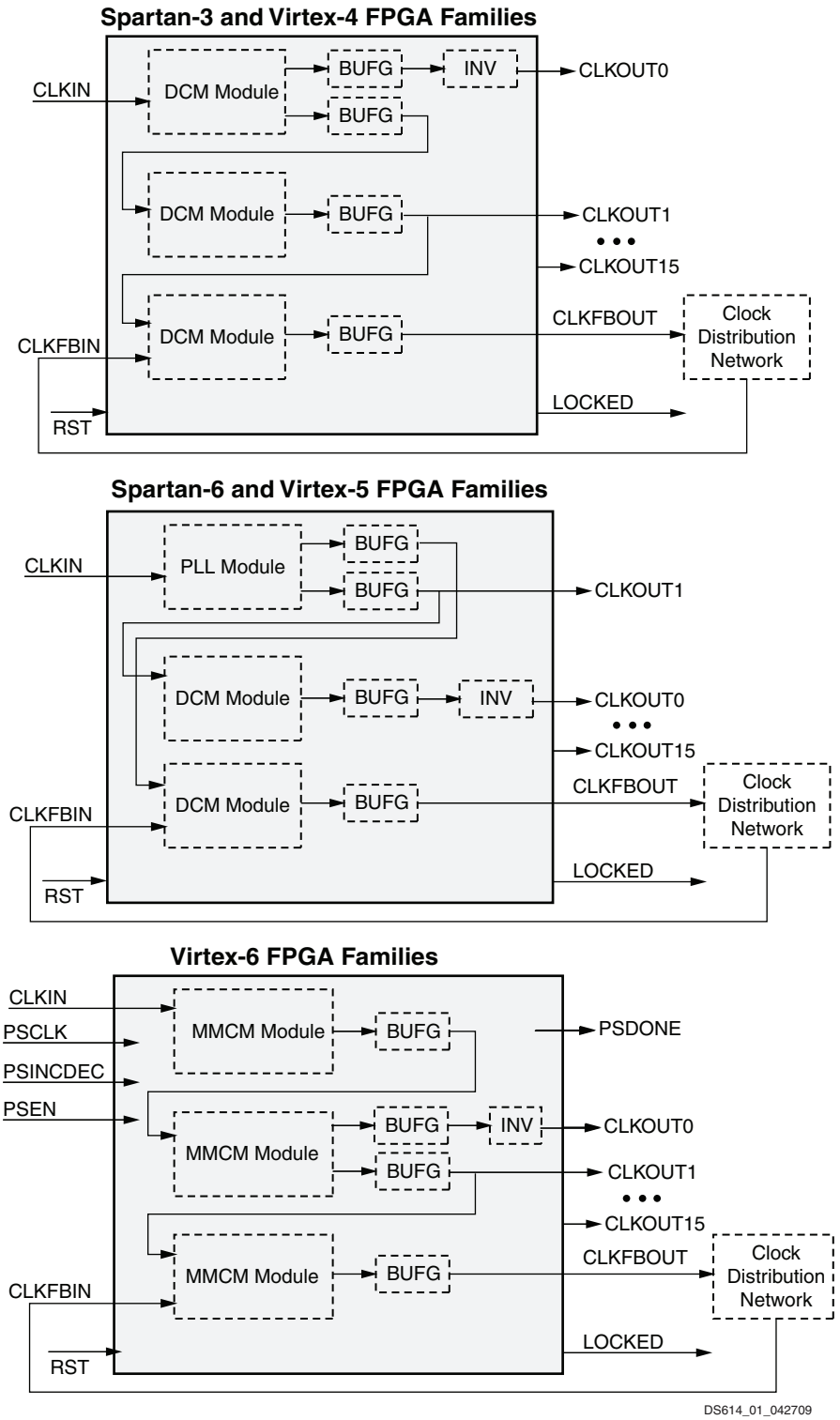

Figure 1: **Clock Generator Modules Block Diagram**

The Clock Generator module provides clock signals according to system wide clock requirements. The sub-system, depending on the FPGA family, is composed of up to four MMCM modules, four DCM modules, two PLL modules, BUFGs, clock inverters, and reset logics.

The Clock Generator module supports the following clock requirements:

- One input reference clock
- One feedback clock for clock deskew
- Up to 16 output clocks: see the DCM, PLL, and MMCM primitives for clock frequency ranges
- Fixed phase shift (0 to 359 degrees) for output clocks
- Variable phase shift on Virtex-6 devices
- Skew between clock outputs can be reduced through grouping. The outputs within the same group are generated from the respective DCM, PLL or MMCM module
- Supports device families listed in the Supported Device Family field of the LogiCORE Facts Table. Input and output clock frequency range check according to device family selection using the slowest speed grade
- Supports both active high and active low external reset

If clock requirements can not be met, then the LOCKED output signal remains inactive and the output clocks are undetermined.

Clock Generator I/O Signals

The interface signals for the Clock Generator module are listed and described in Table 1.

Table 1: **Clock Generator Signal Descriptions**

Signal Name	I/O	Initial State	Description
RST	I		If C_EXT_RESET_HIGH = 0, an inverter is inserted; otherwise, this signal is connected to the reset port of the DCM, PLL, or MMCM.
CLKIN	I		Connect to CLKIN of DCM, PLL, or MMCM.
CLKFBIN	I		Connect to CLKFB of a DCM, if used. CLKBIN is not used typically, because the Clock Generator will connect up the feedback connects automatically.
PSCLK	I		Phase shift clock input
PSINCDEC	I		Phase shift increment/decrement input
PSEN	I		Phase shift enable input
PSDONE	O		Phase shift done input
CLKOUT0-15	O	Low	Connect to the clock output port of a DCM, PLL, or MMCM. A BUFG is inserted; a clock inverter may be inserted.
CLKFBOUT	O	Low	Connect to the CLK0 port of a DCM, if used, a BUFG is inserted.
LOCKED	O	Low	LOCKED = High indicates all required clocks are stable.

Design Parameters

The parameters defined for the Clock Generator module are listed and described in Table 2.

Table 2: **Clock Generator Parameters**

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_CLKIN_FREQ	Frequency (Hz) of CLKIN	natural	0	integer
C_CLKFBIN_FREQ	Frequency (Hz) of CLKFBIN	natural	0	integer
C_CLKFBIN_DESKEW	CLKFIN clock deskew with CLKOUTi	NONE, CLKOUT*i*, *i*=0,..,15	NONE	string
C_CLKOUT*i*_FREQ	*i*=0,..,15, frequency (Hz) of CLKOUT*i*	natural	0	integer
C_CLKOUT*i*_PHASE	*i*=0,..,15, phase shift of CLKOUT*i*	0 to 359	0	integer
C_CLKOUT*i*_GROUP	*i*=0,..,15, group name of CLKOUT*i*	NONE, DCM0, DCM1, DCM2, DCM3, PLL0, PLL0_ADJUST, PLL1, PLL1_ADJUST, MMCM0, MMCM1, MMCM2, MMCM3	NONE	string
C_CLKOUT*i*_BUF	*i*=0,..,15, if TRUE, insert BUFG for CLKOUT*i*	TRUE, FALSE	TRUE	boolean
C_CLKOUTi_VARIABLE PHASE	*i*=0,..,15, if TRUE, set MMCM clock output USE_FINE_PS	TRUE, FALSE	TRUE	boolean
C_CLKFBOUT_FREQ	Frequency (Hz) of CLKFBOUT	natural	0	integer
C_CLKFBOUT_GROUP	Group name of CLKFBOUT	NONE, MMCM0, MMCM1, MMCM2, MMCM3	NONE	string
C_CLKFBOUT_BUF	Insert BUFG for CLKFBOUT*i*	TRUE, FALSE	NONE	boolean
C_PSDONE_GROUP	Group name of PSDONE to specify the variable phase controlled MMCM name	NONE, MMCM0, MMCM0_FB, MMCM1, MMCM1_FB, MMCM2, MMCM2_FB, MMCM3, MMCM3_FB	NONE	string
C_EXT_RESET_HIGH	External reset active high	0, 1	0	integer
C_FAMILY	Target architecture family for design	spartan3, spartan3e, spartan3a, spartan3adsp, aspartan3, aspartan3e, aspartan3a, aspartan3adsp,spartan6, virtex4, qvirtex4, qvvirtex4, virtex5, virtex5fx, virtex6, virtex6cx	virtex5	string
C_SPEEDGRADE	Allowable values for target device speed grade	string	default	string

The parameters to describe the internal view of Clock Generator module are listed and described in Table 3.

Table 3: **Clock Generator Parameters (low level internal view)**

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_CLK_GEN	Set the value to UPDATE to generate the clock circuit from high level parameters. The value is changed to PASSED if all required CLKOUTs are generated by DCM, PLL, or MMCM; otherwise changed to FAILED	UPDATE, PASSED, FAILED	UPDATE	string
C_CLKOUT*i*_ MODULE	*i*=0,..,15, module connected toCLKOUT*i*	NONE, CLKGEN, DCM0-3, PLL0-1, MMCM0-3	NONE	string
C_CLKOUT*i*_ PORT	*i*=0,..,15, port connected to CLKOUT*i*, (use *port_name*B if BUFG is inserted)	NONE, CLKIN, CLKFBIN, CLKOUT0-6(B), CLKFBOUT(B), CLK0(B), CLK90(B), CLK180(B), CLK270(B), CLKDV(B), CLKDV180(B), CLK2X(B), CLK2X180(B), CLKFX(B), CLKFX180(B)	NONE	string
C_CLKFBOUT_ MODULE	Module connected to CLKFBOUT	Same as C_CLKOUT*i*_ MODULE	NONE	string
C_CLKFBOUT_ PORT	Port connected to CLKFBOUT	Same as C_CLKOUT*i*_ PORT	NONE	string
C_PSDONE_ MODULE	Module connected to CLKFBOUT	Same as C_CLKOUTi_ MODULE	NONE	string
C_DCM*i*_DFS_ FREQUENCY_MODE	*i*=0,..,3, C_DFS_FREQUENCY of DCM*i*	Same as DCM primitive	LOW	string
C_DCM*i*_DLL_ FREQUENCY_MODE	*i*=0,..,3, C_DLL_FREQUENCY of DCM*i*	Same as DCM primitive	LOW	string
C_DCM*i*_CLK_ FEEDBACK	*i*=0,..,3, C_CLK_FEEDBACK of DCM*i*	Same as DCM primitive	1X	string
C_DCM*i*_CLKOUT_ PHASE_SHIFT	*i*=0,..,3, C_CLKOUT_PHASE_SHIFT of DCM*i*	Same as DCM primitive	NONE	string
C_DCM*i*_PHASE_ SHIFT	*i*=0,..,3, C_PHASE_SHIFT of DCM*i*	Same as DCM primitive	0	integer
C_DCM*i*_CLKFX_ MULTIPLY	*i*=0,..,3, C_CLKFX_MULTIPLY of DCM*i*	Same as DCM primitive	4	integer
C_DCM*i*_CLKFX_ DIVIDE	*i*=0,..,3, C_CLKFX_DIVIDE of DCM*i*	Same as DCM primitive	1	integer
C_DCM*i*_CLKDV_ DIVIDE	*i*=0,..,3, C_CLKDV_DIVIDE of DCM*i*	Same as DCM primitive	2.0	real

Table 3: **Clock Generator Parameters (low level internal view) *(Cont'd)***

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_DCM*i*_CLK0_BUF	*i*=0,..,3, if TRUE, a BUFG is inserted for DCM*i* CLK0	TRUE, FALSE	FALSE	boolean
C_DCM*i*_CLK90_BUF	*i*=0,..,3, if TRUE, a BUFG is inserted for DCM*i* CLK90	TRUE, FALSE	FALSE	boolean
C_DCM*i*_CLK180_BUF	*i*=0,..,3, if TRUE, a BUFG is inserted for DCM*i* CLK180	TRUE, FALSE	FALSE	boolean
C_DCM*i*_CLK270_BUF	*i*=0,..,3, if TRUE, a BUFG is inserted for DCM*i* CLK270	TRUE, FALSE	FALSE	boolean
C_DCM*i*_CLKDV_BUF	*i*=0,..,3, if TRUE, a BUFG is inserted for DCM*i* CLKDV	TRUE, FALSE	FALSE	boolean
C_DCM*i*_CLKDV180_BUF	*i*=0,..,3, if TRUE, a BUFG is inserted for DCM*i* CLKDV180	TRUE, FALSE	FALSE	boolean
C_DCM*i*_CLK2X_BUF	*i*=0,..,3, if TRUE, a BUFG is inserted for DCM*i* CLK2X	TRUE, FALSE	FALSE	boolean
C_DCM*i*_CLK2X180_BUF	*i*=0,..,3, if TRUE, a BUFG is inserted for DCM*i* CLK2X180	TRUE, FALSE	FALSE	boolean
C_DCM*i*_CLKFX_BUF	*i*=0,..,3, if TRUE, a BUFG is inserted for DCM*i* CLKFX	TRUE, FALSE	FALSE	boolean
C_DCM*i*_CLKFX180_BUF	*i*=0,..,3, if TRUE, a BUFG is inserted for DCM*i* CLKFX180	TRUE, FALSE	FALSE	boolean
C_DCM*i*_CLKIN_MODULE	*i*=0,..,3, module connect to CLKIN of DCM*i*	Same as C_CLKOUT*i*_MODULE	NONE	string
C_DCM*i*_CLKIN_PORT	*i*=0,..,3, port connect to CLKIN of DCM*i*	Same as C_CLKOUT*i*_PORT	NONE	string
C_DCM*i*_CLKFB_MODULE	*i*=0,..,3, module connect to CLKFB of DCM*i*	Same as C_CLKOUT*i*_MODULE	NONE	string
C_DCM*i*_CLKFB_PORT	*i*=0,..,3, port connect to CLKFB of DCM*i*	Same as C_CLKOUT*i*_PORT	NONE	string
C_DCM*i*_RST_MODULE	*i*=0,..,3, module connect to RST of DCM*i*	Same as C_CLKOUT*i*_MODULE	NONE	string
C_PLL*i*_DIVCLK_DIVIDE	*i*=0,1, C_DIVCLK_DIVIDE of PLL*i*	Same as PLL primitive	1	integer
C_PLL*i*_CLKFBOUT_MULT	*i*=0,..,3, C_CLKFBOUT_MULT of PLL*i*	Same as PLL primitive	1	integer
C_PLL*i*_CLKFBOUT_PHASE	*i*=0,1, C_CLKFBOUT_PHASE of PLL*i*	Same as PLL primitive	0	integer
C_PLL*i*_CLKIN1_PERIOD	*i*=0,1, C_CLKIN1_PERIOD of PLL*i*	Same as PLL primitive	0.0	real
C_PLL*i*_CLKOUT0_DIVIDE	*i*=0,1, C_CLKOUT0_DIVIDE of PLL*i*	Same as PLL primitive	1	integer
C_PLL*i*_CLKOUT0_PHASE	*i*=0,1, C_CLKOUT0_PHASE of PLL*i*	Same as PLL primitive	0	integer

Table 3: **Clock Generator Parameters (low level internal view)** ***(Cont'd)***

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_PLL*i*_CLKOUT0_DESKEW_ADJUST	*i*=0,1, C_CLKOUT0_DESKEW_ADJUST of PLL*i*	Same as PLL primitive	NONE	string
C_PLL*i*_CLKOUT1_DIVIDE	*i*=0,1, C_CLKOUT1_DIVIDE of PLL*i*	Same as PLL primitive	1	integer
C_PLL*i*_CLKOUT1_PHASE	*i*=0,1, C_CLKOUT1_PHASE of PLL*i*	Same as PLL primitive	0	integer
C_PLL*i*_CLKOUT1_DESKEW_ADJUST	*i*=0,1, C_CLKOUT1_DESKEW_ADJUST of PLL*i*	Same as PLL primitive	NONE	string
C_PLL*i*_CLKOUT2_DIVIDE	*i*=0,1, C_CLKOUT2_DIVIDE of PLL*i*	Same as PLL primitive	1	integer
C_PLL*i*_CLKOUT2_PHASE	*i*=0,1, C_CLKOUT2_PHASE of PLL*i*	Same as PLL primitive	0	integer
C_PLL*i*_CLKOUT2_DESKEW_ADJUST	*i*=0,1, C_CLKOUT2_DESKEW_ADJUST of PLL*i*	Same as PLL primitive	NONE	string
C_PLL*i*_CLKOUT3_DIVIDE	*i*=0,1, C_CLKOUT3_DIVIDE of PLL*i*	Same as PLL primitive	1	integer
C_PLL*i*_CLKOUT3_PHASE	*i*=0,1, C_CLKOUT3_PHASE of PLL*i*	Same as PLL primitive	0	integer
C_PLL*i*_CLKOUT3_DESKEW_ADJUST	*i*=0,1, C_CLKOUT3_DESKEW_ADJUST of PLL*i*	Same as PLL primitive	NONE	string
C_PLL*i*_CLKOUT4_DIVIDE	*i*=0,1, C_CLKOUT4_DIVIDE of PLL*i*	Same as PLL primitive	1	integer
C_PLL*i*_CLKOUT4_PHASE	*i*=0,1, C_CLKOUT4_PHASE of PLL*i*	Same as PLL primitive	0	integer
C_PLL*i*_CLKOUT4_DESKEW_ADJUST	*i*=0,1, C_CLKOUT4_DESKEW_ADJUST of PLL*i*	Same as PLL primitive	NONE	string
C_PLL*i*_CLKOUT5_DIVIDE	*i*=0,1, C_CLKOUT5_DIVIDE of PLL*i*	Same as PLL primitive	1	integer
C_PLL*i*_CLKOUT5_PHASE	*i*=0,1, C_CLKOUT5_PHASE of PLL*i*	Same as PLL primitive	0	integer
C_PLL*i*_CLKOUT5_DESKEW_ADJUST	*i*=0,1, C_CLKOUT5_DESKEW_ADJUST of PLL*i*	Same as PLL primitive	NONE	string
C_PLL*i*_CLKFBOUT_DESKEW_ADJUST	*i*=0,1, C_CLKFBOUT_DESKEW_ADJUST of PLL*i*	Same as PLL primitive	NONE	string
C_PLL*i*_CLKOUT0_BUF	*i*=0,1, if TRUE, a BUFG is inserted for PLL*i* CLKOUT0	TRUE, FALSE	FALSE	boolean
C_PLL*i*_CLKOUT1_BUF	*i*=0,1, if TRUE, a BUFG is inserted for PLL*i* CLKOUT1	TRUE, FALSE	FALSE	boolean

Table 3: **Clock Generator Parameters (low level internal view)** ***(Cont'd)***

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_PLL*i*_CLKOUT2_BUF	*i*=0,1, if TRUE, a BUFG is inserted for PLL*i* CLKOUT2	TRUE, FALSE	FALSE	boolean
C_PLL*i*_CLKOUT3_BUF	*i*=0,1, if TRUE, a BUFG is inserted for PLL*i* CLKOUT3	TRUE, FALSE	FALSE	boolean
C_PLL*i*_CLKOUT4_BUF	*i*=0,1, if TRUE, a BUFG is inserted for PLL*i* CLKOUT4	TRUE, FALSE	FALSE	boolean
C_PLL*i*_CLKOUT5_BUF	*i*=0,1, if TRUE, a BUFG is inserted for PLL*i* CLKOUT5	TRUE, FALSE	FALSE	boolean
C_PLL*i*_CLKIN1_MODULE	*i*=0,1, module connect to CLKIN1 of PLL*i*	Same as C_CLKOUT*i*_MODULE	NONE	string
C_PLL*i*_CLKIN1_PORT	*i*=0,1, port connect to CLKIN1 of PLL*i*	Same as C_CLKOUT*i*_PORT	NONE	string
C_PLL*i*_CLKFBIN_MODULE	*i*=0,1, module connect to CLKFBIN of PLL*i*	Same as C_CLKOUT*i*_MODULE	NONE	string
C_PLL*i*_CLKFBIN_PORT	*i*=0,1, port connect to CLKFBIN of PLL*i*	Same as C_CLKOUT*i*_PORT	NONE	string
C_PLL*i*_RST_MODULE	*i*=0,1, module connect to RST of PLLi	Same as C_CLKOUT*i*_MODULE	NONE	string
C_MMCM*i*_BANDWIDTH	*i*-1,..,3, C_BANDWITH of MMCMi	Same as MMCM primitive	OPTIMIZED	string
C_MMCM*i*_CLKFBOUT	*i*-1,..,3, C_CLKFBOUT_MULT_F of MMCM/	Same as MMCM primitive	1.0	real
C_MMCM*i*_CLKFBOUT_PHASE	*i*-1,..,3, C_CLKFBOUT_PHASE of MMCM*i*	Same as MMCM primitive	0.0	real
C_MMCM*i*_CLKFBOUT_USE_FINE_PS	*i*-1,..,3, C_CLKFBOUT_USE_FINE_PS of MMCM*i*	Same as MMCM primitive	FALSE	boolean
C_MMCM*i*_CLKIN1_PERIOD	*i*-1,..,3, C_CLK1_PERIOD of MMCM*i*	Same as MMCM primitive	0.0	real
C_MMCM*i*_CLKOUT0_DIVIDE_F	*i*-1,..,3, C_CLKOUT0_DIVIDE_F of MMCM*i*	Same as MMCM primitive	1.0	real
C_MMCM*i*_CLKOUT0_DUTY_CYCLE	/-1,..,3, C_CLKOUT0_DUTY_CYCLE of MMCM*i*	Same as MMCM primitive	0.5	real
C_MMCM*i*_CLKOUT0_PHASE	*i*-1,..,3, C_CLKOUT0_PHASE of MMCM*i*	Same as MMCM primitive	0.0	real
C_MMCM*i*_CLKOUT1_DIVIDE	*i*-1,..,3, C_CLKOUT1_DIVIDE of MMCM*i*	Same as MMCM primitive	1	integer
C_MMCM*i*_CLKOUT1_DUTY_CYCLE	*i*-1,..,3, C_CLKOUT1_DUTY_CYCLE of MMCM*i*	Same as MMCM primitive	0.5	real
C_MMCM*i*_CLKOUT1_PHASE	*i*-1,..,3, C_CLKOUT1_PHASE of MMCM*i*	Same as MMCM primitive	0.0	real
C_MMCM*i*_CLKOUT2_DIVIDE	*i*-1,..,3, C_CLKOUT2_DIVIDE of MMCM*i*	Same as MMCM primitive	1	integer

Table 3: **Clock Generator Parameters (low level internal view)** ***(Cont'd)***

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_MMCM*i*_CLKOUT2_DUTY_CYCLE	*i*-1,..,3, C_CLKOUT2_DUTY_CYCLE of MMCM*i*	Same as MMCM primitive	0.5	real
C_MMCM*i*_CLKOUT2_PHASE	*i*-1,..,3, C_CLKOUT2_PHASE of MMCM*i*	Same as MMCM primitive	0.0	real
C_MMCM*i*_CLKOUT3_DIVIDE	*i*-1,..,3, C_CLKOUT3_DIVIDE of MMCM*i*	Same as MMCM primitive	1	integer
C_MMCM*i*_CLKOUT3_DUTY_CYCLE	*i*-1,..,3, C_CLKOUT3_DUTY_CYCLE of MMCM*i*	Same as MMCM primitive	0.5	real
C_MMCM*i*_CLKOUT3_PHASE	*i*-1,..,3, C_CLKOUT3_PHASE of MMCM*i*	Same as MMCM primitive	0.0	real
C_MMCM*i*_CLKOUT4_DIVIDE	*i*-1,..,3, C_CLKOUT4_DIVIDE of MMCM*i*	Same as MMCM primitive	1	integer
C_MMCM*i*_CLKOUT4_DUTY_CYCLE	*i*-1,..,3, C_CLKOUT4_DUTY_CYCLE of MMCM*i*	Same as MMCM primitive	0.5	real
C_MMCM*i*_CLKOUT4_PHASE	*i*-1,..,3, C_CLKOUT4_PHASE of MMCM*i*	Same as MMCM primitive	0.0	real
C_MMCM*i*_CLKOUT5_DIVIDE	*i*-1,..,3, C_CLKOUT5_DIVIDE of MMCM*i*	Same as MMCM primitive	1	integer
C_MMCM*i*_CLKOUT5_DUTY_CYCLE	*i*-1,..,3, C_CLKOUT5_DUTY_CYCLE of MMCM*i*	Same as MMCM primitive	0.5	real
C_MMCM*i*_CLKOUT5_PHASE	*i*-1,..,3, C_CLKOUT5_PHASE of MMCM*i*	Same as MMCM primitive	0.0	real
C_MMCM_CLKOUT6_DIVIDE	*i*-1,..,3, C_CLKOUT3_DIVIDE of MMCM*i*	Same as MMCM primitive	1	integer
C_MMCM*i*_CLKOUT6_DUTY_CYCLE	*i*-1,..,3, C_CLKOUT3_DUTY_CYCLE of MMCM*i*	Same as MMCM primitive	0.5	real
C_MMCM*i*_CLKOUT6_PHASE	*i*-1,..,3, C_CLKOUT3_PHASE of MMCM*i*	Same as MMCM primitive	0.0	real
C_MMCM*i*_CLKOUT0_USE_FINE_PS	*i*-1,..,3, C_CLKOUT0_USE_FINE_PS of MMCM*i*	Same as MMCM primitive	FALSE	boolean
C_MMCM*i*_CLKOUT1_USE_FINE_PS	*i*-1,..,3, C_CLKOUT1_USE_FINE_PS of MMCM*i*	Same as MMCM primitive	FALSE	boolean
C_MMCM*i*_CLKOUT2_USE_FINE_PS	*i*-1,..,3, C_CLKOUT2_USE_FINE_PS of MMCM*i*	Same as MMCM primitive	FALSE	boolean
C_MMCM*i*_CLKOUT3_USE_FINE_PS	*i*-1,..,3, C_CLKOUT3_USE_FINE_PS of MMCM*i*	Same as MMCM primitive	FALSE	boolean
C_MMCM*i*_CLKOUT4_USE_FINE_PS	*i*-1,..,3, C_CLKOUT4_USE_FINE_PS of MMCM*i*	Same as MMCM primitive	FALSE	boolean
C_MMCM*i*_CLKOUT5_USE_FINE_PS	*i*-1,..,3, C_CLKOUT5_USE_FINE_PS of MMCM*i*	Same as MMCM primitive	FALSE	boolean

Table 3: **Clock Generator Parameters (low level internal view) *(Cont'd)***

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_MMCM*i*_CLKOUT6_USE_FINE_PS	*i*-1,..,3, C_CLKOUT6_USE_FINE_PS of MMCM*i*	Same as MMCM primitive	FALSE	boolean
C_MMCM*i*_COMPENSATION	*i*-1,..,3, C_COMPENSATION of MMCM*i*	Same as MMCM primitive	ZHOLD	string
C_MMCM*i*_DIVCLK_DIVIDE	*i*-1,..,3, DIVCLK_DIVIDE of MMCM*i*	Same as MMCM primitive	1	integer
C_MMCM*i*_REF_JITTER1	*i*-1,..,3, REF_JITTER1 of MMCM*i*	Same as MMCM primitive	0.010	real
C_MMCM*i*_CLKIN1_BUF	*i*-1,..,3, C_CLKIN_BUF of MMCM*i*	Same as MMCM primitive	FALSE	real
C_MMCM*i*_CLKFBOUT_BUF	*i*-1,..,3, C_CLKFBOUT_BUF of MMCM*i*	Same as MMCM primitive	FALSE	boolean
C_MMCM*i*_CLOCK_HOLD	*i*-1,..,3, C_CLOCK_HOLD of MMCM*i*	Same as MMCM primitive	FALSE	boolean
C_MMCM*i*_STARTUP_WAIT	*i*-1,..,3, C_STARTUP_WAIT of MMCM*i*	Same as MMCM primitive	FALSE	boolean
C_MMCM*i*_EXT_RESET_HIGH	*i*-1,..,3, C_EXT_RESET_HIGH of MMCM*i*	Same as MMCM primitive	1	integer
C_MMCM*i*_FAMILY	*i*-1,..,3, C_FAMILY of MMCM*i*	Same as MMCM primitive	Virtex6	string
C_MMCM*i*_CLKOUT0_BUF	*i*-0,1, if TRUE, a BUFG is inserted for MMCM*i* CLKOUT0	TRUE/FALSE	FALSE	boolean
C_MMCM*i*_CLKOUT1_BUF	*i*-0,1, if TRUE, a BUFG is inserted for MMCM*i* CLKOUT1	TRUE/FALSE	FALSE	boolean
C_MMCM*i*_CLKOUT2_BUF	*i*-0,1, if TRUE, a BUFG is inserted for MMCM*i* CLKOUT2	TRUE/FALSE	FALSE	boolean
C_MMCM*i*_CLKOUT3_BUF	*i*-0,1, if TRUE, a BUFG is inserted for MMCM*i* CLKOUT3	TRUE/FALSE	FALSE	boolean
C_MMCM*i*_CLKOUT4_BUF	*i*-0,1, if TRUE, a BUFG is inserted for MMCM*i* CLKOUT4	TRUE/FALSE	FALSE	boolean
C_MMCM*i*_CLKOUT5_BUF	*i*-0,1, if TRUE, a BUFG is inserted for MMCM*i* CLKOUT5	TRUE/FALSE	FALSE	boolean
C_MMCM*i*_CLKOUT6_BUF	*i*-0,1, if TRUE, a BUFG is inserted for MMCM*i* CLKOUT6	TRUE/FALSE	FALSE	boolean
C_MMCM*i*_CLKIN1_MODULE	*i*-1,..,3, module connect to CLKIN1 of MMCM*i*	Same as C_CLKOUT*i*_MODULE	NONE	string
C_MMCM*i*_CLKIN1_PORT	*i*-1,..,3, port connect to CLKIN1 of MMCM*i*	Same as C_CLKOUT*i*_PORT	NONE	string

Table 3: **Clock Generator Parameters (low level internal view) *(Cont'd)***

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_MMCM*i*_CLKFBIN_MODULE	*i*-1,..,3, module connect to CLKFBIN of MMCM*i*	Same as C_CLKOUT*i*_MODULE	NONE	string
C_MMCM*i*_CLKFBIN_PORT	*i*-1,..,3, port connect to CLKFBIN of MMCM*i*	Same as C_CLKOUT*i*_PORT	NONE	string
C_MMCM*i*_RST_MODULE	*i*-0.3, module connect to RST of MMCM*i*	Same as C_CLKOUT*i*_MODULE	NONE	string

The parameter values in Table 3 are generated automatically from the parameter values in Table 2.

Parameter - Port Dependencies

Table 4 contains the effects of setting various parameters.

Table 4: **Clock Generator Parameter-Port Dependencies**

Parameter	Port	Description
C_CLKIN_FREQ	CLKIN	0 - CLKIN is not used
C_CLKFBIN_FREQ	CLKFBIN, CLKFBOUT	0 - CLKFBIN is not used. It has to be equal to C_CLKFBOUT_FREQ. The edges from CLKFBIN line up with the edges from the first *CLKOUTi (i=0, .., 15)* clock that has C_CLKOUT*i*_FREQ = C_CLKFBIN_FREQ.
C_CLKFBIN_DESKEW	CLKFBIN, CLKFBOUT	CLKFBIN clock deskew with CLKOUT
C_CLKOUT*i*_FREQ	CLKOUT*i* (*i*=0,..,15)	0 - CLKOUT*i* is not used
C_CLKOUT*i*_PHASE	CLKOUT*i* (*i*=0,..,15)	
C_CLKOUT*i*_GROUP	CLKOUT*i* (*i*=0,..,15)	NONE - CLKOUT*i* has no group requirement
C_CLKOUT*i*_BUF	CLKOUT*i* (*i*=0,..,15)	Set to FALSE if C_CLKOUT*i*_FREQ is 0
C_CLKOUT*i*_VARIABLE_PHASE	CLKOUT*i* (*i*=0,..,15)	Set MMCM clock USE_FINE_PS if CLKOUTi is variable phase shifted output of MMCM; see "Differences Between Clock Generator v3.02a and v3.01a" on page 12.
C_CLKFBOUT_FREQ	CLKFBIN, CLKFBOUT	0 - CLKFBOUT is not used; has to be equal to C_CLKFBIN_FREQ
C_CLKFBOUT_GROUP	CLKFBIN, CLKFBOUT	NONE - Do not specify MMCM for external feedback
C_CLKFBOUT_BUF	CLKFBOUT	Set to FALSE if C_CLKBOUT_FREQ is 0
C_PSDONE_GROUP	PSDONE	NONE - Do not specify MMCM connected to variable phase shift control signal

Differences Between Clock Generator v3.02a and v3.01a

The differences between versions 3.01a and 3.02a determine how the core is used in Virtex-6 FPGA designs with variable phase enabled clocks.

When the variable phase on the feedback clock is *not* enabled, the value of parameter C_PSDONE_GROUP is MMCM<i>_FB — there is no difference between the 2 versions.

Although the value of parameter C_PSDONE_GROUP remains at MMCMi_FB when the variable phase on the feedback clock is enabled, the values of parameter C_CLKOUTi have opposite implications between the two versions.

For v3.01.a core, when C_CLKOUT<i>_VARIABLE_PHASE is TRUE, the corresponding clock output from the core has a fixed phase shift. When the value is FALSE, the phase of the corresponding clock output from the core is dynamically shifted.

For v3.02.a core, when C_CLKOUT<i>_VARIABLE_PHASE is FALSE, the corresponding clock output from the core has fixed phase shift; when the value is TRUE, the phase of the corresponding clock output from the core is dynamically shifted.

The differences are summarized in Table 5 and Table 6.

Table 5: **Variable Phase Shift Parameters, their Values and the Implications in v3.01a**

C_PSDONE_GROUP	C_CLKOUTi_VARIABLE_PHASE	Phase Shift of CLKOUTi
MMCMi (i=0~3) or NONE	TRUE	Variable phase shift.
MMCMi (i=0~3) or NONE	FALSE	Fixed phase shift.
MMCMi_FB (i=0~3)	TRUE	Fixed phase shift.
MMCMi_FB (i=0~3)	FALSE	Variable phase shift.

Table 6: **Variable Phase Shift Parameters, their Values, and the Implications in v3.02a**

C_PSDONE_GROUP	C_CLKOUTi_VARIABLE_PHASE	Phase Shift of CLKOUTi
MMCMi (i=0~3) or NONE	TRUE	Variable phase shift.
MMCMi (i=0~3) or NONE	FALSE	Fixed phase shift.
MMCMi_FB (i=0~3)	TRUE	Variable phase shift.
MMCMi_FB (i=0~3)	FALSE	Fixed phase shift.

Below is an example Virtex-6 FPGA design using the v3.01a core:

```
BEGIN clock_generator
 PARAMETER INSTANCE = clock_generator_0
 PARAMETER HW_VER = 3.01.a
 PARAMETER C_EXT_RESET_HIGH = 1
 PARAMETER C_CLKIN_FREQ = 200000000
 PARAMETER C_CLKOUT0_FREQ = 400000000
 PARAMETER C_CLKOUT0_BUF = TRUE
 PARAMETER C_CLKOUT0_PHASE = 0
 PARAMETER C_CLKOUT0_GROUP = MMCM0
 PARAMETER C_CLKOUT0_VARIABLE_PHASE = TRUE
 PARAMETER C_CLKOUT1_FREQ = 200000000
 PARAMETER C_CLKOUT1_BUF = TRUE
 PARAMETER C_CLKOUT1_PHASE = 0
 PARAMETER C_CLKOUT1_GROUP = MMCM0
 PARAMETER C_CLKOUT1_VARIABLE_PHASE = TRUE
 PARAMETER C_CLKOUT2_FREQ = 400000000
 PARAMETER C_CLKOUT2_BUF = FALSE
 PARAMETER C_CLKOUT2_PHASE = 0
 PARAMETER C_CLKOUT2_GROUP = MMCM0
 PARAMETER C_CLKOUT3_FREQ = 100000000
 PARAMETER C_CLKOUT3_BUF = TRUE
 PARAMETER C_CLKOUT3_PHASE = 0
 PARAMETER C_CLKOUT3_GROUP = MMCM0
 PARAMETER C_CLKOUT3_VARIABLE_PHASE = TRUE
 PARAMETER C_CLKOUT4_FREQ = 125000000
 PARAMETER C_CLKOUT4_BUF = TRUE
 PARAMETER C_CLKOUT4_PHASE = 0
 PARAMETER C_CLKOUT4_GROUP = MMCM1
 PARAMETER C_CLKOUT5_FREQ = 200000000
 PARAMETER C_CLKOUT5_BUF = TRUE
 PARAMETER C_CLKOUT5_PHASE = 0
 PARAMETER C_CLKOUT5_GROUP = MMCM1
```

```
 PARAMETER C_PSDONE_GROUP = MMCM0_FB
 PORT CLKOUT0 = Clk_400_0000MHzMMCM0
 PORT CLKOUT1 = Clk_200_0000MHzMMCM0
 PORT CLKOUT2 = Clk_400_0000MHzMMCM0_nobuf_varphase
 PORT CLKOUT3 = clk_100_0000MHzMMCM0
 PORT CLKOUT4 = clk_125_0000MHzMMCM1
 PORT CLKOUT5 = clk_200_0000MHzMMCM1
 PORT PSCLK = Clk_200_0000MHzMMCM0
 PORT PSDONE = MPMC_DCM_PSDONE
 PORT PSEN = MPMC_DCM_PSEN
 PORT PSINCDEC = MPMC_DCM_PSINCDEC
 PORT CLKIN = dcm_clk_s
 PORT LOCKED = clock_generator_0_locked
 PORT RST = sys_rst_s
END
```

To generate the same clocking circuitry using v3.02a core, the following changes must be performed:

- Remove parameter C_CLKOUT0_VARIABLE_PHASE or set its value to FALSE. Do the same to parameter C_CLKOUT1_VARIABLE_PHASE and C_CLKOUT3_VARIABLE_PHASE.
- Add parameter C_CLKOUT2_VARIABLE_PHASE and set its value to TRUE

Below is an example Virtex-6 FPGA design after the changes have been made:

```
BEGIN clock_generator
 PARAMETER INSTANCE = clock_generator_0
 PARAMETER HW_VER = 3.02.a
 PARAMETER C_EXT_RESET_HIGH = 1
 PARAMETER C_CLKIN_FREQ = 200000000
 PARAMETER C_CLKOUT0_FREQ = 400000000
 PARAMETER C_CLKOUT0_BUF = TRUE
 PARAMETER C_CLKOUT0_PHASE = 0
 PARAMETER C_CLKOUT0_GROUP = MMCM0
 PARAMETER C_CLKOUT1_FREQ = 200000000
 PARAMETER C_CLKOUT1_BUF = TRUE
 PARAMETER C_CLKOUT1_PHASE = 0
 PARAMETER C_CLKOUT1_GROUP = MMCM0
 PARAMETER C_CLKOUT2_FREQ = 400000000
 PARAMETER C_CLKOUT2_BUF = FALSE
 PARAMETER C_CLKOUT2_PHASE = 0
 PARAMETER C_CLKOUT2_GROUP = MMCM0
 PARAMETER C_CLKOUT2_VARIABLE_PHASE = TRUE
 PARAMETER C_CLKOUT3_FREQ = 100000000
 PARAMETER C_CLKOUT3_BUF = TRUE
 PARAMETER C_CLKOUT3_PHASE = 0
 PARAMETER C_CLKOUT3_GROUP = MMCM0
 PARAMETER C_CLKOUT4_FREQ = 125000000
 PARAMETER C_CLKOUT4_BUF = TRUE
 PARAMETER C_CLKOUT4_PHASE = 0
 PARAMETER C_CLKOUT4_GROUP = MMCM1
 PARAMETER C_CLKOUT5_FREQ = 200000000
 PARAMETER C_CLKOUT5_BUF = TRUE
 PARAMETER C_CLKOUT5_PHASE = 0
```

```
 PARAMETER C_CLKOUT5_GROUP = MMCM1
 PARAMETER C_PSDONE_GROUP = MMCM0_FB
 PORT CLKOUT0 = Clk_400_0000MHzMMCM0
 PORT CLKOUT1 = Clk_200_0000MHzMMCM0
 PORT CLKOUT2 = Clk_400_0000MHzMMCM0_nobuf_varphase
 PORT CLKOUT3 = clk_100_0000MHzMMCM0
 PORT CLKOUT4 = clk_125_0000MHzMMCM1
 PORT CLKOUT5 = clk_200_0000MHzMMCM1
 PORT PSCLK = Clk_200_0000MHzMMCM0
 PORT PSDONE = MPMC_DCM_PSDONE
 PORT PSEN = MPMC_DCM_PSEN
 PORT PSINCDEC = MPMC_DCM_PSINCDEC
 PORT CLKIN = dcm_clk_s
 PORT LOCKED = clock_generator_0_locked
 PORT RST = sys_rst_s
END
```

Register Descriptions

Not Applicable.

Interrupt Descriptions

Not Applicable.

Design Implementation

Target Technology

The target technology is an FPGA listed in the Supported Device Family field of the LogiCORE IP Facts table.

Device Utilization and Performance Benchmarks

The device utilization depends on the number of output clocks used and the value of the parameters of each output clock. Up to four DCM modules, two PLL modules, and four MMCM modules may be instanced with BUFGs, clock inverters, and reset logics. See respective FPGA family user guide for details on DCM, PLL, MMCM, and BUFG primitive performance and available resources.

In one Clock Generator v3.02a module:

- Virtex-6 family FPGAs will use up to four MMCMs (no DCM or PLL)
- Virtex-5 and Spartan-6 family FPGAs will use up to 2 PLLs and 4 DCMs (no MMCM)
- All other FPGA families will use up to 4 DCMs (no PLL or MMCMs)

Specification Exceptions

Not Applicable.

Reference Documents

None.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Revision History

Date	Version	Description of Revisions
5/15/07	1.0	Initial Xilinx release.
1/16/08	1.1	Released v2.00a; added PLL support.
4/22/08	1.2	Released v2.01a; added Automotive SP3E, SP3A, SP3, and SP3A DSP support.
7/25/08	1.3	Added QPro Virtex-4 Hi-Rel, QPro Virtex-4 Rad Tolerant, and SP-3AN support.
3/31/09	1.4	Release v3.00a, changed C_CLK_GEN parameter, removed obsolete parameters.
6/24/09	1.5	Released v3.01a; added MMCM support.
12/2/09	1.6	Created v3.02a for EDK_L 11.4 release.

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