FX12 Board Reference Manual

Featuring the Xilinx Virtex-4 FPGA

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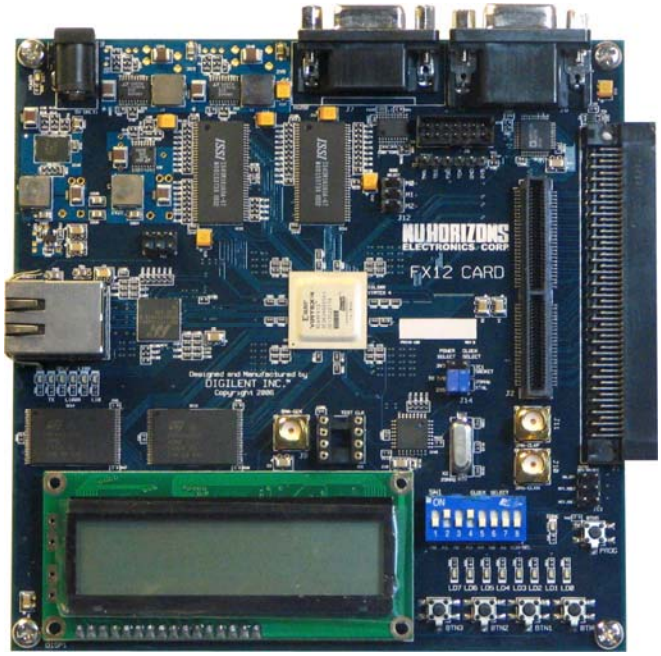
Overview

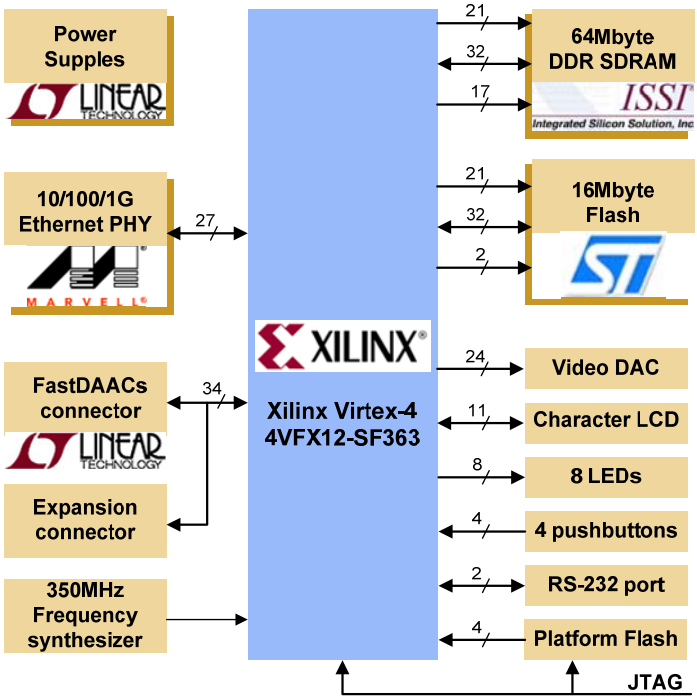
The Digilent FX12 board (the FX12) is an integrated circuit development platform for Xilinx's Virtex-4 FX12 FPGA. The FX12 is based on Xilinx's newest programmable architecture and contains a PowerPC core, dual Ethernet MACs, 32 XtremeDSP slices, 80Kbytes of block RAM, advanced clock management, and flexible I/O's. The FX12 also features external memories, a flexible time base, power supplies, an Ethernet PHY, ports, and other I/O devices.



The FX12 provides an ideal platform for investigating a new generation of highly integrated designs made possible by Xilinx's Virtex-4 family.

Features include:

- a Virtex-4 FX12 FPGA
- JTAG programming port that can accommodate all Digilent and Xilinx programming cables
- XCF08S Xilinx Platform Flash ROM to store FPGA configurations
- Marvell 88E1111 "Alaska" Gigabit PHY
- 24-bit Analog Devices high-speed Video DAC
- 64 Mbytes of ISSI DDR SDRAM
- 16 Mbytes of Micron Flash ROM
- high-current Linear Technology switching power supplies
- Linear Technology FastDAACS connector for driving high-speed analog peripherals
- user-settable Integrated Circuit System frequency synthesizer (up to 350MHz)
- on board serial port, LCD display, buttons, switches, and LEDs
- high-speed-capable expansion connector



FX12 Block Diagram

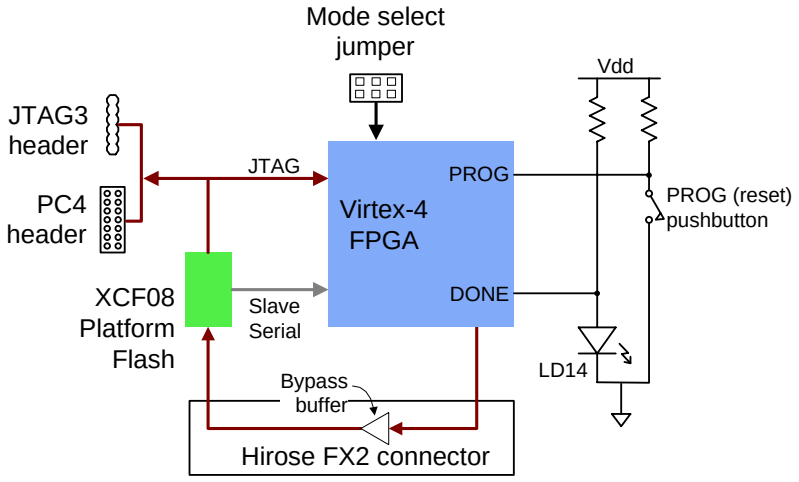
Functional Description

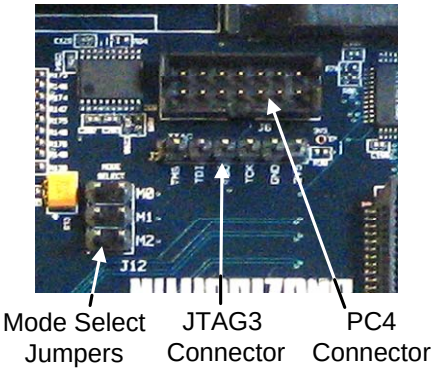
The FX12 showcases the many advanced features of Xilinx's Virtex-4 FPGA, especially its ability to serve as the single device at the core of an embedded system. The FX12 includes a host of advanced features, including an embedded PowerPC core, a hard-IP MAC, XtremeDSP slices that include fast hardware multipliers, advanced clock management, Smart RAM, and other features, bringing new capabilities to highly-integrated embedded platforms. The FX12 board enhances the abilities of the FPGA by adding peripheral devices such as 64Mbytes of DDR memory, 16Mbytes of Flash ROM, and an Ethernet port, making it well suited to support a variety of embedded system designs.

The FX12 is supported by world-class design tools, including ISE, Chipscope-Pro, Embedded developers Kit (EDK), and System Generator.

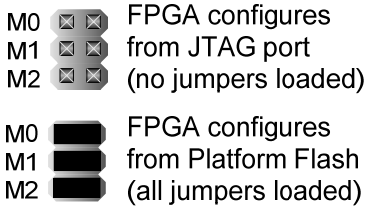
JTAG Ports and Device Configuration

The FX12 can be programmed from a PC or directly from an on-board Flash ROM at power-on. PC programming requires a programming cable such as Digilent's JTAG3 or JTAG-USB cable, or Xilinx's PC4 or Platform USB cable. Programming files for the Virtex-4 and XCF08 Platform Flash ROM can be created using Xilinx's ISE or EDK software, or a variety of other third-party tools. Please refer to the appropriate CAD tool reference materials for information on creating programming files.





A .bit file may be programmed into the FPGA from a PC by setting the mode jumpers to "JTAG" mode, attaching a programming cable to the PC and to one of the two programming headers (JTAG3 or PC4), and running Digilent's Adept software or Xilinx's iMPACT programming tool (Adept is a free download from the Digilent website and iMPACT is a free download from the Xilinx website). The configuration software will automatically identify all devices in the scan chain, and allow the FPGA and ROM to either be bypassed individually, or programmed individually with any available .bit or .mcs file. Note that both the FPGA and Platform Flash ROM will always appear in the scan chain. If a JTAG-aware peripheral board is attached to the Hirose FX2 expansion connector, it will appear in the scan chain between the FPGA and Platform Flash.



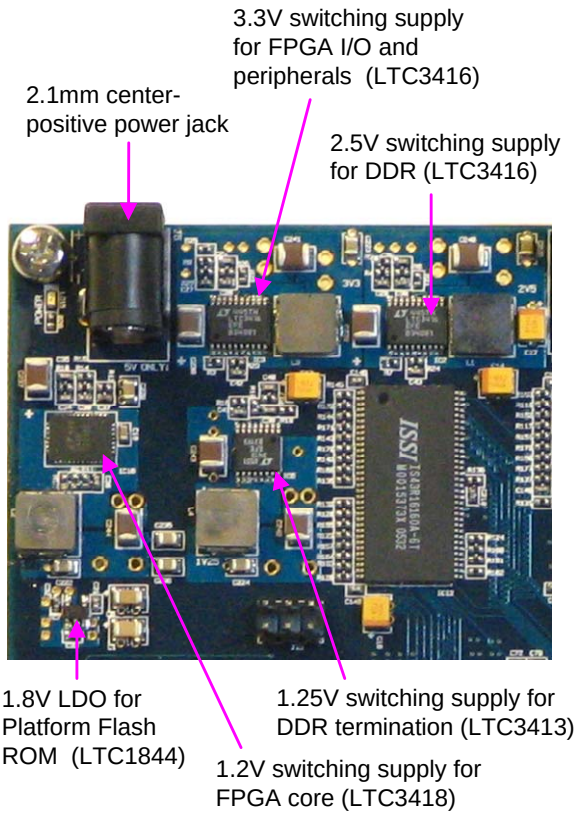
Mode Select Jumper Settings

After the Platform Flash ROM has been loaded with a configuration file, the FPGA can load that file at power-on if the mode select jumpers are set in the Platform Flash position.

An FPGA system-reset button labeled PROG has been provided to allow a user-initiated FPGA reset. Pressing the PROG button will clear all configuration memory and cause the FPGA to await the next programming cycle. An LED on the DONE signal will illuminate at the end of a successful configuration.

Power Supplies

Power is delivered to the FX12 board via a 2.1mm, center-positive power connector that can be driven from any suitable 4VDC-5.5VDC source (like a wall-plug supply). Power is routed from the connector to four switching regulators and single LDO that produce all required supply voltages. Input power is also routed directly to the character LCD and high-speed expansion connector (pins A49 and A50) for use by peripheral circuits.



FX12 Power Supplies

Current Consumption

Total board current is dependant on FPGA configuration, synthesizer clock frequency, and external connections. In test configurations using the PPC core to run DDR and Flash memory tests, with roughly 10% of the FPGA routed and a 100MHz input clock, approximately 650mA of supply current is drawn from the main power supply. Required current will increase if larger circuits are configured in the FPGA, if clock frequency is increased, and if peripheral boards are attached.

Power Distribution

The FX12 uses an eight-layer PCB, with the stack-up shown in the table. The Vdd planes are split into several localized islands to accommodate the various component's supply voltage requirements. Bulk ceramic bypass capacitors are placed strategically around the board, and every component Vdd pin has one, two, or three local bypass caps in the .001 to .047uF range. The power supply routing and bypass capacitors result in a very clean low-noise power supply.

FX12 Stack-Up

Layer	Usage	Copper
1	Signal	1 oz.
2	GND	.5 oz.
3	Signal	.5 oz.
4	Vdd	.5 oz.
5	Vdd	.5 oz.
6	Signal	.5 oz.
7	GND	.5 oz.
8	Signal	1 oz.

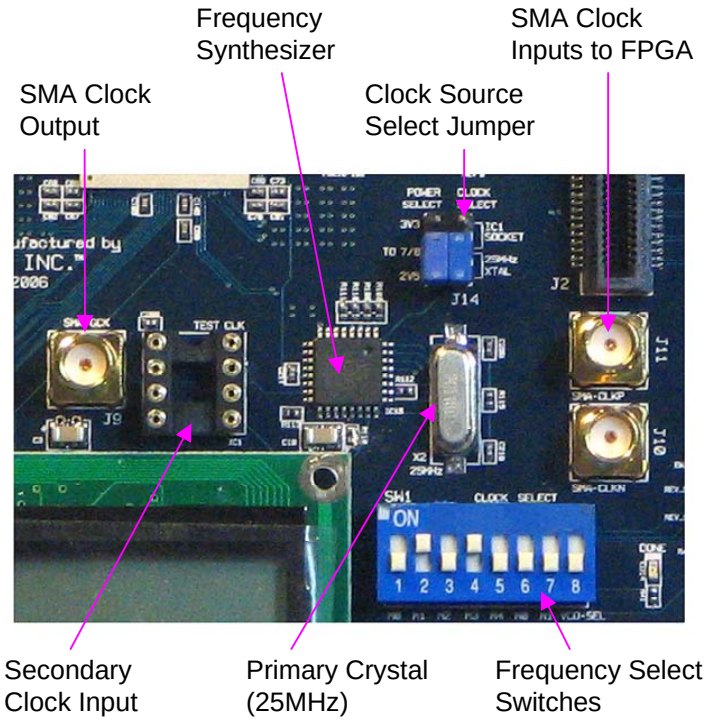
Supply Details

Supply	Max Current	Regulator Part Number	Devices Powered	Notes
3.3V	4A	LTC3416	• Hirose expansion connector • Xilinx FPGA I/O banks 2, 4, 6, 7, and 8 • Micron Flash memory • RS-232 level shifter • Analog Devices Video DAC • ICS frequency synthesizer	Uses oversized 3.3uH inductor for stability at low current.
2.5V	4A	LTC3416	• Xilinx Platform Flash • Xilinx FPGA I/O banks 1, 3, 5, 7, and 8 • ISSI DDR DRAM's • Marvell 88E1111 Ethernet PHY	Uses oversized 3.3uH inductor for stability at low current.
1.8V	150mA	LTC1844	• Xilinx Platform Flash	
1.25V	2A	LTC3413	• DDR termination networks	Uses oversized 1.5uH inductor for stability at low current.
1.2V	8A	LTC3418	• Xilinx FPGA core • Marvell PHY core	

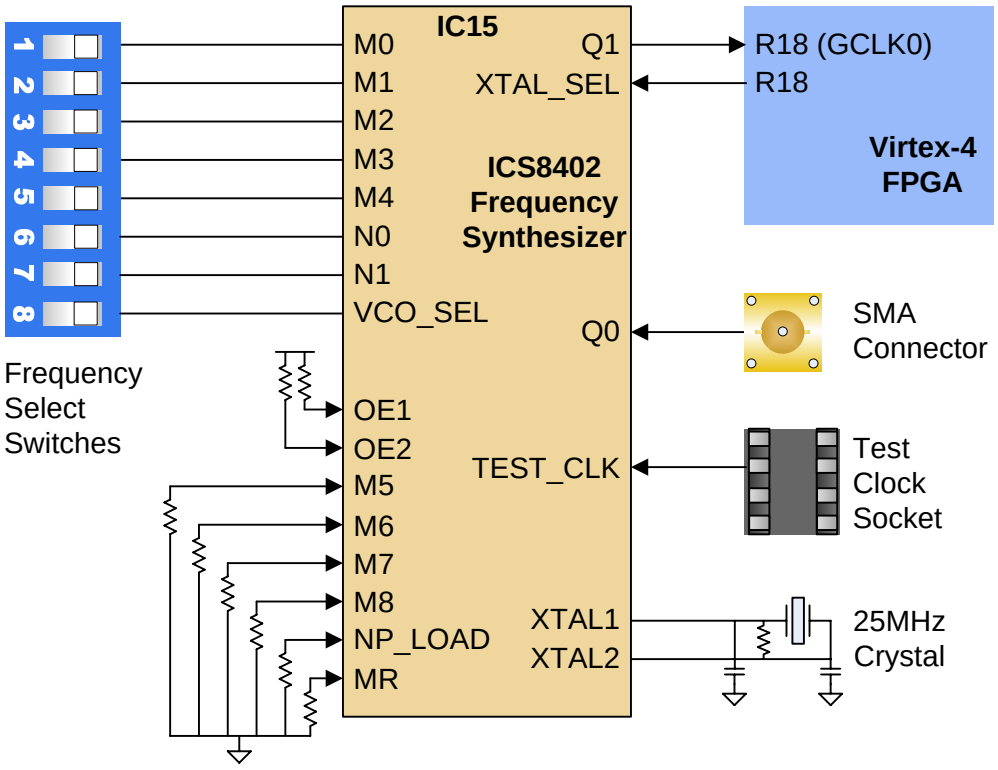
Oscillator

The FX12 includes a 350MHz, crystal-to-LVCMOS frequency synthesizer from Integrated Circuit Systems Inc (PN ICS8402). The synthesizer gets its primary frequency input from a 25MHz crystal, and then multiplies that input up to the desired output frequency. The output frequency is selected by the DIP switches at SW1, according to the table in Appendix A. The clock output from the synthesizer is delivered to the FPGA on the GCLK0 input at pin Y5.

A secondary input is also available to drive a different base frequency into the synthesizer. The socket labeled "test_clk" can accommodate any 12-40MHz LVCMOS oscillator in a half-DIP package. This secondary source will drive the synthesizer if the XTAL_SEL signal is driven high from the FPGA. The oscillator circuit is shown in the accompanying figure. Please see the ICS8402 data sheet for further information.



FX12 Oscillator Circuit



FX12 Frequency Synthesizer Diagram

DDR

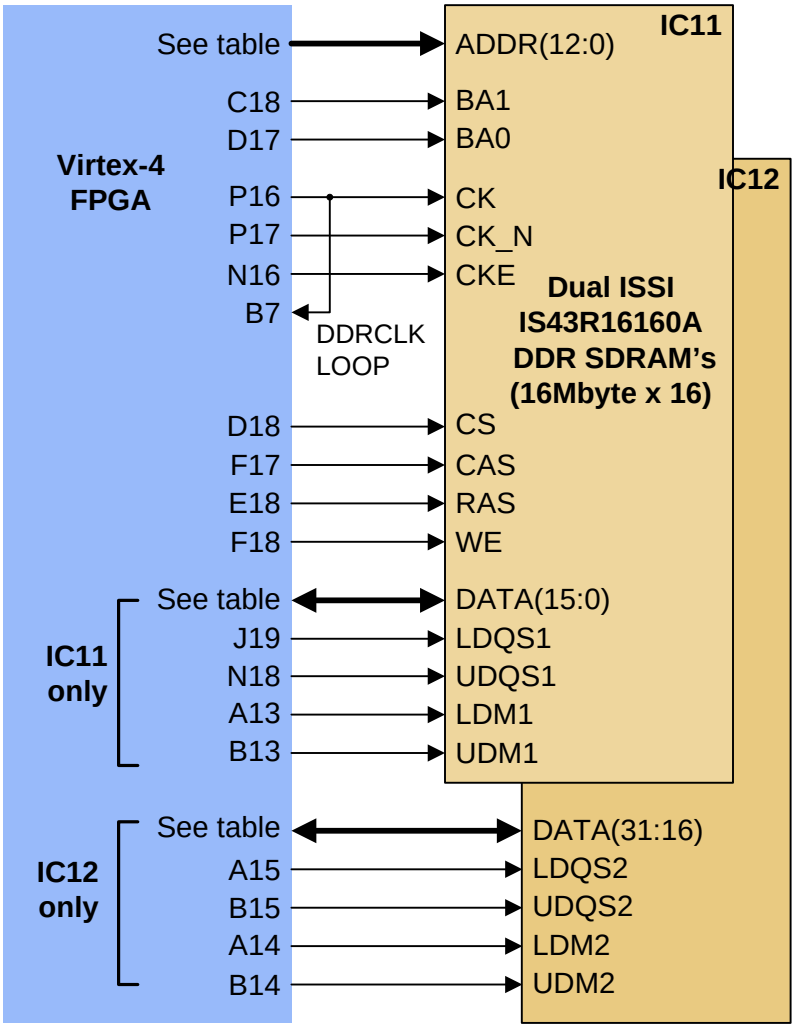
The 64Mbyte DDR memory array consists of two 32Mbyte (16M x 16) ISSI IS43R16160A-6T devices connected as a 16M x 32 array. Individual byte selects for both memories are brought to the FPGA so byte, word, and long-word read/writes are possible. A differential clock is routed from the FPGA to the memories, and a length-matched clock return is routed back to the FPGA to allow for timing optimization. All data signals are delay and impedance matched (with 48-ohm trace impedance), and all DDR signals are actively terminated through 47-ohm resistors to a 1.25V supply for optimal bus performance.

UCF File

Signals routed to the DDR SDRAM should use the SSTL2_I standard as shown in the example .ucf file entry below. All VREF pins on Bank 5 (used by the DDR signal connections) should have "prohibit" constraints in the .ucf file to prohibit software from assigning these pins to other functions.

```
NET    "DDR_D0"     LOC = "P20"  |  IOSTANDARD  =  SSTL2_I ;

CONFIG PROHIBIT = C17;
```



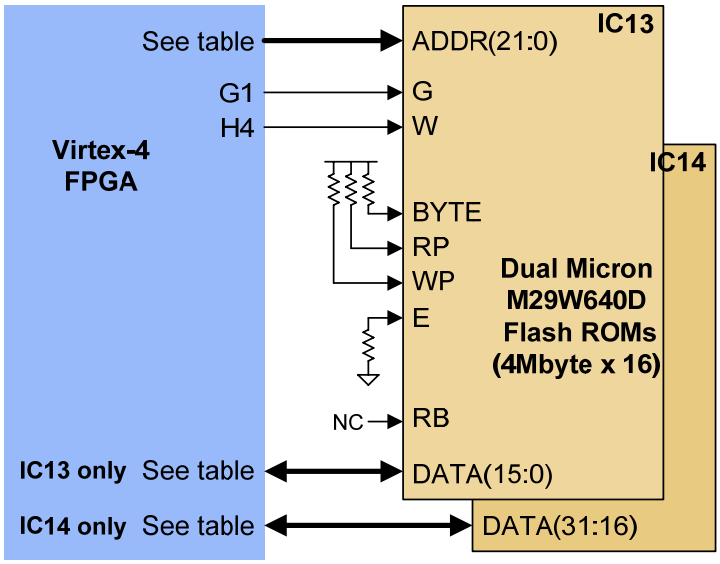
FX12 DDR Circuit Diagram

DDR Address Pins	
ADDR12	M15
ADDR11	M16
ADDR10	F16
ADDR9	K17
ADDR8	K16
ADDR7	J15
ADDR6	J16
ADDR5	H16
ADDR4	G16
ADDR3	C15
ADDR2	C16
ADDR1	D16
ADDR0	E16

DDR Data Pins			
DATA31	H18	DATA15	G17
DATA30	H20	DATA14	H17
DATA29	G20	DATA13	J17
DATA28	G19	DATA12	J18
DATA27	F20	DATA11	K18
DATA26	F19	DATA10	M18
DATA25	E20	DATA9	M17
DATA24	D19	DATA8	N17
DATA23	A16	DATA7	K20
DATA22	B16	DATA6	K19
DATA21	B17	DATA5	L20
DATA20	A18	DATA4	M19
DATA19	B18	DATA3	M20
DATA18	B19	DATA2	N19
DATA17	C19	DATA1	P19
DATA16	C20	DATA0	P20

Flash Memory

The FX12 contains two Micron M29W64OD 4Mbyte Flash devices, for a total of 8Mbytes. The Flash array is organized as a 2M x 32 array, with all control signals routed in parallel to the two devices.



FX12 Flash Circuit Diagram

Flash Address Pins				
ADDR21	H3		ADDR10	D3
ADDR20	G4		ADDR9	E3
ADDR19	F3		ADDR8	F4
ADDR18	J4		ADDR7	K4
ADDR17	J3		ADDR6	K3
ADDR16	C6		ADDR5	L4
ADDR15	C5		ADDR4	M3
ADDR14	D5		ADDR3	M4
ADDR13	C4		ADDR2	L5
ADDR12	D4		ADDR1	M5
ADDR11	C11		ADDR0	M6

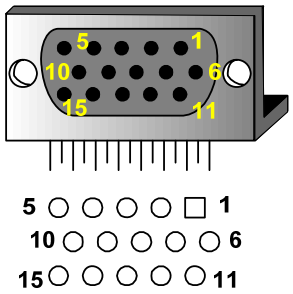
Flash Data Pins				
DATA31	A6		DATA15	H2
DATA30	A5		DATA14	J2
DATA29	B4		DATA13	K1
DATA28	B3		DATA12	L1
DATA27	C2		DATA11	M2
DATA26	D2		DATA10	F5
DATA25	E1		DATA9	H5
DATA24	F1		DATA8	J5
DATA23	B6		DATA7	H1
DATA22	B5		DATA6	K2
DATA21	A3		DATA5	L2
DATA20	B2		DATA4	M1
DATA19	C1		DATA3	E5
DATA18	E2		DATA2	G5
DATA17	F2		DATA1	J6
DATA16	G2		DATA0	K5

VGA Port

The five standard VGA signals Red, Green, Blue, Horizontal Sync (HS), and Vertical Sync (VS) available at the VGA connector arise from the FPGA (sync signals) and an Analog Devices ADV7125 high speed video DAC (color signals). The video DAC presents three parallel 8-bit data ports to the

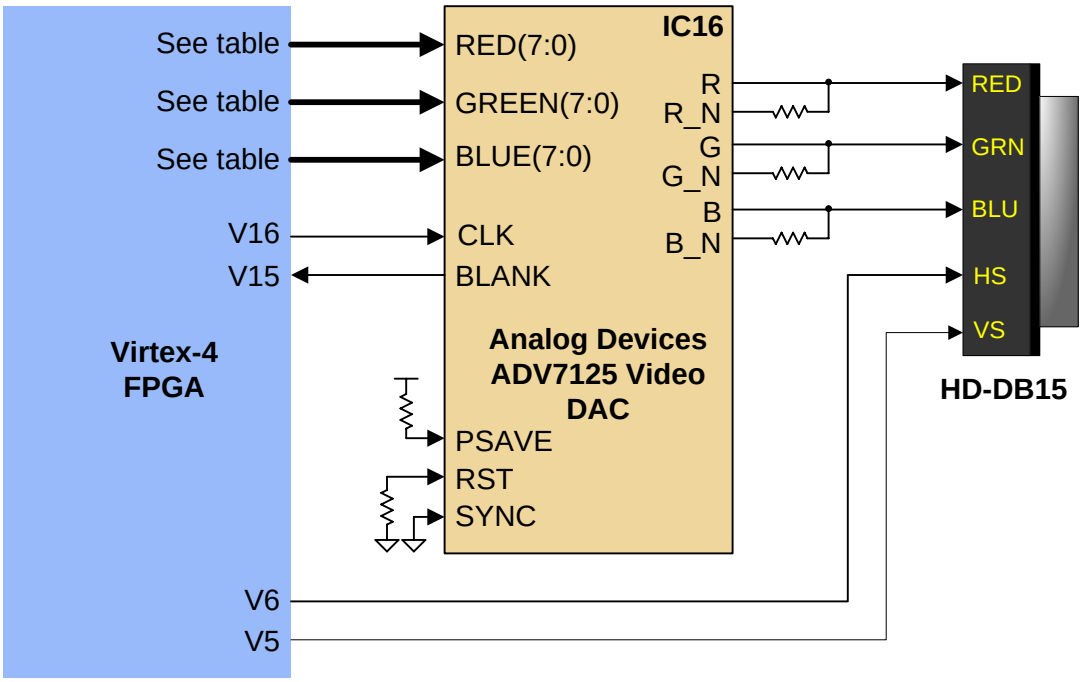
FPGA, and the inputs to those ports determine the corresponding color signal voltage delivered to the VGA connector. The sync signals must be produced by a controller residing in the FPGA.

VGA signal timings are specified, published, copyrighted and sold by the VESA organization (www.vesa.org). The following VGA system timing information is provided as an example of how a VGA monitor might be driven in 640 by 480 mode. For more precise information, or for information on higher VGA frequencies, refer to documentation available at the VESA website.



Pin	Signal	Pin	Signal
1	Red	9	NC
2	Green	10	GND
3	Blue	11	NC
4	NC	12	NC
5	GND	13	HS
6	GND	14	VS
7	GND	15	NC
8	GND		

HD DB-15 connector, PCB hole pattern, and pin assignments



FX12 VGA Circuit Diagram

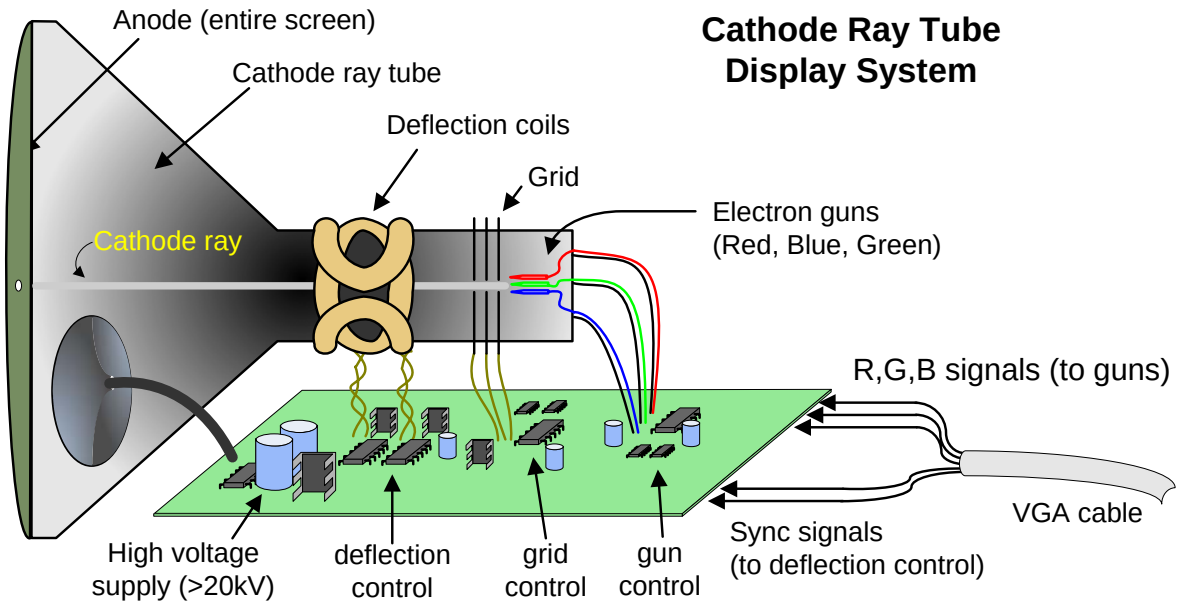
RED	
RED7	V8
RED6	U9
RED5	V9
RED4	V10
RED3	V11
RED2	V12
RED1	U1
RED0	V13

GREEN	
GREEN7	W10
GREEN6	Y11
GREEN5	W11
GREEN4	Y12
GREEN3	W12
GREEN2	W13
GREEN1	T7
GREEN0	U8

BLUE	
BLUE75	W6
BLUE6	W5
BLUE5	W7
BLUE4	Y7
BLUE3	W8
BLUE2	W9
BLUE1	Y9
BLUE0	Y10

VGA System Timing

CRT-based VGA displays use amplitude-modulated moving electron beams (or cathode rays) to display information on a phosphor-coated screen. LCD displays use an array of switches that can impose a voltage across a small amount of liquid crystal, thereby changing light permitivity through the crystal on a pixel-by-pixel basis. Although the following description is limited to CRT displays, LCD displays have evolved to use the same signal timings as CRT displays (so the "signals" discussion below pertains to both CRTs and LCDs). Color CRT displays use three electron beams (one for red, one for blue, and one for green) to energize the phosphor that coats the inner side of the display end of a cathode ray tube (see illustration). Electron beams emanate from "electron guns", which are finely-pointed heated cathodes placed in close proximity to a positively charged annular plate called a "grid". The electrostatic force imposed by the grid pulls rays of energized electrons from the cathodes, and those rays are fed by the current that flows into the cathodes. These particle rays are initially accelerated towards the grid, but they soon fall under the influence of the much larger electrostatic force that results from the entire phosphor-coated display surface of the CRT being charged to 20kV (or more). The rays are focused to a fine beam as they pass through the center of the grids, and then

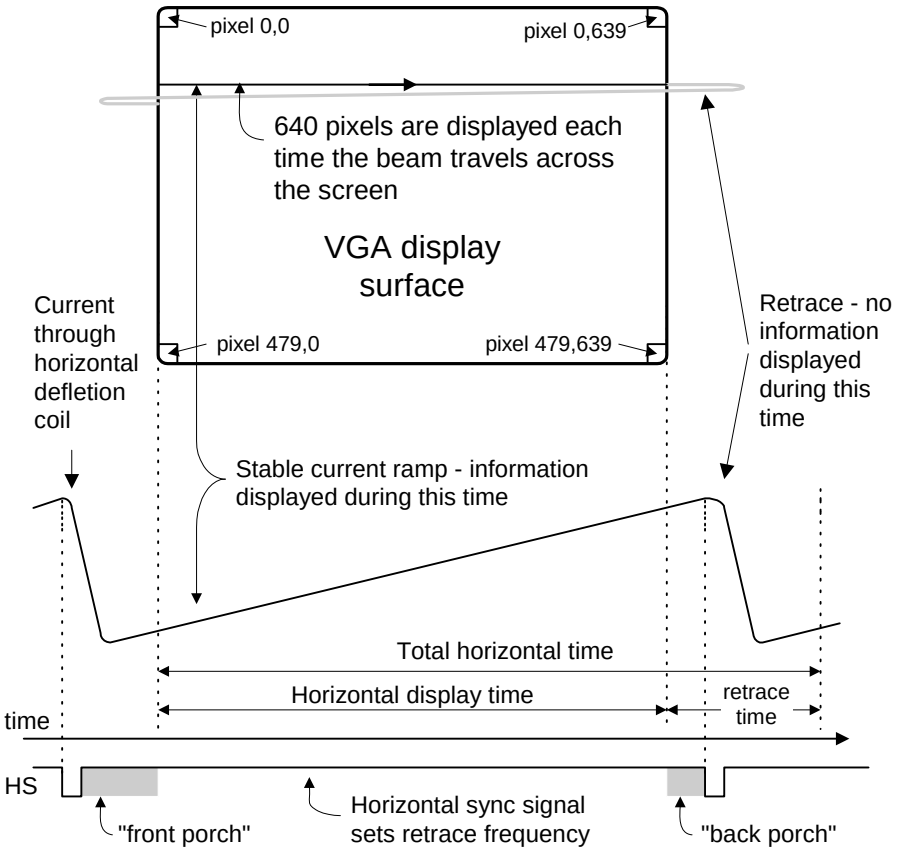


they accelerate to impact on the phosphor-coated display surface. The phosphor surface glows brightly at the impact point, and the phosphor continues to glow for several hundred microseconds after the beam is removed. The larger the current fed into the cathode, the brighter the phosphor will glow.

Between the grid and the display surface, the beam passes through the neck of the CRT where two coils of wire produce orthogonal electromagnetic fields. Because cathode rays are composed of charged particles (electrons), they can be deflected by these magnetic fields. Current waveforms are passed through the coils to produce magnetic fields that interact with the cathode rays and cause them to transverse the display surface in a "raster" pattern, horizontally from left to right and vertically from top to bottom. As the cathode ray moves over the surface of the display, the current sent to the electron guns can be increased or decreased to change the brightness of the display at the cathode ray impact point.

Information is only displayed when the beam is moving in the “forward” direction (left to right and top to bottom), and not during the time the beam is reset back to the left or top edge of the display. Much of the potential display time is therefore lost in “blanking” periods when the beam is reset and stabilized to begin a new horizontal or vertical display pass. The size of the beams, the frequency at which the beam can be traced across the display, and the frequency at which the electron beam can be modulated determine the display resolution. Modern VGA displays can accommodate different resolutions, and a VGA controller circuit dictates the resolution by producing timing signals to control the raster patterns. The controller must produce synchronizing pulses at 3.3V (or 5V) to set the frequency at which current flows through the deflection coils, and it must ensure that video data is applied to the electron guns at the correct time. Raster video displays define a number of “rows” that corresponds to the number of horizontal passes the cathode makes over the display area, and a number of “columns” that corresponds to an area on each row that is assigned to one “picture element” or pixel. Typical displays use from 240 to 1200 rows and from 320 to 1600 columns. The overall size of a display and the number of rows and columns determines the size of each pixel.

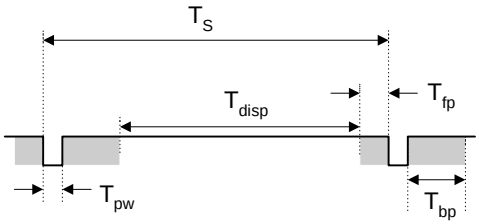
Video data typically comes from a video refresh memory, with one or more bytes assigned to each pixel location (the FX12 uses 8-bits per pixel). The controller must index into video memory as the beams move across the display, and retrieve and apply video data to the display at precisely the time the electron beam is moving across a given pixel.



A VGA controller circuit must generate the HS and VS timings signals and coordinate the delivery of video data based on the pixel clock. The pixel clock defines the time available to display one pixel of information. The VS signal defines the “refresh” frequency of the display, or the frequency at which all information on the display is redrawn. The minimum refresh frequency is a function of the display’s phosphor and electron beam intensity, with practical refresh frequencies falling in the 50Hz to 120Hz range. The number of lines to be displayed at a given refresh frequency defines the horizontal “retrace” frequency. For a 640-pixel by 480-row display using a 25MHz pixel clock and 60 +/-1Hz refresh, the signal timings shown in the table below can be derived. Timings for sync pulse width and front and back porch intervals (porch intervals are the pre- and post-sync pulse times during which information cannot be displayed) are based on observations taken from actual VGA displays.

A VGA controller circuit decodes the output of a horizontal-sync counter driven by the pixel clock to generate HS signal timings. This counter can be used to locate any pixel location on a given row. Likewise, the output of a vertical-sync counter that increments with each HS pulse can be used to generate VS signal timings, and this counter can be used to locate any given row. These two continually running counters can be used to form an address into video RAM. No time relationship between the onset of the HS pulse and the onset of the VS pulse is specified, so the designer can arrange the counters to easily form video RAM addresses, or to minimize decoding logic for sync pulse generation.

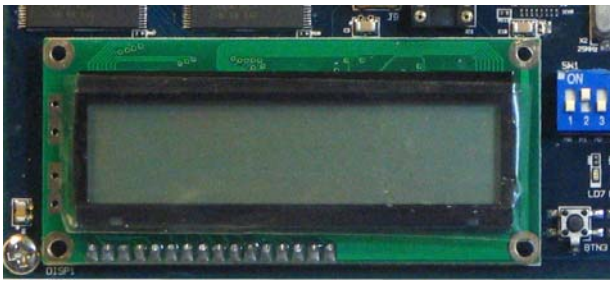
Symbol	Parameter	Vertical Sync			Horizontal Sync	
		Time	Clocks	Lines	Time	Clocks
T_S	Sync pulse time	16.7ms	416,800	521	32 us	800
T_{disp}	Display time	15.36ms	384,000	480	25.6 us	640
T_{pw}	VS pulse width	64 us	1,600	2	3.84 us	96
T_{fp}	VS front porch	320 us	8,000	10	640 ns	16
T_{bp}	VS back porch	928 us	23,200	29	1.92 us	48



Signal Timings

LCD

The FX12 contains a 16x2 character LCD manufactured by PowerTip (PN 1602D – see www.powertip.com.tw). The display uses an LCD controller IC compatible with the Samsung KS066U and Sitronix ST7066U devices. All pins are routed directly to the Virtex FPGA as shown below.



The LCD controller contains a character-generator ROM (CGROM) with 208 preset 5x8 character patterns, a character-generator RAM (CGRAM) that can hold eight user-defined 5x8 characters, and a display data RAM (DDRAM) that can hold 80 character codes. Character codes written into the DDRAM serve as indexes into the CGROM (or CGRAM). Writing a character code into a particular DDRAM location will cause the associated character to appear at the corresponding display location. Display positions can be shifted left or right by setting a bit in the instruction register (IR). The write-only IR directs display operations (such as clear display, shift left or right, set DDRAM address, etc). Available instructions (and the associated IR codes) are shown in the right-most column of the “LCD Instructions and Codes” table below. A busy flag shows whether the display has competed the last requested operation; prior to initiating a new operation, the flag can be checked to see if the previous operation has been completed.

The display has more DDRAM locations than can be displayed at any given time. DDRAM locations 00H to 27H map to the first display row, and locations 40H to 67H map to the second row. Normally, DDRAM location 00H maps to the upper left display corner, and 40H to the lower left. Shifting the display left or right can change this mapping. The display uses a temporary data register (DR) to hold data during DDRAM /CGRAM reads or writes, and an internal address register to select the RAM location. Address register contents, set via the IR, are automatically incremented after each read or write operation. The LCD display uses ASCII character codes. Codes up through 7F are standard

ASCII (which includes all “normal” alphanumeric characters). Codes above 7F produce various international characters – please see the manufacturers data sheet for more information on international codes.

The display is connected to the FX12 board by a 16-pin connector (pins 15 and 16 are for an optional backlight, and they are not used). The 14-pin interface includes eight data signals, three control signals, and three voltage supply signals. The eight data bus signals are passed through the CPLD to/from the system bus for read/write cycles directed to the LCD memory space (address 10X). The three LCD control signals are driven from the CPLD: the RS (Register Strobe) signal clocks data into registers, the R/W signal determines bus direction, and the E signal enables the bus for read or write operations. In the standard CPLD configuration, the R/S and R/W signals are connected to ADDR0 and WE respectively. The E signal can be driven directly from the LCDEN signal available on the system connector, or if LCDEN is left at logic ‘0’, then E is driven whenever address “10X” is present on the bus, CS is asserted, and AS or DS are low. LCD bus signals and timings are illustrated below.

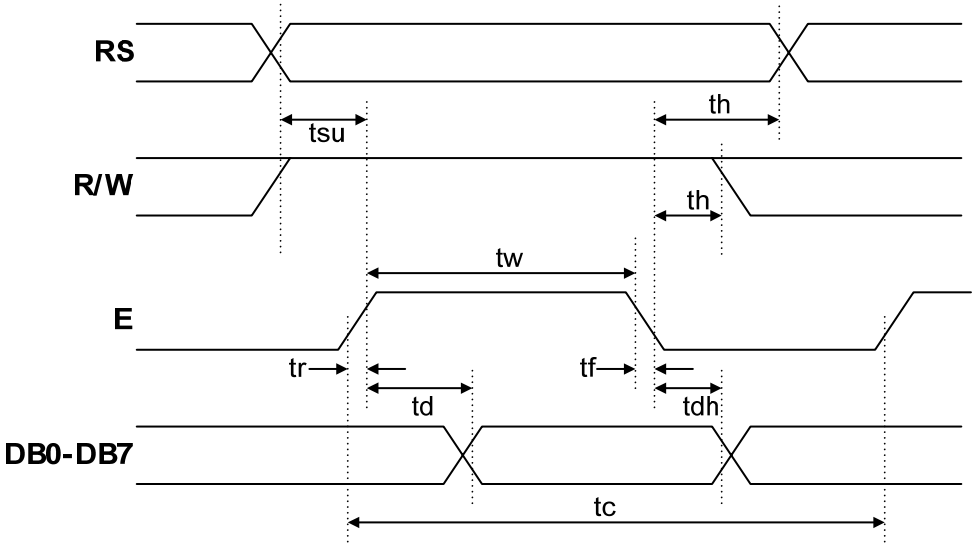
LCD Instructions and Codes

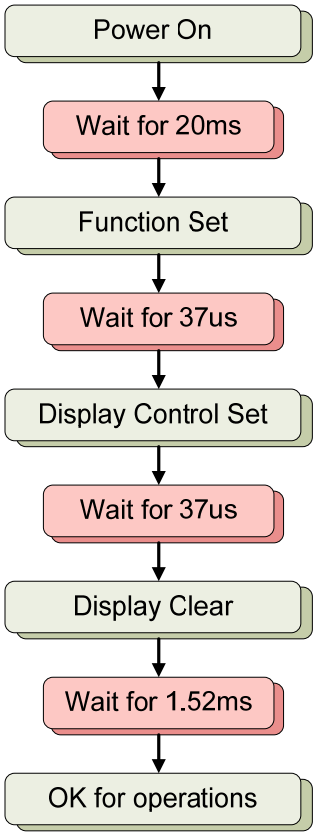
Instruction	Instruction Bit Assignments										Description
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear display by writing a 20H to all DDRAM locations, set DDRAM address register to 00H, and return cursor to home.
Return Home	0	0	0	0	0	0	0	0	1	X	Return cursor to home (upper left corner), and set DDRAM address to 0H. DDRAM contents not changed.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	I/D = ‘1’ for right-moving cursor and address increment, SH = ‘1’ for display shift (direction set by I/D bit).
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking cursor (B) on or off.
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	SC = ‘0’ to shift cursor right or left, ‘1’ to shift entire display right or left (R/L = ‘1’ for right).
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length (DL = ‘1’ for 8 bit), number of display lines (N = ‘1’ for 2 lines), display font (F = ‘0’ for 5x 8 dots).
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address counter.
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address counter.
Read Busy Flag/ Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag and address counter.
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into DDRAM or CGRAM, depending on which address was last set.
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from DDRAM or CGRAM, depending on which address was last set.

A startup sequence with specific timings ensures proper LCD operation. After power-on, at least 20ms must elapse before the function-set instruction code can be written to set the bus width, number of lines, and character patterns (8-bit interface, 2 lines, and 5x8 dots are appropriate). After the function-set instruction, at least 37us must elapse before the display-control instruction can be written (to turn the display on, turn the cursor on or off, and set the cursor to blink or no blink). After another 37us, the display-clear instruction can be issued. After another 1.52ms, the entry-mode instruction can set address increment (or address decrement) mode, and display shift mode (on or off). After this sequence, data can be written into the DDRAM to cause information to appear on the display.

LCD Connector Signals		
Pin No.	**Symbol**	**Signal Description**
1	Vss	Signal ground
2	Vdd	Power supply (5V)
3	Vo	Operating (contrast) voltage (LCD drive, typically 100mV at 20C)
4	RS	Register select: high for data transfer, low for instruction register
5	R/W	Read/write signal: high for read mode, low for write mode
6	E	Read/write strobe: high for read OE; falling edge writes data
7-14	Data Bus	Bidirectional data bus

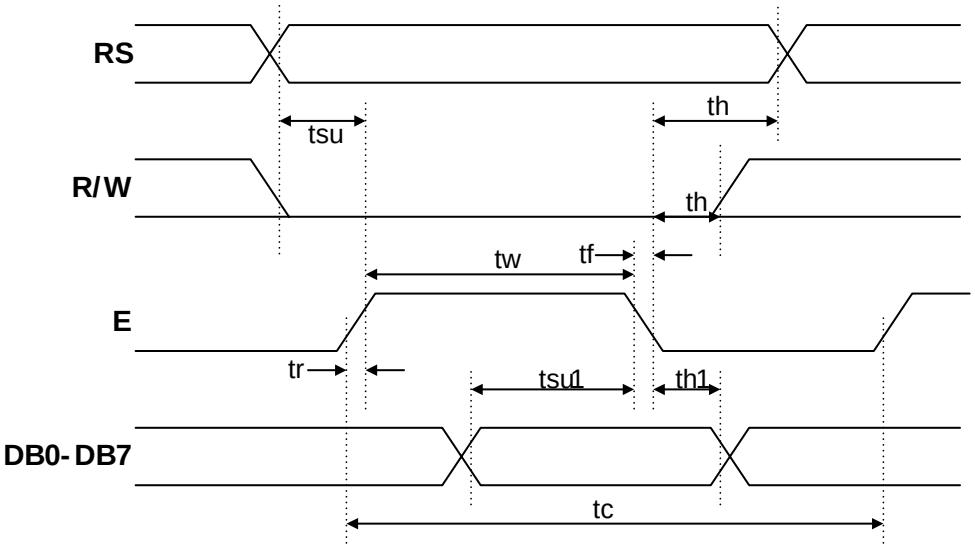
LCD Read Cycle





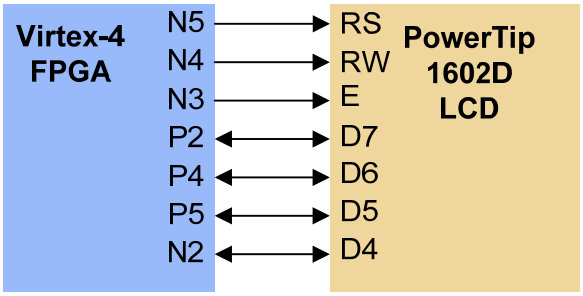
LCD Startup Sequence

LCD Write Cycle



LCD Bus Timings					
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Pin**
Enable cycle time	tc	500		ns	E
Enable High pulse width	tw	220		ns	E
Enable rise/fall time	tr, tf		25	ns	E
RS, R/W setup time	tsu	40		ns	RS, R/W
RS, R/W hold time	th	10		ns	RS, R/W
Read data output delay	td	60	120	ns	DB0-DB7
Read data hold time	tdh	20		ns	DB0-DB7
Write data setup time	tsu1	40		ns	DB0-DB7
Write data hold time	th1	10		ns	DB0-DB7

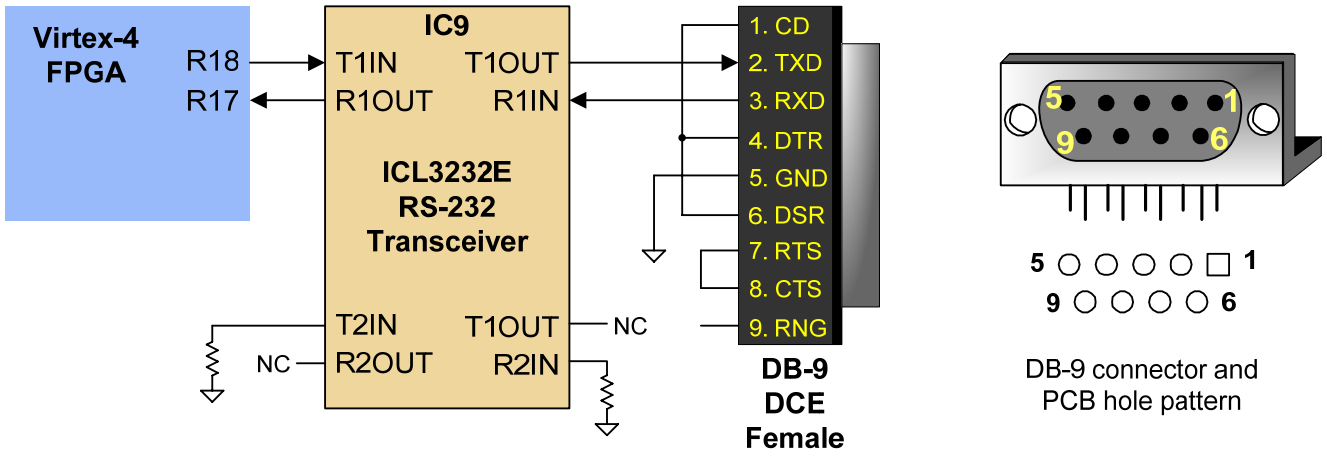
The LCD connections to the Virtex-4 are shown below. Note the LCD uses a 4-bit data interface, and the same FPGA pins that connect to the data bus are shared with the pushbutton inputs.



FX12 LCD Circuit Diagram

Serial Port

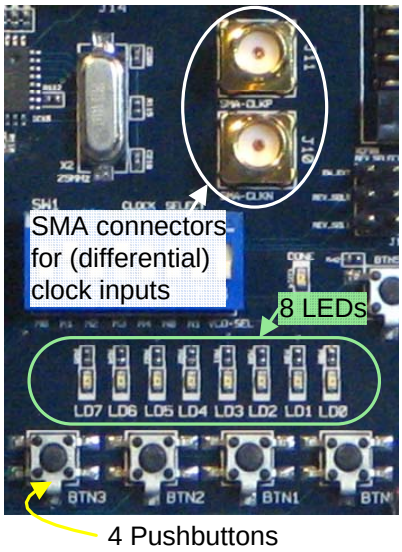
The FX12 provides an RS-232 based serial port for user data transfers and embedded processor debug operations. RS-232 level translation is provided by an Intersil ICL3232 transceiver.

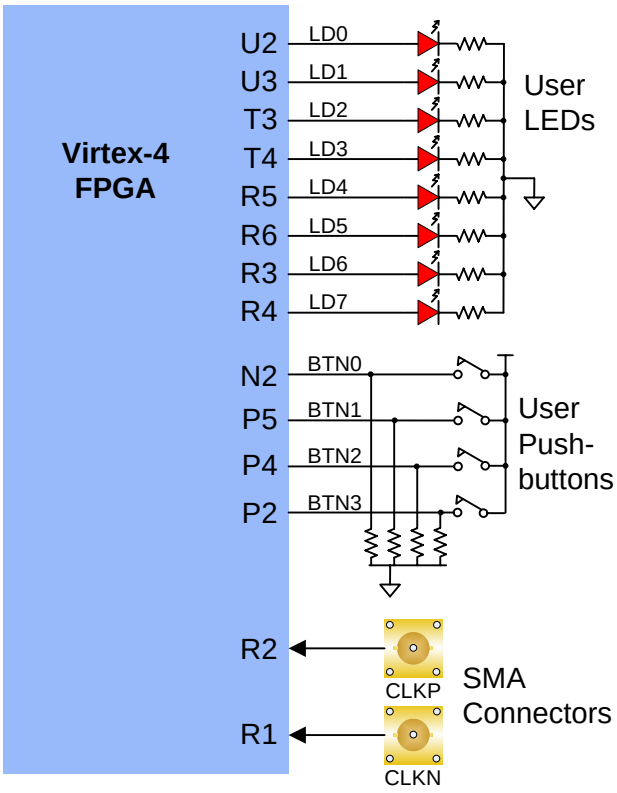


FX12 Serial Port Circuit Diagram

Other User I/O

Eight LEDs, four pushbuttons, and two SMA connectors are provided for general user I/O. Pushbutton inputs are normally low, and they are driven high only when the pushbutton is pressed. Anodes of the high-bright LEDs are connected to FPGA pins, so that a logic high signal will illuminate them with just 3-4mA of current. Separate LEDs are provided for power-on indication and successful completion of FPGA configuration. The two SMA connectors provide a differential pair of I/O's suitable for high-frequency signals such as clocks.



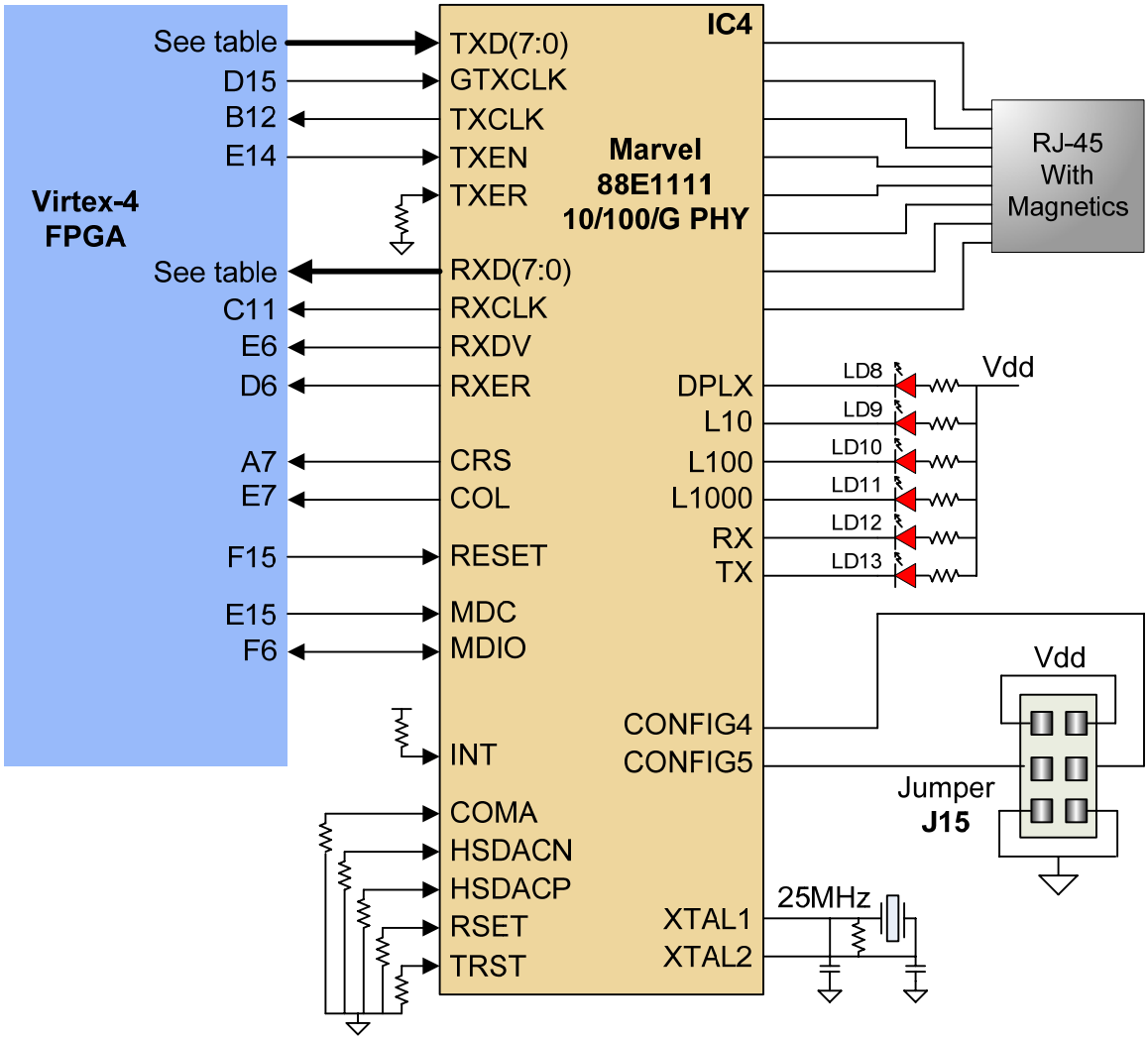


User I/O Devices Circuit Diagram

Marvell Ethernet Transceiver

The FX12 board includes a Marvell 10/100/1G Ethernet Transceiver (the "PHY"). The Virtex-4 contains a hard-IP Ethernet MAC that can directly drive the Marvell PHY, or a soft-IP MAC can be programmed into available gates in the Virtex-4 fabric.

Marvell maintains tight control of their data sheets. For further information on the Marvell PHY, please contact NuHorizons for assistance with entering into a non-disclosure agreement with Marvell.



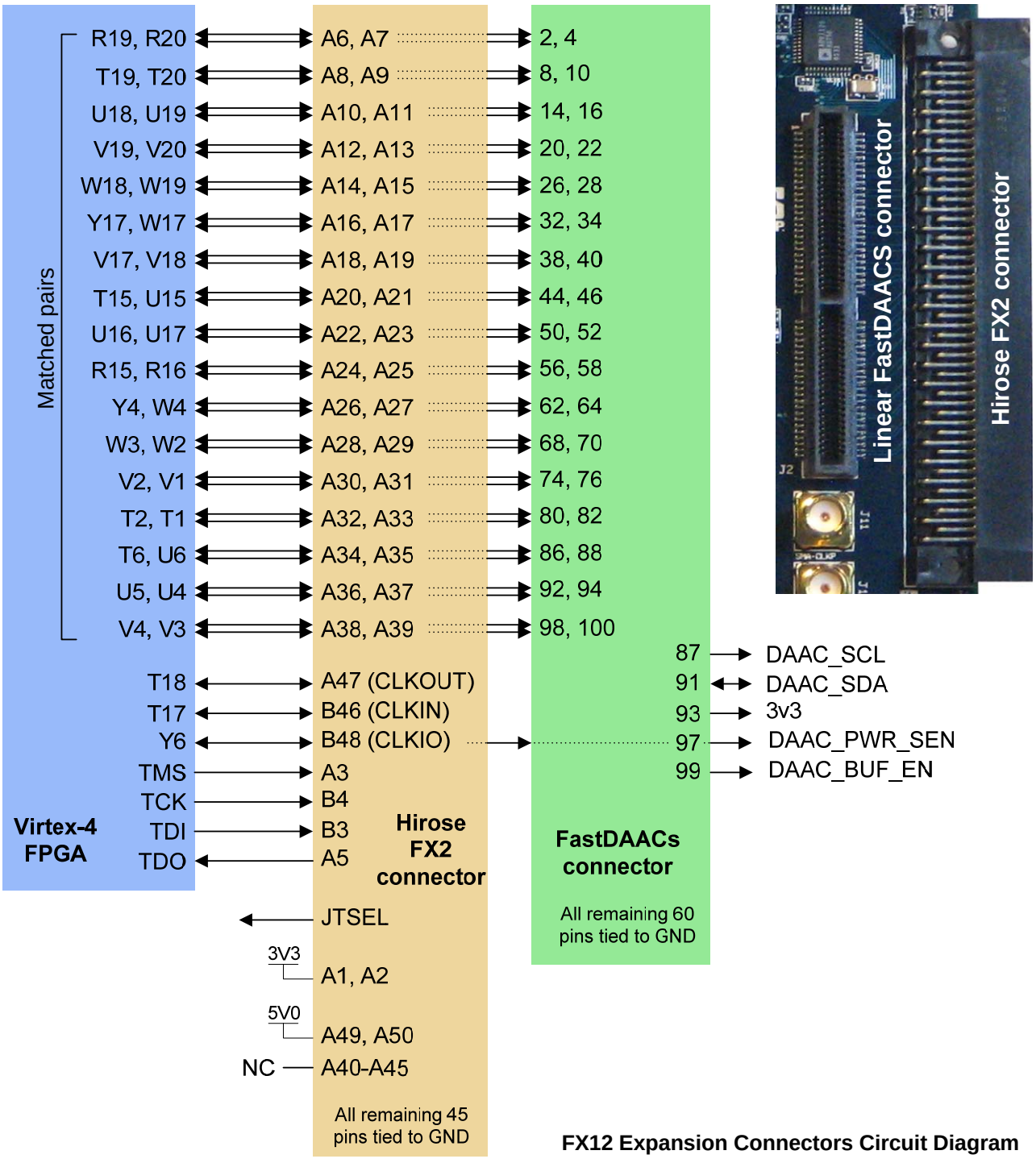
FX12 Marvel PHY Circuit Diagram

Expansion Connectors

The FX12 provides two primary expansion connectors: a Hirose 100-pin FX2 high-density board-to-board or board-to-cable connector and a second connector that can accommodate FastDAACS A/D and D/A demo boards from Linear Technology. The FX2 connector includes 17 matched pairs of I/O signals from the FPGA (34 total signals), as well as the JTAG programming signals and three clock signals (which can also be used as general I/O's). Mating board or cable connectors can readily be

obtained from several catalog distributors (see for example the mating part number FX2-100S-1.27DS available from Digikey).

The 100-pin FastDAACS connector supports direct connection of a number of A/D and D/A sample boards produced by Linear Technology (see www.linear.com for more information). The FastDAACs connector shares the 17 matched pairs of FPGA I/Os with the Hirose Expansion connector, plus five control signals that constitute Linear Technology's FastDAACs serial control bus.



FX12 Expansion Connectors Circuit Diagram

Appendix A: Switch settings for various synthesizer frequencies.

Frequency (MHz)	M0	M1	M2	M3	M4	N0	N1	VCOSEL
350	0	0	1	1	1	0	0	0
337.5	1	1	0	1	1	0	0	0
325	0	1	0	1	1	0	0	0
312.5	1	0	0	1	1	0	0	0
300	0	0	0	1	1	0	0	0
287.5	1	1	1	0	1	0	0	0
275	0	1	1	0	1	0	0	0
262.5	1	0	1	0	1	0	0	0
250	0	0	1	0	1	0	0	0
237.5	1	1	0	0	1	0	0	0
225	0	1	0	0	1	0	0	0
212.5	1	0	0	0	1	0	0	0
200	0	0	0	0	1	0	0	0
187.5	1	1	1	1	0	0	0	0
175	0	0	1	1	1	1	0	0
168.75	1	1	0	1	1	1	0	0
162.5	0	1	0	1	1	1	0	0
156.25	1	0	0	1	1	1	0	0
150	0	0	0	1	1	1	0	0
143.75	1	1	1	0	1	1	0	0
137.5	0	1	1	0	1	1	0	0
131.25	1	0	1	0	1	1	0	0
125	0	0	1	0	1	1	0	0
118.75	1	1	0	0	1	1	0	0
112.5	0	1	0	0	1	1	0	0
106.25	1	0	0	0	1	1	0	0
100	0	0	0	0	1	1	0	0
93.75	1	1	1	1	0	1	0	0
87.5	0	0	1	1	1	0	1	0
84.375	1	1	0	1	1	0	1	0
81.25	0	1	0	1	1	0	1	0
78.125	1	0	0	1	1	0	1	0
75	0	0	0	1	1	0	1	0
71.875	1	1	1	0	1	0	1	0
68.75	0	1	1	0	1	0	1	0
65.625	1	0	1	0	1	0	1	0
62.5	0	0	1	0	1	0	1	0
56.25	0	1	0	0	1	0	1	0
53.125	1	0	0	0	1	0	1	0
50	0	0	0	0	1	0	1	0
46.875	1	1	1	1	0	0	1	0
42.1875	1	1	0	1	1	1	1	0
40.625	0	1	0	1	1	1	1	0
39.0625	1	0	0	1	1	1	1	0
37.5	0	0	0	1	1	1	1	0
35.9375	1	1	1	0	1	1	1	0
34.375	0	1	1	0	1	1	1	0
32.8125	1	0	1	0	1	1	1	0
31.25	0	0	1	0	1	1	1	0
29.6875	1	1	0	0	1	1	1	0
28.125	0	1	0	0	1	1	1	0
26.5625	1	0	0	0	1	1	1	0
25	0	0	0	0	1	1	1	0
21.875	0	1	1	1	0	1	1	0
20.3125	1	0	1	1	0	1	1	0
18.75	0	0	1	1	0	1	1	0
17.1875	1	1	0	1	0	1	1	0
15.625	0	1	0	1	0	1	1	0