Specifications

PCI-DAS6070

Document Revision 1.0, July, 2002

Specifications

Typical for 25°C unless otherwise specified.

Analog Input Section

A/D converter type	Successive Approximation	
Maximum Sample Rate	1.25 MS/s	
Resolution	12 bits, 1-in-4096	
Number of channels	16 single ended / 8 differential, Software selectable	
Input ranges	Bipolar: ±10V, ±5V, ±2.5V, ±1V, ±0.5V, ±0.25V, ±0.1V, ±0.05V, Unipolar: 0 to 10V, 0 to 5V, 0 to 2V, 0 to 1V, 0 to 0.5V, 0 to 0.2V, 0 to 0.1V Software selectable	
A/D pacing (SW programmable)	Internal counter – ASIC. Software selectable time base: ▪ Internal 40MHz, 50ppm stability ▪ External Source via AUXIN<5:0>, Software selectable.	
	External convert strobe: A/D CONVERT	
	Software paced	
Burst mode	Software selectable option, burst rate = 800nS	
A/D Gate Sources	External digital:	A/D GATE
	External analog:	ATRIG input CH0 IN through CH15 IN
A/D gating modes	External digital:	Programmable, active high or active low, level or edge
	External analog:	See Analog Trigger section
A/D trigger sources	External digital:	A/D START TRIGGER A/D STOP TRIGGER
	External analog:	ATRIG input CH0 IN through CH15 IN
A/D triggering modes	External digital:	Software-configurable for rising or falling edge.
	External analog:	See Analog Trigger section
	Pre-/Post-trigger:	Unlimited number of pre-trigger samples, 16 Meg post-trigger samples.
ADC Pacer Out	Available at user connector: A/D PACER OUT	
RAM buffer size	8K samples	
Data transfer	DMA	
	Programmed I/O	
DMA Modes	Demand or Non-Demand using scatter gather.	
Configuration Memory	Up to 8K elements. Programmable channel, gain, and offset	
Streaming-to-disk rate	1.25 MS/s, system dependent	

Accuracy

1.25 MS/s rate, single channel operation and a 15-minute warm-up. Accuracies listed are for measurements made following an internal calibration. They are valid for operational temperatures within ±1°C of internal calibration temperature and ±10°C of factory calibration temperature. Calibrator test source high side tied to Channel 0 High and low side tied to Channel 0 Low. Low-level ground is tied to Channel 0 Low at the user connector.

Table 1. Absolute Accuracy

Range	Absolute Accuracy (LSB)
±10V	±2.9
±5V	±2.1
±2.5V	±3.0
±1V	±3.0
±500mV	±3.0
±250mV	±3.1
±100mV	±3.3
±50mV	±3.7
0 to 10V	±2.8
0 to 5V	±4.4
0 to 2V	±4.4
0 to 1V	±4.5
0 to 500mV	±4.6
0 to 200mV	±4.8
0 to 100mV	±5.2

Table 2. Absolute Accuracy components - All values are (±)

Range	% of Reading	Offset (mV)	Noise + Quantization (mV)		Temp Drift (%/DegC)	Absolute Accuracy at FS (mV)
			Single Pt	Averaged [1]		
±10V	0.0714	6.38	6.10	0.846	0.0010	14.369
±5V	0.0314	3.20	3.05	0.423	0.0005	5.193
±2.5V	0.0714	1.61	1.53	0.211	0.0010	3.605
±1V	0.0714	0.653	0.610	0.085	0.0010	1.452
±500mV	0.0714	0.335	0.305	0.042	0.0010	0.735
±250mV	0.0714	0.176	0.208	0.024	0.0010	0.379
±100mV	0.0714	0.081	0.098	0.011	0.0010	0.163
±50mV	0.0714	0.049	0.071	0.007	0.0010	0.091
0 to 10V	0.0314	3.20	3.05	0.423	0.0005	6.765
0 to 5V	0.0714	1.61	1.53	0.211	0.0010	5.391
0 to 2V	0.0714	0.653	0.610	0.085	0.0010	2.167

Range	% of Reading	Offset (mV)	Noise + Quantization (mV)		Temp Drift (%/DegC)	Absolute Accuracy at FS (mV)
			Single Pt	Averaged [1]		
0 to 1V	0.0714	0.335	0.305	0.042	0.0010	1.092
0 to 500mV	0.0714	0.176	0.208	0.024	0.0010	0.558
0 to 200mV	0.0714	0.081	0.098	0.011	0.0010	0.235
0 to 100mV	0.0714	0.049	0.071	0.007	0.0010	0.127

1. Averaged measurements assume dithering and averaging of 100 single-channel readings

Each PCI-DAS6070 is tested at the factory to assure the board's overall error does not exceed absolute accuracy limits described in Table 1 above.

Table 3. Relative Accuracy - All values are (±)

Range	Relative Accuracy (mV)	
	Single Point	Averaged [1]
±10V	7.37	1.11
±5V	3.68	0.557
±2.5V	1.84	0.278
±1V	0.737	0.111
±500mV	0.368	0.056
±250mV	0.238	0.032
±100mV	0.111	0.015
±50mV	0.082	0.009
0 to 10V	3.68	0.557
0 to 5V	1.84	0.278
0 to 2V	0.737	0.111
0 to 1V	0.368	0.056
0 to 500mV	0.238	0.032
0 to 200mV	0.111	0.015
0 to 100mV	0.082	0.009

1. Averaged measurements assume dithering and averaging of 100 single-channel readings

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function. ADC resolution, noise and front-end non-linearity are included in this measurement.

Table 4. Differential non-linearity

All Ranges	±0.5 LSB typ	±1.0 LSB max

Settling Time

Settling time is defined here as the time required for a channel to settle to within a specified accuracy in response to a full-scale (FS) step. Two channels are scanned at a specified rate. A –FS DC signal is presented to Channel 1; a +FS DC signal is presented to Channel 0.

Condition	Range	Accuracy			
			±0.012% (±0.5 LSB)	±0.024% (±1.0 LSB)	±0.098% (±4.0 LSB)
Same range to same range	±10V	Typ	2.0µS	1.5µS	1.5µS
		Max	3.0µS	2.0µS	2.0µS
	±5V	Typ	2.0µS	1.5µS	1.3µS
		Max	3.0µS	2.0µS	1.5µS
	±2.5V	Typ	2.0µS	1.5µS	0.9µS
		Max	3.0µS	2.0µS	1.0µS
	±1V	Typ	2.0µS	1.5µS	0.9µS
		Max	3.0µS	2.0µS	1.0µS
	±500mV	Typ	2.0µS	1.5µS	0.9µS
		Max	3.0µS	2.0µS	1.0µS
	±250mV	Typ	2.0µS	1.5µS	0.9µS
		Max	3.0µS	2.0µS	1.0µS
	±100mV	Typ	2.0µS	1.5µS	0.9µS
		Max	3.0µS	2.0µS	1.0µS
	±50mV	Typ	2.0µS	1.5µS	1.0µS
		Max	3.0µS	2.0µS	1.5µS
	0 to 10V	Typ	2.0µS	1.5µS	1.3µS
		Max	3.0µS	2.0µS	1.5µS
	0 to 5V	Typ	2.0µS	1.5µS	0.9µS
		Max	3.0µS	2.0µS	1.0µS
	0 to 2V	Typ	2.0µS	1.5µS	0.9µS
		Max	3.0µS	2.0µS	1.0µS
	0 to 1V	Typ	2.0µS	1.5µS	0.9µS
		Max	3.0µS	2.0µS	1.0µS
	0 to 500mV	Typ	2.0µS	1.5µS	0.9µS
		Max	3.0µS	2.0µS	1.0µS
	0 to 200mV	Typ	2.0µS	1.5µS	0.9µS
		Max	3.0µS	2.0µS	1.0µS
	0 to 100mV	Typ	2.0µS	1.5µS	1.0µS
		Max	3.0µS	2.0µS	1.5µS

Parametrics

Max working voltage (signal + common-mode)	Input must remain within ±11V of ground	
CMRR @ 60Hz	±10V	95 dB
	±5V, 0 to 10V	100 dB
	All other ranges	106 dB
Small signal bandwidth, all ranges	1.6 MHz	
Large signal bandwidth, all ranges	1.0 MHz	
Input coupling	DC	
Input impedance	100 Gohm in parallel with 100pF in normal operation.	
	820 Ohm in powered off or overload condition.	
Input bias current	±200 pA	
Input offset current	±100 pA	
Absolute maximum input voltage	±25 power on, ±15V power off. Protected Inputs: ▪ CH0 IN through CH15 IN ▪ AISENSE	
Crosstalk, DC to 100 kHz	Adjacent Channels: -75 dB	
	All other Channels: -90 dB	

Noise Performance

Table 5 below summarizes the noise performance for the PCI-DAS6070. Noise distribution is determined by gathering 50K samples with inputs tied to ground at the user connector. Samples are gathered at the maximum specified single-channel sampling rate. Specification applies to both single-ended and differential modes of operation.

Table 5. Analog Input Noise Performance (not including quantization)

Range	Counts Dithered	LSBrms Dithered	Counts Undithered	LSBrms Undithered
±10V	5	0.5	3	0.25
±5V	5	0.5	3	0.25
±2.5V	5	0.5	3	0.25
±1V	5	0.5	3	0.25
±500 mV	6	0.5	3	0.25
±250 mV	6	0.6	4	0.4
±100 mV	7	0.7	5	0.5
±50 mV	9	0.9	8	0.8
0 to 10V	5	0.5	3	0.25
0 to 5V	5	0.5	3	0.25
0 to 2V	5	0.5	3	0.25

Range	Counts Dithered	LSBrms Dithered	Counts Undithered	LSBrms Undithered
0 to 1V	6	0.5	3	0.25
0 to 500 mV	6	0.6	4	0.4
0 to 200 mV	7	0.7	5	0.5
0 to 100 mV	9	0.9	8	0.8

Analog Output Section

D/A Converter type	Double-buffered, multiplying
Resolution	12-bits, 1-in-4096
Number of Channels	2 voltage output
Voltage Range	±10V, 0 to 10V, ±EXT REF., 0 to EXT REF., software selectable
Monotonicity	12-bits, guaranteed
Slew Rate	20 V/µs min
Settling Time (full scale step)	3.0 µS to ±0.5 LSB accuracy
Noise	200 µVrms, DC to 1MHz BW
Glitch Energy	±20 mV @ 1.5µS duration measured at mid-scale transition.
Current Drive	±5 mA
Output short-circuit duration	Indefinite @25mA
Output coupling	DC
Output impedance	0.1 ohms max
Gain temperature coefficient, internal or external reference	25 ppm/°C
Offset temperature coefficient	±50 µV/°C
Power up and reset	DACs cleared to 0 volts ±200 mV max

Table 6. Analog Output Absolute Accuracy

Range	Absolute Accuracy (LSB)
±10V	±1.7 LSB
0 to 10V	±2.3 LSB

Table 7. Analog Output Absolute Accuracy Components

Range	% of Reading	Offset (mV)	Temp Drift (%/DegC)	Absolute Accuracy at FS (mV)
±10V	±0.0219	±5.93	±0.0005	±8.127
0 to 10V	±0.0219	±3.49	±0.0005	±5.685

Each PCI-DAS6070 is tested at the factory to assure the board's overall error does not exceed the limits listed in *Table 6* above.

Table 8. Relative Accuracy

Range	**Relative Accuracy**	
All Ranges	±0.3 LSB, typical	±0.5 LSB, max

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function.

Table 9. Differential non-linearity

All Ranges	±0.3 LSB, typical	±1.0 LSB, max

Analog Output Pacing and Triggering

DAC Pacing (SW programmable)	Internal counter – ASIC. Selectable time base: ▪ Internal 40 MHz ▪ External Source via AUXIN<5:0>, SW selectable.
	External convert strobe: D/A UPDATE
	Software paced
DAC Gate Source (Software programmable)	External digital: D/A START TRIGGER
	External analog: ATRIG input CH0 IN through CH15 IN
	Software gated
DAC Gating Modes	External digital: Programmable, active high or active low, level or edge
	External analog: See Analog Trigger section
DAC Trigger Sources	External digital: D/A START TRIGGER
	External analog: ATRIG input CH0 IN through CH15 IN
	Software triggered
DAC Triggering Modes	External digital: Software-configurable for rising or falling edge.
	External analog: See Analog Trigger section on page 8
DAC Pacer Out	Available at user connector: D/A PACER OUT
RAM Buffer Size	16K samples
Data transfer	DMA
	Programmed I/O
	Update DACs individually or simultaneously, software selectable.
DMA Modes	Demand or Non-Demand using scatter gather.
Waveform generation throughput	1 MS/s max per channel, 2 channels simultaneous

Analog Output External Reference Input (D/A EXTREF)

Range	**±11V**
Overvoltage Protection	±25V powered on, ±15V powered off
Input Impedance	10k ohms
Bandwidth (-3dB)	1 MHz
Gain Error – EXTREF mode	0 to 0.5%, not adjustable.

Analog Trigger

Analog Trigger Sources Software selectable	External: ATRIG input CH0 IN through CH15 IN, first channel in scan	
Analog Trigger Levels	ATRIG input: ±10V	
	CH0 IN through CH15 IN: ± Full-scale, range dependent	
Analog Trigger Modes	External analog: Software-configurable for: ▪ Positive or Negative slope	
Analog Gate Modes	External analog: Software-configurable for: ▪ Above or Below reference ▪ Positive or Negative hysteresis ▪ In or Out of window	
Resolution	8-bits, 1-in-256	
Accuracy	±5% Full-scale range max	
Bandwidth (-3 dB)	ATRIG input	1.3 MHz
	CH0 IN through CH15 IN	2.0 MHz

Analog Input / Output Calibration

Recommended warm-up time	15 minutes
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.
Onboard calibration reference	DC Level: 5.000V± 2.5 mV. Actual measured values stored in EEPROM.
	Tempco: 5 ppm/°C max, 2 ppm/°C typical
	Long-term stability: 20 ppm, T = 1000 hrs, non-cumulative
Calibration interval	1 year

Digital Input / Output

Digital Type	Discrete, 5V/TTL compatible
Number of I/O	8
Configuration	8 bits, independently programmable for input or output. All pins pulled up to +5V via 47K resistors (default). Positions available for pull down to ground. Hardware selectable via solder gap.
Input high voltage	2.0V min, 7.0V absolute max
Input low voltage	0.8V max, –0.5V absolute min
Output high voltage (IOH = -32 mA)	3.80V min, 4.20V typ
Output low voltage (IOL = 32mA)	0.55V max, 0.22V typ
Data Transfer	Programmed I/O
Power-up / reset state	Input mode (high impedance)

Interrupt Section

Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time	
Interrupt enable	Programmable through PLX9080	
ADC Interrupt sources (Software Programmable)	DAQ_ACTIVE:	Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP:	Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE:	Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL:	Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE:	Interrupt is generated after each conversion completes.
	DAQ_EOSCAN:	Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ:	Interrupt is generated after each interval delay during multi-channel scans.
DAC Interrupt sources (Software Programmable)	DAC_ACTIVE:	Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE:	Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY:	Interrupt is generated when the DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL:	Interrupt is generated when the DAC high channel output is updated.

Counter Section

User counter type	82C54
Number of Channels	2
Resolution	16-bits
Compatibility	5V/TTL
CTRn base clock source (Software selectable)	Internal 10 MHz, Internal 100 kHz or External connector (CTRn CLK)
Internal 10 MHz clock source stability	50ppm
Counter n Gate	Available at connector (CTRn GATE).
Counter n Output	Available at connector (CTRn OUT).
Clock input frequency	10 MHz max
High pulse width (clock input)	15 ns min
Low pulse width (clock input)	25 ns min
Gate width high	25 ns min
Gate width low	25 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Configurable AUXIN<5:0>, AUXOUT<2:0> External Trigger/Clocks

The PCI-DAS6070 provides nine user-configurable Trigger/Clock pins that are available at the 100-pin I/O connector. Of these, six are configurable as inputs while three are configurable as outputs.

AUXIN<5:0> Sources (SW selectable)	A/D CONVERT: A/D TIMEBASE IN: A/D START TRIGGER: A/D STOP TRIGGER: A/D PACER GATE: D/A START TRIGGER D/A UPDATE: D/A TIMEBASE IN:	External ADC convert strobe External ADC pacer timebase ADC Start Trigger ADC Stop Trigger External ADC gate DAC trigger/gate DAC update strobe External DAC pacer time base
AUXOUT<2:0> Sources (SW Selectable)	STARTSCAN: SSH: A/D STOP: A/D CONVERT: SCANCLK: CTR1 CLK D/A UPDATE CTR2 CLK A/D START TRIGGER: A/D STOP TRIGGER: A/D PACER GATE: D/A START TRIGGER:	A pulse indicating start of conversion Active signal that terminates at the start of the last conversion in a scan. Indicates end of a scan ADC convert pulse Delayed version of ADC convert CTR1 clock source D/A update pulse CTR2 clock source ADC Start Trigger Out ADC Stop Trigger Out External ADC gate DAC Start Trigger Out
Default Selections:	AUXIN0: AUXIN1: AUXIN2: AUXIN3: AUXIN4: AUXIN5: AUXOUT0: AUXOUT1: AUXOUT2:	A/D CONVERT A/D START TRIGGER A/D STOP TRIGGER D/A UPDATE D/A START TRIGGER A/D PACER GATE D/A UPDATE A/D CONVERT SCANCLK
Compatibility	5V/TTL	
Edge-sensitive polarity	Rising/falling, software selectable	
Level-sensitive polarity	Active high/active low, software selectable	
Minimum pulse width	3.75nS	

DAQ-Sync inter-board Triggers/Clocks

The DAQ-Sync bus provides inter-board triggering and synchronization capability. Five trigger/strobe I/O pins and one clock I/O pin are provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction may be set.

DAQ-Sync Signals	DS A/D START TRIGGER
	DS A/D STOP TRIGGER
	DS A/D CONVERT
	DS D/A UPDATE
	DS D/A START TRIGGER
	SYNC CLK

Power Consumption

+5V	0.9 A typical, 1.1 A max. Does not include power consumed through the I/O connector.
+5V available at I/O connector	1A max, protected with a resettable fuse

Environmental

Operating Temperature Range	0 to 55°C
Storage Temperature Range	-20 to 70°C
Humidity	0 to 90% non-condensing

Mechanical

Card dimensions	PCI half card: 174.6mm(L) x 106.9mm(W) x 11.65mm(H)

DAQ-Sync Connector and Pin Out

Connector type	14-Pin right-angle 100mil box header
Compatible Cables	MCC p/n: CDS-14-x, 14 pin ribbon cable. x = number of boards (2 - 5)

Pin	Signal Name
1	**DS A/D START TRIGGER**
2	**GND**
3	**DS A/D STOP TRIGGER**
4	**GND**
5	**DS A/D CONVERT**
6	**GND**
7	**DS D/A UPDATE**
8	**GND**
9	**DS D/A START TRIGGER**
10	**GND**
11	**RESERVED**
12	**GND**
13	**SYNC CLK**
14	**GND**

Main Connector and Pin Out

Connector type	Shielded SCSI 100 D-Type
Compatible Cables	C100HD50-x, unshielded ribbon cable. x= 3 or 6 feet
	C100MMS-x, shielded round cable. x= 1, 2, or 3 meters
Compatible accessory products (with C100HD50-xx cable)	ISO-RACK16/P ISO-DA02/P BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50
Compatible accessory products (with C100MMS-x cable)	SCB-100

8 Channel Differential Mode

Pin	Signal Name	Pin	Signal Name
1	**LLGND**	**51**	**n/c**
2	**CH0 IN HI**	**52**	**n/c**
3	**CH0 IN LO**	**53**	**n/c**
4	**CH1 IN HI**	**54**	**n/c**
5	**CH1 IN LO**	**55**	**n/c**
6	**CH2 IN HI**	**56**	**n/c**
7	**CH2 IN LO**	**57**	**n/c**
8	**CH3 IN HI**	**58**	**n/c**
9	**CH3 IN LO**	**59**	**n/c**
10	**CH4 IN HI**	**60**	**n/c**
11	**CH4 IN LO**	**61**	**n/c**
12	**CH5 IN HI**	**62**	**n/c**
13	**CH5 IN LO**	**63**	**n/c**
14	**CH6 IN HI**	**64**	**n/c**
15	**CH6 IN LO**	**65**	**n/c**
16	**CH7 IN HI**	**66**	**n/c**
17	**CH7 IN LO**	**67**	**n/c**
18	**LLGND**	**68**	**n/c**
19	**n/c**	**69**	**n/c**
20	**n/c**	**70**	**n/c**
21	**n/c**	**71**	**n/c**
22	**n/c**	**72**	**n/c**
23	**n/c**	**73**	**n/c**
24	**n/c**	**74**	**n/c**
25	**n/c**	**75**	**n/c**
26	**n/c**	**76**	**n/c**
27	**n/c**	**77**	**n/c**
28	**n/c**	**78**	**n/c**
29	**n/c**	**79**	**n/c**
30	**n/c**	**80**	**n/c**
31	**n/c**	**81**	**n/c**
32	**n/c**	**82**	**n/c**
33	**n/c**	**83**	**n/c**
34	**n/c**	**84**	**n/c**
35	**AISENSE**	**85**	**DIO0**
36	**D/A OUT 0**	**86**	**DIO1**
37	**D/A GND**	**87**	**DIO2**
38	**D/A OUT1**	**88**	**DIO3**
39	**PC +5 V**	**89**	**DIO4**
40	**AUXOUT0 / D/A PACER OUT**	**90**	**DIO5**
41	**AUXOUT1 / A/D PACER OUT**	**91**	**DIO6**
42	**AUXOUT2 / SCANCLK**	**92**	**DIO7**
43	**AUXIN0 / A/D CONVERT / ATRIG**	**93**	**CTR1 CLK**
44	**D/A EXTREF**	**94**	**CTR1 GATE**
45	**AUXIN1 / A/D START TRIGGER**	**95**	**CTR1 OUT**
46	**AUXIN2 / A/D STOP TRIGGER**	**96**	**GND**
47	**AUXIN3 / D/A UPDATE**	**97**	**CTR2 CLK**
48	**AUXIN4 / D/A START TRIGGER**	**98**	**CTR2 GATE**
49	**AUXIN5 / A/D PACER GATE**	**99**	**CTR2 OUT**
50	**GND**	**100**	**GND**

16 Channel Single-Ended Mode

Pin	Signal Name	Pin	Signal Name
1	**LLGND**	**51**	**n/c**
2	**CH0 IN**	**52**	**n/c**
3	**CH8 IN**	**53**	**n/c**
4	**CH1 IN**	**54**	**n/c**
5	**CH9 IN**	**55**	**n/c**
6	**CH2 IN**	**56**	**n/c**
7	**CH10 IN**	**57**	**n/c**
8	**CH3 IN**	**58**	**n/c**
9	**CH11 IN**	**59**	**n/c**
10	**CH4 IN**	**60**	**n/c**
11	**CH12 IN**	**61**	**n/c**
12	**CH5 IN**	**62**	**n/c**
13	**CH13 IN**	**63**	**n/c**
14	**CH6 IN**	**64**	**n/c**
15	**CH14 IN**	**65**	**n/c**
16	**CH7 IN**	**66**	**n/c**
17	**CH15 IN**	**67**	**n/c**
18	**LLGND**	**68**	**n/c**
19	**n/c**	**69**	**n/c**
20	**n/c**	**70**	**n/c**
21	**n/c**	**71**	**n/c**
22	**n/c**	**72**	**n/c**
23	**n/c**	**73**	**n/c**
24	**n/c**	**74**	**n/c**
25	**n/c**	**75**	**n/c**
26	**n/c**	**76**	**n/c**
27	**n/c**	**77**	**n/c**
28	**n/c**	**78**	**n/c**
29	**n/c**	**79**	**n/c**
30	**n/c**	**80**	**n/c**
31	**n/c**	**81**	**n/c**
32	**n/c**	**82**	**n/c**
33	**n/c**	**83**	**n/c**
34	**n/c**	**84**	**n/c**
35	**AISENSE**	**85**	**DIO0**
36	**D/A OUT 0**	**86**	**DIO1**
37	**D/A GND**	**87**	**DIO2**
38	**D/A OUT1**	**88**	**DIO3**
39	**PC +5 V**	**89**	**DIO4**
40	**AUXOUT0 / D/A PACER OUT**	**90**	**DIO5**
41	**AUXOUT1 / A/D PACER OUT**	**91**	**DIO6**
42	**AUXOUT2 / SCANCLK**	**92**	**DIO7**
43	**AUXIN0 / A/D CONVERT / ATRIG**	**93**	**CTR1 CLK**
44	**D/A EXTREF**	**94**	**CTR1 GATE**
45	**AUXIN1 / A/D START TRIGGER**	**95**	**CTR1 OUT**
46	**AUXIN2 / A/D STOP TRIGGER**	**96**	**GND**
47	**AUXIN3 / D/A UPDATE**	**97**	**CTR2 CLK**
48	**AUXIN4 / D/A START TRIGGER**	**98**	**CTR2 GATE**
49	**AUXIN5 / A/D PACER GATE**	**99**	**CTR2 OUT**
50	**GND**	**100**	**GND**

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