PCI-CTR20HD

Specifications

Document Revision 1.1, February, 2010

Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Counters

Refer to CTS9513-2 data sheet for complete 9513 specifications and operating modes. The SAVE command for the CTS9513 device does not behave predictably when using clocks which are not synchronous with the logic timing. If the SAVE command must be used, we strongly recommend that the 3.3 MHz clock derived from the 33 MHz PCI clock be selected as the clock source. The CTS9513-2 data sheet is available on our web site at www.mccdaq.com/PDFmanuals/9513A.pdf.

Table 1. Counter specifications

Parameter	Conditions
Counter type	9513
Configuration	Four 9513 devices. Five up/down counters per 9513, 16-bits each.
Compatibility	5V/TTL
Each 9513 device is programmable for:	
Clock source	Software selectable: External: ▪ Counter 1-5 clock inputs ▪ Counter 1-5 gate inputs Internal: ▪ Terminal count of previous counter ▪ X2 clock frequency scaler
Gate	Software selectable source: External: ▪ Active high or low level or edge, counter 1 – 5 gate input ▪ Active high level previous gate or next gate ▪ All external gate signals (CTRxGATEn) individually pulled up through 10 K resistors to +5V. Internal: ▪ Active high previous counter terminal count ▪ No gating.
Output	Software selectable: ▪ Always low ▪ High pulse on terminal count ▪ Low pulse on terminal count ▪ Toggle on terminal count ▪ Inactive, high impedance at user connector counter # output
Osc Out	Software selectable source: ▪ Counter #1-5 input ▪ Gate #1-5 input ▪ Prescaled clock source (X2 clock frequency scaler) Software selectable divider: ▪ Division by 1-16 Software selectable enable: ▪ On or low impedance to ground
Clock input frequency	6.8 MHz max (145 nS min period)
X2 clock input sources	Software selectable: (each counter individually) ▪ External (max = 7.0 MHz) EXT SRCA_IN, EXT SRCB_IN, EXT SRCC_IN, EXT SRCD_IN ▪ 1.0 MHz (10MHz Xtal divided by 10) ▪ 5.0 MHz (10MHz Xtal divided by 2) ▪ 3.33 MHz (33 MHz PCI clock divided by 10) ▪ 1.67 MHz (33 MHz PCI clock divided by 20)
X2 clock frequency scaler	BCD scaling (X2 divided by 10, 100, 1000 or 10000) or Binary scaling (X2 divided by 16, 256, 4096 or 65536)

Parameter	Conditions
High pulse width (clock input)	*70 ns min*
Low pulse width (clock input)	*70 ns min*
Gate width high	*145 ns min*
Gate width low	*145 ns min*
Input low voltage	*-0.5 V min, 0.8 V max*
Input high voltage	*2.2 V min, Vcc max*
Output low voltage @ IIl = 3.2 mA	*0.4 V max*
Output high voltage @ IIH = -200 µA	*2.4 V min*
Crystal oscillator frequency	10 MHz
Frequency accuracy	50 ppm

Interrupts

Table 2. Interrupt specifications

Number of user interrupt inputs	Two
PCI Interrupt	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	External: Programmable through PLX-9030; 0 = disabled (default) 1 = enabled
Interrupt sources	External: IRQAB_IN, IRQCD_ IN, polarity programmable through PLX-9030; 1 = active high 0 = active low (default) IRQAB_IN and IRQCD_IN pulled up through 10K resistor to +5V
	IRQAB_IN maps to PLX 9030 LINT1
	IRQCD_IN maps to PLX 9030 LINT2

Power consumption

Table 3. Power consumption specifications

+5V	1 A typical, 1.2 A max. Does not include power consumed through the I/O connector.
+5V available at each I/O connector	1 A max, protected with a resettable fuse
Resettable fuse	▪ Type: Raychem *miniSMDC110*. ▪ Hold Current: 1.1 A max ▪ Series resistance: 0.21 Ω max

Environmental

Table 4. Environmental specifications

Operating temperature range	0 to 55 °C
Storage temperature range	-20 to 70 °C
Humidity	0 to 90% non-condensing

Mechanical

Table 5. Mechanical specifications

Card dimensions	202.8 mm (L) x 106.7 mm (W) x14.48 mm (H)
Form factor	Universal PCI keying. Compatible with 3.3V/5V 32-bit, 33 MHz back planes

Main connector and pin out

Table 6. Main connector specifications

Connector type	J1: 100-pin high density unshielded
Compatible cables	C100FF-x, unshielded ribbon cable
Compatible accessory products	CIO-MINI50 CIO-SPADE50 CIO-TERM100 SCB-50

Table 7. J1 pin out

Counter C, D		**Counter A, B**	
Pin	**Signal Name**	**Pin**	**Signal Name**
100	GND	50	GND
99	PC +5V	49	PC +5V
98	OSC OUT_D	48	OSC OUT_B
97	EXT SRCD_IN	47	EXT SRCB_IN
96	GND	46	GND
95	CTR5GATE_D	45	CTR5GATE_B
94	CTR5OUT_D	44	CTR5OUT_B
93	CTR5CLK_D	43	CTR5CLK_B
92	GND	42	GND
91	CTR4GATE_D	41	CTR4GATE_B
90	CTR4OUT_D	40	CTR4OUT_B
89	CTR4CLK_D	39	CTR4CLK_B
88	GND	38	GND
87	CTR3GATE_D	37	CTR3GATE_B
86	CTR3OUT_D	36	CTR3OUT_B
85	CTR3CLK_D	35	CTR3CLK_B
84	GND	34	GND
83	CTR2GATE_D	33	CTR2GATE_B
82	CTR2OUT_D	32	CTR2OUT_B
81	CTR2CLK_D	31	CTR2CLK_B
80	GND	30	GND
79	CTR1GATE_D	29	CTR1GATE_B
78	CTR1OUT_D	28	CTR1OUT_B
77	CTR1CLK_D	27	CTR1CLK_B
76	IRQCD_IN	26	IRQAB_IN
75	PC +5V	25	PC +5V
74	GND	24	GND
73	PC +5V	23	PC +5V
72	OSC OUT_C	22	OSC OUT_A
71	EXT SRCC_IN	21	EXT SRCA_IN
70	GND	20	GND
69	CTR5GATE_C	19	CTR5GATE_A
68	CTR5OUT_C	18	CTR5OUT_A
67	CTR5CLK_C	17	CTR5CLK_A
66	GND	16	GND
65	CTR4GATE_C	15	CTR4GATE_A
64	CTR4OUT_C	14	CTR4OUT_A
63	CTR4CLK_C	13	CTR4CLK_A
62	GND	12	GND
61	CTR3GATE_C	11	CTR3GATE_A
60	CTR3OUT_C	10	CTR3OUT_A
59	CTR3CLK_C	9	CTR3CLK_A
58	GND	8	GND
57	CTR2GATE_C	7	CTR2GATE_A
56	CTR2OUT_C	6	CTR2OUT_A
55	CTR2CLK_C	5	CTR2CLK_A
54	GND	4	GND
53	CTR1GATE_C	3	CTR1GATE_A
52	CTR1OUT_C	2	CTR1OUT_A
51	CTR1CLK_C	*1*	CTR1CLK_A

Measurement Computing Corporation
10 Commerce Way
Suite 1008
Norton, Massachusetts 02766
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@mccdaq.com
www.mccdaq.com