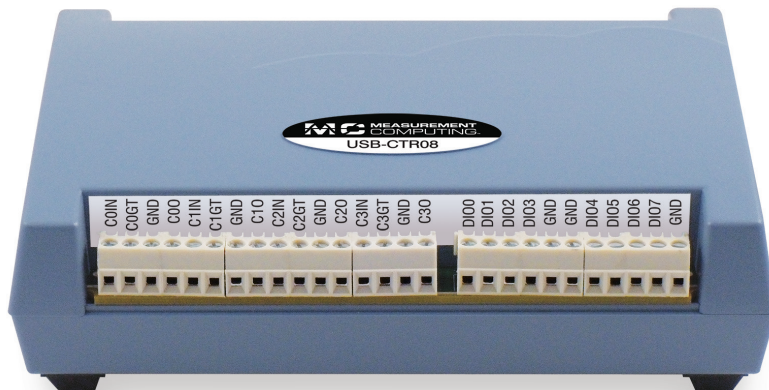


USB-CTR Series

High-Speed Counter/Timer Devices with Digital I/O



USB-CTR Series devices support multiple counter input modes and synchronous operation

Features

- High-speed pulse counter for general counting applications
- Up to 8 counter channels
- 48 MHz maximum input frequency
- Software-selectable resolution up to 64-bits
- Aggregate scan rate of 8 MB/s
- Supports Totalize, Period, Pulse-width, and Timing counter input modes
- Four independent pulse-width modulation (PWM) timers
- Eight bit-configurable digital I/O channels
- Synchronous high-speed reads of digital and counter inputs

Supported Operating Systems

- Windows® 10/8/7/Vista®XP 32/64-bit
- Linux®

Overview

USB-CTR Series devices provide high-speed counter/timer operations synchronized with digital I/O functions. Both the eight-channel USB-CTR08 and the four-channel USB-CTR04 feature high frequency and scan rates, debounce filtering, support for multiple counting modes, and software-selectable resolution up to 64 bits. Both devices also provide eight individually-configurable digital I/O channels.

Counter I/O and Gating

USB-CTR Series devices support an aggregate throughput rate of 8 MB/s.

USB-CTR Series devices can be configured for any resolution up to 64-bits, eliminating the need to cascade counters. The following data streaming rates for these common resolution settings are supported:

- 16-bit: 4 MS/s
- 32-bit: 2 MS/s
- 64-bit: 1 MS/s

Each counter channel has a connection point for counter input, counter output, and counter gate.

Counter Inputs

Counter inputs can be read asynchronously under program control, or synchronously with digital inputs as part of a digital scan group.

In both cases, counters can be configured to function in one of the following ways:

- counter resets to 0 after each read
- counter counts up or down and then rolls over at a user-set limit
- counter counts until the user-set limit has been reached

Counter inputs can concurrently monitor time periods, frequencies, pulses, and other event-driven incremental occurrences directly from pulse-generators, limit switches, proximity switches, and magnetic pick-ups.

Counter Gates

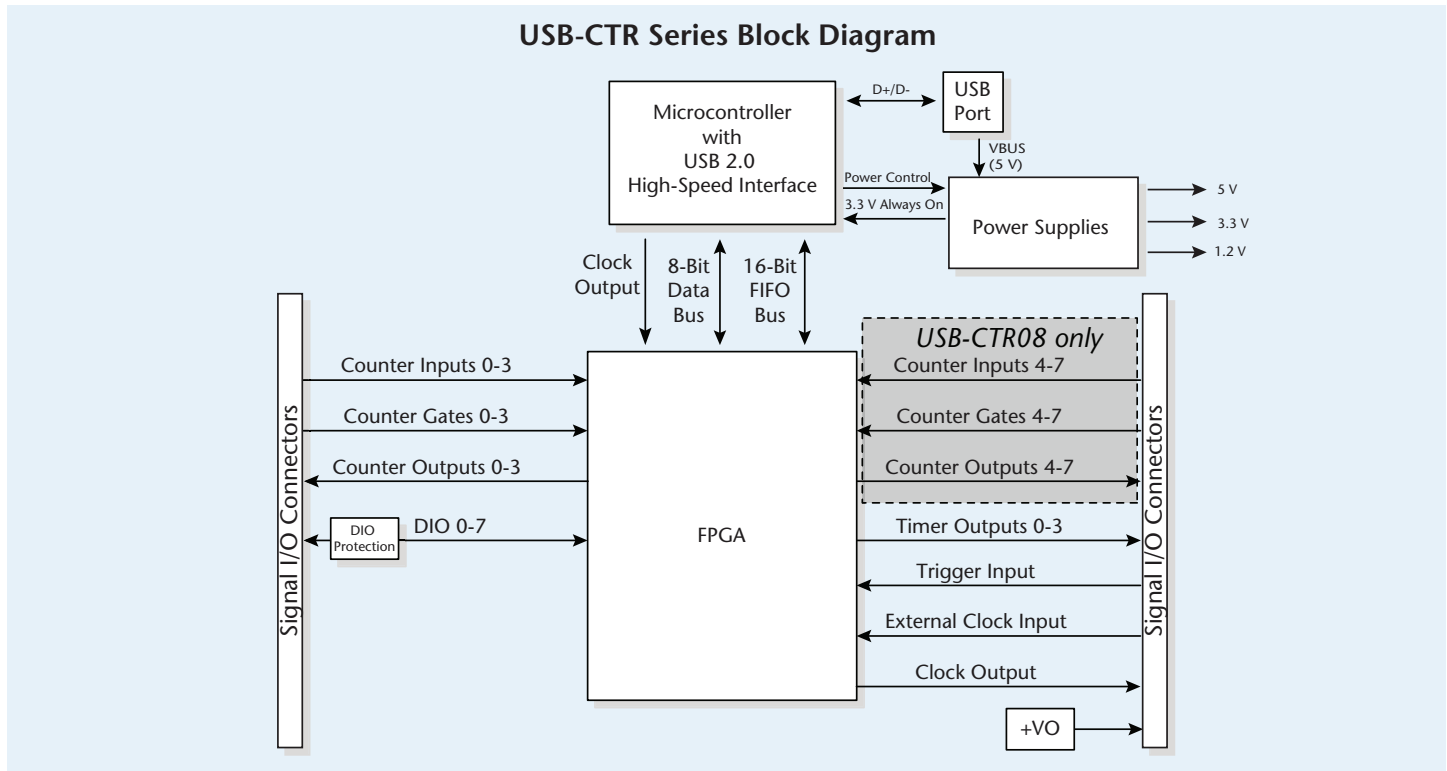
Counter gates use input signals to clear a counter, change counter direction, or start/stop counting. Gate options are software-selectable.

Counter Outputs

Counter outputs can be used to control or transmit signals to external devices, and also to counter inputs, counter gates, or digital inputs on a USB-CTR Series device.

USB-CTR Series Selection Chart

Model	Counter I/O and Gates	Aggregate Scan Rate	PWM Timers	Signal I/O	USB Cable and SW CD
USB-CTR04	4	8 MB/s	4	Screw Terminal	✓
USB-CTR08	8	8 MB/s	4	Screw Terminal	✓
USB-CTR04-OEM	4	8 MB/s	4	Header	–
USB-CTR08-OEM	8	8 MB/s	4	Header	–



Counter Input Modes

USB-CTR Series devices support the following counter input modes:

- totalize mode (event counter)
- period measurement mode
- pulse-width measurement mode
- timing measurement mode

Counter input modes are software-selectable. Some modes include the *max limit* and the *min limit* register values, which do not directly affect the current count, but set limits in some modes to determine counter behavior.

Each mode supports additional counter options.

Totalize Mode

In totalize mode, a USB-CTR Series device functions as a high speed pulse event counter for general counting applications.

Each counter can be set to any resolution up to 64-bits based on the software-selectable max limit and min limit register values. The counters can accept frequency inputs up to 48 MHz.

The counter input connector (CxIN) is used as the primary counter input, and the counter gate connector (CxGT) can be used to perform one of the following functions:

- set the count direction
- gate the counter
- clear/reload the counter with the min limit value
- trigger a particular counter to begin counting.

The following totalize measurement mode options are software-selectable:

Clear on Read: The counter is cleared after each read (synchronous or asynchronous). The value of the counter before it was cleared is latched and returned. It is typically cleared to zero, but depending on counting mode, it may be cleared to the value stored in the min limit register.

Range Limit: Set max limit and min limit register values to mimic limit switches in a mechanical counter.

- When counting up, the counter freezes or rolls over to the min limit count whenever the count reaches the max limit register value.
- When counting down, the counter freezes or rolls over to the max limit count whenever the count reaches the min limit register value.

Features

Non-recycle: The counter freezes if the max limit or min limit is reached.

- When counting up, the counter stops when the max limit is reached.
- When counting down, the counter stops when the min limit is reached.

Counting resumes if the direction is reversed or if the counter is reloaded with a value between max limit and min limit.

CountDown: Enables count down mode. This mode is overridden by the state of the gate input if the gate is programmed for direction control.

Output On: Enables counter output mode. By default, the counter output goes high when the counter reaches the value of output register 0, and low when the counter reaches the value of output register 1.

Output Initial State: Sets the initial state of the counter output to either high or low.

Direction Control: Allows the counter input connector (CxIN) to act as the pulse source and the counter gate connector (CxGT) to act as the direction. By default, the counter increments when CxGT=1 (high), and decrements when CxGT=0 (low).

Gating: Allows the counter gate connector (CxGT) to gate the counter. By default, the counter is enabled when the CxGT signal is high. When the CxGT signal is low, the counter is disabled, but holds the count value.

Clear/Reload: Clears the count to zero unless counting in Range Limit mode. If counting in Range Limit mode, the counter gate signal reloads the counter from the min limit register.

Count Trigger: The counter starts counting when the counter gate signal goes active. By default, active is on the rising edge.

Period Measurement Mode

In period measurement mode, a USB-CTR Series device measures the period of any signal at a counter input (CxIN). The device counts the integral number of ticks that make up the period, and the data returned is always time measured in ticks.

The measurement period is the time from edge-to-edge, either both rising or both falling. Period data is latched as it becomes available, and is acquired at the counter read rate.

The data returned is interpreted as time measured in ticks. This data represents the number of tick size intervals counted during the period measurement.

Optionally, the counter gate connector (CxGT) can be used to gate the counter.

- When CxGT is high, the counter is enabled.
- When CxGT is low, the counter is disabled, but holds the count value.

The 96 MHz system clock is used as the timing source. Periods from sub-microsecond to many seconds can be measured.

The following period measurement mode options are software-selectable:

Period mode: Select one of the following period modes:

- X1 – The measurement is latched each time one complete period is observed.
- X10 – The measurement is latched each time 10 complete periods are observed.
- X100 – The measurement is latched each time 100 complete periods are observed
- X1000 – The measurement is latched each time 1000 complete periods are observed.

Tick size: The tick size (or period resolution) is a fundamental unit of time derived from the period of the 96 MHz system clock. Four counter channel tick sizes are available – 20.83 ns, 208.3 ns, 2083.3 ns, and 20833.3 ns.

Pulse Width Measurement Mode

In pulse width measurement mode, a USB-CTR Series device measures the time from the rising edge to the falling edge, or vice versa, on a counter input signal (CxIN). The measurement is either pulse width low or pulse width high, depending upon the edge detection setting.

Every time the pulse width measurement is latched from the counter, the counter is immediately cleared and enabled to count the time for the next pulse width. The pulse width measurements are latched as they become available.

The data returned is interpreted as time measured in ticks. This data represents the number of tick size intervals counted during the pulse width measurement.

Optionally, the counter gate connector (CxGT) can be used to gate the counter.

- When CxGT is high, the counter is enabled.
- When CxGT is low, the counter is disabled, but holds the count value.

The 96 MHz system clock is used as the timing source. Pulse widths from sub-microsecond to many seconds can be measured.

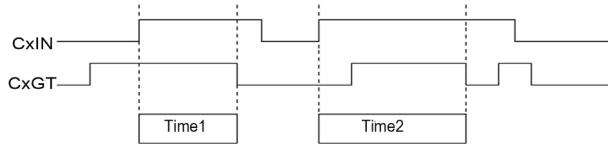
Tick size: The tick size (or pulse width resolution) is a fundamental unit of time derived from the period of the 96 MHz system clock. Four counter channel tick sizes are available – 20.83 ns, 208.3 ns, 2083.3 ns, and 20833.3 ns.

Timing Mode

In timing mode, a USB-CTR Series device measures the time between an event on the counter input (CxIN) and a subsequent event on the counter gate (CxGT), such as the rising or falling edge of one event with respect to the rising or falling edge of another event (based on the edge detection setting).

Whenever the time measurement is latched from the counter, the counter is immediately cleared and enabled for accepting the subsequent time period, which starts with the next edge on the main channel.

The following example measures the time between the rising edge on a counter input (CxIN) and the falling edge on the counter gate (CxGT). The counter read operation returns zeroes until one complete time measurement has been taken. Then, the time in ticks is latched by the device until the next time measurement has been completed. Rising edges on the counter input channel clear the counter and falling edges on the gate input latch the output of the counter at that time.



Example of a counter input channel in timing mode

The data returned is interpreted as time measured in ticks. This data represents the number of tick size intervals counted during the timing measurement.

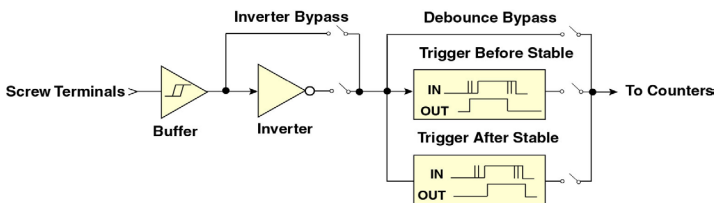
Tick size: The tick size (or timing resolution) is a fundamental unit of time derived from the period of the 96 MHz system clock. Four counter channel tick sizes are available – 20.83 ns, 208.3 ns, 2083.3 ns, and 20833.3 ns.

Debounce Filters

USB-CTR Series devices have debounce circuitry which eliminates switch-induced transients that are typically associated with electromechanical devices including relays, proximity switches, and encoders.

All debounce filter options are software selectable. You can select a debounce time, debounce mode, and rising-edge or falling-edge sensitivity. Each channel can be debounced with 16 programmable debounce times in the range of 500 ns to 25.5 ms.

The signal from the buffer can be inverted before it enters the debounce circuitry. The inverter is used to make the input rising-edge or falling-edge sensitive.



Debounce filter modes – trigger after stable and trigger before stable – and a debounce bypass

Edge selection is available with or without debounce. In this case, the debounce time setting is ignored and the input signal goes straight from the inverter or inverter bypass to the counter module.

The two debounce filter modes are *trigger after stable* and *trigger before stable*. In either mode, the selected debounce time determines how fast the signal can change and still be recognized.

Trigger After Stable Mode

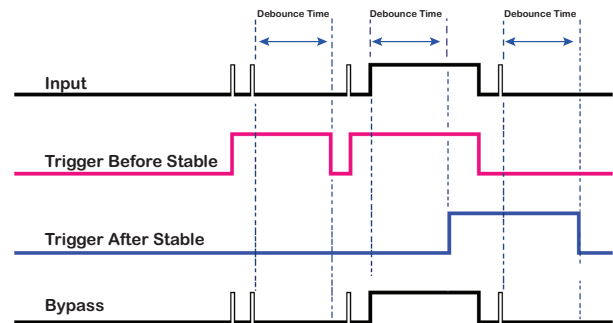
In trigger after stable mode, the output of the debounce module does not change state until a period of stability has been achieved. The input has an edge, and then must be stable for a period of time equal to the debounce time.

Trigger Before Stable Mode

In trigger before stable mode, the output of the debounce module immediately changes state, but does not change state again until a period of stability has passed. Use this mode to detect glitches.

Debounce Filter Mode Comparisons

The following diagram shows how the two modes interpret the same input signal, which exhibits glitches. Notice that the trigger before stable mode recognizes more glitches than the trigger after stable mode. Use the *bypass* option to achieve maximum glitch recognition.



Example of two debounce filter modes interpreting the same signal

Trigger after stable mode behaves more like a traditional debounce function: rejecting glitches and only passing state transitions after a required period of stability. *Trigger after stable* mode is used with electromechanical devices like encoders and mechanical switches to reject switch bounce and disturbances due to a vibrating encoder that is not otherwise moving.

Digital I/O

USB-CTR Series devices can connect up to eight digital I/O lines. The digital I/O connectors can detect the state of any TTL-level input.

Pull-Up/Down Jumper

The digital port has 47 kΩ resistors that you can configure as pull-up or pull-down with internal jumper.

Unconnected inputs are pulled low by default to 0 V through 47 kΩ resistors. The pull-up/down voltage is common to all of these resistors.

Features

Synchronous Counter and Digital Inputs

USB-CTR Series devices can read digital and counter inputs simultaneously at the supported data streaming rates (refer to [Counter I/O and Gating](#)).

Timer Output

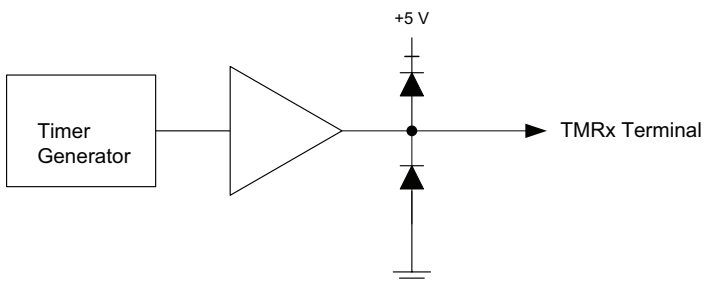
USB-CTR Series devices have four 32-bit timer outputs. Each timer can generate a programmable width pulse with a software-selectable frequency in the range of 0.02235 Hz to 48 MHz. At higher frequencies, the timer output frequency and duty cycle depend on the load impedance and the supply.

The timer output rate and pulse width can be updated asynchronously at any time; however, doing so results in a pulse stream that is not seamless.

The following timer output options are software-selectable:

- pulse frequency
- duty cycle (pulse width divided by the pulse period)
- number of pulses to generate
- time delay before starting the timer output after it's enabled
- resting state of the output (*idle high* or *idle low*)

Both the period and time delay ranges are 20.83 ns to 44.739 seconds.



USB-CTR Series PWM timer channel

Trigger Input

USB-CTR Series devices can trigger synchronous acquisitions of counter data internally with software or externally using the digital trigger input connector.

The digital trigger input allows TTL-level triggering with latencies guaranteed to be less than 20.83 ns. The acquisition can be triggered on a rising or falling edge, or on a high or low level. The trigger input is TTL logic. Latency is one sample period, maximum. The input signal range is -0.5 V to 5.5 V maximum. The logic level (1 or 0) and the rising or falling edge for the discrete trigger input are software-selectable.

When using the external trigger, the counter begins counting when the scan starts, even though acquisition of the count is held off by the trigger. To coordinate the start of the acquisition with the start of the count, you could use the trigger signal to also trigger the gate of the counter in use. Clearing the counter before starting the scan re-arms the gate trigger.

External Clock Pacing

You can pace synchronous acquisition of counter data by the onboard clock or by an external clock connected to the external clock input connector.

Power Output

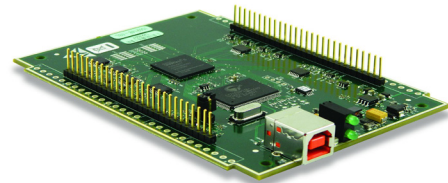
Use the +VO connector to supply power to external devices or circuitry.

The maximum total output current that can be drawn from all USB-CTR Series device connections (counter outputs, timer outputs, digital outputs, pacer clock output, and +VO) is 240 mA. This maximum applies to most personal computers and self-powered USB hubs. Bus-powered hubs and notebook computers may limit the maximum available output current to 100 mA.

If the device requires current that exceeds the current available from the computer, connect the device to a self-powered hub or power the computer with an external power adapter.

USB-CTR Series OEM Versions

OEM versions have board-only form factors with header connectors for OEM and embedded applications. All devices can be further customized to meet customer needs.



The OEM versions have the same specifications as the standard devices, but come in a board-only form factor with header connectors instead of screw terminals.

Software Support

USB-CTR Series devices are supported by the software in the table below.

Ready-to-Run Applications

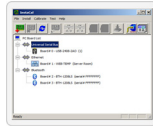
[DAQami™](#)



Data acquisition companion software with drag-and-drop interface that is used to acquire, view, and log data, and generate signals. DAQami can be configured to log analog, digital, and counter channels, and to view that data in real-time or post-acquisition on user-configurable displays. Logged data can be exported for use in Excel® or MATLAB®. Windows OS

DAQami is included with the free MCC DAQ Software bundle. Install DAQami and try the fully-functional software for 30 days. After 30 days, all features except for data logging and data export will continue to be available – data logging and data export features can be unlocked by purchasing the software.

[InstaCal™](#)



An interactive installation, configuration, and test utility for MCC hardware. Windows OS

InstaCal is included with the free MCC DAQ Software bundle.

[TracerDAQ™](#) and
[TracerDAQ Pro](#)



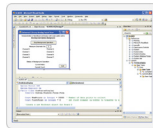
Virtual strip chart, oscilloscope, function generator, and rate generator applications used to generate, acquire, analyze, display, and export data. Supported features may vary by hardware. The Pro version provides enhanced features. Windows OS

TracerDAQ is included with the free MCC DAQ Software bundle.

TracerDAQ Pro is available as a purchased software download.

General-Purpose Programming Support

[Universal Library™
\(UL\) for Windows](#)



Library for developing applications in C, C++, VB, C# .Net, VB .Net, and Python on Windows.

The UL for Windows is included with the free MCC DAQ Software bundle.

The UL Python API for Windows is available on GitHub (<https://github.com/mccdaq/mcculw>).

[UL for Linux®](#)



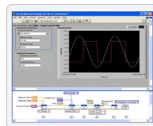
Library for developing applications in C, C++, and Python on Linux.

UL for Linux is available on GitHub (<https://github.com/mccdaq/uldaq>).

Open-source, third-party Linux drivers are also available for supported MCC devices.

Application-Specific Programming Support

[ULx for
NI LabVIEW™](#)



A comprehensive library of VIs and example programs for NI LabVIEW that is used to develop custom applications that interact with most MCC devices. Windows OS

ULx for NI LabVIEW is included with the free MCC DAQ Software bundle.

[DASYLab®](#)



Icon-based data acquisition, graphics, control, and analysis software that allows users to create complex applications in minimal time without text-based programming. Windows OS

DASYLab is available as a purchased software download. An evaluation version is available for 28 days.

Specifications

All specifications are subject to change without notice. Typical for 25°C unless noted otherwise.

These specifications apply to both USB-CTR Series standard and OEM versions unless noted otherwise.

Counter

Counter type: FPGA

Counters

USB-CTR08: 8

USB-CTR04: 4

Each counter channel has a corresponding input, gate, and output connector

Counter input modes: Totalize, Pulse width, Period, Timing

Mode options: Non-Recycle, range limit, clear on read, up/down

Gate options: Clear/reload, direction control, gate, count trigger; mode dependent

Resolution: Up to 64-bits (software-selectable)

Maximum input frequency: 48 MHz

Debounce times: 16 steps from 500 ns to 25.5 ms; positive or negative edge sensitive; glitch detect mode or debounce mode; software-selectable.

Timebase and accuracy: 96 MHz (24 MHz – 30 ppm with a 4x DLL (delay-locked loop))

Counter read pacer: Internal or external scan pacer up to 4 MHz

Period/pulse width/timing resolution: 20.83 ns; 208.3 ns; 2.083 μ s; or 20.83 μ s

Input type (counter input and gate connectors): Schmitt trigger, 47 k Ω pull-down to ground with 33 Ω in series

Schmitt trigger hysteresis (C0IN to C7IN and C0GT to C7GT): 0.76 V typ, 0.4 V min, 1.2 V max

Input high voltage threshold (C0IN to C7IN and C0GT to C7GT): 1.74 V typ, 1.3 V min, 2.2 V max

Input high voltage limit (C0IN to C7IN and C0GT to C7GT): 5.5 V absolute max

Input low voltage threshold (C0IN to C7IN and C0GT to C7GT): 0.98 V typ, 0.6 V min, 1.5 V max

Input low voltage limit (C0IN to C7IN and C0GT to C7GT): –0.5 V absolute min, 0 V recommended min

Output high voltage: 4.4 V min (IOH = –50 μ A); 3.76 V min (IOH = –24 mA)

Output low voltage: 0.1 V max (IOL = 50 μ A); 0.44 V max (IOL = 24 mA)

Output current: 24 mA max per pin, constrained to 240 mA across all output pins (counter outputs, timer outputs, digital outputs, pacer clock output, and +VO)

Timers

Terminal names: TMR0, TMR1, TMR2, TMR3

Timer type: PWM output with count, period, delay, and pulse width registers

Output value: Default state is idle low with pulses high, software-selectable output invert

Internal clock frequency: 96 MHz

Effective frequency range: 0.022 Hz to 48 MHz

Register widths: 32-bit

High pulse width: 10.42 ns min

Low pulse width: 10.42 ns min

Output high voltage: 4.4 V min (IOH = –50 μ A); 3.76 V min (IOH = –24 mA)

Output low voltage: 0.1 V max (IOL = 50 μ A); 0.44 V max (IOL = 24 mA)

Output current: 24 mA max per pin, constrained to 240 mA across all output pins (counter outputs, timer outputs, digital outputs, pacer clock output, and +VO)

Digital Input/Output

Digital type: TTL

Number of I/O: 8

Configuration: Bit-configurable as input (power on default) or output

Pull-up configuration: The port has a 47 k Ω resistor configurable as a pull-up or pull-down (default) with an internal jumper.

Digital I/O transfer rate (system-paced, asynchronous): 33 to 8000 port reads/writes or single bit reads/writes per second typical, system dependent.

Digital input pacing: Onboard clock, external input scan clock (CLKI)

Digital input trigger source: External single channel digital trigger (TRIG)

Input high voltage: 2.0 V min, 5.0 V absolute max

Input low voltage: 0.8 V max, 0 V recommended min

Output high voltage: 4.4 V min (IOH = –50 μ A), 3.76 V min (IOH = –24 mA)

Output low voltage: 0.1 V max (IOL = 50 μ A), 0.44 V max (IOL = 24 mA)

Output current: 24 mA max per pin, constrained to 240 mA across all output pins (counter outputs, timer outputs, digital outputs, pacer clock output, and +VO)

External Trigger

Trigger source: External digital; TRIG terminal

Trigger mode: Software-selectable for edge or level sensitive, rising or falling edge, high or low level.

Trigger latency: 100 ns max

Trigger pulse width: 100 ns min

Input type: Schmitt trigger, 47 k Ω pull-down to ground with 33 Ω in series

Schmitt trigger hysteresis: 0.76 V typ, 0.4 V min, 1.2 V max

Input high voltage threshold: 1.74 V typ, 1.3 V min, 2.2 V max

Input high voltage limit: 5.5 V absolute max

Input Low voltage threshold: 0.98 V typ, 0.6 V min, 1.5 V max

Input low voltage limit: –0.5 V absolute min, 0 V recommended min

External Clock Input/Output

Terminal names: CLKI, CLKO

Terminal type

CLKI: Input, active on rising edge

CLKO: Output, power on default is 0 V, active on rising edge

Input clock frequency: 4 MHz, max

Input clock pulse width: 10.417 ns min

Input type: Schmitt trigger, 47 k Ω pull-down to ground with 33 Ω in series

Input Schmitt trigger hysteresis: 0.76 V typ, 0.4 V min, 1.2 V max

Input high voltage threshold: 1.74 V typ, 1.3 V min, 2.2 V max

Input high voltage limit: 5.5 V absolute max

Input low voltage threshold: 0.98 V typ, 0.6 V min, 1.5 V max

Input low voltage limit: –0.5 V absolute min, 0 V recommended min

Output clock frequency: 4 MHz, max

Output clock pulse width: 10.417 ns

Output high voltage: 4.4 V min (IOH = –50 μ A), 3.76 V min (IOH = –24 mA)

Output low voltage: 0.1 V max (IOL = 50 μ A), 0.44 V max (IOL = 24 mA)

Output current: 24 mA max per pin, constrained to 240 mA across all output pins (counter outputs, timer outputs, digital outputs, pacer clock output, and +VO)

Memory

FIFO: 8 KS

Non-volatile EEPROM: 32 KB (10 KB firmware storage, 22 KB calibration/user data)

Power

Supply current, USB source

During enumeration: < 100 mA

After USB enumeration: < 500 mA

+VO power available: After USB enumeration: 5 V, \pm 5%

+VO output current: After USB enumeration: 24 mA max per pin, constrained to

240 mA across all output pins (counter outputs, timer outputs, digital outputs, pacer clock output, and +VO)

USB

USB device type: USB 2.0 (high-speed)

Device compatibility: USB 1.1, USB 2.0, USB 3.0

USBCable type: A-B cable, UL type AWM 2725 or equivalent. (min 24 AWG VBUS/GND, min 28 AWG D+/D–)

USB cable length: 3 m (9.84 ft) max

Environmental

Operating temperature range: 0 °C to 50 °C

Storage temperature range: –40 °C to 70 °C

Humidity: 0% to 90% non-condensing

Mechanical

Dimensions (L \times W \times H)

Standard versions: 127 \times 89.9 \times 35.6 mm (5.00 \times 3.53 \times 1.40 in.)

OEM versions: 127 \times 89.9 \times 35.6 mm (4.7 \times 3.4 \times 0.60 in.)

User connection length: 3 m (9.84 ft) max

Signal Connector

Standard versions: Two banks of screw-terminal blocks

Wire gauge range: 16 AWG to 30 AWG

OEM versions: Two 1 \times 28 pin 0.1 in. pitch headers, labeled W1 and W3

USB-CTR Series

Ordering



Order Information

Hardware

Part No.	Description
USB-CTR04	High-speed counter/timer device with 4 counter I/O, 4 PWM timer outputs, and 8 digital I/O. Includes USB cable and MCC DAQ software.
USB-CTR08	High-speed counter/timer device with 8 counter I/O, 4 PWM timer outputs, and 8 digital I/O. Includes USB cable and MCC DAQ software.
USB-CTR04-OEM	Board-only high-speed counter/timer device with 4 counter I/O, 4 PWM timer outputs, and 8 digital I/O.
USB-CTR08-OEM	Board-only high-speed counter/timer device with 8 counter I/O, 4 PWM timer outputs, and 8 digital I/O.

Software also Available from MCC

Part No.	Description
DAQami	Data acquisition companion software for acquiring data and generating signals
TracerDAQ Pro	Out-of-the-box virtual instrument suite with strip chart, oscilloscope, function generator, and rate generator – professional version
DASyLab	Icon-based data acquisition, graphics, control, and analysis software