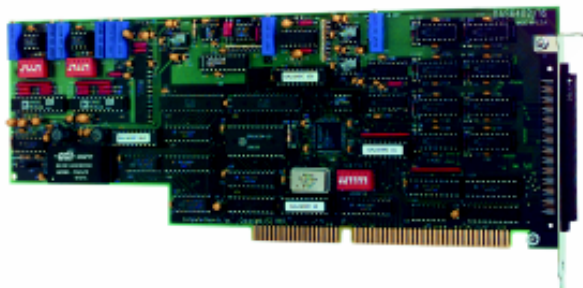# CIO-DAS6402/16 & CIO-DAS6402/12

High Speed 64 Channel Analog Input boards
with 2 Analog Output Channels & 8 Digital I/O bits

CIO-DAS6402/16

Features

- 32 ch diff. / 64 single-ended
- 16-bit A/D resolution
- 100Khz sample rate
- Dual 16-bit D/As
- 1024 sample FIFO
- 16-bits digital I/O
- 3 CTRs

CIO-DAS6402/12

Features

- 32 ch diff. / 64 single-ended
- 12-bit A/D resolution
- 330 KHz sample rate
- Dual 12-bit D/As
- 1024 sample FIFO
- 16-bits digital I/O
- 3 CTRs

DESCRIPTION

The CIO-DAS6402 multifunction analog and digital I/O boards set the new standard for high channel count, high speed data acquisition.

Installed in any ISA-bus compatible personal computer the CIO-DAS6402 turns your personal computer into a high speed data acquisition and control station suitable for laboratory data collection, instrumentation, production test, or industrial monitoring.

The CIO-DAS6402 is supported by the Universal Library software allowing users to program in and DOS or Windows-based language. The board is also supported by a wide vareity of powerful applications packages including HP VEE.

FIFO Buffer = Windows Ready

The FIFO Buffer collects the results of A/D conversions and stores them until the personal computer CPU is able to transfer the data into PC memory. A FIFO buffer allows the PC to store up the A/D transfer requests, then service the requests in batches. Under Windows, many demanding resources employ block transfers. Your A/D board should work in concert rather than conflict with your high performance PC.

FIFO Stores data, PC stores transfer requests. All transfer requests are serviced.
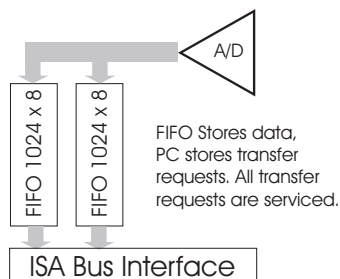
12- AND 16-BIT RESOLUTION

The CIO-DAS6402/16 provides a full 16 bits of A/D resolution (1 part in 65,536) while the CIO-DAS6402/12 provides 12-bit resolution (1 part in 4096).

The only difference between the 12 and 16 bit A/D control registers is the A/D least significant byte data register. Shown below is A/D data registers for the 6402/12 and 6402/16. The 16 bit board simply has useful data in the 4 least significant bits (instead of 0). This is also the format difference when writing the D/A registers.

12 Bit Board A/D Data format

D15	D14	D13	...	D5	D4	D3	D2	D1	D0
A11	A10	A9	...	A1	A0	0	0	0	0

16 Bit Board A/D Data format

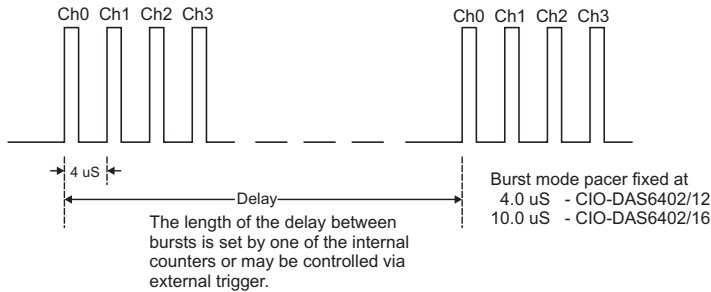| D15	D14	D13	...	D5	D4	D3	D2	D1	D0
A15	A14	A13	...	A5	A4	A3	A2	A1	A0

All A/D range selection on the CIO-DAS6402 is selected via software. The D/A range on the CIO-DAS6402/12 is also set via software while the output range of the CIO-DAS6402/16 is set by DIP switches on the board. The ranges and resolutions available on the CIO-DAS6402 boards are shown below.

Bipolar Range	12-bit Res.	16-bit Res.	Unipolar Range	12-bit Res.	16-bit Res.
±10V	4.88mV	305uV	0 - 10V	2.44mV	153uV
±5V	2.44mV	153uV	0 - 5V	1.22mV	76.3uV
±2.5V	1.22mV	76.3uV	0-2.5V	0.61mV	38.1uV
±1.25V	0.61mV	38.1uV	0-1.25V	0.305mV	19.1uV

MINIMIZING CHANNEL-CHANNEL SKEW (BURST MODE)

Channel to channel skew is the result of multiplexing the A/D inputs and is defined as the time between consecutive samples. For example, if four channels are sampled at a rate of 1Khz per channel, the channel skew is 250uS (1mS / 4).

Burst mode minimizes channel to channel skew by clocking the A/D at the maximum rate between successive channels. For example, at the 1mS pulse channel 0 is sampled, then channel 1 is sampled 4uS later, then channel 2, 4uS after that and channel 3, 4uS after that. Then no samples are taken until the next 1mS pulse when channel 0 is sampled again. In this scheme the rate for all channels is 1KHz but the channel to channel skew (delay) is now 10uS between channels or 12uS total. The minimum burst mode delay is 10 uS on the CIO-DAS6402/16 and 4 uS for the CIO-DAS6402/12.

Ch0 Ch1 Ch2 Ch3   Ch0 Ch1 Ch2 Ch3

4 uS

Delay

The length of the delay between bursts is set by one of the internal counters or may be controlled via external trigger.

Burst mode pacer fixed at
4.0 uS   - CIO-DAS6402/12
10.0 uS - CIO-DAS6402/16

CONNECTOR

All I/O signals are brought through a 100-pin high-density connector. Field wiring is greatly simplified by using the optional C100-FF2 cable and CIO-TERM100 screw terminal board. The Pinout of the CIO-DAS6402 is shown below.

LLGND	1	51	LLGND
IN0+	2	52	IN16+
IN0-/IN32+	3	53	IN16-/IN48+
IN1+	4	54	IN17+
IN1-/IN33+	5	55	IN17-/IN49+
IN2+	6	56	IN18+
IN2-/IN34+	7	57	IN18-/IN50+
IN3+	8	58	IN19+
IN3-/IN35+	9	59	IN19-/IN51+
IN4+	10	60	IN20+
IN4-/IN36+	11	61	IN20-/IN52+
IN5+	12	62	IN21+
IN5-/IN37+	13	63	IN21-/IN53+
IN6+	14	64	IN22+
IN6-/IN38+	15	65	IN22-/IN54+
IN7+	16	66	IN23+
IN7-/IN39+	17	67	IN23-/IN55+
LLGND	18	68	LLGND
IN8+	19	69	IN24+
IN8-/IN40+	20	70	IN24-/IN56+
IN9+	21	71	IN25+
IN9-/IN41+	22	72	IN25-/IN57+
IN10+	23	73	IN26+
IN10-/IN42+	24	74	IN26-/IN58+
IN11+	25	75	IN27+
IN11-/IN43+	26	76	IN27-/IN59+
IN12+	27	77	IN28+
IN12-/IN44+	28	78	IN28-/IN60+
IN13+	29	79	IN29+
IN13-/IN45+	30	80	IN29-/IN61+
IN14+	31	81	IN30+
IN14-/IN46+	32	82	IN30-/IN62+
IN15+	33	83	IN31+
IN15-/IN47+	34	84	IN31-/IN63+
GROUND FOR DAC0	35	85	DOUT0
DAC0 OUTPUT	36	86	DOUT1
GROUND FOR DAC1	37	87	DOUT2
DAC1 OUTPUT	38	88	DOUT3
CTR0 CLK IN	39	89	CHASSIS GND
DIN2/CTR0 GATE	40	90	+12V SUPPLY OUT
COUNTER 0 OUTPUT	41	91	CHASSIS GND
DIN0/AD PACER IN	42	92	-12V SUPPLY OUT
DIN1/AD GATE/AD TRIG	43	93	DIN6
DIN 3	44	94	DIN7
DIN 4	45	95	DOUT4
DIN 5	46	96	DOUT5
-5V REF OUT	47	97	DOUT6
+5V SUPPLY OUT	48	98	DOUT7
SSH OUT	49	99	EXTERNAL INTERRUPT IN
CHASSIS GND	50	100	CHASSIS GND

CIO-DAS6402 ANALOG SIGNAL CONNECTOR - View from rear of the computer.

SPECIFICATIONS
(Typical for 25 Deg. C unless otherwise specified.)

Analog input section (6402/16)

Resolution	16 bits
A/D conversion time	5 µs
Throughput	100KHz min
Integral Linearity error	±2LSB max
No missing codes guaranteed	16 bits
Gain drift (A/D specs)	±7ppm/°C, all ranges
Zero drift (A/D specs)	±2ppm/°C, all ranges
Input leakage current	200nA
Input impedance	Min 10Meg Ohms
Absolute maximum input voltage	±15V
A/D Triggering Modes	Edge (triggered) or level (gated). Programmable polarity Unlimited pre- and post-trigger samples.

Analog input section (6402/12)

Resolution	12 bits
A/D conversion time	3 µs
Throughput	333KHz min
Differential Linearity error	±.75LSB
Integral Linearity error	±.5LSB
Gain drift (A/D specs)	±6ppm/°C, all ranges
Zero drift (A/D specs)	±1ppm/°C, all ranges
Input leakage current	200nA
Input impedance	Min 10Meg Ohms
Absolute maximum input voltage	±15V
A/D Triggering Modes	Edge (triggered) or level (gated). Programmable polarity Unlimited pre- ans post-trigger samples.

Analog Output (6402/16)

Resolution	16 bits
Number of channels	2 Voltage Output
Voltage Ranges	±2.5, ±5, ±10, 0-2.5, 0-5, 0-10 switch selectable
Differential nonlinearity	±2LSB max over temperature
Integral nonlinearity	±2LSB max over temperature
Monotonicity	Guaranteed monotonic to 15 bits
Gain drift	±15 ppm/°C max
Bipolar offset drift	±5 ppm/°C max
Unipolar offset drift	±3 ppm/°C max
Settling time (20V step to ±½LSB)	12µs typ, 19us max
Settling time (10V step to ±½LSB)	6µs typ, 9us max
Slew Rate	2.8 V/uS Typical
Current Drive	±5mA min
Output short-circuit duration	40 mA min Continuous
Amp Output Impedance (OP-27)	0.1 Ohms max
Miscellaneous	On power up and reset, all DAC's cleared to 0 volts

Analog Output (6402/12)

Channels	two
Resolution	12-bit
Channel configuration	Voltage Output
Voltage Ranges	±10V, ±5V, 0-5V, 0-10V. Software programmable
Differential nonlinearity	±1 LSB max
Integral nonlinearity	±1 LSB max
Monotonicity	Guaranteed monotonic over temperature
D/A Gain drift	±15 ppm/°C max
D/A Bipolar offset drift	±5 ppm/°C max
D/A Unipolar offset drift	±3 ppm/°C max
Throughput	System dependent (software paced)
Settling time (20V step to ±½ LSB)	5 μs typ, 8 μs max
Slew Rate	4V/μs typ
Current Drive	±2 mA min
Output short-circuit duration	25 mA indefinite
Amp Output Impedance (AD711)	0.1 Ohms max
Miscellaneous	On power up and reset, all DAC's cleared to 0 volts

Digital Input / Output

Digital Type	Output: 74LS244 Input: 74LS273
Configuration	Enhanced: Two dedicated ports, 8 input and 8 output
Output High	2.7 volts @ -.4mA min
Output Low	0.4 volts @ 8 mA min
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min

Counter section

Counter type	82C54
Configuration	3 down counters, 16 bits each

Environmental

Operating temperature range	0 to 70°C
Storage temperature range	-40 to 100°C
Humidity	0 to 90% non-condensing

Power consumption

Icc: Operating (6402/16)	1.17A typical, 1.67A max
Icc: Operating (6402/12)	1.05A typical, 1.6A max

SOFTWARE

All CIO-DAS6402 boards come complete with ComputerBoard's powerful and helpful *InstaCal*™ software package. *InstaCal*™ is a complete installation, calibration and test program for all ComputerBoards data acquisition and control boards. Complete with extensive error checking, *InstaCal*™ guides you through installation and setup of your data acquisition board and creates the board configuration file for the Universal Library

The CIO-DAS6402 boards are also fully compatible with ComputerBoards' powerful UniversalLibrary. The Universal Library is a complete set of I/O libraries and drivers for all of our boards, for all Windows and DOS languages.

Universal means **board** to board the **syntax** for an analog input is the same. From CIO-DAS08 to CIO-DAS16/M1 the programming line looks the same. In addition, the UniversalLibrary is intelligent. It knows about individual boards and their capabilities. If you ask for something the board cannot do, a warning message supplies the information you need to correct the program.

Universal means language-to-language the **syntax** remains constant. The functions and features remain constant. The intelligent capability parser remains constant. Want to change programming languages? The UniversalLibrary requires no relearning.

ACCESSORIES

Field wiring is greatly simplified when you purchase the optional C100-FF2 cable and CIO-TERM100 screw terminal board. This combination brings all 100 CIO-DAS6402 pins out to easy to connect to screw terminals. The screw terminals accept wire sizes 12-22 AWG. The board provides positions to mount pull-up and pull down resistors or other user installed circuitry.
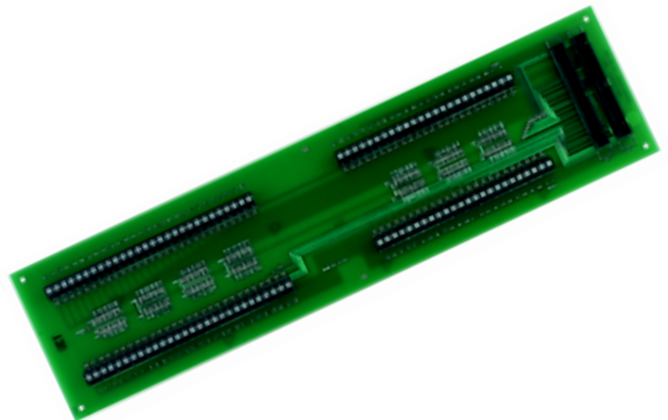
ORDERING GUIDE

CIO-DAS6402/16	64 channel, 16-bit analog I/O board
CIO-DAS6402/12	64 channel, 12-bit analog I/O board
C100-FF2	100 conductor cable
CIO-TERM100	100 terminal screw terminal adapter board