Specifications

USB-1616HS

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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

A/D converter type	Successive approximation	
Resolution	16 bits	
Number of channels	16 single-ended/8 differential, software-selectable. Up to 48 additional analog inputs per module are available with the optional AI-EXP48 module. Expansion channel features are the same as those of the main channels.	
Input ranges (software and sequencer programmable)	Bipolar: ±10 V, ±5 V, ±2 V, ±1 V , ±0.5 V, ±0.2 V, ±0.1 V	
Maximum sample rate	1 MHz	
Nonlinearity (integral)	±2 LSB maximum	
Nonlinearity (differential)	±1 LSB maximum	
A/D pacing	Onboard input scan clock, external source (APR)	
Trigger sources and modes	See Table 7	
Acquisition data buffer	1 MSample	
Data transfer	DMA	
Configuration memory	Programmable I/O	
Maximum usable input voltage + common mode voltage (CMV + V_{in})	Range: ±10 V, ±5 V, ±2 V, ±1 V, ±0.5 V	10.5 V maximum
	Range: ±0.2 V, ±0.1 V	2.1 V maximum
Signal to noise and distortion	*72 dB typical for ±10 V range, 1 kHz fundamental*	
Total harmonic distortion	*-80 dB typical for ±10 V range, 1 kHz fundamental*	
Calibration	Auto-calibration, calibration factors for each range stored onboard in non-volatile RAM.	
CMRR @ 60 Hz	-70 dB typical DC to 1 kHz	
Bias current	*40 pA typical (0 °C to 35°C)*	
Crosstalk	*-75 dB typical DC to 60 Hz; -65 dB typical @ 10 kHz*	
Input impedance	*10 MΩ single-ended, 20 MΩ differential*	
Absolute maximum input voltage	*±30 V*	

Accuracy

Table 2. Analog input accuracy specifications

Voltage range		**Accuracy ±(% of reading + % range) 23°C ±10 °C, 1 year**	**Temperature coefficient ±(ppm of reading + ppm range)/°C**	**Noise (cts RMS)**	
-10 V to 10 V	Note 1	*0.031% + 0.008%*	*14 + 8*	2.0	Note 2
-5 V to 5 V		*0.031% + 0.009%*	*14 + 9*	3.0	
-2 V to 2 V		*0.031% + 0.010%*	*14 +10*	2.0	
-1 V to 1 V		*0.031% + 0.02%*	*14 + 12*	3.5	
-500 mV to 500 mV		*0.031% + 0.04%*	*14 +18*	5.5	
-200 mV to 200 mV		*0.036% + 0.075%*	*14 +12*	8.0	
-100 mV to 100 mV		*0.042% + 0.15%*	*14 +18*	14.0	

Note 1: Specifications assume differential input single-channel scan, 1 MHz scan rate, unfiltered, CMV=0.0 V, 30 minute warm-up, exclusive of noise, range is +FS to -FS.

Note 2: Noise reflects 10,000 samples at 1 MHz, typical, differential short.

Thermocouples

Table 3. Thermocouple (TC) types and accuracy (Note 3)

TC type	Temperature range (°C)	Accuracy (±°C)	Noise typical (±°C)
J	-200 to + 760	1.7	0.2
K	-200 to + 1200	1.8	0.2
T	-200 to + 400	1.8	0.2
E	-270 to + 650	1.7	0.2
R	-50 to + 1768	4.8	1.5
S	-50 to + 1768	4.7	1.5
N	-270 to + 1300	2.7	0.3
B	+300 to + 1400	3.0	1.0

Note 3: Assumes 16384 oversampling applied, CMV = 0.0V, 60 minute warm-up, still environment, and 25 °C ambient temperature; excludes thermocouple error; TC_{in} = 0° C for all types except B (1000 °C), TR-2U power supply for external power.

Digital input/output

Table 4. Digital input/output specifications

Number of I/O	24
Ports	Three banks of eight. Each port is programmable as input or output
Input scanning modes	Two programmable ▪ Asynchronous, under program control at any time relative to input scanning ▪ Synchronous with input scanning
Input characteristics	220 Ω series resistors, 20 pF to common
Logic keeper circuit	Holds the logic value to 0 or 1 when there is no external driver
Input protection	±15 kV ESD clamp diodes parallel
Input high	*+2.0 V to +5.0 V*
Input low	*0 to 0.8 V*
Output high	*>2.0 V*
Output low	*<0.8 V*
Output current	Output 1.0 mA per pin Sourcing more current may require a TR-2U power supply.
Digital input pacing	Onboard input scan clock, external input scan clock (APR)
Digital output pacing	Four programmable sources: ▪ Onboard output scan clock, independent of input scan clock ▪ Onboard input scan clock ▪ External output scan clock (DPR), independent of external input scan clock (APR) ▪ External input scan clock (APR)
Digital input trigger sources and modes	See Table 7
Digital output trigger sources	Start of input scan
Data transfer	DMA
Sampling/update rate	4 MHz maximum (rates up to 12 MHz are sustainable on some platforms)
Pattern generation output	Two of the 8-bit ports can be configured for 16-bit pattern generation. The pattern can also be updated synchronously with an acquisition at up to 4 MHz.

Counters

Counter inputs can be scanned based on an internal programmable timer or an external clock source.

Table 5. Counter specifications

Channels	4 independent
Resolution	32-bit
Input frequency	20 MHz maximum
Input signal range	-5 V to 10 V
Input characteristics	10 kΩ pull-up, 200 Ω series resistor, ±15 kV ESD protection
Trigger level	TTL
Minimum pulse width	25 ns high, 25 ns low
Debounce times	16 selections from 500 ns to 25.5 ms, positive or negative edge sensitive, glitch detect mode or debounce mode
Time base accuracy	50 ppm (0 ° to 50 °C)
Counter read pacer	Onboard input scan clock, external input scan clock (APR)
Trigger sources and modes	See Table 7
Programmable mode	Counter
Counter mode options	Totalize, clear on read, rollover, stop at all Fs, 16- or 32-bit, any other channel can gate the counter

Input sequencer

Analog, digital, and counter inputs can be scanned based on either an internal programmable timer or an external clock source.

Table 6. Input sequencer specifications

Input scan clock sources: two (see Note 4)	Internal, programmable: ▪ Analog channels from 1 µs to 1 s in 20.83 ns steps. ▪ Digital channels and counters from 250 ns to 1 s in 20.83 ns steps. External. TTL level input (APR): ▪ Analog channels down to 1 µs minimum ▪ Digital channels and counters down to 250 ns minimum
Programmable parameters per scan:	Programmable channels (random order), programmable gain
Depth	512 locations
Onboard channel-to-channel scan rate	Analog: 1 MHz maximum Digital: 4 MHz if no analog channels are enabled, 1 MHz with analog channels enabled
External input scan clock (APR) maximum rate	Analog: 1.0 MHz Digital: 4 MHz if no analog channels are enabled, 1 MHz with analog channels enabled
Clock signal range:	Logical zero: 0 V to 0.8 V Logical one: 2.4 V to 5.0 V
Minimum pulse width	50 ns high, 50 ns low

Note 4: The maximum scan clock rate is the inverse of the minimum scan period. The minimum scan period is equal to 1 µs times the number of analog channels. If a scan contains only digital channels, then the minimum scan period is 250 ns.

Some platforms can sustain clock rates up to 83.33 ns.

Triggering

Table 7. Trigger sources and modes

Trigger source	Explanation
Single channel analog hardware trigger	Any analog input channel can be software programmed as the analog trigger channel, including any of the analog expansion channels. ▪ Input signal range: -10 V to +10 V maximum ▪ Trigger level: Programmable (12-bit resolution) ▪ Latency: 350 ns typical, 1.3 µs max ▪ Accuracy: ±0.5% of reading, ±2 mV offset maximum ▪ Noise: 2 mV RMS typical
Single channel analog software trigger	Any analog input channel—including any of the analog expansion channels, can be selected as the software trigger channel. If the trigger channel involves a calculation, such as temperature, then the driver automatically compensates for the delay required to obtain the reading, resulting in a maximum latency of one scan period. ▪ Input signal range: Anywhere within range of the trigger channel ▪ Trigger level: Programmable (16-bit resolution) ▪ Latency: One scan period (maximum)
External-single channel digital trigger	A separate digital input is provided for digital triggering. ▪ Input signal range: -15 V to +15 V maximum ▪ Trigger level: TTL level sensitive ▪ Minimum pulse width: 50 ns high, 50 ns low ▪ Latency: One scan period maximum
Digital pattern triggering	8-bit or 16-bit pattern triggering on any of the digital ports. Programmable for trigger on equal, not equal, above, or below a value. ▪ Individual bits can be masked for "don't care" condition. ▪ Latency: One scan period, maximum
Counter/totalizer triggering	Counter/totalizer inputs can trigger an acquisition. User can select to trigger on a frequency or on total counts that are equal, not equal, above, or below a value, or within/outside of a window rising/falling edge. ▪ Latency: One scan period, maximum

Frequency/pulse generators

Table 8. Frequency/pulse generator specifications

Channels	2 × 16-bit
Output waveform	Square wave
Output rate	1 MHz base rate divided by 1 to 65535 (programmable)
High-level output voltage	2.0 V minimum @ -1.0 mA, 2.9 V minimum @ -400 µA
Low-level output voltage	0.4 V maximum @ 400 µA

Power consumption

Power consumption specification is for a USB-1616HS. Add 400mW for a USB-1616HS connected to an AI-EXP48 expansion module.

Table 9. Power consumption specifications (Note 5)

Power consumption (per board)	3000 mW

External power

Table 10. External power specifications (Note 5)

Connector	Switchcraft # RAPC-712
Power range	6 to 16 VDC (used when USB port supplies insufficient power, or when an independent power supply is desired)
Over-voltage	20 V for 10 seconds, maximum

Note 5: The power supply (MCC p/n TR-2U) and line cord (MCC p/n CA-1) are required if the USB port cannot supply adequate power. By USB 2.0 standards, USB 2.0 ports must supply 2500 mW (nominal at 5 V, 500 mA)

USB specifications

Table 11. USB specifications

USB-device type	USB 2.0 high-speed mode (480 Mbps) if available (recommended), otherwise, USB1.1 full-speed mode (12 Mbps)
Device compatibility	USB 2.0 (recommended) or USB 1.1

Environmental

Table 12. Environmental specifications

Operating temperature range	-30 °C to +70 °C
Storage temperature range	-40 °C to +80 °C
Relative humidity	0 to 95% non-condensing

Mechanical

Table 13. Mechanical specifications

Vibration	MIL STD 810E category 1 and 10
Dimensions	269 mm (W) x 92 mm (D) x 45 mm (H)(10.6” x 3.6” x 1.6”)
Weight	431 g (0.95 lbs)

Signal I/O connectors and pin out

Table 14. Screw connector specifications

Connector type	Screw terminal
Wire gauge range	14 AWG to 30 AWG
Expansion connector type	25-pin DSUB, female
Compatible expansion products	AI-EXP48 expansion module with screw terminals

Table 15. USB-1616HS screw terminal pin out – single-ended connections

Analog Out	Analog common (A▼)		Port A	Digital common (D▼)	**DIG-Tmr I/O**
	NC			FIRSTPORTA Bit 0 (A0)	
	NC			FIRSTPORTA Bit 1 (A1)	
	NC			FIRSTPORTA Bit 2 (A2)	
	NC			FIRSTPORTA Bit 3 (A3)	
	Analog common (A▼)			FIRSTPORTA Bit 4 (A4)	
	CAL (Reserved for self-calibration)			FIRSTPORTA Bit 5 (A5)	
	Signal ground (S▼)			FIRSTPORTA Bit 6 (A6)	
	Digital common (D▼)			FIRSTPORTA Bit 7 (A7)	
	TTL trigger (TRG)			Digital common (D▼)	
	Output scan clock I/O (DPR)			Timer 0 (T0)	
	Input scan clock I/O (APR)			Timer 1 (T1)	
Analog In	Analog common (A▼)		Port B	Digital common (D▼)	**Dig-Ctr I/O**
	CH 0 (0H)			FIRSTPORTB Bit 0 (B0)	
	CH 8 (8L)			FIRSTPORTB Bit 1 (B1)	
	Analog common (A▼)			FIRSTPORTB Bit 2 (B2)	
	CH 1 (1H)			FIRSTPORTB Bit 3 (B3)	
	CH 9 (9L)			FIRSTPORTB Bit 4 (B4)	
	Analog common (A▼)			FIRSTPORTB Bit 5 (B5)	
	CH 2 (2H)			FIRSTPORTB Bit 6 (B6)	
	CH 10 (10L)			FIRSTPORTB Bit 7 (B7)	
	Analog common (A▼)			Digital common (D▼)	
	CH 3 (3H)			Counter 0 (CT0)	
	CH 11 (11L)			Counter 1 (CT1)	
Analog In	Analog common (A▼)		Port C	Digital common (D▼)	**Dig-Ctr I/O**
	CH 4 (4H)			FIRSTPORTC Bit 0 (C0)	
	CH 12 (12L)			FIRSTPORTC Bit 1 (C1)	
	Analog common (A▼)			FIRSTPORTC Bit 2 (C2)	
	CH 5 (5H)			FIRSTPORTC Bit 3 (C3)	
	CH 13 (13L)			FIRSTPORTC Bit 4 (C4)	
	Analog common (A▼)			FIRSTPORTC Bit 5 (C5)	
	CH 6 (6H)			FIRSTPORTC Bit 6 (C6)	
	CH 14 (14L)			FIRSTPORTC Bit 7 (C7)	
	Analog common (A▼)			Digital common (D▼)	
	CH 7 (7H)			Counter 2 (CT2)	
	CH 15 (15L)			Counter 3 (CT3)	

Table 16. USB-1616HS screw terminal pin out – differential connections

Analog Out	Analog common (A▾)		Port A	Digital common (D▾)	**DIG-Tmr I/O**
	NC			FIRSTPORTA Bit 0 (A0)	
	NC			FIRSTPORTA Bit 1 (A1)	
	NC			FIRSTPORTA Bit 2 (A2)	
	NC			FIRSTPORTA Bit 3 (A3)	
	Analog common (A▾)			FIRSTPORTA Bit 4 (A4)	
	CAL (Reserved for self-calibration)			FIRSTPORTA Bit 5 (A5)	
	Signal ground (S▾)			FIRSTPORTA Bit 6 (A6)	
	Digital common (D▾)			FIRSTPORTA Bit 7 (A7)	
	TTL trigger (TRG)			Digital common (D▾)	
	Output scan clock I/O (DPR)			Timer 0 (T0)	
	Input scan clock I/O (APR)			Timer 1 (T1)	
Analog In	Analog common (A▾)		Port B	Digital common (D▾)	**Dig-Ctr I/O**
	CH 0 HI (0H)			FIRSTPORTB Bit 0 (B0)	
	CH 0 LO (8L)			FIRSTPORTB Bit 1 (B1)	
	Analog common (A▾)			FIRSTPORTB Bit 2 (B2)	
	CH 1 HI (1H)			FIRSTPORTB Bit 3 (B3)	
	CH 1 LO (9L)			FIRSTPORTB Bit 4 (B4)	
	Analog common (A▾)			FIRSTPORTB Bit 5 (B5)	
	CH 2 HI (2H)			FIRSTPORTB Bit 6 (B6)	
	CH 2 LO (10L)			FIRSTPORTB Bit 7 (B7)	
	Analog common (A▾)			Digital common (D▾)	
	CH 3 HI (3H)			Counter 0 (CT0)	
	CH 3 LO (11L)			Counter 1 (CT1)	
Analog In	Analog common (A▾)		Port C	Digital common (D▾)	**Dig-Ctr I/O**
	CH 4 HI (4H)			FIRSTPORTC Bit 0 (C0)	
	CH 4 LO (12L)			FIRSTPORTC Bit 1 (C1)	
	Analog common (A▾)			FIRSTPORTC Bit 2 (C2)	
	CH 5 HI (5H)			FIRSTPORTC Bit 3 (C3)	
	CH 5 LO (13L)			FIRSTPORTC Bit 4 (C4)	
	Analog common (A▾)			FIRSTPORTC Bit 5 (C5)	
	CH 6 HI (6H)			FIRSTPORTC Bit 6 (C6)	
	CH 6 LO (14L)			FIRSTPORTC Bit 7 (C7)	
	Analog common (A▾)			Digital common (D▾)	
	CH 7 HI (7H)			Counter 2 (CT2)	
	CH 7 LO (15L)			Counter 3 (CT3)	

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