

USB-1208HS-2AO

Specifications



**MEASUREMENT
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Specifications

All specifications are subject to change without notice.

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

Parameter	Conditions	Specification
A/D converter		Analog Devices AD7329 - 13-bit successive approximation type
Input ranges	Software-selectable per channel	<ul style="list-style-type: none"> ▪ Differential: ± 20 V, ± 10 V, ± 5 V (The voltage level on each individual AIN input is limited to ± 14 V.) ▪ SE: ± 10 V, ± 5 V, ± 2.5 V, 0 – 10 V
Number of channels		4 differential/8 single-ended, software selectable
Input configuration		Multiplexed
Channel gain queue	8 unique consecutive elements	Software configurable range for each channel
<i>Absolute maximum input voltage</i>	<i>CHx IN to GND.</i>	± 25 V <i>maximum (power on)</i> ± 12 V <i>maximum (power off)</i>
Input impedance		35 M Ω minimum.
Input bandwidth (-3 db)	All input ranges	2 MHz typical
Input leakage current		± 250 nA typical
Input capacitance		32 pF typical
Offset error drift		5 ppm/ $^{\circ}$ C typical
Gain error drift		25 ppm/ $^{\circ}$ C typical.
Maximum working voltage (signal + common mode)	± 20 V	± 14 V
	± 10 V	± 11 V
	± 5 V	± 5.5 V
Sampling rate		1 S/s to 1 MS/s, software programmable
Sample clock source		Internal A/D clock or AICKI
Burst mode		Software selectable, burst rate = 1 μ s
Throughput	Software paced	33 to 4000 S/s typical, system dependent
	Scan to PC memory	1 MS/s maximum
Resolution		13 bits
<i>A/D no missing codes (uncalibrated)</i>	<i>Differential Mode</i>	<i>13 bits</i>
	<i>Single-ended Mode</i>	<i>12 bits</i>
<i>CMRR</i>	<i>60 Hz</i>	<i>74 dB typical</i>
<i>Crosstalk</i>	<i>Single-ended mode, All ranges, 250 kHz input signal</i>	<i>-62 dB typical</i>
	<i>Differential mode, all ranges, 250 kHz input signal</i>	<i>-78 dB typical</i>

Table 2. Calibrated absolute accuracy

Range	Accuracy (mV)
±20 V (differential mode)	±9.55 typical, ±13.18 maximum
±10 V (differential mode)	±4.59 typical, ±6.23 maximum
±5 V (differential mode)	±2.25 typical, ±2.75 maximum
±10 V (single-ended mode)	±5.10 typical, ±8.06 maximum
±5 V (single-ended mode)	±2.63 typical, ±4.03 maximum
±2.5 V (single-ended mode)	±1.59 typical, ±2.70 maximum
0 – 10 V (single-ended mode)	±3.29 typical, ±5.13 maximum

Table 3 summarizes the noise performance for the USB-1208HS-2AO. Noise distribution is determined by gathering 50 kS with inputs tied to ground at the user connector. Samples are gathered at the maximum specified sampling rate of 1 MS/s.

Table 3. Noise performance

Range	Typical counts	LSBrms
±20 V (differential mode)	3	0.45
±10 V (differential mode)	3	0.45
±5 V (differential mode)	3	0.45
±10 V (single-ended mode)	5	0.91
±5 V (single-ended mode)	5	0.91
±2.5 V (single-ended mode)	5	0.91
0 – 10 V (single-ended mode)	5	0.91

Table 4. Input settling time in μ s, typical

Condition	Range	±1 LSB	±4 LSB	±8 LSB
+ full-scale to – full-scale channel switch, same range to same range	±10 V	1.5	1.1	1.0
	±5 V	2.1	1.1	1.0
	±2.5 V	2.2	1.1	1.0
	0-10 V	2.6	1.1	1.0

Analog output

Table 5. Analog output specifications

Parameter	Conditions	Specifications
D/A converter		Texas Instruments DAC7553
Number of channels		2 independent
Resolution		12 bits
Output range	Calibrated	±10 V
	Uncalibrated	±10.2 V
Output transient	Host PC is reset, powered on, suspended, or a reset command is issued to device.	Duration: 3 ms typical Amplitude: 6 V p-p typical
D/A update rate	Software paced	33 to 5000 S/s typical, system dependent
	Hardware paced	1 MHz maximum (per channel)
Sample clock source		Internal D/A clock or AOCKI
Monotonicity		12 bits
Output current		±3 mA maximum per channel
Output short-circuit protection	Output connect to GND	Unlimited duration (10 mA typical)

Output coupling		DC
Power up and reset state		0 V
Output noise		0.53 mV rms
Settling time (to 0.05%)	20 V output step, ($R_L=5\text{ k}\Omega$, $C_L=200\text{ pf}$)	5 μs maximum.
Absolute accuracy		$\pm 0.1\%$
Slew rate		6.7 V/ μs typical
Offset error drift		10 ppm/ $^{\circ}\text{C}$ typical
Gain error drift		65 ppm/ $^{\circ}\text{C}$ typical

Digital input/output

Table 6. Digital I/O specifications

Digital type	CMOS
Number of I/O	16
Configuration	Each bit may be configured as input (power on default) or output
Pull-up configuration	The port has 47 k Ω resistors configurable as pull-ups or pull-downs via internal jumper (default setting is pull-down.)
Digital I/O transfer rate (system-paced)	33 to 8000 port reads/writes or single bit reads/writes per second typical, system dependent.
Input high voltage	2.0 V minimum 5.5 V absolute maximum
Input low voltage	0.8 V maximum -0.5 V absolute minimum 0 V recommended minimum
Output high voltage	4.4 V minimum ($\text{IOH} = -50\text{ }\mu\text{A}$) 3.76 V minimum ($\text{IOH} = -24\text{ mA}$)
Output low voltage	0.1 V maximum ($\text{IOL} = 50\text{ }\mu\text{A}$) 0.44 V maximum ($\text{IOL} = 24\text{ mA}$)
Output current	$\pm 24\text{ mA}$ maximum per terminal (see " Power " section for additional information)

External trigger

Table 7. External trigger specifications

Parameter	Specification
Trigger source	TRIG input
Trigger mode	Software configurable for edge or level sensitive, rising or falling edge, high or low level. Power on default is edge sensitive, rising edge.
Trigger latency	1 μs + 1 clock cycle maximum
Trigger pulse width	100 ns minimum
Input type	Schmitt Trigger, 33 Ω series resistor and 47 K Ω pull-down to ground
Schmitt trigger hysteresis	0.4 V to 1.2 V
Input high voltage	2.2 V minimum 5.5 V absolute maximum
Input low voltage	1.5 V maximum -0.5 V absolute minimum 0 V recommended minimum

External clock input/output

Table 8. External clock I/O specifications

Parameter	Specification
Terminal names	AICKI, AICKO, AOCKI, AOCKO
Terminal type	AxCKI: Input, active on rising edge AxCKO: Output, power on default is 0 V, active on rising edge
Terminal descriptions	AxCKI: Receives sampling clock from external source AxCKO: Outputs internal sampling clock (D/A or A/D clock) or pulse generated from AxCKI when in external clock mode
Input clock rate	1 MHz maximum.
Clock pulse width	AxCKI: 400 ns minimum AxCKO: 400 ns minimum
Input type	Schmitt trigger, 33 Ω series resistor, 47 k Ω pull-down to ground
Schmitt trigger hysteresis	0.4 V to 1.2 V
Input high voltage	2.2 V minimum 5.5 V absolute maximum
Input low voltage	1.5 V maximum -0.5 V absolute minimum 0 V recommended minimum
Output high voltage	4.4 V minimum (IOH = -50 μ A) 3.76 V minimum (IOH = -24 mA)
Output low voltage	0.1 V maximum (IOL = 50 μ A) 0.44 V maximum (IOL = 24 mA)
Output current	\pm 24 mA maximum per terminal (see " Power " section for additional information)

Counters

Table 9. Counter specifications

Counter terminal names	CTR0, CTR1
Counter type	Event counter
Number of channels	2
Input type	Schmitt trigger, 33 Ω series resistor, 47 k Ω pull-down to ground
Schmitt trigger hysteresis	0.4 V to 1.2 V
Input high voltage	2.2 V minimum 5.5 V absolute maximum
Input low voltage	1.5 V maximum -0.5 V absolute minimum 0 V recommended minimum
Resolution	32 bits
Maximum input frequency	20 MHz
Counter read/write rates (software paced)	33 to 8000 reads/writes per second typical, system dependent
High pulse width	25 ns minimum
Low pulse width	25 ns minimum

Timer

Table 10. Timer specifications

Timer terminal name	TMR
Timer type	PWM output with count, period, delay, and pulse width registers
Output value	Default state is idle low with pulses high, software selectable output invert
Internal clock frequency	40 MHz
Register widths	32 bits
High pulse width	20 ns minimum
Low pulse width	20 ns minimum
Output high voltage	4.4 V minimum (IOH = -50 μ A) 3.76 V minimum (IOH = -24 mA)
Output low voltage	0.1 V maximum (IOL = 50 μ A) 0.44 V maximum (IOL = 24 mA)
Output current	\pm 24 mA maximum per pin (see " Power " section for additional information)

Memory

Table 11. Memory specifications

Data FIFO	4 kS analog input/4 kS analog output
Non-volatile memory	32 KB (16 KB firmware storage, 16 KB calibration/user data)

Power

Table 12. Power specifications

Parameter	Conditions	Specification
Operating modes		Bus-powered, USB 5 V supply
Supply current (see Note 1)	Suspend mode	<2.5 mA
	Enumeration	<100 mA
	Run mode	<500 mA
Power consumption excluding analog and digital outputs	Run mode	1.125 W maximum (225 mA input current)
Power available for +5 V, AICKO, AOCKO, TMR, analog outputs, digital I/O	Run mode	1.375 W maximum The total power consumption for all external loads must be less than this value and each load must meet the individual specification for the terminal.
Digital output power calculation		Power per output = $I_{out} * 5 \text{ V}$ (for example, @ 24mA, $P = 0.024 * 5 = 120 \text{ mW/ output}$)
Analog output power calculation		Power per output = $(I_{out} * 16.5 \text{ V}) / 0.78$ (for example, @ 3mA, $P = (0.003 * 16.5) / 0.80 = 63.5 \text{ mW/ output}$)
+5 V output power calculation		Power (W) = $I_{out} * 5 \text{ V}$
+5 V output voltage range (see Note 2)	Run mode	4.5 V minimum, 5.25 V maximum
	Suspend mode, enumeration	0 V
+5 V output current	Run mode, no other output loads	275 mA maximum (1.375 W).
Fuses	On USB supply	0452.750 - Littelfuse 0.750A NANO2® Slo-Bl® Subminiature Surface Mount Fuse. Spare fuse mounted in holder on PCB.

Note 1: This is the total current consumption for the USB-1208HS-2AO including +5 V, digital output and analog output currents.

Note 2: Output voltage range assumes input power is within specified limits.

USB specifications

Table 13. USB specifications

USB device type	USB 2.0 (high-speed)
USB device compatibility	USB 1.1, 2.0
USB cable length	5 meters maximum.
USB cable type	A-B cable, UL type AWM 2527 or equivalent (minimum 24 AWG VBUS/GND, minimum 28 AWG D+/D-).

Environmental

Table 14. Environmental specifications

Operating temperature range	0 to 50 °C
Storage temperature range	-40 to 85 °C
Humidity	0 to 90% non-condensing

Mechanical

Table 15. Mechanical specifications

Dimensions	127 mm (L) x 88.9 mm (W) x 35.56 (H)
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Main connector and pin out

Table 16. Main connector specifications

Connector type	Screw terminal
Wire gauge range	16 AWG to 30 AWG

Table 17. Main connector single-ended pin out

Pin	Signal name	Pin	Signal name
1	AIN0	29	AOUT0
2	AGND	30	AOUT1
3	AIN1	31	AGND
4	AGND	32	NC
5	AIN2	33	NC
6	AGND	34	AGND
7	AIN3	35	AICKI
8	AGND	36	AICKO
9	AIN4	37	AOCKI
10	AGND	38	AOCKO
11	AIN5	39	TRIG
12	AGND	40	GND
13	AIN6	41	CTR0
14	AGND	42	CTR1
15	AIN7	43	TMR
16	AGND	44	GND
17	empty	45	empty
18	+5V	46	+5V
19	GND	47	GND
20	DIO0	48	DIO8
21	DIO1	49	DIO9
22	DIO2	50	DIO10
23	DIO3	51	DIO11
24	DIO4	52	DIO12
25	DIO5	53	DIO13
26	DIO6	54	DIO14
27	DIO7	55	DIO15
28	GND	56	GND

Table 18. Main connector differential pin out

Pin	Signal name	Pin	Signal name
1	AIN0 +	29	AOUT0
2	AGND	30	AOUT1
3	AIN0 -	31	AGND
4	AGND	32	NC
5	AIN1 +	33	NC
6	AGND	34	AGND
7	AIN1 -	35	AICKI
8	AGND	36	AICKO
9	AIN2 +	37	AOCKI
10	AGND	38	AOCKO
11	AIN2 -	39	TRIG
12	AGND	40	GND
13	AIN3 +	41	CTR0
14	AGND	42	CTR1
15	AIN3 -	43	TMR
16	AGND	44	GND
17	empty	45	empty
18	+5V	46	+5V
19	GND	47	GND
20	DIO0	48	DIO8
21	DIO1	49	DIO9
22	DIO2	50	DIO10
23	DIO3	51	DIO11
24	DIO4	52	DIO12
25	DIO5	53	DIO13
26	DIO6	54	DIO14
27	DIO7	55	DIO15
28	GND	56	GND

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