PCI-CTR10

Specifications

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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Counters

Refer to CTS9513-2 data sheet for complete 9513 specifications and operating modes. The SAVE command for the CTS9513 device does not behave predictably when using clocks which are not synchronous with the logic timing. If the SAVE command must be used, we strongly recommend that the 3.3 MHz clock derived from the 33 MHz PCI clock be selected as the clock source. The CTS9513-2 data sheet is available on our web site at www.mccdaq.com/PDFmanuals/9513A.pdf.

Table 1. Counter specifications

Parameter	Conditions
Counter type	CTS9513
Configuration	Two 9513 devices. Five up/down counters per 9513, 16-bits each.
Compatibility	5V/TTL
Each 9513 device is programmable for:	
Clock source	Software selectable: External: ▪ Counter 1-5 clock inputs ▪ Counter 1-5 gate inputs Internal: ▪ Terminal count of previous counter ▪ X2 clock frequency scaler
Gate	Software selectable source: External: ▪ Active high or low level or edge, counter 1 – 5 gate input ▪ Active high level previous gate or next gate ▪ All external gate signals (CTRnGATE) individually pulled up through 10K resistors to +5V. Internal: ▪ Active high previous counter terminal count ▪ No gating.
Output	Software selectable: ▪ Always low ▪ High pulse on terminal count ▪ Low pulse on terminal count ▪ Toggle on terminal count ▪ Inactive, high impedance at user connector counter # output.
Osc Out	Software selectable source: ▪ Counter # input ▪ Gate # input ▪ Prescaled clock source (X2 clock frequency scaler) Software selectable divider: ▪ Division by 1-16 Software selectable enable: ▪ On or low impedance to ground.
Clock input frequency	6.8 MHz max (145 nS min period)
X2 clock input sources	Software selectable: ▪ 1.0 MHz (10 MHz Xtal divided by 10) ▪ 5.0 MHz (10 MHz Xtal divided by 2) ▪ 3.3 MHz (33 MHz PCI clock divided by 10)

Parameter	Conditions
X2 clock frequency scaler	BCD scaling (X2 divided by 10, 100, 1000 or 10000) or Binary scaling (X2 divided by 16, 256, 4096 or 65536)
High pulse width (clock input)	*70 ns min*
Low pulse width (clock input)	*70 ns min*
Gate width high	*145 ns min*
Gate width low	*145 ns min*
Input low voltage	*-0.5 V min, 0.8 V max*
Input high voltage	*2.2 V min, Vcc max*
Output low voltage @ IIl = 3.2 mA	*0.4 V max*
Output high voltage @ IIH = -200 µA	*2.4 V min*
Crystal oscillator frequency	10 MHz
Frequency accuracy	50 ppm
Data transfer	Programmed I/O, interrupt
Power-up / reset state	CTRnOUT_x: low impedance OSCOUT_x: enabled

Digital input / output

Table 2. Digital I/O specifications

Digital type	Discrete, 5V/TTL compatible
	Output:74ACT273
	Input: 74LS373
Number of I/O	8 input, 8 output per 37-pin D connector
Configuration, per connector	1 bank of 8 as output, 1 bank of 8 as strobed input
Input high voltage	*2.0 V min, 7.0 V absolute max*
Input low voltage	*0.8 V max, –0.5 V absolute min*
Output high voltage	*3.94 volts min @ -24 mA (Vcc = 4.5 V)*
Output low voltage	*0.36 volts max @ 24 mA (Vcc = 4.5 V)*
Data transfer	Programmed I/O
Power-up / reset state	Digital outputs power on and Reset to TTL low
Din Strobe	Active low latch enable input, internally pulled high through 10 Kohm resistor
Din Strobe pulse width high/low	15 nS min
Data setup to Din Strobe	*5 nS min*
Data hold from Din Strobe	*20 nS min*

Interrupts

Table 3. Interrupt specifications

Number of user interrupts	Two
PCI interrupt	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enables	External: IRQ_A ENABLE, IRQ_B ENABLE, active low, disabled by default through internal resistor to TTL high) and programmable through PCI9052-1: 0 = disabled 1 = enabled (default)
Interrupt sources	External: IRQ_A IN, IRQ_B IN, polarity programmable through PCI9052-1: 1 = active high 0 = active low (default)
	IRQ_A IN maps to PLX 9052 LINT1
	IRQ_B IN maps to PLX 9052 LINT2

Power consumption

Table 4. Power consumption specifications

+5V	550 mA typical, 800 mA max. Does not include power consumed through the I/O connector.
+5V available at each I/O connector	1A max, protected with a resettable fuse
Resettable fuse	Raychem type *miniSMDC110*. ▪ Hold Current: 1.1 A max ▪ Series resistance 0.21 Ohms max.

Environmental

Table 5. Environmental specifications

Operating Temperature Range	0 to 55°C
Storage Temperature Range	-20 to 70°C
Humidity	0 to 90% non-condensing

Mechanical

Table 6. Mechanical specifications

Card dimensions	PCI half card: 174.4 mm(L) x 106.7 mm(W) x11.65 mm(H)
Form factor	PCI 5V keying. Compatible with 5V, 32-bit. 33 MHz back planes

Main connector and pin out

The P1 connector is compatible with the CIO-CTR05 and the PCI-CTR05. Both P1 and P2 are compatible with the CIO-CTR10.

Table 7. Main connector specifications

Connector types	P1: 37-pin shielded D-type, right angle. P2: 37-pin unshielded D-type, straight.
Compatible Cables	C37FF-x, unshielded ribbon cable.
	C37FFS-x, shielded round cable
Compatible accessory products	BP37/P (Note 1) CIO-MINI37 CIO-MINI37-VERT CIO-TERMINAL SCB-37

Note 1: BP37/P is required in order to cable all CTR B signals from P2 to the PC bulkhead.

Table 8. P1 pin out (Counter A)

Pin	Signal Name
1	IRQ_A INPUT
2	IRQ_A ENABLE
3	DOUT7_A
4	DOUT6_A
5	DOUT5_A
6	DOUT4_A
7	DOUT3_A
8	DOUT2_A
9	DOUT1_A
10	DOUT0_A
11	GND
12	CTR5GATE_A
13	CTR5CLK_A
14	CTR4GATE_A
15	CTR4CLK_A
16	CTR3GATE_A
17	CTR3CLK_A
18	CTR2GATE_A
19	CTR2CLK_A
20	PC +5V
21	DIN STROBE_A
22	DIN7_A
23	DIN6_A
24	DIN5_A
25	DIN4_A
26	DIN3_A
27	DIN2_A
28	DIN1_A
29	DIN0_A
30	OSC OUT_A
31	CTR5OUT_A
32	CTR4OUT_A
33	CTR3OUT_A
34	CTR2OUT_A
35	CTR1OUT_A
36	CTR1CLK_A
37	CTR1GATE_A

Table 9. P2 pin out (Counter B)

Pin	Signal Name
1	IRQ_B INPUT
2	IRQ_B ENABLE
3	DOUT7_B
4	DOUT6_B
5	DOUT5_B
6	DOUT4_B
7	DOUT3_B
8	DOUT2_B
9	DOUT1_B
10	DOUT0_B
11	GND
12	CTR5GATE_B
13	CTR5CLK_B
14	CTR4GATE_B
15	CTR4CLK_B
16	CTR3GATE_B
17	CTR3CLK_B
18	CTR2GATE_B
19	CTR2CLK_B
20	PC +5V
21	DIN STROBE_B
22	DIN7_B
23	DIN6_B
24	DIN5_B
25	DIN4_B
26	DIN3_B
27	DIN2_B
28	DIN1_B
29	DIN0_B
30	OSC OUT_B
31	CTR5OUT_B
32	CTR4OUT_B
33	CTR3OUT_B
34	CTR2OUT_B
35	CTR1OUT_B
36	CTR1CLK_B
37	CTR1GATE_B

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