SPECIFICATIONS

CIO-DASJR/16
Analog Input & Digital I/O

Revision 4, May, 2001

Power consumption

+5V quiescent	850 mA typical, 1250 mA max

Analog input section

A/D converter type	AD7805PB
Resolution	16 bits
Number of channels	8 differential or 16 single-ended (switch-selectable)
Input ranges	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V, fully programmable
Polarity	Unipolar/Bipolar programmable, 11 ms max switching delay
A/D pacing	Programmable: internal counter or external source (DIG. IN 0 / TRIGGER, rising edge) or software polled
A/D Trigger sources	External polled gate trigger (DIG. IN 0 / TRIGGER, active high)
A/D Triggering Modes	
Digital:	Gated pacer, software polled. (Gate must be disabled by software after trigger event.)
Data transfer	DMA, interrupt or software polled
DMA Channels	1 and 3, switch-selectable
DMA enable	Programmable
A/D conversion time	10 µs
Throughput	100 kHz typical, PC dependent
Absolute accuracy	0.0023% of reading ±1.5 LSB
Differential Linearity error	+1.5/-1 LSB
Integral Linearity error	±1.5 LSB
No missing codes (guaranteed)	16 Bits
Gain drift (A/D specs)	±10 ppm/°C
Zero drift (A/D specs)	±5 ppm/°C
Common Mode Range	±10V
CMRR @ 60 Hz	–96 dB
Input leakage current (@ 25 deg C)	200 nA
Input impedance	30 MegΩ
Absolute maximum input voltage	±35V

Digital I/O Section

Digital type	
Output	74LS197
Input	74LS244
Configuration	4 fixed input, 4 fixed output
Number of channels	8
Output High	2.7 volts min @ –0.4 mA
Output Low	0.5 volts max @ 8 mA
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, –0.5 volts absolute min
Interrupts	Programmable: levels 2 thru 7
Interrupt enable	Programmable
Interrupt sources	A/D End-of-conversion, DMA terminal count

Counter Section

Counter type	82C54
Configuration	3 down counters, 16 bits each

Counter 0 - independent, available to user

Source:	programmable: external (CTR0 Clock In) or 100 kHz internal
Gate:	programmable: external (Dig In 2 / Ctr 0 Gate, active high) or disabled
Output:	Available at user connector (CTR 0 Out)

Counter 1 - ADC Pacer Lower Divider

Source:	10 MHz internal
Gate:	Tied to Counter 2 gate, programmable source: internal or external (DIG. IN 0 / TRIGGER).
Output:	Chained to Counter 2 Clock.

Counter 2 - ADC Pacer Upper Divider

Source:	Counter 1 Output.
Gate:	Tied to Counter 1 gate, programmable source: internal or external (DIG. IN 0 / TRIGGER).
Output:	ADC Pacer clock, available at user connector (CTR 2 Out)

Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Crystal oscillator

Frequency	10 MHz
Frequency accuracy	100 ppm

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	–20 to 70°C
Humidity	0 to 90% non-condensing

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