

# CIO-DAS801

## Specifications



**MEASUREMENT  
COMPUTING™**

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# Specifications

All specifications are subject to change without notice.

Typical for 25°C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

## Analog input

Table 1. Analog input specifications

Parameter	Specification
<i>A/D converter type</i>	<i>AD674A, successive approximation</i>
Resolution	12-bits
Number of channels	8
Input ranges	$\pm 10\text{ V}$ , $\pm 5\text{ V}$ , $\pm 1\text{ V}$ , $\pm 0.5\text{ V}$ , $\pm 0.1\text{ V}$ , $\pm 0.05\text{ V}$ , $\pm 0.01\text{ V}$ , $\pm 0.005\text{ V}$ , 0 to 10 V, 0 to 1 V, 0 to 0.1 V, 0 to 0.01 V, fully programmable
Polarity	Unipolar/Bipolar programmable
A/D pacing	Programmable: internal counter or external source (IR Input / XCLK, falling edge) or software polled
A/D trigger sources	External hardware (DIN1 / Trig, rising edge)
Data transfer	Interrupt or software polled from 256 sample FIFO buffer
Channel configuration	Differential (or pseudo-differential with installation of a SIP resistor) or single-ended, switch selectable for each channel
DMA	None
<i>A/D conversion time</i>	<i>20 <math>\mu\text{s}</math></i>
Throughput	50 kHz
Accuracy	$\pm 0.01\%$ of full scale $\pm 1\text{ LSB}$ typ, $\pm 0.05\%$ of full scale $\pm 1\text{ LSB}$ max
Differential linearity error	$\pm 0.5\text{ LSB}$ max
Integral linearity error	$\pm 1\text{ LSB}$
<i>No missing codes (guaranteed)</i>	<i>12-bits</i>
Gain drift (A/D specs)	$\pm 50\text{ ppm}/^\circ\text{C}$
Zero drift (A/D specs)	$\pm 10\text{ ppm}/^\circ\text{C}$
Common mode range	$\pm 10\text{ V}$
CMRR @ 60 Hz	Gain = 1      70 dB min Gain = 10     90 dB min Gain $\geq 100$ 100 dB min
<i>Input leakage current (@ 25 °C)</i>	<i><math>\pm 30\text{ nA}</math></i>
<i>Input leakage current (over temperature)</i>	<i><math>\pm 250\text{ nA}</math></i>
<i>Input impedance</i>	<i><math>&gt;1\text{ Gohm}</math> typical</i>
<i>Absolute maximum input voltage</i>	<i><math>\pm 35\text{ V}</math></i>
Noise distribution (results presented as Average % $\pm 2$ bins, Average % $\pm 1$ bin, Average # bins):	
Bipolar	10 V, 5 V, 1 V    100% / 100% / 3 bins 0.5 V, 0.1 V    100% / 99.3% / 4 bins 0.05 V           100% / 99.1% / 5 bins 0.01 V           95.2% / 79.8% / 11 bins 0.005 V          72% / 48.3% / 21 bins
Unipolar	10 V              100% / 99.96% / 4 bins 1 V                100% / 99.59% / 4 bins 0.1 V             99.95% / 98.73% / 6 bins 0.01 V            72.8% / 49% / 24 bins

## Digital input/output

Table 2. Digital I/O specifications

Digital type	FPGA
Configuration	Two ports, 3 input and 4 output
Input low voltage	0.8 V max
Input high voltage	2.0 V min
Output low voltage (IOL = 4 mA)	0.32 V max
Output high voltage (IOH = -4 mA)	3.86 V min
Absolute maximum input voltage	-0.5 V, +5.5 V
Interrupts	Jumper selectable: levels 2, 3, 4, 5, 6, 7 or not connected Positive edge triggered
Interrupt enable	Programmable
Interrupt sources	External (IR Input / XCLK), A/D End-of-conversion, A/D FIFO-half-full

## Counters

Table 3. Counter specifications

Counter type	82C54
Configuration	3 down counters, 16-bits resolution
Counter 0 — Independent, user counter	Source: External, user connector (CTR0 In) Gate: External, user connector (CTR0 Gate) Output: User connector (CTR0 Out)
Counter 1 — ADC Pacer Lower Divider or independent user counter	Source: User connector (CTR1 In) and optionally CTR2 Out, selectable by software Gate: Programmable, disabled or user connector (CTR1 Gate) Output: User connector (CTR1 Out) and optionally to A/D start convert, software selectable
Counter 2 — ADC Pacer Upper Divider	Source: Internal 1 MHz oscillator Gate: Programmable, disabled or user connector (CTR2 Gate) Output: User connector (CTR2 Out) and optionally to CTR1 In, software selectable
Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8 V max
Input high voltage	2.0 V min
Output low voltage	0.4 V max
Output high voltage	3.0 V min
Crystal oscillator	Frequency: 10 MHz Frequency accuracy: 100 ppm

## Power consumption

Table 4. Power consumption specifications

+5 V quiescent	500 mA typical, 750 mA max
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## Environmental

Table 5. Environmental specifications

Operating temperature range	0 to 50 °C
Storage temperature range	-20 to 70 °C
Humidity	0 to 90% non-condensing

## Main connector and pin out

Table 6. Main connector specifications

Connector type	37-pin D type connector
Compatible cable	C37FF-x
Compatible accessory products with the C37FF-x cable	CIO-MINI37 CIO-EXP16 CIO-EXP32 CIO-TERMINAL ISO-RACK08

Table 7. Connector pin out

Pin	Signal Name	Pin	Signal Name
1	+15V from DC/DC	20	-15V from DC/DC
2	CTR0 In	21	CTR0 Gate
3	CTR0 Out	22	CTR1 Gate
4	CTR1 In	23	CTR2 Gate
5	CTR1 Out	24	IR Input / XCLK
6	CTR2 Out	25	DIN1 / Trig
7	DOU1	26	DIN2
8	DOU2	27	DIN3
9	DOU3	28	DGND
10	DOU4	29	PC +5V
11	LLGND	30	CH7 HI
12	CH7 LO	31	CH6 HI
13	CH6 LO	32	CH5 HI
14	CH5 LO	33	CH4 HI
15	CH4 LO	34	CH3 HI
16	CH3 LO	35	CH2 HI
17	CH2 LO	36	CH1 HI
18	CH1 LO	37	CH0 HI
19	CH0 LO		

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