CIO-DAS16/Jr

Specifications

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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic* text are guaranteed by design.

Analog input

Table 1. Analog input specifications

Parameter	Specification
A/D converter type	*AD7800*
Resolution	12 bits
Number of channels	8 differential or 16 single-ended, switch selectable
Input ranges	±10 V, ±5 V, ±2.5 V, ±1.25 V, ±0.625 V, 0 to 10 V, 0 to 5 V, 0 to 2.5 V, 0 to 1.25 V, 0 to 0.625 V, fully programmable
Polarity	Unipolar/Bipolar, software selectable
A/D pacing	Programmable: ▪ internal counter or external source (DIG. IN 0 / TRIGGER, rising edge), or ▪ software polled
A/D trigger sources	External polled gate trigger (DIG. IN 0 / TRIGGER, active high)
A/D triggering modes	Digital: Gated pacer, software polled. (Gate must be disabled by software after trigger event.)
Data transfer	Interrupt, DMA or software polled
DMA	Channel 1 or 3
A/D conversion time	*3 µs*
Throughput	120 kHz typical, PC dependant
Absolute accuracy	0.01% of reading ±1 LSB
Differential linearity error	±1 LSB
Integral linearity error	±1 LSB
Differential linearity error	±1 LSB
No missing codes guaranteed	*12-bits*
Gain drift (A/D specs)	*±25 ppm/°C*
Zero drift (A/D specs)	*±10ppm/°C*
Common mode range	±10 V
CMRR @ 60 Hz	-72 dB
Input leakage current (@ 25 °C)	*200 nA*
Input impedance	*10 Meg Ohms min*
Absolute maximum input voltage	*±35 V*

Table 2. Noise distribution (Rate = 1-100 kHz)

Range	Average % ±2 bins	Average % ±1 bin	Average # bins
Bipolar (10 V)	98%	86%	8 bins
Bipolar (5 V)	97%	86%	9 bins
Bipolar (2.5 V)	97%	82%	8 bins
Bipolar (1.25 V)	95%	73%	9 bins
Unipolar (10 V)	95%	79%	9 bins
Unipolar (5 V)	96%	80%	9 bins
Unipolar (2.5 V)	92%	70%	10 bins
Unipolar (1.25 V)	89%	68%	11 bins

Digital input/output

Table 3. Digital input/output specifications

Digital type	FPGA
Configuration	4 bits as input , 4 bits as output
Number of channels	4 input, 4 output
Input low voltage	0.8 V max
Input high voltage	2.0 V min
Output low voltage (IOL = 4 mA)	0.32 V max
Output high voltage (IOH = -4 mA)	3.86 V min
Absolute maximum input voltage	-0.5V, +5.5V
Interrupts	2 through 7, programmable
Interrupt enable	Programmable
Interrupt sources	A/D End-of-conversion, DMA terminal count

Counters

Table 4. Counter specifications

Counter type	82C54	
Configuration	82C54 device. 3 down counters, 16-bits each	
Counter 0 — Independent, available to user	Source:	100 kHz on board clock or external (CTR 0 Clock In)
	Gate:	External (CTR 0 Gate)
	Output:	Available at the user connector (CTR 0 Out)
Counter 1 — ADC Pacer Lower Divider	Source:	1 or 10 MHz oscillator, jumper-selectable
	Gate:	Tied to Counter 2 gate, programmable source: internal or external (DIG. IN 0 / TRIGGER)
	Output:	Chained to Counter 2 Clock
Counter 2 — ADC Pacer Upper Divider	Source:	Counter 1 Output.
	Gate:	Tied to Counter 1 gate, programmable source: internal or external (DIG. IN 0 / TRIGGER)
	Output:	ADC Pacer clock, available at user connector (CTR 2 Out)
Clock input frequency	10 MHz max	
High pulse width (clock input)	30 ns min	
Low pulse width (clock input)	50 ns min	
Gate width high	50 ns min	
Gate width low	50 ns min	
Input low voltage	0.8 V max	
Input high voltage	2.0 V min	
Output low voltage	0.4 V max	
Output high voltage	3.0 V min	
Crystal oscillator	▪ Frequency:	10 MHz
	▪ Frequency accuracy:	100 ppm

Power consumption

Table 5. Power consumption specifications

Parameter	**Specification**
+5 V	680 mA typical, 850 mA max

Environmental

Table 6. Environmental specifications

Operating temperature range	0 to 50 ° C
Storage temperature range	-20 to 70 ° C
Humidity	0 to 90% non-condensing

Main connector and pin out

Table 7. Connector specifications

Connector type	37-pin male "D" connector
Compatible cables	C37FF-x C37FFS-x C-EXP2DAS16-10 DFCON-37 (D-connector, D-shell, and termination pins to construct your own cable)
Compatible accessory products with the C37FF-x cable or C37FFS-x cable	CIO-MINI37 CIO-TERMINAL CIO-SSH16 ISO-RACK16
Compatible accessory products with the C-EXP2DAS16-10 cable	CIO-EXP16 CIO-EXP32

Table 8. Connector pin out

Pin	Signal Name	Pin	Signal Name
1	+5V PC Bus	20	CTR2 Out
2	Ctr0 Out	21	CTR0 Clock In
3	Dig. Out 3	22	Dig. Out 2
4	Dig. Out 1	23	Dig. Out 0
5	Dig. In 3	24	Dig. In 2 /CTR0 Gate
6	Dig. In 1	25	Dig. In 0 / TRIGGER
7	GND	26	SS&H Out
8	NC	27	NC
9	NC	28	LLGND
10	NC	29	LLGND
11	CH7 Low / CH15 High	30	CH7 High
12	CH6 Low / CH14 High	31	CH6 High
13	CH5 Low / CH13 High	32	CH5 High
14	CH4 Low / CH12 High	33	CH4 High
15	CH3 Low / CH11 High	34	CH3 High
16	CH2 Low / CH10 High	35	CH2 High
17	CH1 Low / CH9 High	36	CH1 High
18	CH0 Low / CH8 High	37	CH0 High
19	LLGND		

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