## CIO-DAS1602/16

## High Speed 16 Channel 16 Bit Analog Input, 2 Channel 12 Bit Analog Output with 32 Digital I/O \& 3, 16 Bit Counters



## DESCRIPTION

The CIO-DAS1600 multifunction analog and digital I/O board is designed to be compatible with MetraByte's popular DAS-1600 and provide additional features.

Installed in any IBM compatible personal computer the CIO-DAS1600 turns your personal computer into a high speed data acquisition and control station suitable for laboratory data collection, instrumentation, production test, or industrial monitoring.

The CIO-DAS1600 is supported by the Universal Library software to allow programmed control in BASIC, C and PASCAL in DOS or Windows languages and HP VEE graphical programming


## FIFO Buffer = Windows Ready

The FIFO Buffer collects the results of A/D conversions and stores them until the personal computer CPU is able to transfer the data into PC memory. A FIFO buffer allows the PC to store up the A/ D transfer requests, then service the requests in batches. Under Windows, many demanding resources employ block transfers. Your A/D board should work in concert rather than conflict with your high performance PC .


## SIXTEEN BIT RESOLUTION \& COMPATIBLE

The CIO-DAS1602/16 provides a full 16 bits of A/D resolution (1 part in 65,536 ). In addition, it is fully compatible with the CIODAS1602/12 (KM DAS-1602), including burst mode and gain codes. Because it is a natural extension of the DAS-16 family architecture, the CIO-DAS1602/16 is also register compatible with the KM DAS-HRES.

The only difference between a the 12 and 16 bit board is one register; the $\mathrm{A} / \mathrm{D}$ least significant byte. Shown here is the LSB register for both the $1600 / 12$ and $1600 / 16$. The 16 bit board the additional 4 A/D bits in the 4 bits allocated to channel number in a 12

## 12 Bit Board A/D LSB <br> D7 D6 D5 D4 D3 D2 D1 D0 <br> A8 A9 A10 LSb CH3 CH2 CH1 CH0

16 Bit Board A/D LSB
$\begin{array}{llllllll}\text { D7 } & \text { D6 } & \text { D5 } & \text { D4 } & \text { D3 } & \text { D2 } & \text { D1 } & \text { D0 }\end{array}$
A8 A9 A10 A11 A12 A13 A14 LSb bit board.

## A/D SPECIFICATIONS

| Channels | $16 \mathrm{SE} / 8 \mathrm{Differential}$ |
| :--- | :--- |
| A/D Type | Successive Approx. |
| Conversion Time | 10 uS |
| A/D Convert \& Transfer Speed (DMA) | 100 KHz |
| Accuracy | $0.0015 \%+/-1.5 \mathrm{LSB}$ |
| Integral Linearity | $+/-1 \mathrm{LSB}$ |
| No missing codes guaranteed over temp. range. | $+/-35 \mathrm{~V}$ Continuous |
| Maximum Overvoltage | $250 \mathrm{nA} \mathrm{Max} \mathrm{@} 25^{\circ} \mathrm{C}$ |
| Input Leakage Current | $+/-25 \mathrm{ppm} / \mathrm{Deg} \mathrm{C} \mathrm{Max}$ |
| Gain Drift | $+/-10 \mathrm{ppm} / \mathrm{Deg} \mathrm{C} \mathrm{Max}$ |
| Zero Drift |  |

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## CONNECTOR

The analog signals are brought on board by a standard 37 pin D connector directly to two multiplexors. The two multiplexors may be configured as 16 channels of single ended input or 8 channels of differential input. Differential inputs can reject noise and ground loops (common mode voltages).

The signal levels, functions and pin assignments are identical to the DAS16 series of boards so applications may be upgraded to CIO-DAS1600 without changes to connector or cable.

|  |  |  |  |
| :---: | :---: | :---: | :---: |
| LLGND | 19 |  |  |
| сненсн |  | 37 | СНо HIGH |
| CH0 LOW/CH8 HIGH | 18 | 36 | CHI HIGH |
| CHi Low /ch9 нIGH | 17 | 35 | CH2 HIGH |
| CH2 Low /CH10 HIGH | 16 | 34 |  |
| CH3 Low /CHII HIGH | 15 | ${ }^{34}$ | $\mathrm{CH3}^{\text {HIGH }}$ |
|  |  | 33 | CH4 HIGH |
| CH4 LOW /CH12 HIGH | 14 | 32 | CH5 HIGH |
| CHS LOw /CH13 HIGH | 13 | 31 | CH6 HIGH |
| CH6Low /CHI4 HIGH | 12 | 3 |  |
| CH7 Low /chis High | 11 | 30 |  |
| d/A O Refin | 10 | 29 |  |
| d/anout | 9 | 28 | LLGND |
| d/a 1 Ref in | 8 | 27 | D/A 1 OUT |
| da mef in |  | 26 | Ss\&h out |
| GND | 7 | 25 | Dig. In 0 /trigcer |
| DGI. In 1 | 6 | 24 | dig. In $2 /$ CTro Gate |
| DIG. IN 3 | 5 | 23 | dig. outo |
| dig. out 1 | 4 | 22 | dig. out 2 |
| dig. 3 Out | 3 | 21 | CTR oclock in |
| стroout | 2 | 20 | CTR 2 OUT |
| +5VPC bus | 1 |  |  |

## ANALOG OUTPUT

Analog voltage output is provided by two 12 bit multiplying D/A converters. This type of converter accepts a reference voltage and provides an output proportional to that. A precision -5 V and -10 V reference provide on-board D/A ranges of $0-5 \mathrm{~V}, 0-10 \mathrm{~V},+/-5 \mathrm{~V}$, and $+/-10 \mathrm{~V}$.

Other ranges between $+/-10 \mathrm{~V}$ are possible if you supply a $+/-10 \mathrm{~V}$ external reference at pin \#10 or \#26 of the 37 pin D connector.

The D/A converters do have program and interrupt transfer capability. Interrupts may be initiated by the on-board pacer clock or by
 external trigger.

If the DAC 0 reference is supplied on board, the external reference input pin of the 37 pin connector may be converted to a simultaneous sample \& hold output sync pulse by installing the jumper labeled SH.

## D/A SPECIFICATIONS <br> 12 BIT <br> Channels <br> D/A Type <br> Conversion Time <br> Integral Linearity <br> Differential Linearity <br> Reference Range <br> Output Range <br> Jumper selectable ranges <br> R Out <br> I Out <br> 2 <br> Multiplying 4 Quadrant <br> 30 nS to $0.01 \%$ <br> +/- 1 LSB <br> +/- 1 LSB <br> $+/-10 \mathrm{~V}$ <br> +/- 10V, Reference dependent <br> $0-5 \mathrm{~V}, 0-10 \mathrm{~V},+/-5 \mathrm{~V},+/-10 \mathrm{~V}$ <br> 0.1 Ohm Max <br> $+/-5 \mathrm{~mA}$ Min

## MINIMIZING CHANNEL-CHANNEL SKEW (BURST MODE)

A/D converter board design begins with a single $A / D$ converter, the most expensive part on the board. An A/D converter chip has only a single input. In many applications, multiple channels of A/D input are desired and so the board's analog inputs are multiplexed one at a time into the $\mathrm{A} / \mathrm{D}$ chip for conversion.

Channel to channel skew is the result of multiplexing the $A / D$ inputs and is nothing more than the time between consecutive samples. For example, if four channels are sampled at a rate of 1 Khz per channel, the channel skew is $250 \mathrm{uS}(1 \mathrm{mS} / 4)$.

Burst mode minimizes channel to channel skew by clocking the A/ D at the maximum rate between successive channels. For example, at the 1 mS pulse channel 0 is sampled, then channel 1 is sampled 10uS later, then channel $2,10 u S$ after that and channel 3,10 uS after that. Then no samples are taken until the next 1 mS pulse when channel 0 is sampled again. In this scheme the rate for all channels is 1 KHz but the channel to channel skew (delay) is now 10 uS between channels or 30uS total.


## GAIN \& RANGE SELECTION

Gain and range selection on the CIO-DAS1600 is accomplished by a combination of bipolar/unipolar switch and a programmable gain amplifier. The ranges available are:

| BOARD | Prog. Gain <br> CODE | Bipolar <br> RANGE | Unipolar <br> RANGE |
| :--- | :--- | :--- | :--- |
| CIO-DAS1602/16 | 0 | $+/-10 \mathrm{~V}$ | $0-10 \mathrm{~V}$ |
|  | 1 | $+/ 5 \mathrm{~V}$ | $0-5 \mathrm{~V}$ |
|  | 2 | $+/-2.5 \mathrm{~V}$ | $0-2.5 \mathrm{~V}$ |
|  | 3 | +-1.25 V | $0-1.25 \mathrm{~V}$ |

The bipolar/unipolar switch must be set.

TheCIO-DAS1602/16is not made available in a 1601 version because of the gains of 100 and 1000. A 16 bit converter at a gain of 100 resolves each bit to 1.5 uV . At that low level we determined the signal to noise made the measurement meaningless. For those with special range requirements, please call the factory to explore other op-

$\mathrm{BIP}=$ Bipolar $(+/-\mathrm{X})$ Ranges Selected UNI $=$ Unipolar ( $0-X$ ) Ranges Selected
Note: This is opposite from DAS-16 tions or custom range configurations.

