SPECIFICATIONS

CIO-DAS16
CIO-DAS16/F
Analog I/O & Digital I/O

Revision 8, October, 2000

Power consumption

+5V:	780 mA typical, 975 mA max
+12V:	20 mA typical, 25 mA max
–12V:	27 mA typical, 34 mA max

Analog Input Section

A/D converter type	
CIO-DAS16	AD674
CIO-DAS16/F	AD774
Resolution	12 bits
Number of channels	8 differential or 16 single-ended, switch selectable
Input Ranges	±10V, ±5V, ±2.5V, ±1V, ±0.5V, 0 to 10V, 0 to 5V, 0 to 2V, 0 to 1V and user settable through resistor selection
Polarity	Unipolar/Bipolar, switch selectable
A/D pacing	Programmable: internal counter or external source (Dig In 0 / Trigger, rising edge) or software polled
A/D Trigger sources	External polled gate trigger (Dig In 0 / Trigger, active high)
A/D Triggering Modes	
Digital:	Gated pacer, software polled. (Gate must be disabled by software after trigger event.)
Data transfer	Interrupt, DMA or software polled
DMA	Channel 1 or 3, switch selectable
A/D conversion time	
CIO-DAS16	15 µs
CIO-DAS16/F	8.5 µs
Throughput	
CIO-DAS16	50 kHz min
CIO-DAS16/F	100 kHz min
Accuracy	0.01% of reading ±1 LSB
Differential Linearity error	±1 LSB
Integral Linearity error	±1 LSB
No missing codes guaranteed	12 bits
Gain drift (A/D specs)	±25 ppm/°C
Zero drift (A/D specs)	±10µV/°C
Common Mode Range	±10V
CMRR @ 60Hz	72 dB
Input leakage current (@25 Deg C)	25 µA
Input impedance	50 Meg Ohms min
Absolute maximum input voltage	±35V

Analog Output

D/A converter type	MX7548
Resolution	12 bits
Number of channels	2
Output Ranges	0 to 5V using on-board reference, ±10V range using external reference (Vout max = –1 * VRef)
Offset error	Adjustable to 0 with potentiometer
Gain error	Adjustable to 0 with potentiometer
Differential non linearity	±1LSB max
Integral non linearity	±1LSB max
Monotonicity	±0.5 LSB
D/A Gain drift	±5 ppm/°C max
D/A pacing	Software paced
D/A trigger modes	Software
Data transfer	Software
Throughput	System dependent
Settling time (output current to ±½LSB)	1µs max
Slew Rate (OP07)	0.3V/µs
Current Drive	±5 mA
Output short-circuit duration	25 mA indefinite
Output coupling	DC
Output impedance	0.1 Ohms max
Miscellaneous	Double buffered output latches

Digital Input / Output

Digital Type (main connector)	
Output:	74LS374
Input:	74S244
Configuration	4 bits as input, 4 bits as output
Number of channels	8
Output High	2.4 volts min @ –2.6 mA
Output Low	0.5 volts max @ 24 mA
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, –0.5 volts absolute min
Digital Type (Digital I/O connector)	82C55
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output High	3.0 volts min @ –2.5 mA
Output Low	0.4 volts max @ 2.5 mA
Input High	2.0 volts min, 5.5 volts absolute max
Input Low	0.8 volts max, –0.5 volts absolute min

Interrupts	2 - 7, software selectable
Interrupt enable	Programmable
Interrupt sources	A/D End-of-conversion, DMA terminal count

Counter Section

Counter type	82C54
Configuration	82C54 device. 3 down-counters, 16 bits each

Counter 0 - Independent user counter

Source:	Internal 100 kHz or external (CTR 0 Clock In), software selectable
Gate:	External (Dig In 2 / CTR 0 Gate), software enabled
Output:	Available at user connector (CTR 0 Out)

Counter 1 - ADC Pacer Lower Divider

Source:	1 or 10 MHz oscillator, jumper selectable
Gate:	Tied to Counter 2 gate, programmable source: external (Dig In 0 / Trigger) or internal
Output:	Chained to Counter 2 Clock.

Counter 2 - ADC Pacer Upper Divider

Source:	Counter 1 Output.
Gate:	Tied to Counter 1 gate, programmable source (external or internal).
Output:	ADC start convert, available at user connector (CTR 2 Out)

Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	–20 to 70°C
Humidity	0 to 95% non-condensing

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