

SPECIFICATIONS

CIO-DAS16-M1-16

Analog Input & Digital I/O



**MEASUREMENT
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Revision 4, November, 2000

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All Specifications typical for 25 DegC unless otherwise specified.

Analog Input Section

A/D converter type	Datel ADS-30356 Subranging
Resolution	16 bits
Programmable ranges	$\pm 5V$, $\pm 2.5V$, $\pm 1.25V$, $\pm .625V$, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
A/D pacing	Programmable: internal counter or external source (Din0, rising edge) or software-pollled
Burst mode intersample time	1 μs
Data transfer	Word wide from 1k sample FIFO via REP INSW, interrupt, DT Connect or software polled
Polarity	Unipolar/Bipolar software selectable, 10 ms delay switching
Number of channels	8 differential
A/D Trigger sources	External trigger/gate (DIN1)
A/D Triggering Modes	
Digital:	Software configurable for edge (triggered) or level-activated (gated). Programmable polarity (rising/falling edge trigger, high/low gate).
A/D conversion time	1 μs
Throughput	1 MHz max
Differential Linearity error	± 1 LSB max
Integral Linearity error	± 6 LSB max
Offset Error	± 10 LSB max ¹
Common Mode Range	+11V, -6V
CMRR (60Hz, $V_{in} = CMR$)	90 dB
No missing codes guaranteed	16 bits
Gain drift (A/D specs)	± 30 ppm/ $^{\circ}C$, all ranges
Input leakage current (@25 Deg C)	200 nA
Input impedance	Min 10 MegOhms
Absolute maximum input voltage	$\pm 15V$

Digital Input / Output

Digital Type (Main Connector)	
Input:	74LS244
Output:	74LS197
Configuration	Two dedicated ports, 4 input and 4 output
Output High	2.7 volts @ -0.4mA min
Output Low	0.4 volts @ 8 mA min
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min

¹Offset error can be trimmed to zero by adjusting the offset potentiometer for zero offset at the sampling frequency to be used.

Digital Type (Auxiliary Connector)	82C55
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Output High	3.0 volts min @ -2.5mA
Output Low	0.4 volts max @ 2.5mA
Input High	2.0 volts min, 5.5 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min
Interrupts	Programmable levels 2 to 7, 10 to 12, 14, 15; Positive-edge triggered
Interrupt enable	Programmable
Interrupt sources	A/D End-of-conversion, A/D FIFO half full, A/D Residual Counter

Counter section

Counter type	82C54
Configuration	3 down-counters, 16 bits each

Counter 0 - General purpose counter or ADC residual sample counter when using REPINSW.

Source: Programmable: external (CTROIN), internal (1 MHz osc) or ADC pacer (when using REPINSW).

Gate: Programmable source: external (DIN2) or internal (when using REPINSW)

Output: Programmable: user connector, end-of-acquisition interrupt (when using REPINSW).

Counter 1 - ADC Pacer Lower Divider

Source: 10 MHz oscillator

Gate: Tied to Counter 2 gate, programmable source: external (DIN1) or internal.

Output: Chained to Counter 2 Clock.

Counter 2 - ADC Pacer Upper Divider

Source: Counter 1 Output.

Gate: Tied to Counter 1 gate, programmable source: external (DIN1) or internal.

Output: ADC Pacer clock, output available at user connector (CTR2 Out).

Clock input frequency	10 Mhz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental

Operating temperature range	0 to 60°C
Storage temperature range	-40 to 100°C
Humidity	0 to 90% non-condensing

Power consumption

+5V: Operating	2.25 A typical / 2.9 A maximum
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