PCI-DAS64/M1/16
PCI-DAS64/M2/16
PCI-DAS64/M3/16

PCI Bus-Compatible
Analog/Digital
Data Acquisition & Control Board

User's Guide

MEASUREMENT
COMPUTING™

Revision 6, February, 2002

Notice

Measurement Computing Corporation does not authorize any Measurement Computing Corporation product for use in life support systems and/or devices without the written approval of the CEO of Measurement Computing Corporation Life support devices/systems are devices or systems which, a) are intended for surgical implantation into the body, or b) support or sustain life and whose failure to perform can be reasonably expected to result in injury. Measurement Computing Corp. products are not designed with the components required, and are not subject to the testing required to ensure a level of reliability suitable for the treatment and diagnosis of people.

TABLE OF CONTENTS

This page is blank

1 Introduction

The PCI-DAS64/Mx/16 family of analog and digital I/O boards offer a combination of high speed, channel count and resolution on a single PCI-bus data acquisition board. It offers:

- 64 single-ended or 32 differential 16-bit analog inputs
- Sample rates up to 3 MHz single-channel, or up to 1.5 MHz multi-channels
- Two 16-bit analog outputs
- 32 bits of digital I/O
- A 16-bit down-counter.
- A variety of analog and digital trigger modes with software-selectable trigger levels and direction.

The heart of the board is Measurement Computing's powerful System Timing Controller (STC) chip. The STC chip controls all A/D sampling and D/A update rates as well as controlling the 8K A/D FIFO, the 8K gain/channel queue and the 16K D/A FIFO buffer. This functionality is based on the STC chip's use of an on-board 32K x 16 SRAM. The STC chip assigns functions to various parts of the SRAM (e.g. A/D FIFO buffer) and provides full-speed control and arbitration among the various functions using the various sections of the SRAM buffer.

The STC allows simultaneous full speed A/D sampling, D/A updating and gain/channel queue sequencing (with variable inter-sample timing if desired). *The STC chip performs these functions up to 5 MHz, and is available as an OEM component for use in your own designs*. The board provides bus-mastering and scatter-gather functionality to assure the desired system timing is maintained.

The PCI-DAS64/Mx/16 family is completely plug-and-play. There are no switches, jumpers or potentiometers on the board. All board addresses, interrupt channels etc. are set by your computers plug-and-play software. Even calibration is performed via software by using on-board trim D/A converters.

1.1 Analog

The PCI-DAS64/Mx/16 provides 32 fully differential or 64 single-ended analog inputs. The input mode is software selectable, with no switches or jumpers to set. The PCI-DAS64/M3/16 board offers a 3 MHz maximum sample rate, while the /M2/16 and /M1/16 offer 2 MHz and 1 MHz sample rates. The boards offer full speed acquisition in single channel scans, and will perform full accuracy multi-channel scans up to 1.5 MHz depending on the operating mode. An 8 K-sample gain/channel queue is available making long, complex sample sequencing simple. An 8 K-sample FIFO buffer combined with Bus-Master DMA and scatter-gather to assure data taken from the board is transferred into computer memory without the possibility of missed samples.

The table below details the input ranges and resolutions for the available input configurations and gains.

Bipolar		**Unipolar**	
Range	**Resolution**	**Range**	**Resolution**
±5V	153 µV	0 to 5V	76.3 µV
±2.5V	76.3 µV	0 to 2.5V	38.1 µV
±1.25V	38.1 µV	0 to 1.25V	19.1 µV
±0.625V	19.1 µV		

1.1.1 Burst Mode

Channel-to-channel skew is the result of multiplexing the A/D inputs. It is defined as the time between consecutive samples. Burst mode minimizes channel-to-channel skew by clocking the A/D at a high rate between successive samples within a scan, then waiting a specified time before starting a new scan. The PCI-DAS64/Mx/16 provides burst mode with a 667 ns (1 µs on 1M) minimum sample skew/delay.

1.1.2 Analog Outputs

The PCI-DAS64/Mx/16 boards provide two high-speed, ±5V 16-bit analog outputs. The outputs are updated via on-board 16 K FIFO buffer and provide a 100 kHz max. update rate. Repetitive D/A-based waveforms can be stored in on-board memory and generated without requiring ongoing PCI bus transfers. The outputs provide rated accuracy to ±15 mA, are short-circuit-protected (25 mA limit) and are cleared to 0 volts on power-up or reset. The board supports simultaneous full speed operation of both the A/D and D/A.

1.2 Digital I/O

The PCI-DAS64/Mx/16 provides 32 bits of digital I/O. An 82C55 chip provides 24 bits of CMOS compatible I/O at the board's 40-pin auxiliary connector. Four LSTTL-compatible digital inputs and four outputs are provided on the main 100-pin connector. On power up or reset, all I/O ports default to the input state (high impedance).

Counter/Timer I/O

The PCI-DAS64/Mx/16 provides one 16-bit down counter (1/3 of an 82C54). Clock, gate and output connections are available at the user I/O connector.

The PCI-DAS64/Mx/16 can be installed in any PCI-bus compatible personal computer, functioning as a ultra high speed data acquisition and control station.

1.3 Software

All PCI-DAS64/Mx/16 boards come complete with the ***Insta*Cal**™ software package. ***Insta*Cal** is a complete installation, calibration and test program for data acquisition and control boards. Complete with extensive error checking, *Insta*Cal guides you through installation and setup of your data acquisition board and creates the board configuration file for use by your program or application software package. *Insta*Cal is described in detail in the *Software Installation Manual*.

The PCI-DAS64/Mx/16 boards are fully supported by Universal Library. Universal Library is a complete set of I/O libraries and drivers for all of our boards, in all Windows based languages. When using the Universal Library, you can switch boards or even programming languages and the syntax remains constant. For details on Universal Library, please refer to the software section of this handbook.

The PCI-DAS64/Mx/16 boards are fully supported by a wide variety of applications software packages including SoftWIRE®, DAS-Wizard™, (and DAS-Wizard Pro™), HP VEE®, HP VEE Lab and LabVIEW™. For further details on these, as well as a variety of other software packages, please refer to the software section provided in the Measurement Computing Corporation catalog.

This page is blank

2 Installation

The PCI-DAS64/Mx/16 is completely plug and play. There are no switches or jumpers to set. Configuration is controlled by your systems' BIOS. Simply turn off your PC, open it up and insert the PCI-DAS64/Mx/16 into any available PCI slot.

If you are using an operating system with support for Plug and Play (such as Windows 95 or 98), a dialog box will display as the system loads indicating that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you are prompted for a disk containing it. The *Insta*Cal™ software supplied with your board contains this file. Simply insert the disk or CD and click OK.

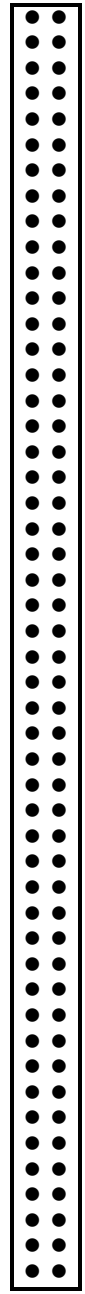
To test your installation, install *Insta*Cal™, the installation, calibration, and test utility supplied with your board. Refer to the *Software Installation Manual* for information on the initial setup, loading, and installation of *Insta*Cal™ and optional Universal Library™ software.

We highly recommend that you allow your computer to warm up for at least 60 minutes before acquiring data with the PCI-DAS64/Mx/16 series boards. The high speed components used on the board generate heat and it takes this amount of time for the board to reach steady state if it has been powered off for a significant amount of time.

We also recommend that you only calibrate the board (using the InstaCal utility) after the board has fully warmed up as well. For best results, calibrate the board immediately before making critical measurements. The high resolution analog components on the board are somewhat sensitive to temperature. This pre-measurement calibration insures that your board is operating at the optimum calibration values.

2.1 I/O Connector

The PCI-DAS64/Mx/16 uses a high-density, 100-pin connector (Figures 2-1 and 2-2). Please make accurate notes and pay close attention to wire connections. See Figure 2-1 for connections when using single-ended inputs. See Figure 2-2 for connections when using differential inputs. See Figure 2-3 for the Auxiliary Digital Connector diagram. Pin outs for all connectors are listed in the Specifications section.



GND	1	● ●	51	GND
CTR 1 Out	2	● ●	52	External Interrupt
CTR 1 Clk	3	● ●	53	A/D External Pacer
CTR 1 Gate	4	● ●	54	A/D Stop Trigger In
DOut 3	5	● ●	55	A/D Start Trigger In
DOut 2	6	● ●	56	Analog Trigger In
DOut 1	7	● ●	57	A/D Pacer Gate
DOut 0	8	● ●	58	A/D Pacer Out
DIn 3	9	● ●	59	SSH Out / DAC PACER OUT
DIn 2	10	● ●	60	EXT. D/A Trigger/Pacer Gate
DIn 1	11	● ●	61	D/A External Pacer
DIn 0	12	● ●	62	PC +5V
GND	13	● ●	63	D/A Out 1
–12V	14	● ●	64	D/A GND 1
GND	15	● ●	65	D/A Out 0
+12V	16	● ●	66	D/A GND 0
CH 63 In	17	● ●	67	CH 31 In
CH 62 In	18	● ●	68	CH 30 In
CH 61 In	19	● ●	69	CH 29 In
CH 60 In	20	● ●	70	CH 28 In
CH 59 In	21	● ●	71	CH 27 In
CH 58 In	22	● ●	72	CH 26 In
CH 57 In	23	● ●	73	CH 25 In
CH 56 In	24	● ●	74	CH 24 In
CH 55 In	25	● ●	75	CH 23 In
CH 54 In	26	● ●	76	CH 22 In
CH 53 In	27	● ●	77	CH 21 In
CH 52 In	28	● ●	78	CH 20 In
CH 51 In	29	● ●	79	CH 19 In
CH 50 In	30	● ●	80	CH 18 In
CH 49 In	31	● ●	81	CH 17 In
CH 48 In	32	● ●	82	CH 16 In
LLGND	33	● ●	83	LLGND
CH 47 In	34	● ●	84	CH 15 In
CH 46 In	35	● ●	85	CH 14 In
CH 45 In	36	● ●	86	CH 13 In
CH 44 In	37	● ●	87	CH 12 In
CH 43 In	38	● ●	88	CH 11 In
CH 42 In	39	● ●	89	CH 10 In
CH 41 In	40	● ●	90	CH 9 In
CH 40 In	41	● ●	91	CH 8 In
CH 39 In	42	● ●	92	CH 7 In
CH 38 In	43	● ●	93	CH 6 In
CH 37 In	44	● ●	94	CH 5 In
CH 36 In	45	● ●	95	CH 4 In
CH 35 In	46	● ●	96	CH 3 In
CH 34 In	47	● ●	97	CH 2 In
CH 33 In	48	● ●	98	CH 1 In
CH 32 In	49	● ●	99	CH 0 In
GND	50	● ●	100	LLGND

Figure 2-1. PCI-DAS64/Mx/16 100-pin Connector – Single-Ended Inputs Configuration

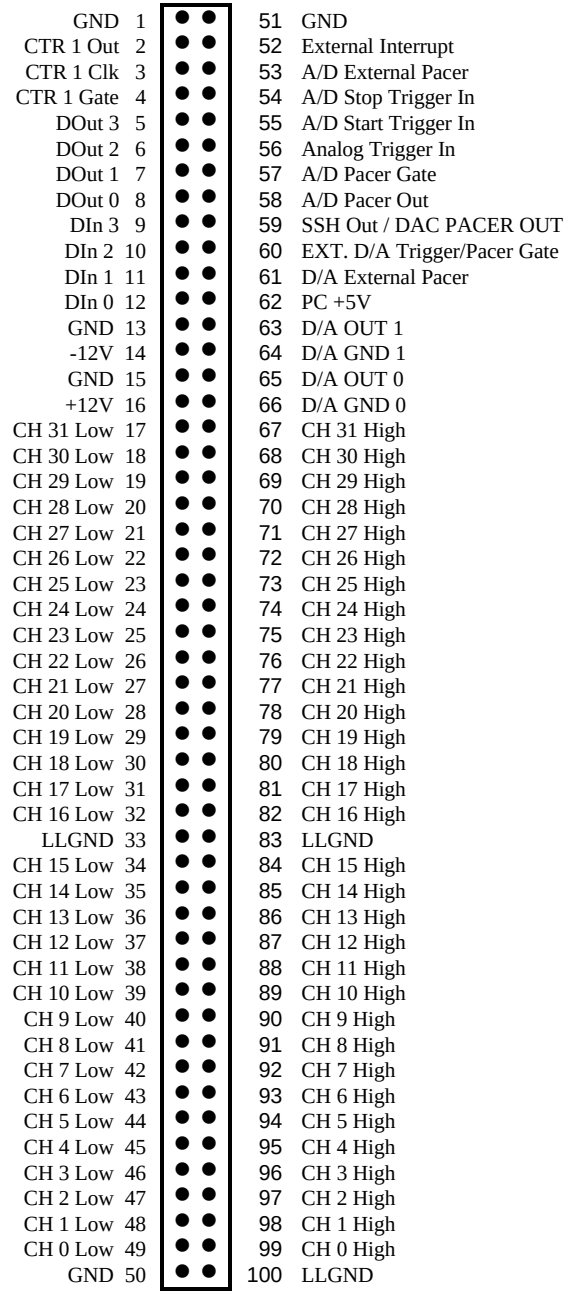


Figure 2-2. PCI-DAS64/Mx/16 100-Pin Connector–Differential Inputs Configuration

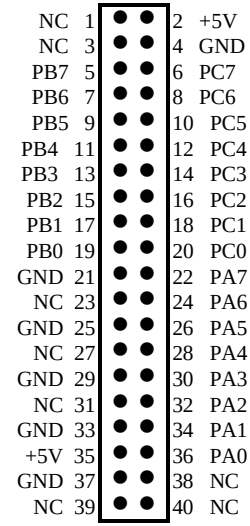


Figure 2-3. Auxiliary/Digital Connector

2.2 Connecting Signals

The analog connector is a 100-pin, high-density D-type connector. It will accept the C100HD50-3 (or -6) cable.

The C100HD50-3 has a 100-pin connector that branches to two, 50-pin ribbon cables. The two 50-pin ribbon cables are terminated with standard 50-pin header connectors. A CIO-TERM100 or two CIO-MINI50 screw terminal boards is the ideal way to terminate real world signals and route them into the PCI-DAS64/Mx/16

The auxiliary digital connector can be accessed using a variety of cabling schemes. To bring the 40-pin header out to a bracket at the back of the PC, use a BP40-37 adapter. This terminates in a CIO-DIO series compatible connector to which you can connect a CIO-MINI37 or CIO-TERMINAL screw terminal board using a C37FF-# or C37FFS-# cable. Other options include direct cabling using a C40-37F-# (which maintains CIO-DIO compatibility) or using the C40FF-# cable with the CIO-MINI40 screw terminal board.

There is additional general information regarding analog signal connection and configuration at http://www.measurementcomputing.com/signals/.

3 Programming & Applications

After following the installation instructions in Section 2, your board is now installed and ready for use. Although the board is part of the larger DAS family, there is no correspondence between registers. Software written at the register level for other DAS models will not work with the PCI-DAS64/Mx/16.

3.1 Programming Languages

Measurement Computing Corporation's Universal Library™ provides complete access to board functions from a variety of Windows programming languages. If you are planning to write programs, or would like to run the example programs for Visual Basic or any other language, please refer to the Universal Library manual.

3.2 Packaged Applications Programs

Many packaged application programs, such as DAS-Wizard™, Labtech Notebook™, and HP-VEE™, now have drivers for the PCI-DAS64/Mx/16. If the package you own does not appear to have drivers for the PCI-DAS64/Mx/16, please fax or e-mail the package name and the revision number from the install disks. We will research the package for you and advise how to obtain the correct drivers.

Some application drivers are included with the Universal Library package, but not with the Application package. If you have purchased an application package directly from the software vendor, you may need to purchase our Universal Library and drivers. Please contact us for more information on this topic.

3.3 Register Level Programming

It is recommended that you make use of the Universal Library or one of the packaged application programs mentioned above for controlling your board. Register level programming should be attempted only by experienced programmers. If you decide that you must use register level programming in your application, additional information may be found at *http://www.measurementcomputing.com/registermaps/registers.htm.*

This page is blank

4 Functional Description

4.1 Functional Overview

The PCI-DAS64/Mx/16 is a multifunction measurement and control board. The design of the board may be simplified into several blocks containing the major functions of the board. Please take a moment to examine Figure 4-1.

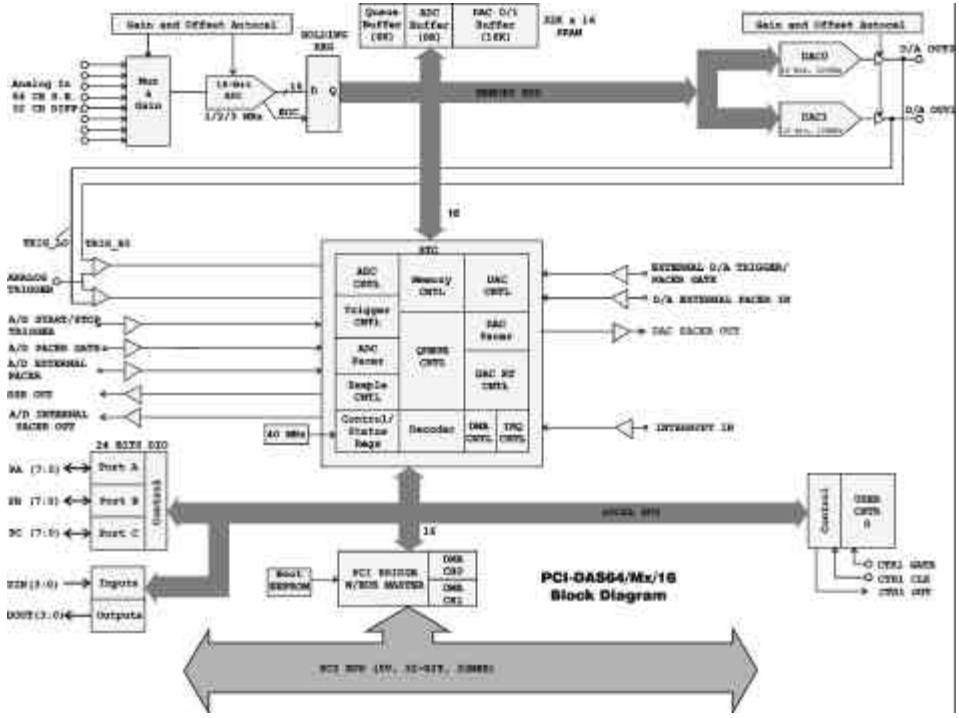


Figure 4.1. PCI-DAS64/Mx/16 Block Diagram

This page is blank

5 Calibration

5.1 Introduction

The PCI-DAS64/Mx/16 provides self-calibration of the analog inputs and outputs, eliminating the need for external equipment and user adjustments. All adjustments are made via 8-bit calibration DACs which are referenced to an on-board factory-calibrated standard. The board is fully calibrated at the factory with calibration coefficients stored in nvRAM. At run time, these calibration factors are loaded into system memory and are automatically retrieved each time a different DAC/ADC range is specified. The user can recalibrate any time using factory voltage standards by selecting the "*Calibrate*" option in *Insta*Cal.

5.2 Calibration

Calibrating the PCI-DAS64/Mx/16 is very easy. Launch *Insta*Cal, and select the “Calibrate” option. A full calibration typically requires less than two minutes. We strongly recommend that you turn your computer on, and allow at least 60 minutes for the internal computer case temperature to stabilize prior to calibrating (or acquiring data with) the board.

Please note that A/D calibration is performed at user-selectable conversion frequencies. This is required in order reduce any frequency dependent offset effects across the operating range. When the “Calibrate -> A/D” option is selected the user is prompted to select one-of-eight possible calibration frequencies as shown in Figure 5.1. We recommend choosing a frequency as close as possible to the applications’ sampling frequency.

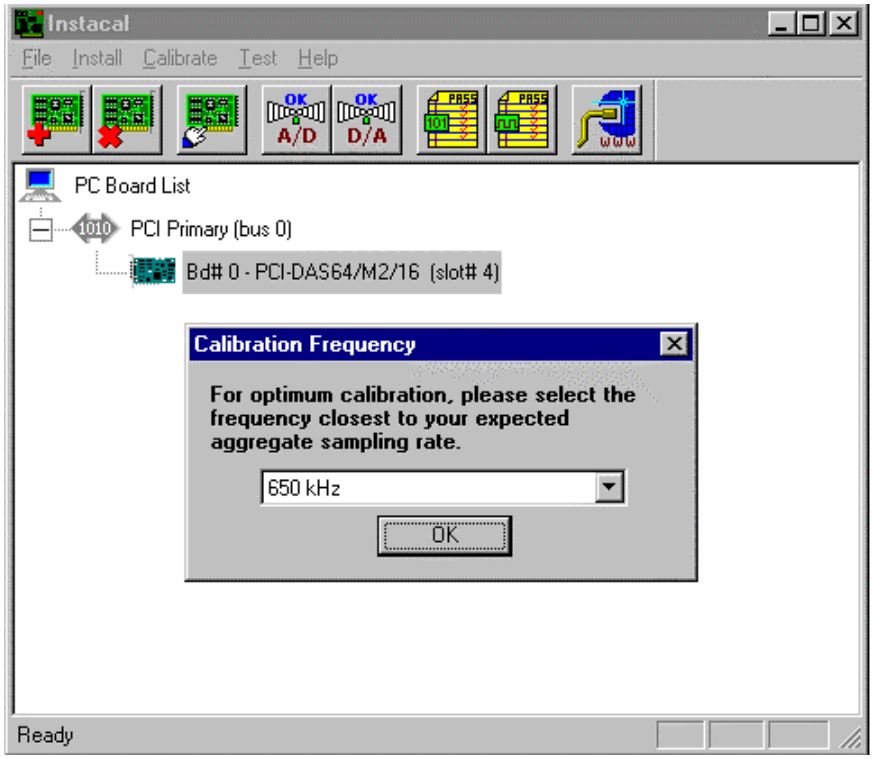


Figure 5-1. InstaCal A/D Calibration Screen

Table 5-1 describes the available calibration frequencies and recommended sampling frequency ranges. Using this table as a guide, a ±1 LSB offset error relative to the calibrated offset is maintained over a given sampling frequency range. We recommend that you perform A/D calibration at 100 kHz if you intend to use the entire sampling frequency range but do not want to re-calibrate for a given sampling frequency span. In that case, you can expect a ±6 LSB offset drift with respect to the calibrated offset over the full 10 Hz to 2 MHz range.

Calibration Frequency (kHz)	Min Sampling Frequency (kHz)	Max Sampling Frequency (kHz)
2	0.01	6
15	6	30
50	30	70
100	70	200
300	200	400
650	400	1000
1250	1000	1500
1850	1500	2000

Table 5-1. Recommended A/D Calibration Frequencies

For best results, calibrate the board immediately prior to making your measurements. The high-resolution analog components on the board are somewhat sensitive to temperature and this pre-measurement calibration helps assure your board operates at the same temperature at which it was calibrated.

5.3 Theory of Calibration

The PCI-DAS64/Mx/16 is easily calibrated using the *Insta*Cal software package.

A variety of methods are used to calibrate the different elements on the board. Offset calibration for the analog front end is performed via adjustments of the ADC itself. Front-end gain adjustment is performed only via the ADC reference. This strategy was chosen since the gain tolerance of the in-amp circuit is quite good and there is adequate gain tuning range using only the ADC.

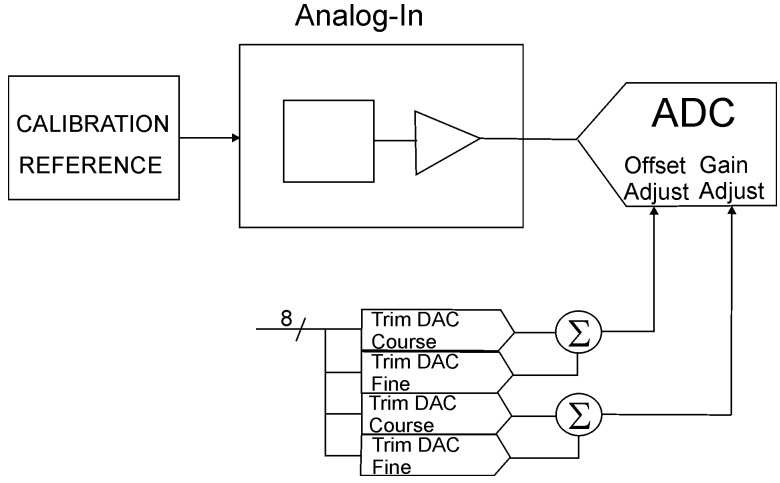


Figure 5-2. Analog Front-End Calibration System

The analog output circuits are calibrated for gain and offset. Gain calibration of the analog outputs is performed via DAC reference adjustments. Offset adjustments for the analog output are made in the output buffer section. The tuning range of this adjustment yields maximum DAC and output buffer offsets. Figure 5-4 is a block diagram of the analog front-end calibration system. The calibration scheme for the Analog Out section is shown in Figure 5-2. This circuit is duplicated for both DAC0 and DAC1

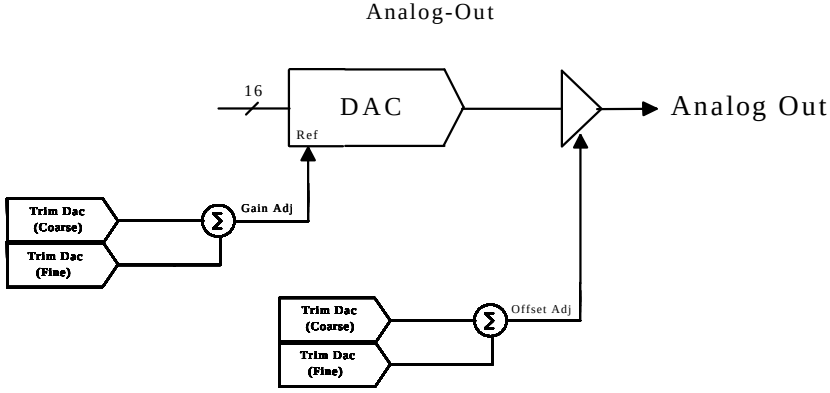


Figure 5-3. Analog Out Calibration

6 Specifications

Typical for 25°C unless otherwise specified.

Specifications for the PCI-DAS16/M3/16 are preliminary and subject to change.

Power Consumption

+5V	2.9A typical, 3.3 max
+12V	10mA max.

Analog Input Section

A/D converter type	Sub-ranging sampling ADC
Resolution	16 bits
Number of channels	32 differential or 64 single-ended, software selectable
Input ranges (SWprogrammable)	±5V, ±2.5V, ±1.25V, ±0.625V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
Polarity	Unipolar/Bipolar, software selectable
A/D pacing (SW programmable)	Internal counter – ASIC
	External source (A/D External Pacer). The total number of sample clocks must be at least 5 greater than the total number of samples desired. This is required to accommodate the pipelined architecture of the ADC.
	Software polled
Burst mode	Software selectable option. Valid for a fixed input range only. Burst rate (/3M, /2M) = 667nS. Burst rate (/1M) = 1µS.
A/D Gate Sources	External digital (A/D Pacer Gate)
	External analog (Analog Trigger In)
A/D gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Software-configurable for: • Above or Below reference • Positive or Negative hysteresis • In or Out of window. Trigger levels set by DAC0 and/or DAC1.

A/D trigger sources	External digital (A/D Start Trigger In and A/D Stop Trigger In)
	External analog (Analog Trigger In)
A/D triggering modes	External digital: Software-configurable for rising or falling edge.
	External analog: Software-configurable for Positive or Negative slope. Trigger levels set by DAC0 and/or DAC1.
	Pre-/Post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples. Compatible with both Digital and Analog trigger options.
Data transfer	From 8k RAM buffer via DMA (demand or non-demand mode) using scatter gather.
	Programmed I/O
Configuration Memory	8K words
Channel/Gain Queue	Up to 8K elements. Programmable channel, gain, and offset.
A/D conversion time	/3M = 333ns, /2M = 500nS, /1M = 1µS
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.

System Throughput

Condition	**Calibration Coefficients**	**Max ADC Rate for /1M**	**Max ADC Rate for /2M**	**Max ADC Rate for /3M**
1. Single channel, single input range.	Per specified range	1.0 M*S/s*	2.0 M*S/s*	3.0 M*S/s*
2. Multiple channel, single input range: ±5V, ±2.5V, ±1.25V, 0 to 5V, 0 to 2.5V	Per specified range	1.0 M*S/s*	1.5 M*S/s*	1.5 M*S/s*
3. Multiple channel, single input range: ±0.625V, 0 to 1.25V	Per specified range	750 *kS/s*	750 *kS/s*	750 *kS/s*
4. Single channel, multiple input ranges.	Default to value for cbAInScan() range	500 *kS/s*	500 *kS/s*	500 *kS/s*
5. Multiple channels, multiple ranges. All samples in Unipolar OR Bipolar Mode.	Default to value for cbAInScan() range	500 *kS/s*	500 *kS/s*	500 *kS/s*

6. Multiple channels, multiple ranges. All samples in Unipolar AND/OR Bipolar Mode.	Default to value for cbAInScan() range	500 *kS/s*	500 *kS/s*	500 *kS/s*
7. Multiple channel, switching Unipolar/Bipolar mode, single input range.	Default to value for cbAInScan() range	750 *kS/s*	750 *kS/s*	750 *kS/s*

Note: For conditions 1-3 above, specified accuracy is maintained at rated throughput. Conditions 4-7 apply calibration coefficients which correspond to the range value selected in cbAInScan(). These coefficients remain unchanged throughout the scan. Errors of up to 25 counts may be incurred when switching gains while in Bipolar or Unipolar mode *only* (conditions 4 & 5). Errors of up to 500 counts may be incurred when mixing Unipolar/Bipolar modes (conditions 6 & 7).

Accuracy

100KHz sampling rate, single channel operation and a 60 minute warm-up. Accuracies are listed for operational temperatures within ±2°C of internal calibration temperature. Calibrator test source high side tied to Channel 0 and low side tied to low-level ground at the user connector

Table 1 – Absolute Accuracy

Range	**Absolute Accuracy PCI-DAS64/M1/16 & PCI-DAS64/M2/16**	**Absolute Accuracy PCI-DAS64/M3/16**
±5.000V	±6.0 LSB	±8.0 LSB
±2.500V	±8.0 LSB	±10.0 LSB
±1.250V	±8.0 LSB	±12.0 LSB
±0.625V	±10.0 LSB	±14.0 LSB
0V to +5.000V	±8.0 LSB	±10.0 LSB
0V to +2.500V	±11.0 LSB	±12.0 LSB
0V to +1.250V	±13.0 LSB	±14.0 LSB

Table 2 -Typical Accuracy

Range	Typical Accuracy PCI-DAS64/M1/16 & PCI-DAS64/M2/16	Typical Accuracy PCI-DAS64/M3/16
±5.000V	±5.5 LSB	±7.0 LSB
±2.500V	±7.5 LSB	±9.0 LSB
±1.250V	±7.5 LSB	±11.0 LSB
±0.625V	±9.5 LSB	±12.0 LSB
0V to +5.000V	±7.5 LSB	±9.0 LSB
0V to +2.500V	±10.5 LSB	±11.0 LSB
0V to +1.250V	±12.5 LSB	±12.0 LSB

Table 3 - Accuracy Components

Range	Gain Error	Offset Error	DLE	ILE
±5.000V	±3.0 max, ±2.0 typ	±3.0 max, ±2.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
±2.500V	±3.0 max, ±2.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
±1.250V	±3.0 max, ±2.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
±0.625V	±5.0 max, ±4.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
0 to +5.000V	±4.0 max, ±3.0 typ	±4.0 max, ±3.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
0 to +2.500V	±6.0 max, ±5.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
0 to +1.250V	±6.0 max, ±5.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ

Each PCI-DAS64/Mx/16 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in *Table 1* above.

As shown in *Table 3*, total board error is a combination of Gain, Offset, Differential Linearity and Integral Linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case errors are realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

Typical accuracy is derived directly from the various component typical errors. These typical, maximum error calculations for the PCI-DAS64/Mx/16 are shown in *Table 2*. This table assumes that each of the errors contributes in the same direction.

Crosstalk

Crosstalk is defined here as the influence of one channel upon another when scanning two channels at the maximum rate. A full scale 100Hz triangle wave is input on Channel 1; Channel 0 is tied to Analog Ground at the 100 pin user connector. The table below summarizes the influence of Channel 1 on Channel 0 with the effects of noise removed. The residue on Channel zero is described in LSB's.

PCI-DAS64/M1/16

Range	Crosstalk (LSB_{pk-pk})	PCI-DAS64/M1/16	
		Per channel Rate (KHz)	ADC Rate (KHz)
±5.000V	15	500	1000
±2.500V	15	500	1000
±1.250V	20	500	1000
±0.625V	8	375	750
0V to +5.000V	15	500	1000
0V to +2.500V	20	500	1000
0V to +1.250V	8	375	750

PCI-DAS64/M2/16

Range	Crosstalk (LSB_{pk-pk})	PCI-DAS64/M2/16	
		Per channel Rate (KHz)	ADC Rate (KHz)
±5.000V	15	750	1500
±2.500V	15	750	1500
±1.250V	20	750	1500
±0.625V	8	375	750
0V to +5.000V	15	750	1500
0V to +2.500V	20	750	1500
0V to +1.250V	8	375	750

PCI-DAS64/M3/16

Range	Crosstalk (LSB_{pk-pk})	PCI-DAS64/M3/16	
		Per channel Rate (KHz)	ADC Rate (KHz)
±5.000V	24	750	1500
±2.500V	22	750	1500
±1.250V	20	750	1500
±0.625V	18	375	750
0V to +5.000V	22	750	1500
0V to +2.500V	20	750	1500
0V to +1.250V	18	375	750

Analog Input Full-Scale Gain drift	+0.3 LSB/°C typical
Analog Input Zero drift	+2.1 LSB/°C typical
Overall Analog Input drift	±2.4 LSB/°C typical
Common Mode Range	±5V
CMRR @ 60Hz	-90dB
Input leakage current	2.3nA
Input impedance	10×10^{11} Ohms
Absolute maximum input voltage	±15V
Warm-up time	60 minutes

Noise Performance

The following tables summarize the worst case noise performance for the PCI-DAS64/Mx/16 products.

Noise distribution is determined by gathering 50K samples with inputs tied to ground at the user connector. Samples are gathered at the maximum specified single-channel sampling rate. Specification applies to both Single-Ended and Differential modes of operation.

PCI-DAS64/M1/16 & PCI-DAS64/M2/16

Range	±2 counts	±1 count	MaxCounts	LSBrms*
± 5.000V	60%	40%	22	3.3
± 2.500V	60%	40%	24	3.6
± 1.250V	60%	40%	26	3.9
± 0.625V	45%	30%	32	4.8
0 to +5.000V	60%	40%	24	3.6
0 to +2.500V	60%	40%	26	3.9
0 to +1.250V	45%	30%	32	4.8

* RMS noise is defined as the peak-to-peak bin spread divided by 6.6

PCI-DAS64/M3/16

Range	±2 counts	±1 count	MaxCounts	LSBrms*
± 5.000V	55%	35%	35	5.3
± 2.500V	55%	35%	35	5.3
± 1.250V	55%	35%	35	5.3
± 0.625V	55%	35%	35	5.3
0 to +5.000V	55%	35%	35	5.3
0 to +2.500V	55%	35%	35	5.3
0 to +1.250V	55%	35%	35	5.3

* RMS noise is defined as the peak-to-peak bin spread divided by 6.6

Analog Output Section

Resolution	16-bits
Number of Channels	2
Voltage Range	±5V
Monotonicity	Guaranteed monotonic over temperature
Analog Output Zero drift	±1.6 LSB/°C
Overall Analog Output drift	±4.0 LSB/°C
Slew Rate	2.5V/µs
Settling Time	FS step to .0008%: 6µs max, all ranges
Current Drive	±15 mA
Output short-circuit duration	Indefinite @25mA
Output coupling	DC
Output impedance	0.1 ohms
Power up and reset	DACs cleared to 0 volts ±75mV max

Absolute Accuracy

Range	Absolute Accuracy
± 5V	±16.0 LSB

Accuracy Components

Range	Gain Error (LSB)	Offset Error (LSB)	DLE (LSB)	ILE (LSB)
±5.0V	±10.0 max	±5.0 max	±1.0 max	±1.0 max

Each PCI-DAS64/Mx/16 is tested at the factory to assure the board's overall error does not exceed the absolute accuracy limits listed in the *Absolute Accuracy* table above

Analog Output Pacing and Triggering

D/A pacing (SW programmable)	Internal counter – ASIC
	External source (D/A External Pacer)
	Software paced
D/A Gate Sources (SW programmable)	External digital (External D/A Trigger/Pacer Gate)
	External analog (Analog Trigger In)
D/A gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Software-configurable for Above or Below reference. Gating levels set by DAC0 or DAC1.
D/A trigger sources	External digital (External D/A Trigger/Pacer Gate)
	Software triggered
D/A triggering modes	External digital: Software-configurable for rising or falling edge.
Data transfer	From 16k RAM buffer via DMA (demand or non-demand mode) using scatter gather.
	Programmed I/O
	100 kS/s max per channel

Digital Input / Output

Digital Type (main connector)	Output: 74LS175
	Input: 74LS244
Configuration	4 inputs, 4 outputs (DIN0 through DIN3; DOUT0 to DOUT3)
Output high voltage (IOH = -0.4mA)	2.7V min
Output low voltage (IOL = 8mA)	0.5V max
Input high voltage	2.0V min, 7 volts absolute max
Input low voltage	0.8V max, –0.5 volts absolute min

Digital Type (Digital I/O connector)	82C55
Number of I/O	24 (Port A0 through Port C7)
Configuration	• 2 banks of 8 and 2 banks of 4, • 3 banks of 8, or • 2 banks of 8 with handshake
Input high voltage	2.0V min, 5.5V absolute max
Input low voltage	0.8V max, –0.5V absolute min
Output high voltage (IOH = -2.5mA)	3.0V min
Output low voltage (IOL = 2.5mA)	0.4V max
Power-up / reset state	Input mode (high impedance)

SSH output	TTL compatible output, HOLD is asserted from start of the conversion for Channel 0 through conversion of the last channel in the scan. Available at user connector (SSH OUT / D/A PACER OUT). This pin is software selectable as SSH OUT (default) or D/A PACER OUT.
SSH polarity	HOLD high (default) or HOLD low, software selectable

Interrupt Section

Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable through PLX9080
ADC Interrupt sources (Software Programmable)	DAQ_ACTIVE: Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP: Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE: Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL: Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE: Interrupt is generated after each conversion completes.
	DAQ_EOSCAN: Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ: Interrupt is generated after each interval delay during multi-channel scans.
DAC Interrupt sources (Software Programmable)	DAC_ACTIVE: Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE: Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY: Interrupt is generated DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL: Interrupt is generated when the DAC high channel output is updated.
	DAC_RETRANSMIT: Interrupt is generated when the end of a waveform sequence has occurred in retransmit mode.
External Interrupt	Interrupt is generated via edge-sensitive transition on the External Interrupt pin. Rising/falling edge polarity software selectable.

Counter Section

User counter type	82C54
Configuration	One down counter, 16 bits. Counters 2 and 3 not used.
Counter 1 Source	External, from connector (CTR1 CLK)
Counter 1 Gate	Available at connector (CTR1 GATE).
Counter 1 Output	Available at connector (CTR1 OUT).
Clock input frequency	10 MHz max
High pulse width (clock input)	30nS min
Low pulse width (clock input)	50nS min
Gate width high	50nS min
Gate width low	50nS min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Pacer Section

ADC Pacer type	ASIC
Configuration	1 down counter, 24 bits (1 scan interval, 1 sample interval)
ADC Pacer Source	40MHz internal source
ADC Pacer Gate	Internally controlled by software/hardware trigger.
ADC Pacer Out	ADC Pacer clock, available at user connector (A/D Pacer Out)
DAC Pacer type	ASIC
Configuration	1 down counter, 24 bits (1 scan interval, 1 sample interval)
DAC Pacer Source	40MHz or 100kHz internal source. Software selectable
DAC Pacer Gate	Internally controlled by software/hardware trigger.
DAC Pacer Out	DAC Pacer clock. Available at user connector (SSH OUT / D/A PACER OUT). This pin is software selectable as SSH OUT (default) or D/A PACER OUT.
Internal Pacer Crystal Oscillator	40 MHz
Frequency Accuracy	50ppm

Environmental

Operating Temperature Range	0 to 50°C
Storage Temperature Range	–40 to 100°C
Humidity	0 to 95% non-condensing

Mechanical

Card dimensions	315mmL x 100.6mmW x 16mmH

Software

Software Support	Universal Library and InstaCal

Main Connector and Pin Out

Connector type	Shielded SCSI 100 D-Type

Differential Analog Input Mode:

Pin	*Signal Name*	*Pin*	*Signal Name*
1	GND	51	GND
2	CTR1 OUT	52	EXTERNAL INTERRUPT
3	CTR1 CLK	53	A/D EXTERNAL PACER
4	CTR1 GATE	54	A/D STOP TRIGGER IN
5	DOUT3	55	A/D START TRIGGER IN
6	DOUT2	56	ANALOG TRIGGER IN
7	DOUT1	57	A/D PACER GATE
8	DOUT0	58	A/D PACER OUT
9	DIN3	59	SSH OUT / D/A PACER OUT
10	DIN2	60	EXTERNAL D/A TRIGGER/PACER GATE
11	DIN1	61	D/A EXTERNAL PACER
12	DIN0	62	PC +5V
13	GND	63	D/A OUT 1
14	-12V	64	D/A GND 1
15	GND	65	D/A OUT 0
16	+12V	66	D/A GND 0
17	CH31 LO	67	CH31 HI
18	CH30 LO	68	CH30 HI
19	CH29 LO	69	CH29 HI
20	CH28 LO	70	CH28 HI
21	CH27 LO	71	CH27 HI
22	CH26 LO	72	CH26 HI
23	CH25 LO	73	CH25 HI
24	CH24 LO	74	CH24 HI
25	CH23 LO	75	CH23 HI
26	CH22 LO	76	CH22 HI
27	CH21 LO	77	CH21 HI
28	CH20 LO	78	CH20 HI
29	CH19 LO	79	CH19 HI
30	CH18 LO	80	CH18 HI
31	CH17 LO	81	CH17 HI
32	CH16 LO	82	CH16 HI
33	LLGND	83	LLGND
34	CH15 LO	84	CH15 HI
35	CH14 LO	85	CH14 HI
36	CH13 LO	86	CH13 HI
37	CH12 LO	87	CH12 HI
38	CH11 LO	88	CH11 HI
39	CH10 LO	89	CH10 HI
40	CH9 LO	90	CH9 HI
41	CH8 LO	91	CH8 HI
42	CH7 LO	92	CH7 HI
43	CH6 LO	93	CH6 HI
44	CH5 LO	94	CH5 HI
45	CH4 LO	95	CH4 HI
46	CH3 LO	96	CH3 HI
47	CH2 LO	97	CH2 HI
48	CH1 LO	98	CH1 HI
49	CH0 LO	99	CH0 HI
50	GND	100	LLGND

Single-Ended Analog Input Mode:

Pin	*Signal Name*	*Pin*	*Signal Name*
1	GND	51	GND
2	CTR1 OUT	52	EXTERNAL INTERRUPT
3	CTR1 CLK	53	A/D EXTERNAL PACER
4	CTR1 GATE	54	A/D STOP TRIGGER IN
5	DOUT3	55	A/D START TRIGGER IN
6	DOUT2	56	ANALOG TRIGGER IN
7	DOUT1	57	A/D PACER GATE
8	DOUT0	58	A/D PACER OUT
9	DIN3	59	SSH OUT / D/A PACER OUT
10	DIN2	60	EXTERNAL D/A TRIGGER/PACER GATE
11	DIN1	61	D/A EXTERNAL PACER
12	DIN0	62	PC +5V
13	GND	63	D/A OUT 1
14	-12V	64	D/A GND 1
15	GND	65	D/A OUT 0
16	+12V	66	D/A GND 0
17	CH63 IN	67	CH31 IN
18	CH62 IN	68	CH30 IN
19	CH61 IN	69	CH29 IN
20	CH60 IN	70	CH28 IN
21	CH59 IN	71	CH27 IN
22	CH58 IN	72	CH26 IN
23	CH57 IN	73	CH25 IN
24	CH56 IN	74	CH24 IN
25	CH55 IN	75	CH23 IN
26	CH54 IN	76	CH22 IN
27	CH53 IN	77	CH21 IN
28	CH52 IN	78	CH20 IN
29	CH51 IN	79	CH19 IN
30	CH50 IN	80	CH18 IN
31	CH49 IN	81	CH17 IN
32	CH48 IN	82	CH16 IN
33	LLGND	83	LLGND
34	CH47 IN	84	CH15 IN
35	CH46 IN	85	CH14 IN
36	CH45 IN	86	CH13 IN
37	CH44 IN	87	CH12 IN
38	CH43 IN	88	CH11 IN
39	CH42 IN	89	CH10 IN
40	CH41 IN	90	CH9 IN
41	CH40 IN	91	CH8 IN
42	CH39 IN	92	CH7 IN
43	CH38 IN	93	CH6 IN
44	CH37 IN	94	CH5 IN
45	CH36 IN	95	CH4 IN
46	CH35 IN	96	CH3 IN
47	CH34 IN	97	CH2 IN
48	CH33 IN	98	CH1 IN
49	CH32 IN	99	CH0 IN
50	GND	100	LLGND

Digital Input / Output Connector and Pin Out

Connector type	40 pin header
Connector Compatibility	Translates to standard CIO-DIO24 type using BP40-37

Pin	*Signal Name*	*Pin*	*Signal Name*
1	NC	2	PC +5V
3	NC	4	DIG GND
5	PORT B 7	6	PORT C 7
7	PORT B 6	8	PORT C 6
9	PORT B 5	10	PORT C 5
11	PORT B 4	12	PORT C 4
13	PORT B 3	14	PORT C 3
15	PORT B 2	16	PORT C 2
17	PORT B 1	18	PORT C 1
19	PORT B 0	20	PORT C 0
21	DIG GND	22	PORT A 7
23	NC	24	PORT A 6
25	DIG GND	26	PORT A 5
27	NC	28	PORT A 4
29	DIG GND	30	PORT A 3
31	NC	32	PORT A 2
33	DIG GND	34	PORT A 1
35	PC +5V	36	PORT A 0
37	DIG GND	38	NC
39	NC	40	NC

For Your Notes

EC Declaration of Conformity

We, Measurement Computing Corporation, declare under sole responsibility that the product:

PCI-DAS64/Mx/16	High speed analog/digital I/O board for the PCI bus
Part Number	Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other informative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

Measurement Computing Corporation
16 Commerce Blvd.
Middleboro, Massachusetts 02346
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@measurementcomputing.com
www.measurementcomputing.com