Digilent D2XL™ System Board

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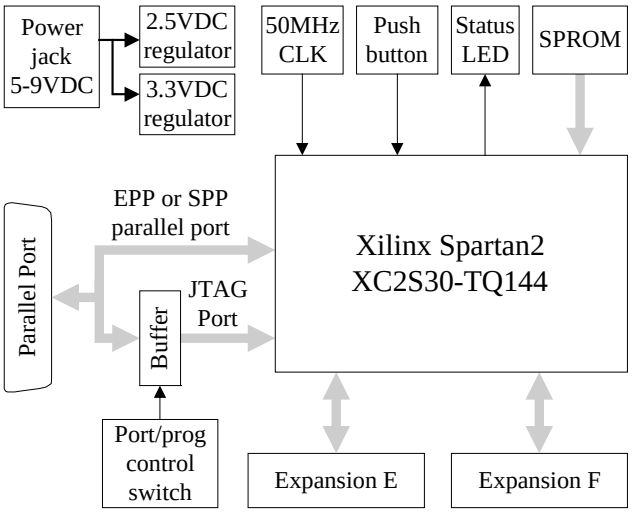
Overview

The Digilent D2XL development board (the D2XL) featuring the Xilinx Spartan 2 XC2S30 FPGA provides an inexpensive and expandable platform on which to design and implement digital circuits of all kinds. D2XL board features include:

- A Xilinx XC2S30 FPGA;
- Dual on-board 1.5A power regulators (2.5V and 3.3V);
- A socketed 50MHz oscillator;
- An EPP-capable parallel port for JTAG-based FPGA programming and user data transfers;
- An SPROM socket for automatic FPGA configuration at power-on;
- A status LED and pushbutton for basic I/O;
- Two 100-mil spaced, right-angle DIP socket 40-pin expansion connectors.



The D2XL board has been designed specifically to work with the Xilinx ISE CAD tools, including the free WebPack tools available from the Xilinx website. Like other Spartan 2 boards in the Digilab family, the D2XL board has been partitioned so that only the hardware required by a particular project need be purchased. Several existing peripheral boards that mate with the expansion connectors are available (see www.digilentinc.com), and new expansion boards are added often. The low-cost, standard expansion connectors allow new peripheral boards, including wire-wrap or manually soldered boards, to be quickly designed and used. The D2 board ships with a power supply and programming cable, so designs can be implemented immediately without the need for any additional hardware.

Functional description

The D2XL board has been designed to offer a low-cost and minimal system for designers who need a flexible platform to gain exposure to the Spartan 2 device, or for those who need to prototype FPGA-based designs rapidly. The D2XL board provides only the essential supporting devices for the Spartan 2, and routes all available FPGA signals to standard expansion connectors. Included on the board are 2.5VDC and 3.3VDC regulators, a JTAG configuration circuit that uses a standard parallel cable, basic communication ports including an enhanced parallel port, a 50MHz oscillator, and a pushbutton and LED for rudimentary I/O.

The D2XL board has been designed to serve as a host for various peripheral boards. The expansion connectors on the board mate with standard 40-pin, 100 mil spaced DIP headers available from any catalog distributor. Expansion connectors provide the unregulated supply voltage (VU), 3.3V, GND, and 37 FPGA signals to peripheral boards, so system designers can quickly develop application-specific peripheral boards. Digilent also produces a collection of expansion boards with commonly used devices. See the Digilent website (www.digilentinc.com) for a listing of currently available boards.

Table 1 shows all signals routed on the D2XL board. These signals and their circuits are described in the following sections.

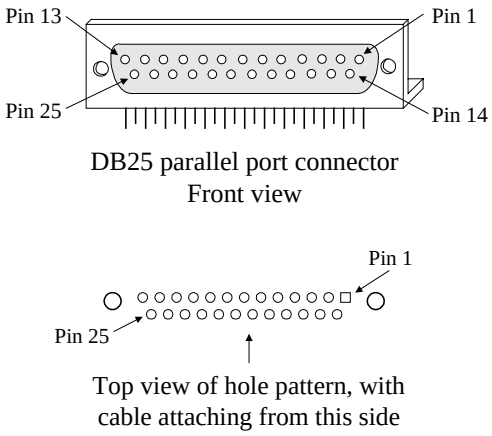
Power Supplies	
VU	Unregulated power supply voltage – depends on power supply used. Must be between 5VDC and 10VDC. Routed to regulators and expansion connectors only.
VDD33	VCCO/VCC for all devices, routed on PCB plane. 1.5A can be drawn with less than 20mV ripple (typical)
VDD25	FPGA VCCINT routed on PCB plane
GND	System ground routed to all devices on PCB ground plane
Programming and parallel port	
PWE	EPP mode write enable signal (in to FPGA)
PD0-PD7	Bi-directional data signals
PINT	Interrupt signal (out from FPGA)
PWT	EPP mode wait signal (out from FPGA)
PDS	EPP mode data strobe (in to FPGA)
PRS	Reset signal (in to FPGA)
PAS	EPP mode address strobe (in to FPGA)
On board devices	
BTN1	User-controllable pushbutton input
LED1	User-controllable status LED
CLK1	CMOS oscillator connected to GCLK0
Expansion Connectors	
E4-E40	E bus signals connecting the E connector to the FPGA
F4-F14	F bus signals connecting the F connectors to the FPGA

Table 1. D2XL board signal definitions

Parallel port and FPGA configuration circuit

The D2XL board uses a DB-25 parallel port connector to route JTAG programming signals from a host computer to the FPGA. This same connector also routes the computer's parallel port pins to the FPGA following the EPP port definition contained in the IEEE 1284 standard. A three-state buffer, controlled by a switch, determines whether the JTAG port or EPP port is enabled. With this circuit, the FPGA can be configured using the JTAG protocol over the parallel cable. The same cable can then be used (after the switch is repositioned) to move data between the board and the host computer using the high-speed EPP protocol. A separate JTAG header is also provided so that a dedicated programming cable (like the Xilinx Parallel III cable) can be used.

The JTAG programming circuit follows the JTAG schematic available from Xilinx, so that the D2XL board is fully compatible with all Xilinx programming tools. The EPP parallel port circuit follows the guidelines in the IEEE 1284 specification, and data rates approaching 2Mbytes/second can be achieved. JTAG and EPP connections are shown in the diagrams below.



Pin	EPP signal	EPP Function
1	Write Enable (O)	Low for read, High for write
2-9	Data bus (B)	Bidirectional data lines
10	Interrupt (I)	Interrupt/acknowledge input
11	Wait (I)	Bus handshake; low to ack
12	Spare	NOT CONNECTED
13	Spare	NOT CONNECTED
14	Data Strobe (O)	Low when data valid
15	Spare	NOT CONNECTED
16	Reset (O)	Low to reset
17	Address strobe (O)	Low when address valid
18-25	GND	System ground

Figure 1. Parallel port connectors and signals

The D2XL board directly supports JTAG and SPROM configuration. Hardware debugger configuration is supported indirectly. To configure the board from a computer using the JTAG mode, set switch 1 (SW1) in the JTAG position, and attach a power supply and programming cable. The power supply must be connected before the parallel cable, or the board may hang in a non-communicating state. The board will be auto-detected by the Xilinx JTAG programming software, and all normal JTAG operations will be available.

To configure the FPGA from an SPROM, load the programmed SPROM into the 8-pin ROM socket (labeled IC6), place SW1 in the PORT position, add jumpers to all mode pins, and apply power.

To configure the board using the hardware debugger protocol, a slight board modification is required – a jumper wire must be soldered to the non-VCC side of R44. Insert wire-wrap posts into the SPROM socket, attach the hardware debugger signals to the appropriate posts, and attach the PROG signal to the jumper wire attached to R44. The hardware debugger programming software will now automatically recognize the board, and hardware debugger programming can proceed as normal.

Programming circuit detail is shown below. Note that all parallel port signals are routed to the test header J12 for easy connection of test and measurement equipment.

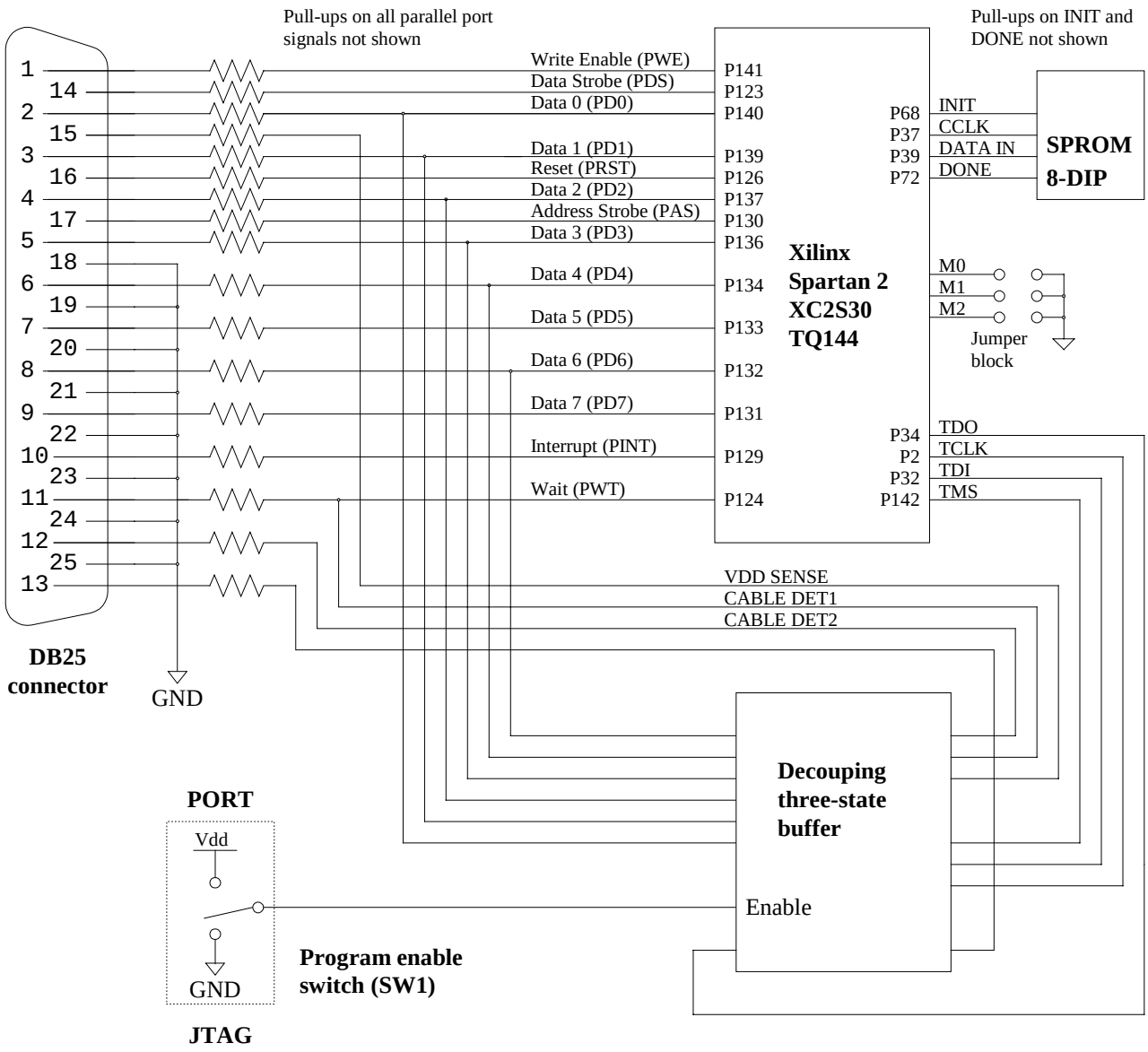


Figure 2. Parallel port and programming circuit schematic

Oscillator

The D2XL board provides a socketed half-size 8-pin DIP oscillator. The board ships with a 50MHz oscillator, allowing for system clocks from virtually DC to 200MHz (using the Spartan 2 DLL circuit and/or clock counter-dividers). Oscillators from 32KHz to 100MHz can easily be substituted, allowing for a wide range of clock frequencies. The oscillator, which is connected to the FPGA GCK0 input (pin 91), is bypassed with a 0.1uF capacitor and it is located as physically close to the FPGA as possible.

Power Supplies

The D2XL board uses two LM317 1.5A voltage regulators to produce 2.5VDC and 3.3VDC supplies. The regulator inputs are driven from an external DC power supply connected to the on-board 2.1mm center-positive power jack. The regulators have 10uF of input capacitance, 20uF of local output capacitance, and 10uF of regulation bypass capacitance. This allows the regulators to produce stable, low noise supplies using inexpensive power supplies, regardless of load (up to 1.5A). The regulator bodies are soldered to the board for improved thermal dissipation. DC supplies in the range of 5VDC to 10VDC may be used.

The D2XL board uses a four layer PCB, with the inner layers dedicated to VCC and GND planes. Most of the VCC plane is at 3.3V, with an island under the FPGA at 2.5V. The FPGA and the other ICs on the board all have 0.1uF bypass capacitors placed as close as possible to the VCC pins.

Total board current is dependant on FPGA configuration, clock frequency, and external connections. In test circuits with roughly 50K gates routed, a 50MHz clock source, and a single expansion board attached (the DIO2 board), approximately 200mA +/- 30% of supply current is drawn from the 2.5V supply, and approximately 150mA +/- 50% is drawn from the 3.3V supply. These currents are strongly dependent on FPGA and peripheral board configurations.

All FPGA VCCO pins are connected to the 3.3V supply. If other VCCO voltages are required, please contact Digilent for information regarding various options (Digilent can be contacted through www.digilentinc.com).

Pushbutton and LED

A single pushbutton and LED are provided on the board allowing basic status and control functions to be implemented without a peripheral board. As examples, the LED can be illuminated from a signal in the FPGA to verify that configuration has been successful, and the pushbutton can be used to provide a basic reset function independent of other inputs. The circuits are shown below.

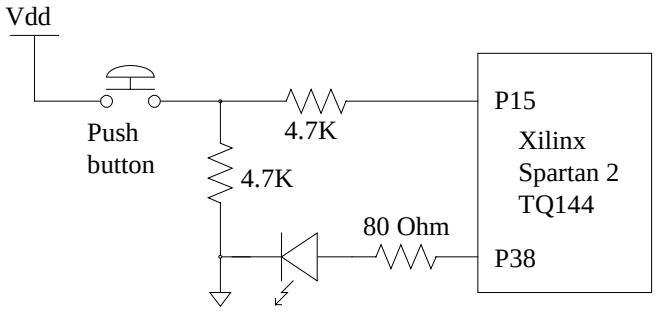
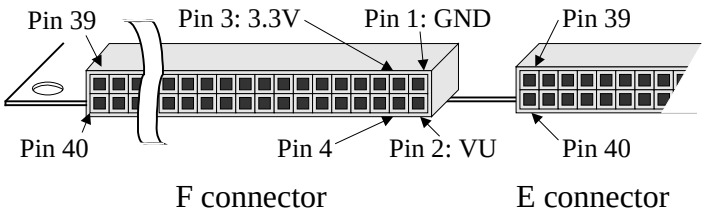


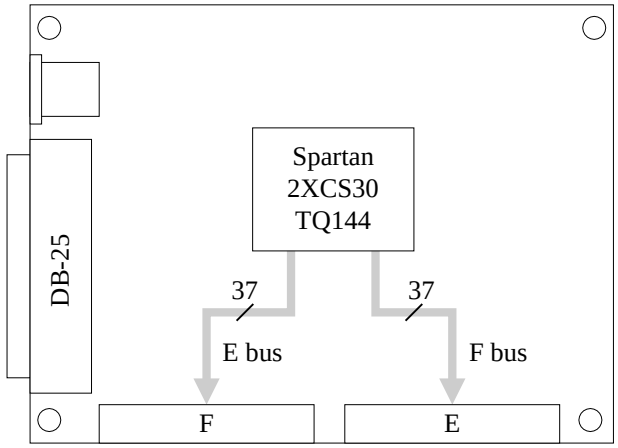
Figure 5. Pushbutton and LED detail

Expansion connectors



The two expansion connectors labeled E and F on the D2XL board use 100 mil spaced DIP headers. Both connectors have GND routed to pin 1, VU routed to pin 2, and 3.3V routed to pin 3. Pins 4-40 for both connectors route directly to individual FPGA pins. The connectors are separated by 400 mils, so any D2-family peripheral board can be placed used with the D2XL board.

The TQ144 package used on the D2XL board has 77 signal pins available to the user (the remaining I/O signals are routed to the parallel connector and other on board devices). Of these, 37 are routed to the E connector, 37 to the F connector, and 3 are left unconnected. Data rates of up to 100MHz are attainable across the E and F connectors.



D2XL expansion connector signals

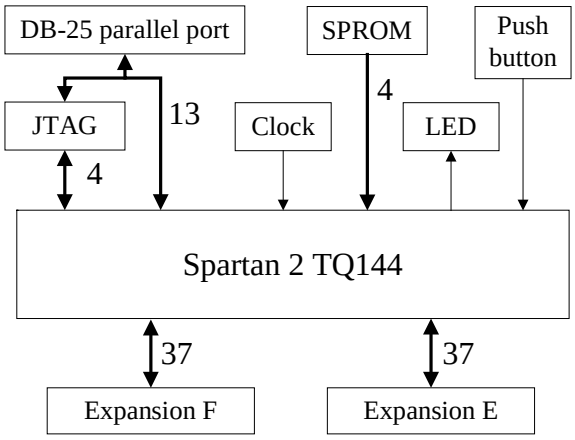
D2XL Expansion Connector pinouts					
E connector			F connector		
Pin	Signal	S-II pin	Pin	Signal	S-II pin
1	GND	-	1	GND	-
2	VU	-	2	VU	-
3	VDD33	-	3	VDD33	-
4	A4	122	4	B4	56
5	A5	121	5	B5	54
6	A6	120	6	B6	51
7	A7	118	7	B7	50
8	A8	117	8	B8	49
9	A9	115	9	B9	48
10	A10	114	10	B10	47
11	A11	113	11	B11	46
12	A12	112	12	B12	44
13	A13	103	13	B13	43
14	A14	102	14	B14	41
15	A15	100	15	B15	40
16	A16	99	16	B16	31
17	A17	96	17	B17	30
18	A18	95	18	B18	29
19	A19	94	19	B19	28
20	A20	93	20	B20	27
21	A21	87	21	B21	26
22	A22	86	22	B22	23
23	A23	85	23	B23	22
24	A24	84	24	B24	21
25	A25	83	25	B25	20
26	A26	80	26	B26	19
27	A27	79	27	B27	13
28	A28	78	28	B28	12
29	A29	77	29	B29	11
30	A30	75	30	B30	10
31	A31	74	31	B31	7
32	A32	67	32	B32	6
33	A33	66	33	B33	5
34	A34	65	34	B34	4
35	A35	63	35	B35	3
36	A36	62	36	B36	76
37	A37	60	37	B37	64
38	A38	59	38	B38	42
39	A39	58	39	B39	88
40	A40	57	40	B40	18

Spartan 2 FPGA

The block diagram of the D2XL board shows all connections between the FPGA and the devices on the board. All FPGA pin connections are shown in the following table.

The Spartan device can be configured using the Xilinx JTAG tools and a parallel cable connecting the D2XL board and the host computer. Note that a separate JTAG header that connects directly to the JTAG pins is also provided.

For further information on the Spartan FPGA, please see the Xilinx data sheets available at the Xilinx website (www.xilinx.com).



D2XL FPGA circuit block diagram

D2XL FPGA Pinout					
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	**VCCO**	49	B8	97	**VCCIN**
2	**TCK**	50	B7	98	**GND**
3	B35	51	B6	99	A16
4	B34	52	**GND**	100	A15
5	B33	53	**VCCO**	101	NC
6	B32	54	B5	102	A14
7	B31	55	**VCCINT**	103	A13
8	**GND**	56	B4	104	NC
9	**VCCINT**	57	A40	105	NC
10	B30	58	A39	106	**M2**
11	B29	59	A38	107	**VCCO**
12	B28	60	A37	108	**VCCO**
13	B27	61	**GND**	109	**M0**
14	**VCCINT**	62	A36	110	**GND**
15	BTN1*	63	A35	111	**M1**
16	**VCCO**	64	A37	112	A12
17	**GND**	65	A34	113	A11
18	B40*	66	A33	114	A10
19	B26	67	A32	115	A9
20	B25	68	**INIT**	116	NC
21	B24	69	**PROG**	117	A8
22	B23	70	**VCCO**	118	A7
23	B22	71	**VCCO**	119	**GND**
24	**VCCINT**	72	**DONE**	120	A6
25	**GND**	73	**GND**	121	A5
26	B21	74	A31	122	A4
27	B20	75	A30	123	PDS
28	B19	76	A36	124	PWT
29	B18	77	A29	125	**VCCINT**
30	B17	78	A28	126	PRS
31	B16	79	A27	127	**VCCO**
32	**TDI**	80	A26	128	**GND**
33	**GND**	81	**GND**	129	PINT
34	**TDO**	82	**VCCINT**	130	PAS
35	**VCCO**	83	A25	131	PD7
36	**VCCO**	84	A24	132	PD6
37	**CCLK**	85	A23	133	PD5
38	LED1	86	A22	134	PD4
39	**DIN**	87	A21	135	**GND**
40	B15	88	B39*	136	PD3
41	B14	89	**GND**	137	PD2
42	B38	90	**VCCO**	138	NC
43	B13	91	MCLK*	139	PD1
44	B12	92	**VCCINT**	140	PD0
45	**GND**	93	A20	141	PWE
46	B11	94	A19	142	**TMS**
47	B10	95	A18	143	**GND**
48	B9	96	A17	144	**VCCO**
* uses GCLK input					