Clock Generator

DS614 April 19, 2010 **Product Specification**

Introduction

The Clock Generator module provides clocks according to system wide clock requirements.

Features

- Automatic instantiation of Digital Clock Manager (DCM) modules and their connections
- Automatic instantiation of PLL modules and their connections
- Automatic instantiation of MMCM modules and their connections
- Automatic BUFG insertion
- Automatic DCM, PLL, and MMCM reset sequence determination and connection

LogiCORE™ IP Facts		
Core Specifics		
Supported Device Family	Virtex®-6/6CX, Spartan®-6, Spartan-3A/3A DSP, Spartan-3, Spartan-3E, Automotive Spartan 3/3E/3A/3A DSP, Virtex-5/5FX, Virtex-4/4Q/4QV,	
Version of core	4.00a	
Resources Used		
	Min	Max
LUTs	N/A	N/A
FFs	N/A	N/A
Block RAMs	N/A	N/A
DCMs	0	4
PLLs	0	2
MMCMs	0	4
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	EDK TCL Generated	
Verification	N/A	
Instantiation Template	EDK	
Design Tool Requirements		
Xilinx Implementation Tools	ISE® 12.1 or later	
Verification	ModelSim PE/SE 6.5c or later, ISIM 12.1 or later.	
Simulation	ModelSim PE/SE 6.5c or later, ISIM 12.1 or later.	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

Functional Description

The block diagram for the Clock Generator module is shown in Figure 1.

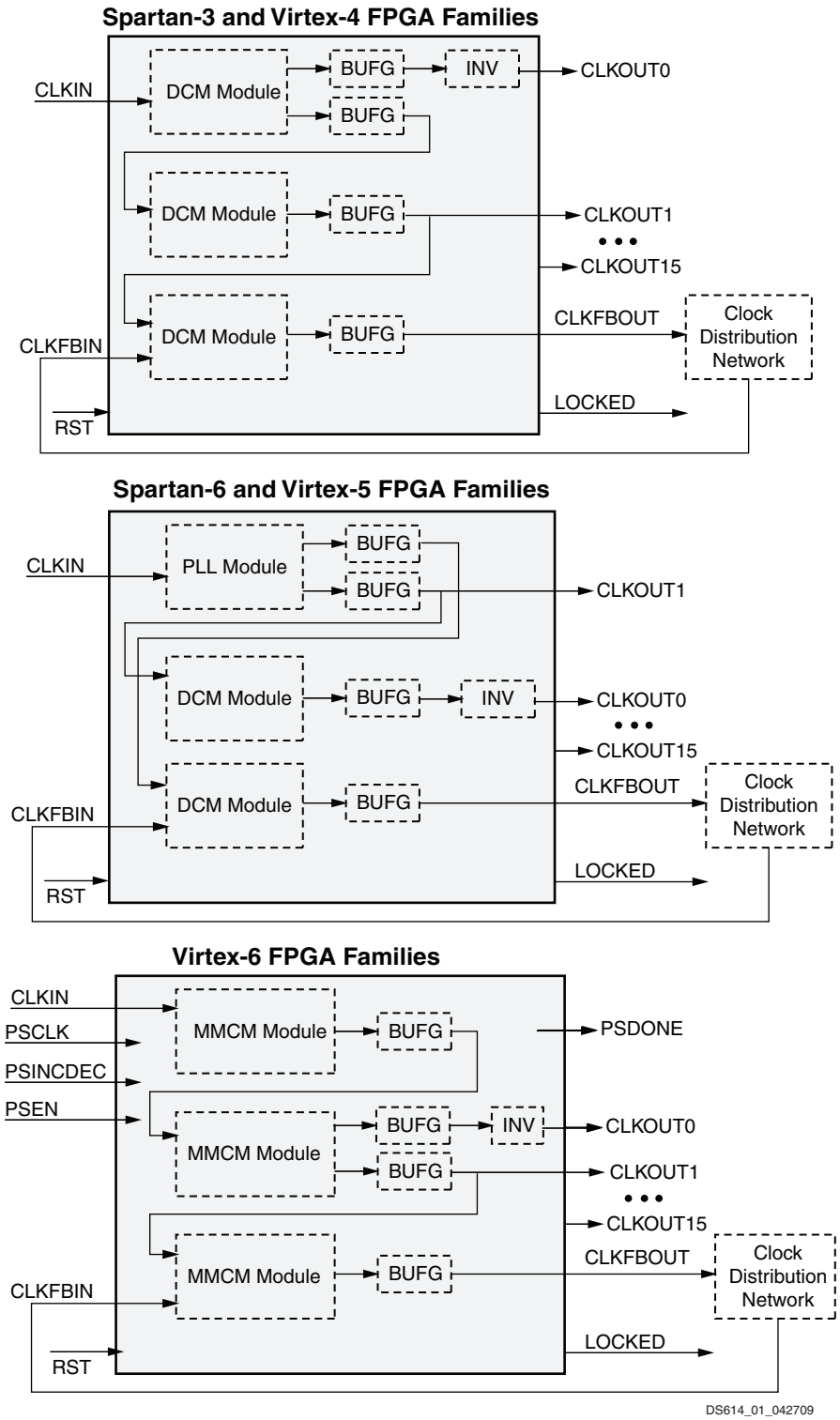

Figure 1: **Clock Generator Modules Block Diagram**

The Clock Generator module provides clock signals according to system wide clock requirements. The sub-system, depending on the FPGA family, is composed of up to four MMCM modules, four DCM modules, two PLL modules, BUFGs, clock inverters, and reset logics.

The Clock Generator module supports the following clock requirements:

- One input reference clock
- One feedback clock for clock deskew
- Up to 16 output clocks: see the DCM, PLL and MMCM primitives for clock frequency ranges
- Fixed phase shift (0 to 359 degrees) for output clocks
- Variable phase shift on Virtex6 devices
- Skew between clock outputs can be reduced through grouping. The outputs within the same group are generated from the same respective DCM, PLL or MMCM module
- Supports device families listed in the Supported Device Family field of the LogiCORE Facts Table. Input and output clock frequency range check according to device family selection by default using the slowest speed grade
- Supports both active high and active low external reset

If clock requirements cannot be met, then the LOCKED output signal remains inactive and the output clocks are undetermined.

Clock Generator I/O Signals

The interface signals for the Clock Generator module are listed and described in Table 1.

Table 1: **Clock Generator Signal Descriptions**

Signal Name	I/O	Initial State	Description
RST	I		If C_EXT_RESET_HIGH = 0, an inverter is inserted; otherwise, this signal is connected to the reset port of the DCM, PLL, or MMCM.
CLKIN	I		Connect to CLKIN of DCM, PLL, or MMCM.
CLKFBIN	I		Connect to CLKFB of a DCM or CLKFBIN of an MMCM for external feedback clock deskew, if used. Its edges line up with one of CLKOUTi, please refer to the description of C_CLKFBIN_FREQ and C_CLKFBIN_DESKEW in Table 3.
PSCLK	I		Phase shift clock input
PSINCDEC	I		Phase shift increment/decrement input
PSEN	I		Phase shift enable input
PSDONE	O		Phase shift done input
CLKOUT0-15	O	Low	Connect to the clock output port of a DCM, PLL, or MMCM. A BUFG is inserted; a clock inverter may be inserted.
CLKFBOUT	O	Low	Connect to the CLK0 port of a DCM or the CLKBOUT port of an MMCM, if used; a BUFG is inserted.
LOCKED	O	Low	LOCKED = High indicates all required clocks are stable.

Design Parameters

The parameters defined for the Clock Generator module are listed and described in Table 2.

Table 2: **Clock Generator Parameters**

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_CLKIN_FREQ	Frequency (Hz) of CLKIN	natural	0	integer
C_CLKFBIN_FREQ	Frequency (Hz) of CLKFBIN	natural	0	integer
C_CLKFBIN_DESKEW	CLKFBIN clock deskew with CLKOUTi	NONE, CLKOUT*i*, *i*=0,..,15	NONE	string
C_CLKOUT*i*_FREQ	*i*=0,..,15, frequency (Hz) of CLKOUT*i*	natural	0	integer
C_CLKOUT*i*_PHASE	*i*=0,..,15, phase shift of CLKOUT*i*	0 to 359	0	integer
C_CLKOUT*i*_GROUP	*i*=0,..,15, group name of CLKOUT*i*	NONE, DCM0, DCM1, DCM2, DCM3, PLL0, PLL0_ADJUST, PLL1, PLL1_ADJUST, MMCM0, MMCM1, MMCM2, MMCM3	NONE	string
C_CLKOUT*i*_BUF	*i*=0,..,15, if TRUE, insert BUFG for CLKOUT*i*	TRUE, FALSE	TRUE	boolean
C_CLKOUTi_VARIABLE PHASE	*i*=0,..,15, if TRUE, set MMCM clock output USE_FINE_PS	TRUE, FALSE	TRUE	boolean
C_CLKFBOUT_FREQ	Frequency (Hz) of CLKFBOUT	natural	0	integer
C_CLKFBOUT_GROUP	Group name of CLKFBOUT	NONE, MMCM0, MMCM1, MMCM2, MMCM3	NONE	string
C_CLKFBOUT_BUF	Insert BUFG for CLKFBOUT*i*	TRUE, FALSE	NONE	boolean
C_PSDONE_GROUP	Group name of PSDONE to specify the variable phase controlled MMCM name.	NONE, MMCM0, MMCM0_FB, MMCM1, MMCM1_FB, MMCM2, MMCM2_FB, MMCM3, MMCM3_FB	NONE	string
C_EXT_RESET_HIGH	External reset active high	0, 1	0	integer
C_FAMILY	Target architecture family for design	spartan3, spartan3e, spartan3a, spartan3adsp, aspartan3, aspartan3e, aspartan3a, aspartan3adsp, spartan6, virtex4, virtex5, virtex6	virtex5	string
C_SPEEDGRADE	Allowable values for target device speed grade	string	default	string
C_CLK_GEN	Set the value to UPDATE to generate clock circuit from high level parameters. The value is changed to PASSED if all required CLKOUTs are generated by DCM, PLL, MMCM, and FAILED.	UPDATE, PASSED, FAILED	UPDATE	string

The parameter values in Table 3 are generated automatically from the parameter values in Table 2.

Parameter - Port Dependencies

Table 3 contains the effects of setting various parameters.

Table 3: **Clock Generator Parameter-Port Dependencies**

Parameter	Port	Description
C_CLKIN_FREQ	CLKIN	0 - CLKIN is not used
C_CLKFBIN_FREQ	CLKFBIN, CLKFBOUT	0 - CLKFBIN is not used. It has to be equal to C_CLKFBOUT_FREQ. The edges from CLKFBIN line up with the edges from the first *CLKOUTi (i=0, .., 15)* clock that has C_CLKOUT*i*_FREQ = C_CLKFBIN_FREQ.
C_CLKFBIN_DESKEW	CLKFBIN, CLKFBOUT	If C_CLKFBIN_DESKEW = CLKOUTi and it is a Virtex-6 design, then CLKFBIN lines up with the edges from the CLKOUTi; otherwise refer to the description of C_CLKFBIN_FREQ in this table.
C_CLKOUT*i*_FREQ	CLKOUT*i* (*i*=0,..,15)	0 - CLKOUT*i* is not used
C_CLKOUT*i*_PHASE	CLKOUT*i* (*i*=0,..,15)	
C_CLKOUT*i*_GROUP	CLKOUT*i* (*i*=0,..,15)	NONE - CLKOUT*i* has no group requirement
C_CLKOUT*i*_BUF	CLKOUT*i* (*i*=0,..,15)	Set to FALSE if C_CLKOUT*i*_FREQ is 0
C_CLKOUT*i*_VARIABLE_PHASE	CLKOUT*i* (*i*=0,..,15)	Set MMCM clock to USE_FINE_PS if CLKOUTi is variable phase shifted output of MMCM.
C_CLKFBOUT_FREQ	CLKFBIN, CLKFBOUT	0 - CLKFBOUT is not used; has to be equal to C_CLKFBIN_FREQ
C_CLKFBOUT_GROUP	CLKFBIN, CLKFBOUT	NONE - Do not specify MMCM for external feedback
C_CLKFBOUT_BUF	CLKFBOUT	Set to FALSE if C_CLKBOUT_FREQ is 0
C_PSDONE_GROUP	PSDONE	NONE - Do not specify MMCM connected to variable phase shift control signal.

Differences Between Clock Generator v3.02a and v4.00a

Clock Generator v4.00a removes low level parameters used to be in previous versions. User is not able to directly manipulate the final clock circuitry and must rely on the core algorithm to generate the circuitry.

Clock Generator v4.00a has same high level parameters as Clock Generator v3.02a. To migrate the design with Clock Generator v3.02a to Clock Generator v4.00a, the user changes the core version from 3.02.a to 4.00.a only. Please note the above does not work if low level parameters of Clock Generator v3.02a are used (PARAMETER C_CLK_GEN is defined in the design and its value is not “UPDATE”).

Design Implementation

Target Technology

The target technology is an FPGA listed in the Supported Device Family field of the LogiCORE IP Facts table.

Device Utilization and Performance Benchmarks

The device utilization depends on the number of output clocks used and the value of the parameters of each output clock. Up to 4 DCM modules, 2 PLL modules and 4 MMCM modules may be instanced with BUFGs, clock inverters, and reset logics. See respective FPGA family user guide for details on DCM, PLL, MMCM, and BUFG primitive performance and available resources.

In one Clock Generator v4.00a module:

- Virtex-6 family FPGAs will use up to 4 MMCMs (no DCM or PLL)
- Virtex-5 and Spartan-6 family FPGAs will use up to 2 PLLs and 4 DCMs (no MMCM)
- All other FPGA families will use up to 4 DCMs (no PLL or MMCM)

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx ISE Design Suite Embedded Edition software under the terms of the Xilinx End User License. The core is generated using the Xilinx ISE Embedded Edition software (EDK)

For more information, please visit the Clock Generator product web page.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

Revision History

Date	Version	Description of Revisions
5/15/07	1.0	Initial Xilinx release.
1/16/08	1.1	Released v2.00a; added PLL support.
4/22/08	1.2	Released v2.01a; added Automotive SP3E, SP3A, SP3, and SP3A DSP support.
7/25/08	1.3	Added QPro Virtex-4 Hi-Rel, QPro Virtex-4 Rad Tolerant, and SP-3AN support.
3/31/09	1.4	Release v3.00a, changed C_CLK_GEN parameter, removed obsolete parameters.
6/24/09	1.5	Released v3.01a; added MMCM support.
12/2/09	1.6	Released v3.02a for EDK_L 11.4.
4/19/10	1.7	Released v4.00a for EDK 12.1; removed low-level internal view parameters.

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