Local Memory Bus (LMB) V10 (v1.00a)

Introduction

The LMB V10 module is used as the LMB interconnect for Xilinx® FPGA-based embedded processor systems. The LMB is a fast, local bus for connecting the MicroBlaze™ processor instruction and data ports to high-speed peripherals, primarily on-chip block RAM (BRAM).
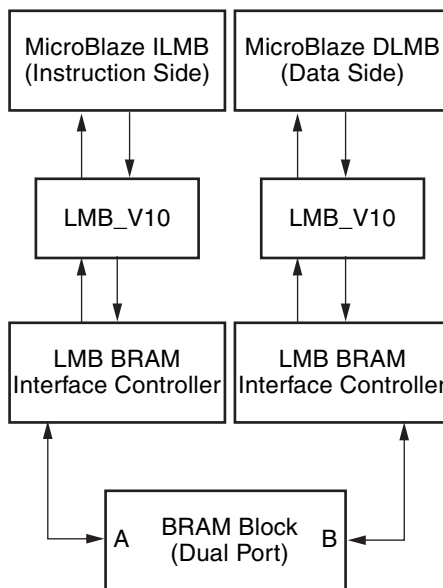
Features

- Efficient, single master bus (requires no arbiter)
- Separate read and write data buses
- Low FPGA resource utilization

LogiCORE™ IP Facts		
Core Specifics		
See EDK Supported Device Families.		
Version of core	lmb_v10	v1.00a
Resources Used		
	Min	Max
Slices	N/A	N/A
LUTs	0	353
FFs	0	0
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	See Tools for requirements.	
Verification		
Simulation		
Synthesis		
Support		
Provided by Xilinx. Inc.		

Functional Description

A MicroBlaze processor system using two LMB V10 modules is shown in Figure 1. This system illustrates the use of both I and D side LMB buses connecting to a dual-ported BRAM Block via separate LMB BRAM interface controllers.

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Figure 1: **MicroBlaze Processor System Using Two LMB V10 Modules**

LMB V10 Module I/O Signals

The I/O ports for the LMB V10 module are listed in Table 1.

Table 1: **LMB V10 Module I/O Ports**

Port Name	MSB:LSB	I/O	Description
LMB_CLK		I	LMB Clock
SYS_Rst		I	External System Reset
LMB_Rst		O	LMB Reset
M_ABus	0:C_LMB_AWIDTH-1	I	Master Address Bus
M_ReadStrobe		I	Master Read Strobe
M_WriteStrobe		I	Master Write Strobe
M_AddrStrobe		I	Master Address Strobe
M_DBus	0:C_LMB_DWIDTH-1	I	Master Databus
M_BE	0:C_LMB_DWIDTH/8-1	I	Master Byte Enables
Sl_DBus	0:C_LMB_DWIDTH*C_LMB_NUM_SLAVES-1	O	Slave Data Bus
Sl_Ready	0:C_LMB_NUM_SLAVES-1	O	Slave Data Ready

Table 1: **LMB V10 Module I/O Ports** *(Cont'd)*

Port Name	MSB:LSB	I/O	Description
LMB_ABus	0:C_LMB_AWIDTH-1	O	LMB Address Bus
LMB_ReadStrobe		O	LMB Read Strobe
LMB_WriteStrobe		O	LMB Write Strobe
LMB_AddrStrobe		O	LMB Address Strobe
LMB_ReadDBus	0:C_LMB_DWIDTH-1	O	LMB Read Data Bus
LMB_WriteDBus	0:C_LMB_DWIDTH-1	O	LMB Write Data Bus
LMB_Ready		O	LMB Data Ready
LMB_BE	0:C_LMB_DWIDTH/8-1	O	LMB Byte Enables

Local Memory Bus Parameters

Table 2: **LMB_V20 Design Parameters**

Parameter Name	Feature/Description	Allowable Values	Default Value	VHDL Type
C_LMB_NUM_SLAVES	Number of LMB Slaves	1–16	4	integer
C_LMB_AWIDTH	LMB Address Bus Width	32	32	integer
C_LMB_DWIDTH	LMB Data Bus Width	32	32	integer
C_EXT_RESET_HIGH	Level of external reset	0 = Active Low reset 1 = Active High reset	1	integer

Allowable Parameter Combinations

There are no restrictions on parameter combinations.

Parameter - Port Dependencies

The LMB V10 module parameter-port dependencies are listed in Table 3.

Table 3: **LMB V10 Module Parameter - Port Dependencies**

Parameter Name	Ports (Port width depends on parameter)
C_LMB_NUM_SLAVES	Sl_DBus, Sl_Ready
C_LMB_AWIDTH	M_ABus, LMB_ABus
C_LMB_DWIDTH	M_DBus, M_BE, Sl_DWIDTH, LMB_ReadDBus, LMB_WriteDBus, LMB_BE
C_EXT_RESET_HIGH	none

Design Implementation

Design Tools

The LMB V10 module design is hand written.

To see the synthesis tool used for this device, go to Tools. The NGC netlist output from XST is then input to the Xilinx Alliance tool suite for actual device implementation.

Target Technology

The target technology is an FPGA listed in EDK Supported Device Families.

Reference Documents

None

Revision History

Date	Version	Revision
09/12/02	1.0	Initial Xilinx release.
01/07/03	1.2	Update for SP3.
07/08/03	1.3	Update to new template.
01/26/04	1.4	Updates to TM and copyright.
08/13/04	1.5	Updated for Gmm; updated content format, reviewed and updated trademarks and supported device family listing.
4/4/05	1.6	Updated for EDK 7.1.1 SP1 release; updated trademarks and supported device listing.
8/24/05	1.7	Converted to new DS template.
12/1/05	1.8	Added Spartan®-3E to supported device listing.
2/22/06	1.9	Updated supported devices listing and design tool requirements. Deleted *125 MHz operation* bullet from Features section.
4/24/09	2.0	Replaced references to supported device families and tool name(s) with hyperlinks to PDF files; Updated trademark information.

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