IP Processor LMB BRAM Interface Controller (v2.10b)

DS452 March 2, 2010 **Product Specification**

Introduction

This document provides the design specification for the Local Memory Bus (LMB) Block RAM (BRAM) Interface Controller.

The LMB BRAM Interface Controller connects to an lmb_v10 bus.

Version 2.00.a and later of the LMB BRAM controller is required for use with MicroBlaze™ v5.00.a and later. Earlier versions of the BRAM controller will not work correctly with MicroBlaze v5.00.a data side LMB accesses.

To correctly handle the address mask computation, v2.10.a and later of the LMB BRAM controller is required for use with MicroBlaze v6.00.a.

Features

- LMB v1.0 bus interfaces with byte enable support
- Used in conjunction with bram_block peripheral to provide fast BRAM memory solution for MicroBlaze ILMB and DLMB ports.
- Supports byte, half-word, and word transfers

LogiCORE™ Facts				
Core Specifics				
Supported Device Family	Virtex®-6, Spartan®-6, Spartan-3, Spartan-3A/3A DSP, Spartan-3E, Automotive Spartan 3/3E/3A/3A DSP, Virtex-4/4Q/4QV, Virtex-5/5FX			
Resources Used	Slices	LUTs	FFs	Block RAMs
	N/A	6	2	0
Provided with Core				
Documentation	Product Specification			
Design File Formats	VHDL			
Constraints File	N/A			
Verification	N/A			
Instantiation Template	N/A			
Design Tool Requirements				
Xilinx Implementation Tools	ISE® 12.1			
Verification	Mentor Graphics ModelSim: v6.5c and above			
Simulation	Mentor Graphics ModelSim: v6.5.c and above			
Synthesis	ISE® 12.1			
Support				
Provided by Xilinx, Inc.				

Functional Description

The LMB BRAM Interface Controller is the interface between the LMB and the bram_block peripheral. A BRAM memory subsystem consists of the controller along with the bram_block peripheral.

The input/output signals of the LMB BRAM interface controller are shown in Figure 1 and are listed and described in Table 1. See the description of LMB Signals in the MicroBlaze Bus Interfaces chapter in the *MicroBlaze Processor Reference Guide.*

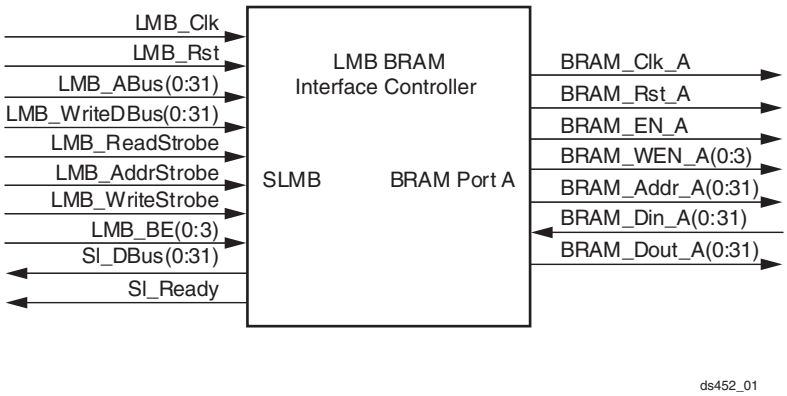

Figure 1: **Dual LMB BRAM Interface Controller Block Diagram**

LMB BRAM Interface Controller I/O Signals

The I/O ports and signals for the LMB BRAM Interface Controller are listed and described in Table 1.

Table 1: **LMB BRAM Interface Controller I/O Signals**

Port Name	MSB:LSB	I/O	Description
LMB_Clk		I	LMB Clock
LMB_Rst		I	LMB Reset (Active High)
LMB_ABus	0:C_LMB_AWIDTH-1	I	LMB Address Bus
LMB_WriteDBus	0:C_LMB_DWIDTH-1	I	LMB Write Data Bus
LMB_ReadStrobe		I	LMB Read Strobe
LMB_AddrStrobe		I	LMB Address Strobe
LMB_WriteStrobe		I	LMB Write Strobe
LMB_BE	0:C_LMB_DWIDTH/8-1	I	LMB Byte Enable Bus
SI_DBus	0:C_LMB_DWIDTH-1	O	LMB Read Data Bus
SI_Ready		O	LMB Data Ready
BRAM_Rst_A		O	BRAM Reset
BRAM_Clk_A		O	BRAM Clock
BRAM_EN_A		O	BRAM Enable
BRAM_WEN_A		O	BRAM Write Enable

Table 1: **LMB BRAM Interface Controller I/O Signals *(Cont'd)***

Port Name	MSB:LSB	I/O	Description
BRAM_Addr_A	0:C_LMB_AWIDTH-1	O	BRAM Address
BRAM_Din_A	0:C_LMB_DWIDTH-1	I	BRAM Data Input
BRAM_Dout_A	0:C_LMB_DWIDTH-1	O	BRAM Data Output

LMB BRAM Interface Controller Parameters

To allow the user to obtain an LMB BRAM Interface Controller that is uniquely tailored a specific system, certain features can be parameterized in the LMB BRAM Interface Controller design. This allows the user to configure a design that only utilizes the resources required by the system, and operates with the best possible performance. The features that can be parameterized in Xilinx LMB BRAM Interface Controller designs are shown in Table 2.

Table 2: LMB **BRAM Interface Controller Parameters**

Parameter Name	Feature/Description	Allowable Values	Default Value	VHDL Type
C_BASEADDR	LMB BRAM Base Address	Valid Address Range(2)	None (1)	std_logic_vector
C_HIGHADDR	LMB BRAM HIGH Address	Valid Address Range(2)	None(1)	std_logic_vector
C_MASK	LMB Decode Mask	Valid decode mask(3)	0x00800000	std_logic_vector
C_LMB_AWIDTH	LMB Address Bus Width	32	32	integer
C_LMB_DWIDTH	LMB Data Bus Width	32	32	integer

1. No default value is specified for C_BASEADDR and C_HIGHADDR to insure that the actual value is set; if the value is not set, a compiler error is generated. These generics must be a power of 2. C_BASEADDR must be a multiple of the range, where the range is C_HIGHADDR - C_BASEADDR +1.
2. The range specified by C_BASEADDR and C_HIGHADDR must comprise a complete, contiguous power-of-two range, such that range = 2^n, and the n least significant bits of C_BASEADDR must be zero.
3. The decode mask determines which bits are used by the LMB decode logic to decode a valid access to LMB.

C_BASEADDR

Base address decoded by this core.

C_HIGHADDR

High address decoded by this core.

C_MASK

If using the Embedded Development Kit, this bit is automatically set by the LMB BRAM Interface Controller when running the Platform Generator tool and users do not need to set the value. The address mask indicates which bits are used in the LMB decode to decode that a valid address is present on the LMB. Any bits that are set to '1' in the mask indicate that the address bit in that position is used to decode a valid LMB access. All other address bits are considered don't care for the purpose of decoding LMB accesses. The LMB BRAM Interface Controller may limit the user's choice for the address mask: the most restrictive case is that only a single bit may be set in the mask. Consult the platform generation tool informational messages for details.

C_LMB_AWIDTH

LMB Address Bus Width. Specifies the width in bits of the LMB address buses connected to this core. The default is 32 bits.

C_LMB_DWIDTH

LMB Data Bus Width. Specifies the width in bits of the LMB data buses connected to this core. The default is 32 bits.

Allowable Parameter Combinations

There are no restrictions on parameter combinations.

Parameter - Port Dependencies

The width of many of the BRAM Interface Controller signals depends on the number of memories in the system and the width of the various data and address buses. The dependencies between the BRAM design parameters and I/O signals are shown in Table 3.

Table 3: Parameter-Port Dependencies

Parameter Name	Ports (Port width depends on parameter)
C_BASEADDR	none
C_HIGHADDR	none
C_MASK	none
C_LMB_AWIDTH	LMB_ABus
C_LMB_DWIDTH	LMB_BE, LMB_WriteDBus, Sl_DBus, BRAM_Din_A, BRAM_Dout_A

Design Implementation

Design Tools

The LMB BRAM interface controller design is hand written. The NGC netlist output from XST is then input to the Xilinx Alliance tool suite for actual device implementation.

Target Technology

The target technology is an FPGA listed in the Supported Device Family field of the LogiCORE Facts table.

Device Utilization and Performance Benchmarks

Because the BRAM interface controller is a module that will be used with other design pieces in the FPGA, the utilization and timing numbers reported in this section are just estimates. Because the BRAM interface controller is combined with other pieces of the FPGA design, the utilization of FPGA resources and timing of the BRAM interface controller design will vary from the results reported here. These numbers do not reflect any BRAM resources used.

Table 4: **Performance and Resource Utilization Benchmarks for Virtex-4 FPGAs**

Parameter Values		Device Resources	
C_LMB_DWIDTH	C_LMB_AWIDTH	Slice Flip- Flops	4-input LUTs
32	32	1	5

1. These benchmark designs contain only the BRAM interface controller with registered inputs/outputs without any additional logic. Benchmark numbers approach the performance ceiling rather than representing performance under typical user conditions.

Programming Model

Supported Memory Sizes

For supported BRAM memory sizes, see DS444 IP Processor Block RAM (BRAM) Block (v1.00a).

Example Base Address, High Address Specifications

The base address (C_BASEADDR) and high address (C_HIGHADDR) must specify a valid range for the BRAM that is attached to the BRAM Controller. The range (C_HIGHADDR – C_BASEADDR) specified by the high address and base address must be equal to 2^n bytes, where n is a positive integer and 2^n is a valid memory size as shown above. In addition, the n least significant bits of C_BASEADDR must be equal to 0.:

Table 5: Example Address Range Specifications

Memory Size (Bytes)	C_BASEADDR	C_HIGHADDR
8 K	0x24000000	0x24001FFF
16 K	0xE0000000	0xE0003FFF
32 K	0x3FF00000	0x3FF07FFF
64 K	0x82000000	0x8200FFFF
128 K	0xB0000000	0xB001FFFF
256 K	0xC0000000	0xC003FFFF

LMB Timing

See the MicroBlaze Bus Interfaces chapter in the *MicroBlaze Processor Reference Guide* for details on the transaction signaling.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Reference Documents

None.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
1/12/06	1.0	Initial release.
7/28/08	1.2	Added QPro Virtex-4 Hi-Rel and QPro Virtex-4 Rad Tolerant FPGA support.
10/1/08	1.3	Initial release of v2.10.b
12/15/08	1.4	In LogiCORE IP Facts Table, replaced device family listing and tool name(s) with link to PDF file; added link to special disclaimer on first page.
4/24/09	1.5	Replaced references to supported device families and tool name(s) with hyperlink to PDF file.
3/2/10	1.6	Incorporated CR543063; inserted link to Block BRAM DS for supported BRAM sizes data, converted to current DS template.

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