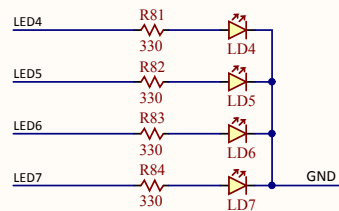
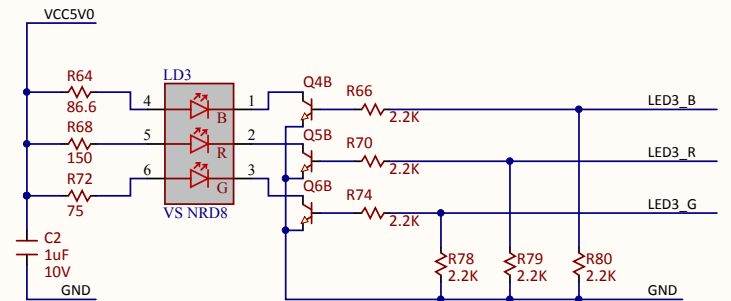
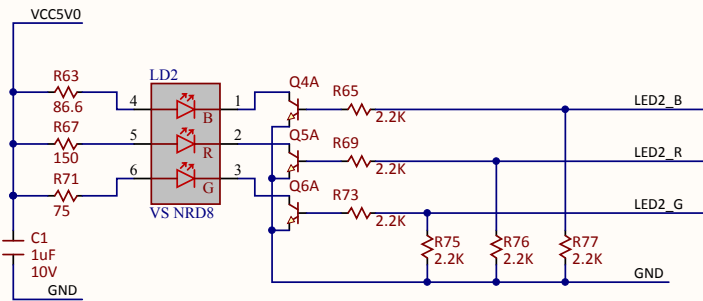
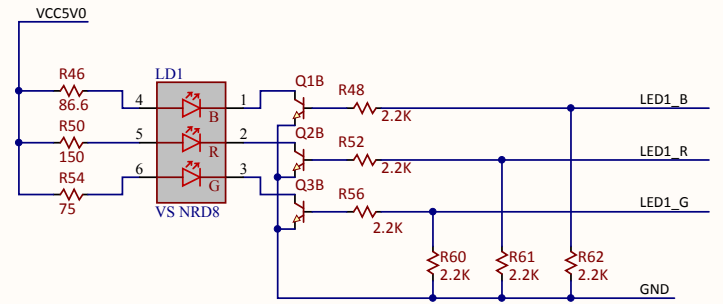
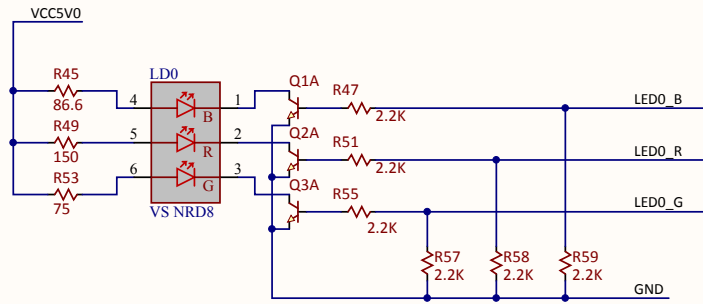


- Foot
- F1
- Foot
- F2
- Foot
- F3
- Foot
- F4

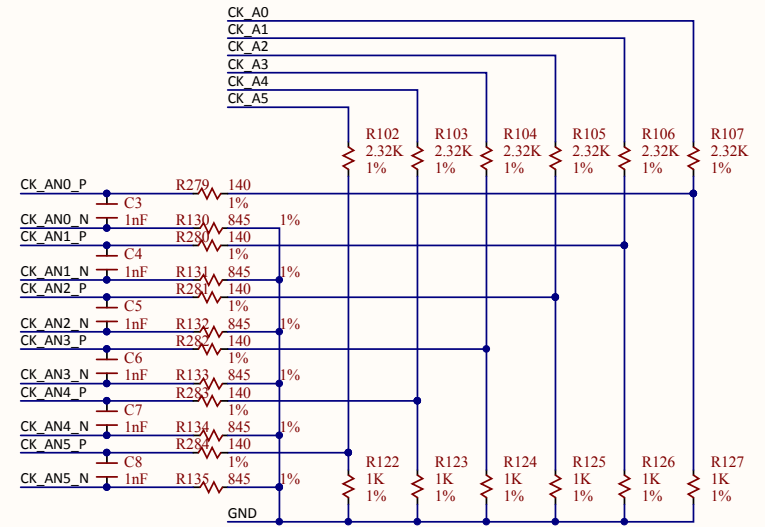
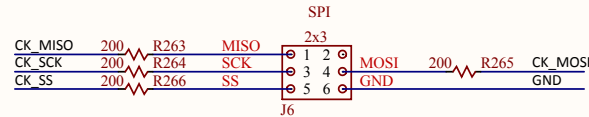
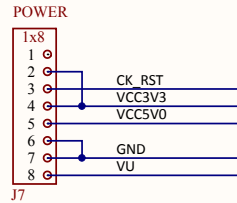
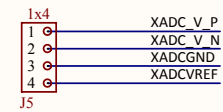
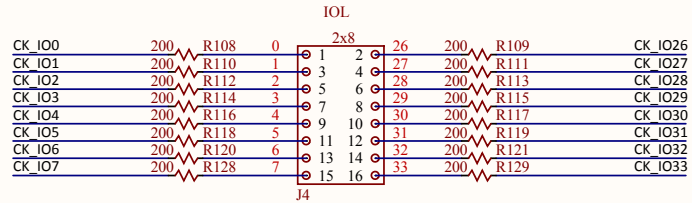
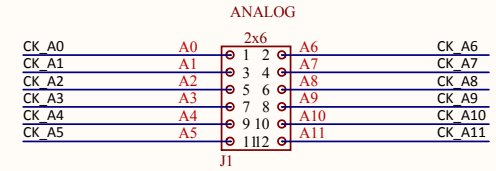
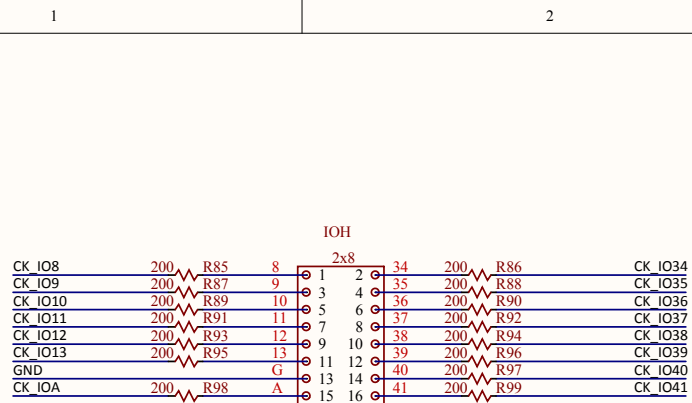
Title Arty		Rev C.0
Circuit PMOD, BTN, SWTs		Copyright 2015
Doc#	500-319	
Engineer	MTA	
Author	GMA	
Date	6/4/2015	
Sheet#	1 out of 12	





Title Arty		Rev C.0 Copyright 2015
Circuit LEDs		
Doc#	500-319	
Engineer	MTA	
Author	GMA	
Date	6/4/2015	
Sheet#	2 out of 12	

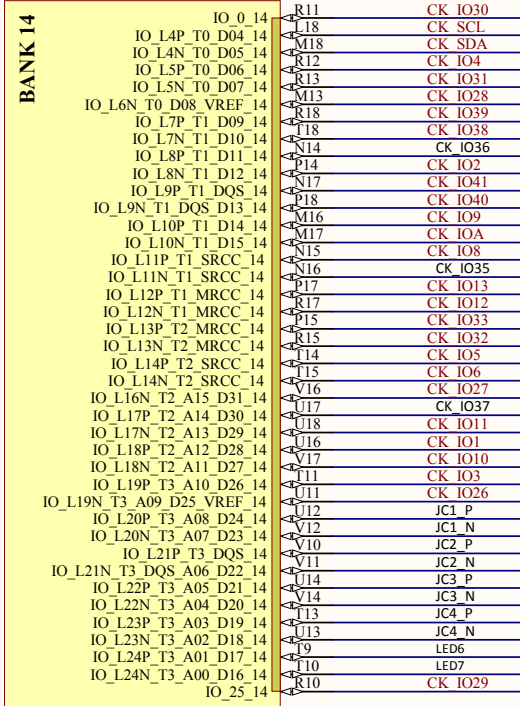




Note: Terminate N signals next to Analog Header

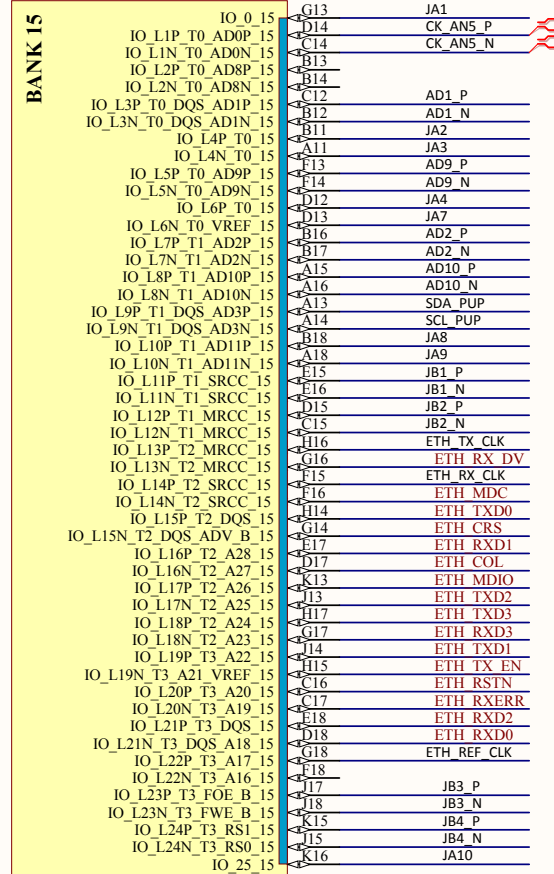
Title		Rev	
Arty		C.0	
Circuit		Copyright 2015	
CHiPkiT IO			
Doc#	500-319		
Engineer	MTA		
Author	GMA		
Date	6/4/2015		
Sheet#	3 out of 12		

IC1A



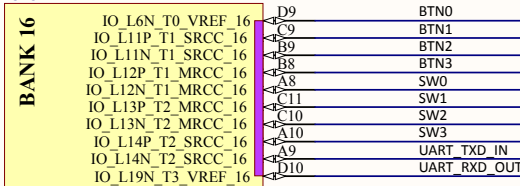
XC7A15T-L1CSG3241

IC1B

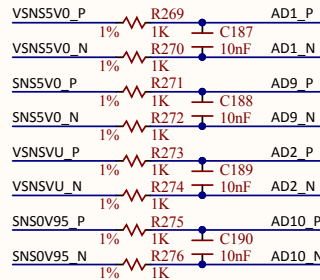


XC7A15T-L1CSG3241


IC1C



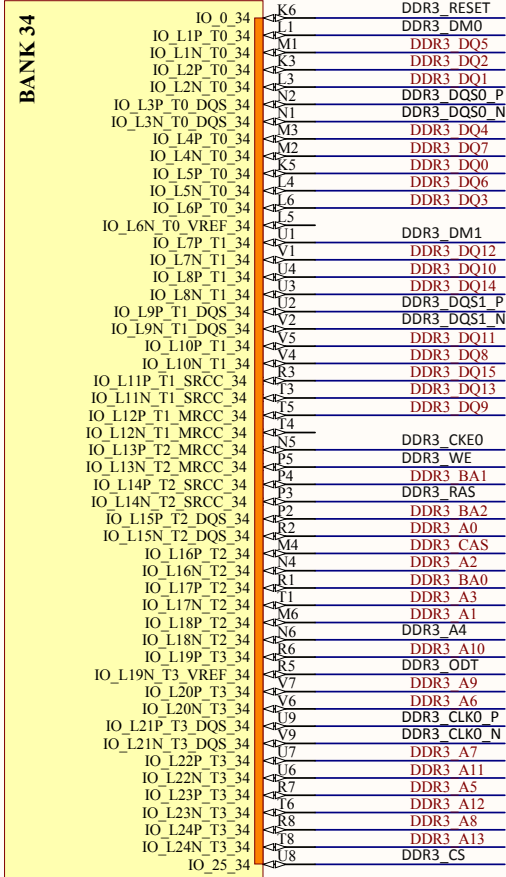
XC7A15T-L1CSG3241



Title		Rev
Arty		C.0
Circuit		Copyright 2015
FPGA Banks		
Doc#	500-319	
Engineer	MTA	
Author	GMA	
Date	6/4/2015	
Sheet#	4	out of 12

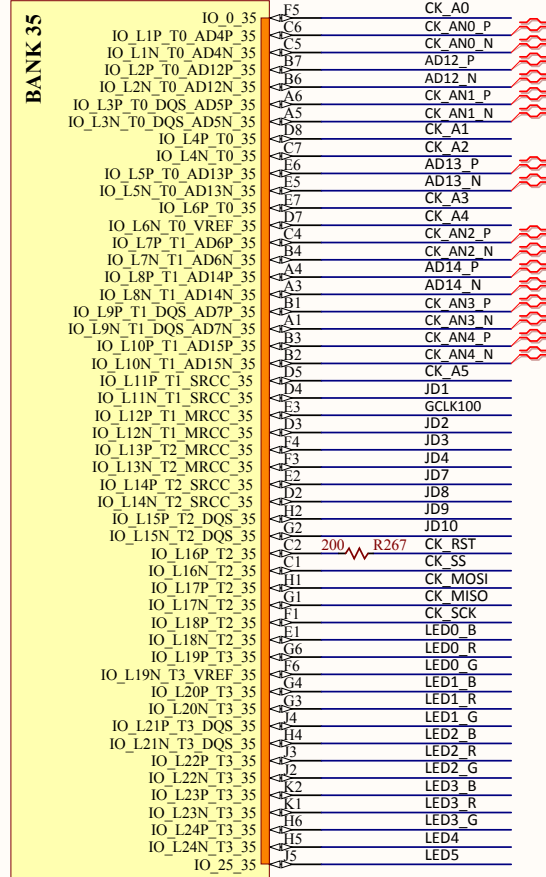


IC1D

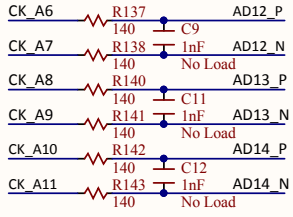
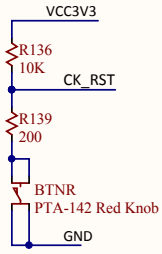
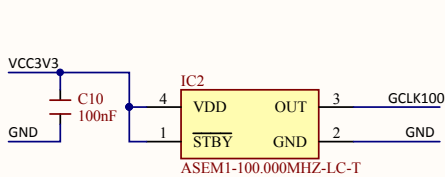


XC7A15T-L1CSG324I

IC1E

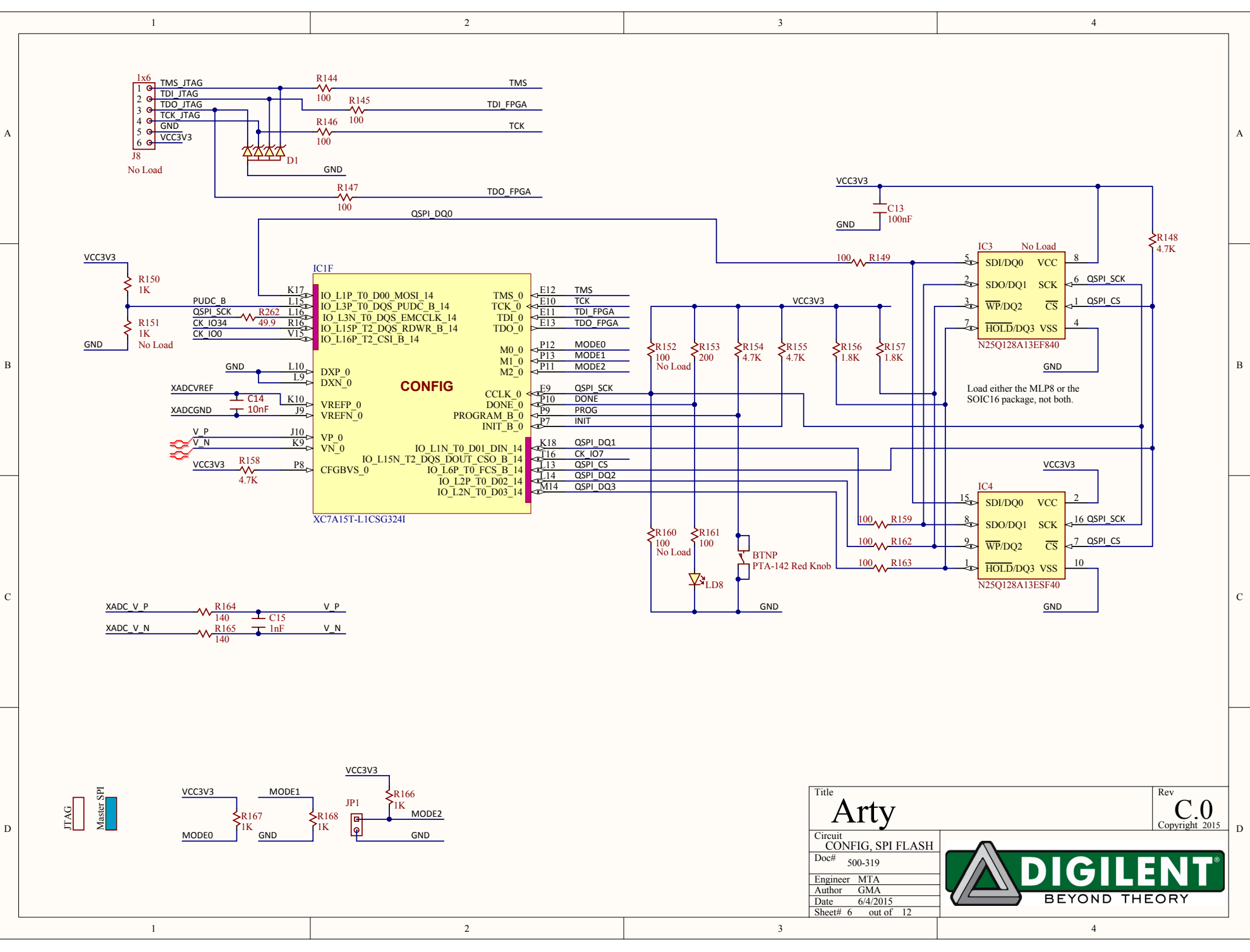


XC7A15T-L1CSG324I



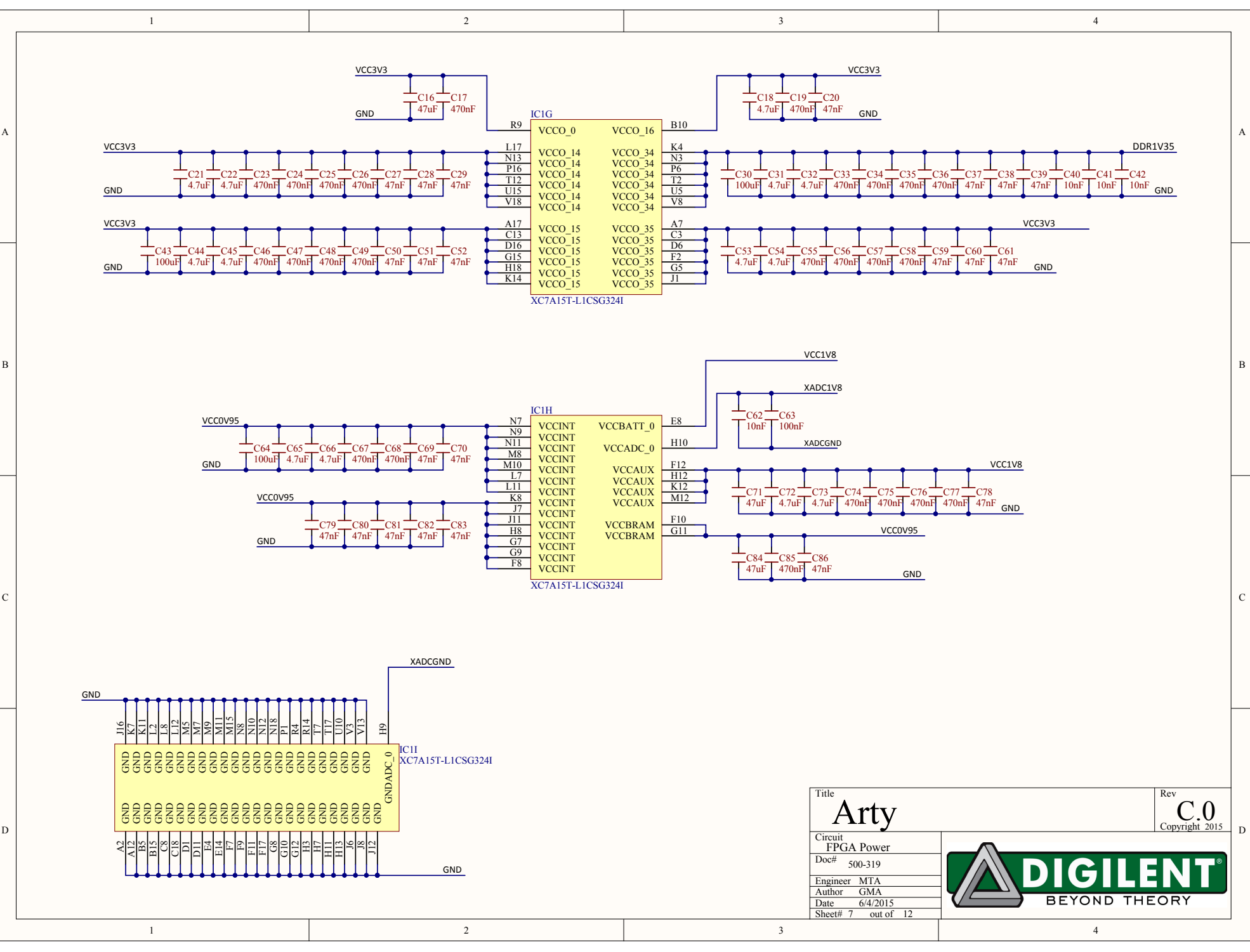
Title		Rev
<h1>Arty</h1>		<h1>C.0</h1>
		Copyright 2015
Circuit	FPGA Banks	
Doc#	500-319	
Engineer	MTA	
Author	GMA	
Date	6/4/2015	
Sheet#	5 out of 12	





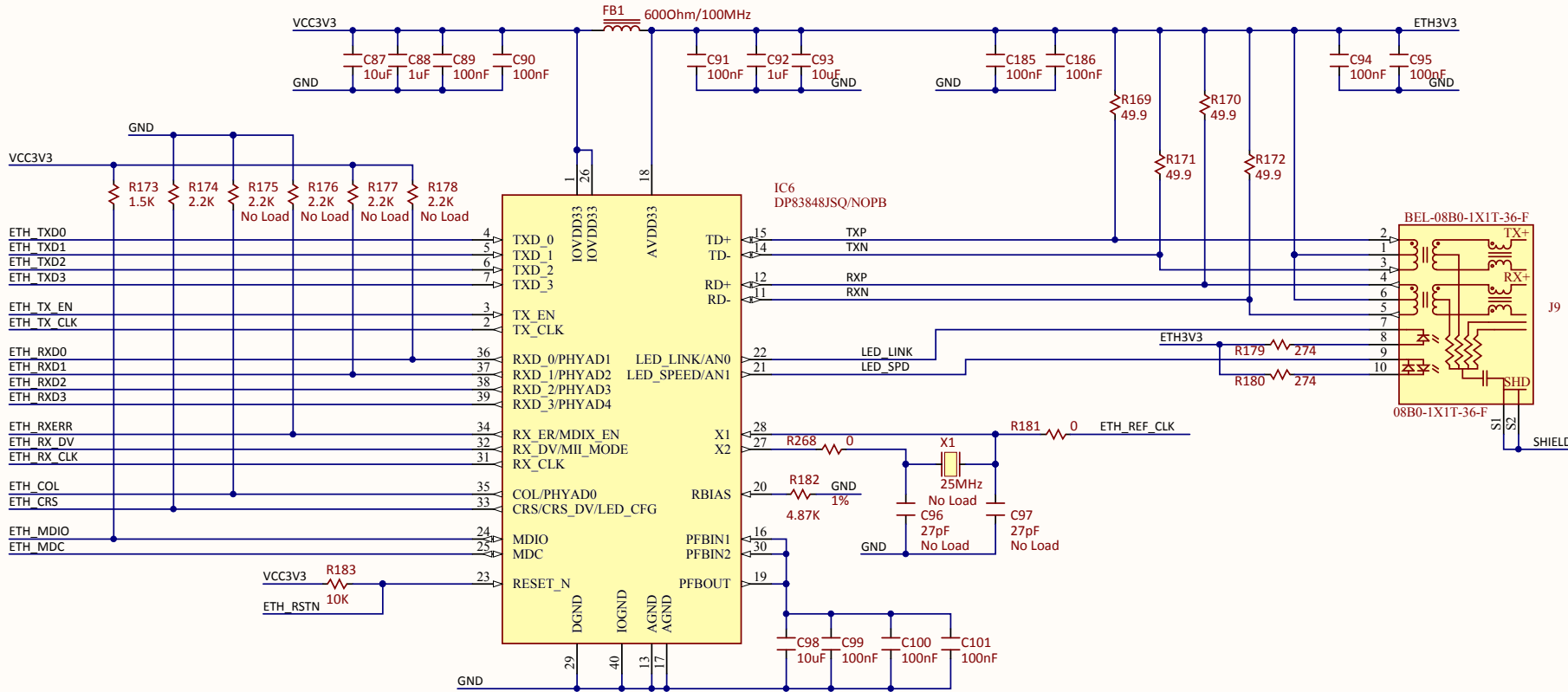
Title		Rev
Arty		C.0
Circuit		Copyright 2015
CONFIG, SPI FLASH		
Doc#	500-319	
Engineer	MTA	
Author	GMA	
Date	6/4/2015	
Sheet#	6 out of 12	





Title		Rev	
<h1>Arty</h1>		<h1>C.0</h1>	
Circuit		Copyright 2015	
FPGA Power			
Doc#	500-319		
Engineer	MTA		
Author	GMA		
Date	6/4/2015		
Sheet#	7 out of 12		

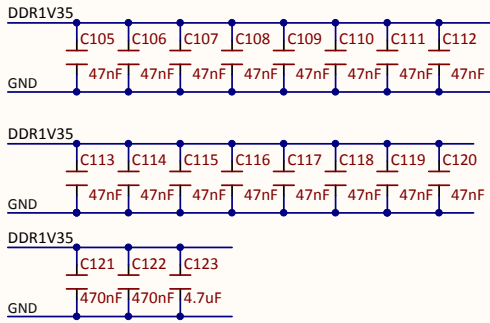
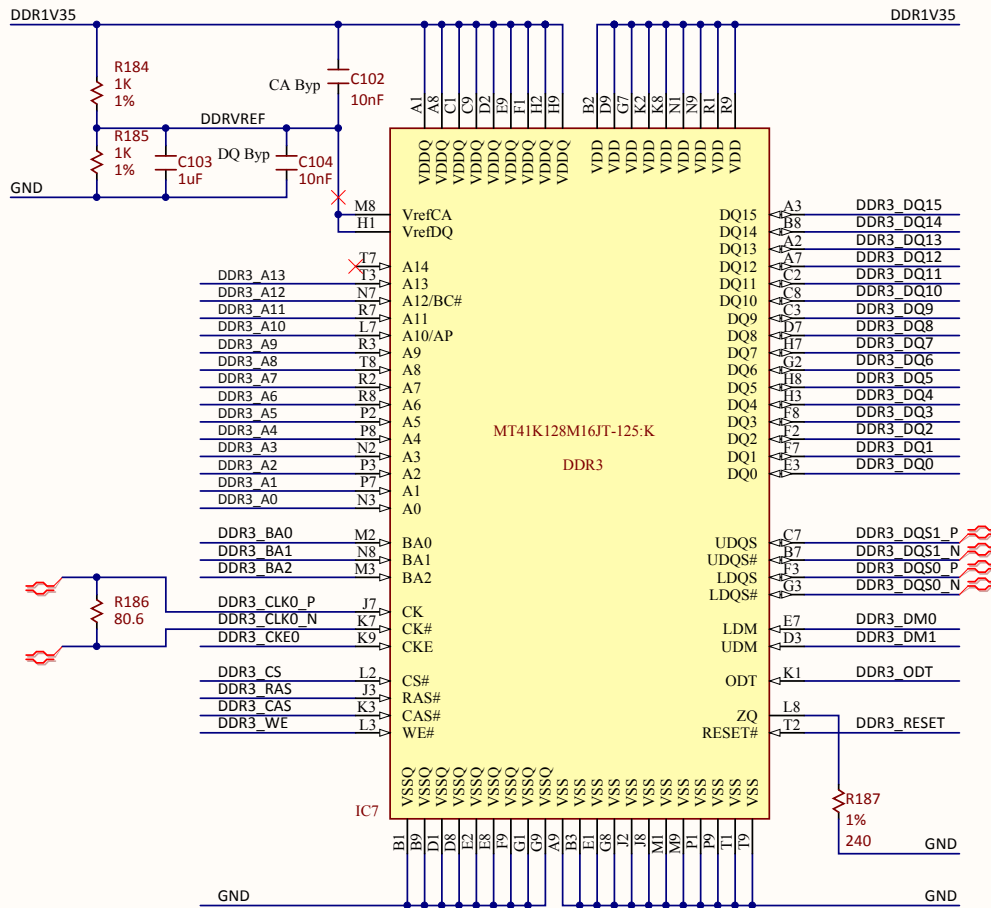




NOTE: REF_CLK In Mode (ETH_REF_CLK = 25MHz)

NOTE: PHY MDIO Address = 00001

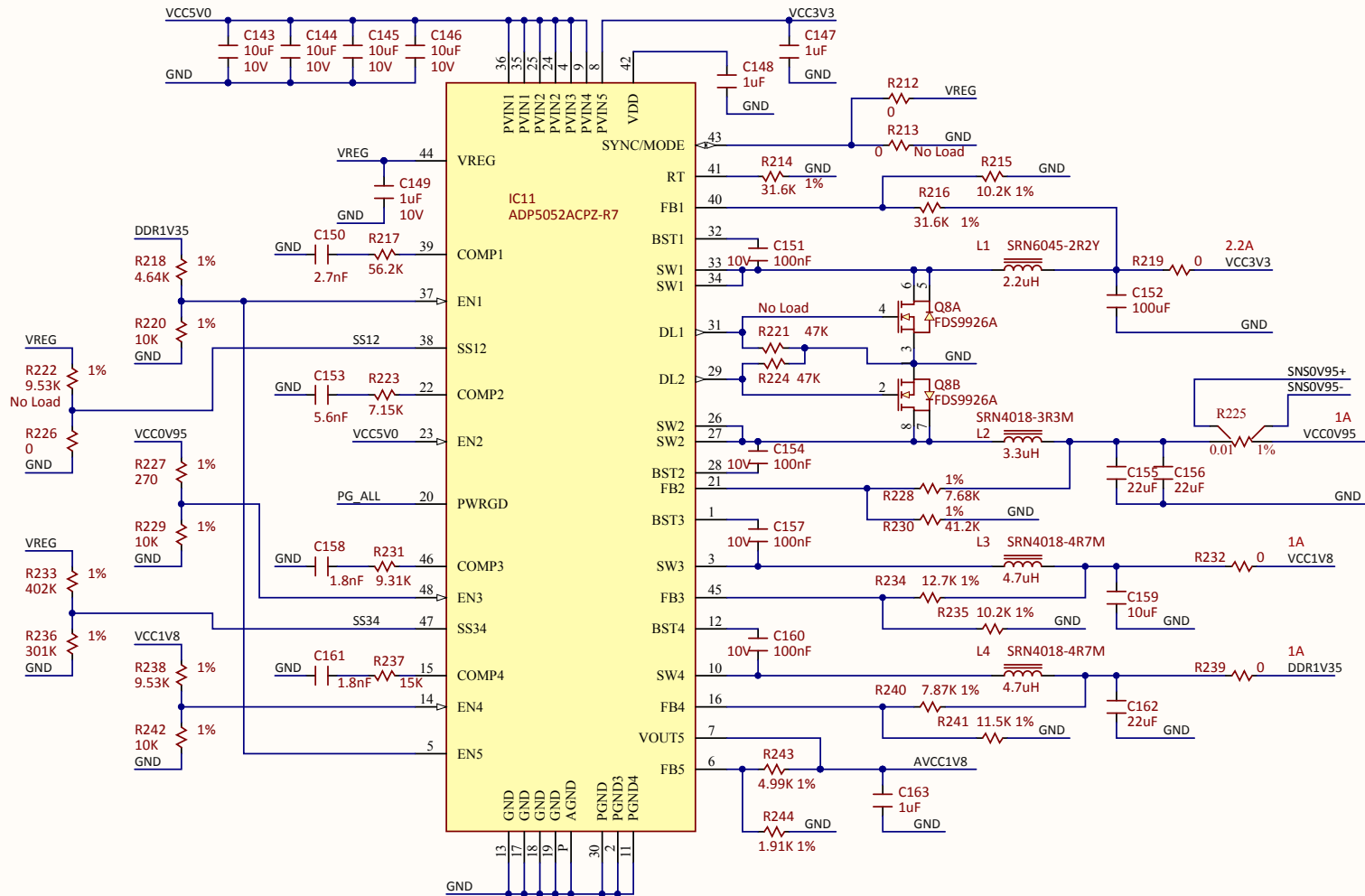
Title		Arty		Rev		C.0	
Circuit		ETHERNET		Copyright		2015	
Doc#		500-319					
Engineer		MTA					
Author		GMA					
Date		6/4/2015					
Sheet#		8 out of 12					




Title		Rev	
Arty		C.0	
Circuit		Copyright 2015	
DDR3			
Doc#	500-319		
Engineer	MTA		
Author	GMA		
Date	6/4/2015		
Sheet#	9 out of 12		



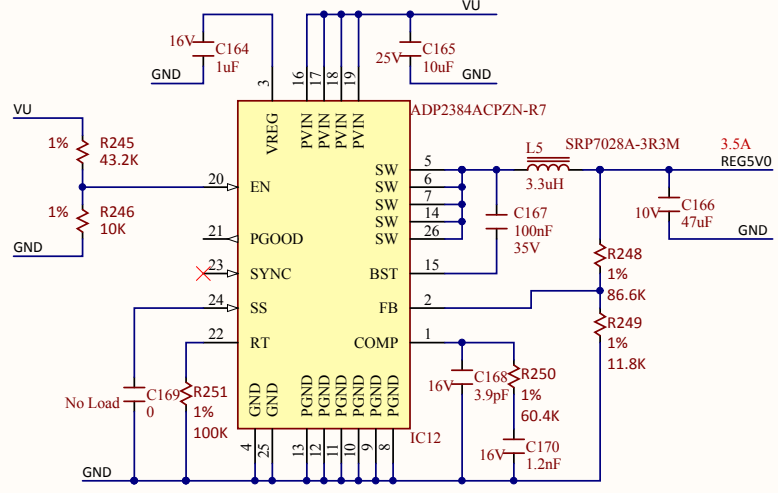
This Page Intentionally Left Blank



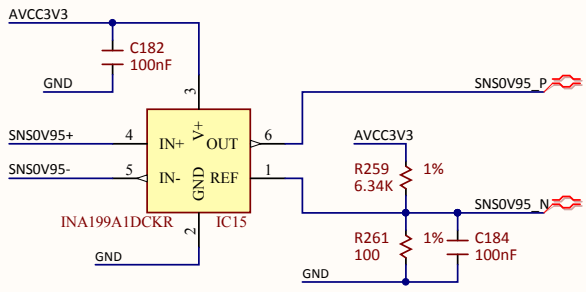
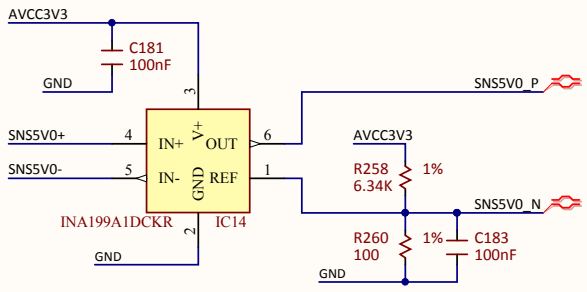
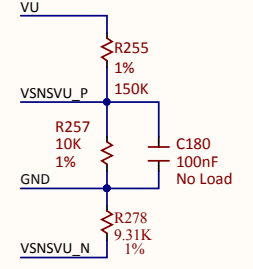
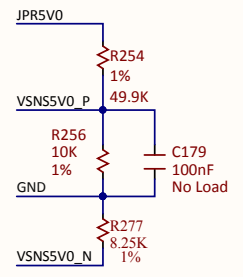
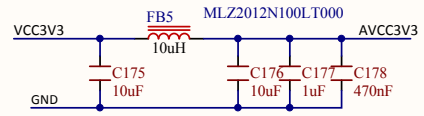
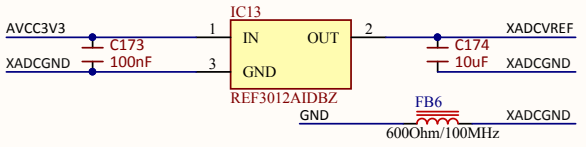
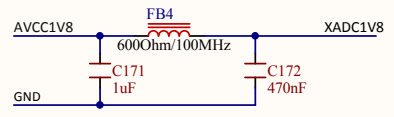
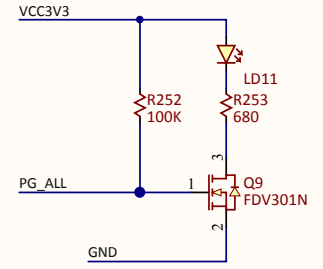
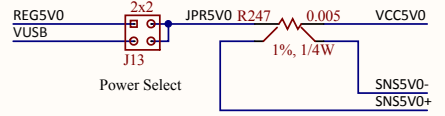
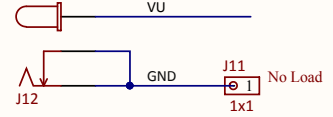
Title		Rev	
<h1>Arty</h1>		<h1>C.0</h1>	
		Copyright 2015	
Circuit	Power Regulation		
Doc#	500-319		
Engineer	MTA		
Author	GMA		
Date	6/4/2015		
Sheet#	11 out of 12		



DIGILENT
BEYOND THEORY



Note: Input Voltage 7-15V.



Title		Rev	
Arty		C.0	
Circuit		Copyright 2015	
Power Regulation			
Doc#	500-319		
Engineer	MTA		
Author	GMA		
Date	6/4/2015		
Sheet#	12 out of 12		